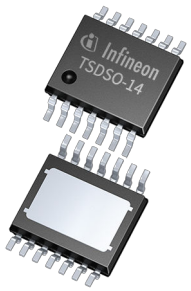
# OPTIREG™ switcher TLS4125D0EPV33

## 2.8 MHz synchronous step down regulator

Order now | Technical documents | Simulation | Support

AEC Qualified | RoHS

## Features




- 2.5 A step down regulator
- Input voltage from 3.7 V to 35 V
- 3.3 V output voltage
- ±1.5% feedback voltage accuracy in PWM mode
- Ultra low current consumption 31 µA
- Integrated high side and low side power MOSFETs
- Peak current mode PWM regulation
- Light load PFM mode with improved efficiency
- Switching frequency range: 320 kHz to 560 kHz or 1.6 MHz to 2.8 MHz
- 100% duty cycle operation
- Synchronization input
- Spread spectrum frequency modulation for improved EMI performance
- Soft-start function
- Integrated compensation network
- Output discharge function in disabled state
- Ultra low current consumption in disabled state (typically 1 µA)
- Undervoltage monitoring
- Overvoltage monitoring
- Overcurrent protection and overload protection
- Input undervoltage shutdown
- Wide temperature range $T_j$ = -40°C to 150°C
- Green Product (RoHS compliant)

## Potential applications

- Body
- ADAS
- Infotainment, telematics
- Navigation

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

# Description

The OPTIREG™ switcher TLS4125D0EPV33 is a synchronous step down regulator especially designed for automotive applications. The device has a current capability of 2.5 A, fixed 3.3 V output voltage and a feedback voltage accuracy of ±1.5% in PWM mode. The integrated power stages, soft-start feature and integrated compensation network reduce the required amount of external components and thus system costs and board space. The wide input voltage range and a 100% duty cycle operation mode make the device suitable for battery cranking scenarios in automotive applications. The wide switching frequency range allows the selection of appropriate coils and capacitors. The switching frequency can be synchronized to an external clock signal. Spread spectrum frequency modulation can be activated to improve the EMI performance in PWM operation. The device offers low current consumption in PFM mode at light loads to optimize efficiency. The TLS4125D0EPV33 can detect undervoltage and overvoltage conditions of the output voltage and indicates this with the reset output signal. Overcurrent and overload protections avoid excessive current to protect the device during short circuit conditions at the buck converter output. The integrated thermal shutdown feature protects the device from overheating. The enhanced PG-TSDSO-14 exposed pad package offers advantageous thermal performance in the application.

| Type | Package | Marking |
|---|---|---|
| TLS4125D0EPV33 | PG-TSDSO-14 | 4125D0V3 |

# Table of contents

**Features** . . . 1
**Potential applications** . . . 1
**Product validation** . . . 1
**Description** . . . 2
**Table of contents** . . . 3
**1 Block diagram** . . . 5
**2 Pin configuration** . . . 6
2.1 Pin assignment . . . 6
2.2 Pin definitions and functions . . . 6
**3 General product characteristics** . . . 8
3.1 Absolute maximum ratings . . . 8
3.2 Functional range . . . 9
3.3 Thermal resistance . . . 10
**4 Buck regulator** . . . 11
4.1 Functional description buck regulator . . . 11
4.1.1 Regulation loop and operation modes . . . 11
4.1.1.1 PWM (Pulse Width Modulation) mode . . . 11
4.1.1.2 PFM (Pulse Frequency Modulation) mode . . . 12
4.1.1.3 Continuous conduction mode and discontinuous conduction mode . . . 12
4.1.1.4 High duty cycle operation . . . 13
4.1.2 Power-up and power-down control . . . 14
4.1.2.1 Startup procedure with soft-start . . . 14
4.1.2.2 Active output discharge . . . 14
4.1.3 Protection features . . . 15
4.1.3.1 Overcurrent protection and overload protection . . . 15
4.1.3.2 Input undervoltage shutdown . . . 15
4.1.3.3 Overtemperature protection . . . 15
4.2 Electrical characteristics buck regulator . . . 16
4.3 Typical performance characteristics buck regulator . . . 18
**5 Oscillator** . . . 23
5.1 Functional description oscillator . . . 23
5.1.1 Synchronization input . . . 23
5.1.2 Spread spectrum . . . 24
5.2 Electrical characteristics oscillator . . . 24
5.3 Typical performance characteristics oscillator . . . 26
**6 Current consumption and enable** . . . 27

## Table of contents

6.1 Functional description current consumption and enable . . . . . 27
6.2 Electrical characteristics current consumption and enable . . . . . 27
6.3 Typical performance characteristics current consumption and enable . . . . . 28
**7 Reset** . . . . . 29
7.1 Functional description reset . . . . . 29
7.2 Electrical characteristics reset . . . . . 31
7.3 Typical performance characteristics reset . . . . . 33
**8 Application information** . . . . . 34
8.1 Layout recommendations . . . . . 36
8.2 Additional information . . . . . 36
**9 Package information** . . . . . 37
**Revision history** . . . . . 38
**Disclaimer** . . . . . 39

# 1 Block diagram

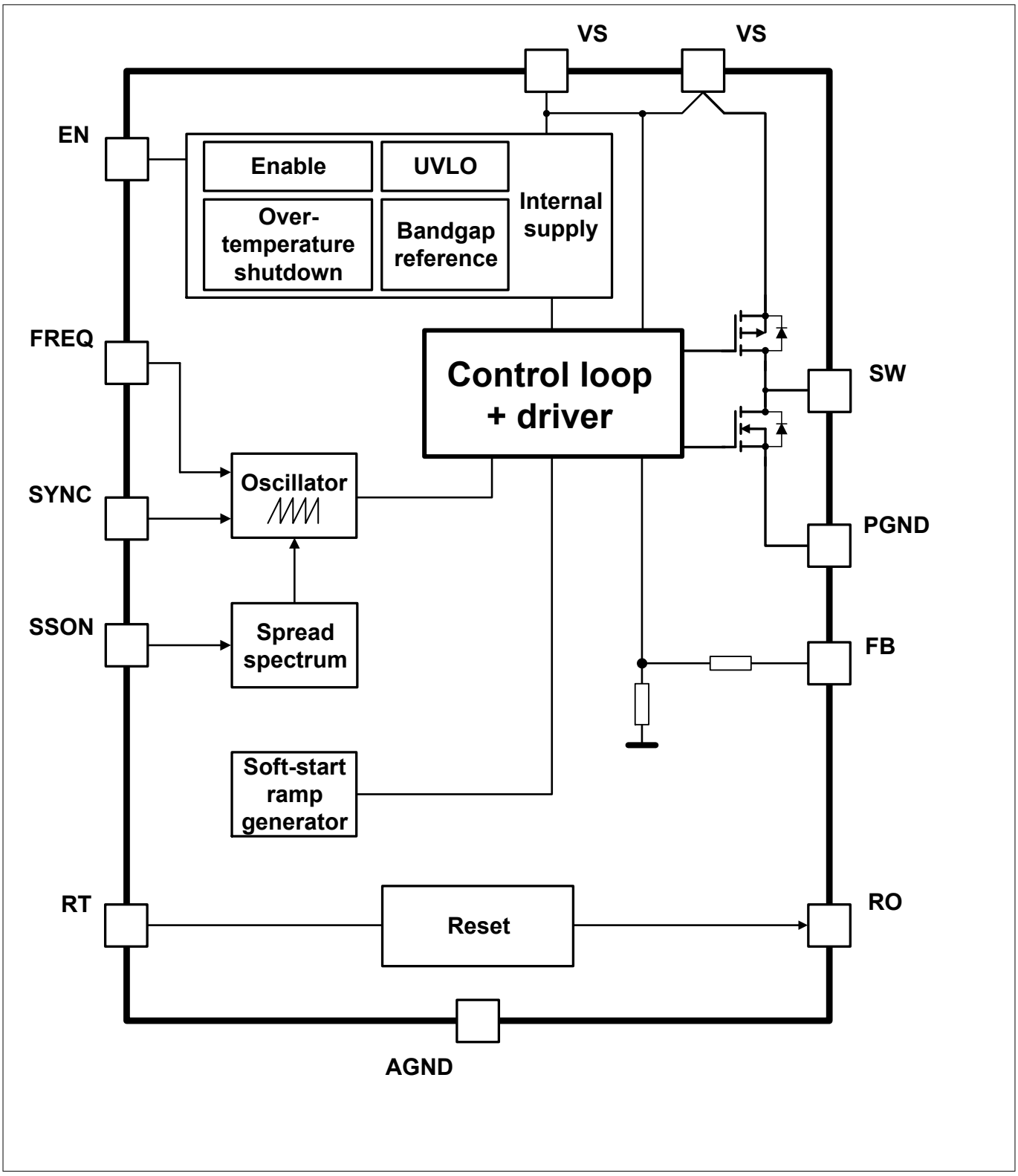



**Figure 1 Block diagram**

# 2 Pin configuration

## 2.1 Pin assignment

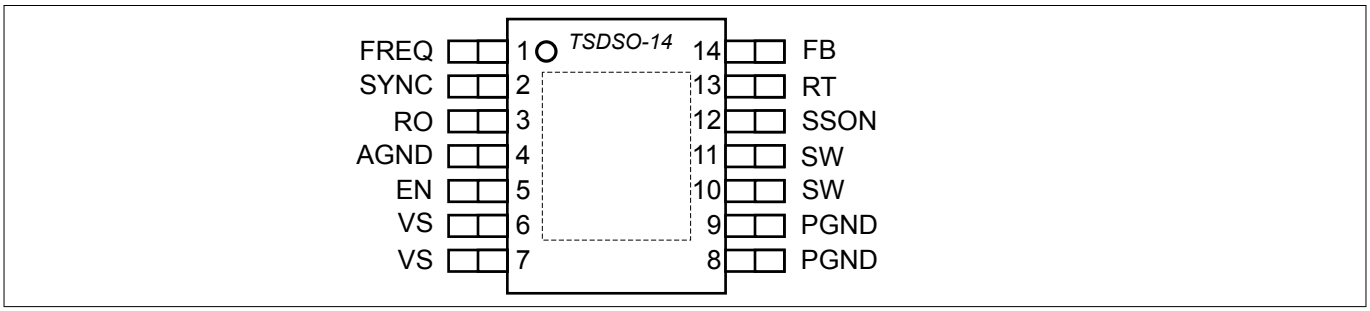



**Figure 2 Pin configuration**

## 2.2 Pin definitions and functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | FREQ | Frequency selection input:<br>Connect this pin to GND via resistor for frequency selection.<br>Leave this pin open to set the default high switching frequency.<br>Connect this pin to GND to set the default low switching frequency. |
| 2 | SYNC | Synchronization input:<br>Connect this pin to external clock to synchronize the switching frequency.<br>If this pin is not used, then connect it to GND. |
| 3 | RO | Reset output:<br>Open drain reset output. Provides the reset output signal.<br>If the reset feature is used, then connect this pin via external resistor to $V_{CC}$ or to an external pull-up voltage.<br>If the reset feature is not used, then leave this pin open. |
| 4 | AGND | Analog ground:<br>Connect this pin to GND using a low inductive, broad PCB trace. |
| 5 | EN | Enable input:<br>This pin has an integrated pull-down resistor.<br>"High" enables the device.<br>"Low" disables the device. |
| 6, 7 | VS | Supply voltage input:<br>Connect this pin to supply voltage.<br>Short pins 6 and 7 at the PCB. |
| 8, 9 | PGND | Power ground:<br>Connect this pin directly to GND using a low inductive, broad PCB trace.<br>Short pins 8 and 9 at the PCB. |
| 10, 11 | SW | Regulator switch node: |

## Pin configuration

| Pin | Symbol | Function |
|---|---|---|
| | | Connect this pin to the buck converter power inductor.<br>Short pins 10 and 11 at the PCB. |
| 12 | SSON | Spread spectrum enable input:<br>This pin has an integrated pull-down resistor.<br>"High" enables spread spectrum.<br>"Low" disables spread spectrum. |
| 13 | RT | Reset configuration input:<br>Connect this pin via a resistor to GND to adjust the reset delay time and the reset undervoltage threshold.<br>Connect this pin to GND, if the reset function is not needed or to configure the default reset delay time and default undervoltage reset threshold. |
| 14 | FB | Feedback input:<br>Feedback input to the regulator. Connect this pin directly to the output capacitor of the buck converter. |
| – | Exposed pad | Connect the exposed pad to a heatsink area and to GND with low inductive and broad PCB trace. |

# 3 General product characteristics

## 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings[1)]**

$T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Enable input | $V_{EN}$ | -20 | – | 35 | V | – | P_3.1.1 |
| Enable input | $V_{EN,dyn}$ | -20 | – | 42 | V | [2)] Transients present on this pin | P_3.1.2 |
| Synchronization input | $V_{SYNC}$ | -0.3 | – | 6 | V | – | P_3.1.3 |
| Spread spectrum enable input | $V_{SSON}$ | -0.3 | – | 6 | V | – | P_3.1.4 |
| Frequency selection | $V_{FREQ}$ | -0.3 | – | 6 | V | – | P_3.1.5 |
| Reset output | $V_{RO}$ | -0.3 | – | 6 | V | – | P_3.1.6 |
| Reset configuration | $V_{RT}$ | -0.3 | – | 6 | V | – | P_3.1.7 |
| Feedback input | $V_{FB}$ | -0.3 | – | 7 | V | – | P_3.1.8 |
| Buck switch output | $V_{SW}$ | -0.3 | – | $V_{VS}$ + 0.3 | V | Minimum -2.0 V in transient condition (single event < 15 ns) | P_3.1.9 |
| Supply voltage input | $V_{VS}$ | -0.3 | – | 35 | V | – | P_3.1.10 |
| Supply voltage input | $V_{VS,dyn}$ | -0.3 | – | 42 | V | [2)] Transients present on this pin | P_3.1.11 |
| Power GND | $V_{PGND}$ | -0.3 | – | 0.3 | V | – | P_3.1.12 |
| Analog GND | $V_{AGND}$ | -0.3 | – | 0.3 | V | – | P_3.1.13 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_3.1.14 |
| Storage temperature | $T_{stg}$ | -55 | – | 150 | °C | – | P_3.1.15 |
| **ESD susceptibility** | | | | | | | |
| ESD susceptibility to GND | $V_{ESD,HBM}$ | -2 | – | 2 | kV | [3)] HBM | P_3.1.16 |
| ESD susceptibility to GND | $V_{ESD,CDM}$ | -500 | – | 500 | V | [4)] CDM | P_3.1.17 |

1 Not subject to production test, specified by design.
2 Transients between 35 V and 42 V can be tolerated for a total lifetime duration shorter than 48 s.
3 ESD susceptibility, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
4 ESD susceptibility, Charged Device Model (CDM) according to JEDEC JESD22-C101.

**Table 1 Absolute maximum ratings[1] (continued)**

$T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| ESD susceptibility corner pins 1, 7, 8, 14 to GND | $V_{ESD,CDM,C}$ | -750 | – | 750 | V | [4] CDM | P_3.1.18 |

*Notes:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 3.2 Functional range

**Table 2 Functional range**

$T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply voltage decreasing | $V_{VS,dec}$ | 3.7 | – | 35 | V | [5] Minimum value represents low battery voltage condition (cranking) | P_3.2.1 |
| Supply voltage increasing | $V_{VS,inc}$ | 6.0 | – | 35 | V | Minimum value represents startup condition | P_3.2.2 |
| Enable input | $V_{EN}$ | 0 | – | 35 | V | – | P_3.2.3 |
| Output voltage | $V_{CC}$ | – | 3.3 | – | V | – | P_3.2.4 |
| SYNC input voltage | $V_{SYNC}$ | 0 | – | 3.5 | V | – | P_3.2.7 |
| Reset output voltage | $V_{RO,hi}$ | 0 | – | 3.5 | V | [6] | P_3.2.10 |
| Output current | $I_{CC}$ | 0 | – | 2.5 | A | – | P_3.2.13 |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_3.2.15 |

1 Not subject to production test, specified by design.
4 ESD susceptibility, Charged Device Model (CDM) according to JEDEC JESD22-C101.
5 With 3.7 V < $V_{VS}$ < 6 V, a reduced performance of parameter settings applies to feedback voltage accuracy, synchronization and the reset function.
6 Allowed external pull-up voltage applied via pull-up resistance to pin RO.

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

## 3.3 Thermal resistance

**Table 3 Thermal resistance[7)]**

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to case | $R_{thJC}$ | – | 8.6 | – | K/W | – | P_3.3.1 |
| Junction to ambient | $R_{thJA,1}$ | – | 34 | – | K/W | [8)] 2s2p | P_3.3.2 |
| Junction to ambient | $R_{thJA,2}$ | – | 45 | – | K/W | [9)] 1s0p + 600 mm² | P_3.3.3 |
| Junction to ambient | $R_{thJA,3}$ | – | 54 | – | K/W | [9)] 1s0p + 300 mm² | P_3.3.4 |
| Junction to ambient | $R_{thJA,4}$ | – | 116 | – | K/W | [9)] 1s0p footprint | P_3.3.5 |

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit **www.jedec.org**.*

7 Not subject to production test, specified by design.

8 Specified $R_{thJA}$ value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.

9 Specified $R_{thJA}$ value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; the product (IC and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 µm Cu).

# 4 Buck regulator

## 4.1 Functional description buck regulator

The TLS4125D0EPV33 is a synchronous current mode step down (buck) regulator with selectable switching frequency $f_{OSC}$. The device regulates the output voltage in pulse width modulation (PWM) or in pulse frequency modulation (PFM) mode and automatically moves between both modes on load change or input voltage change. At low input voltage conditions, for example during battery cranking, the device can operate at a duty cycle of 100%.

### 4.1.1 Regulation loop and operation modes

***Figure 3*** shows the regulation loop. An internal resistor divider is connected between pin FB and pin AGND to reduce the magnitude of the output voltage signal, which is connected to pin FB. The error amplifier processes the difference between scaled output feedback voltage and internal reference voltage to provide a reference current to the PWM comparator. The PWM comparator compares that reference current to a scaled version of the inductor current to determine the PWM duty cycle that is required for stable output voltage regulation. In PFM mode the error amplifier output signal also serves to modulate the switching frequency.

The control logic supervises the handover between operation modes and triggers the drivers of high side PMOS power stage and the low side NMOS power stage accordingly. For the modes of PWM, PFM and 100% duty cycle operation see ***PWM (Pulse Width Modulation) mode***, ***PFM (Pulse Frequency Modulation) mode***, ***Continuous conduction mode and discontinuous conduction mode*** and ***High duty cycle operation*** respectively.

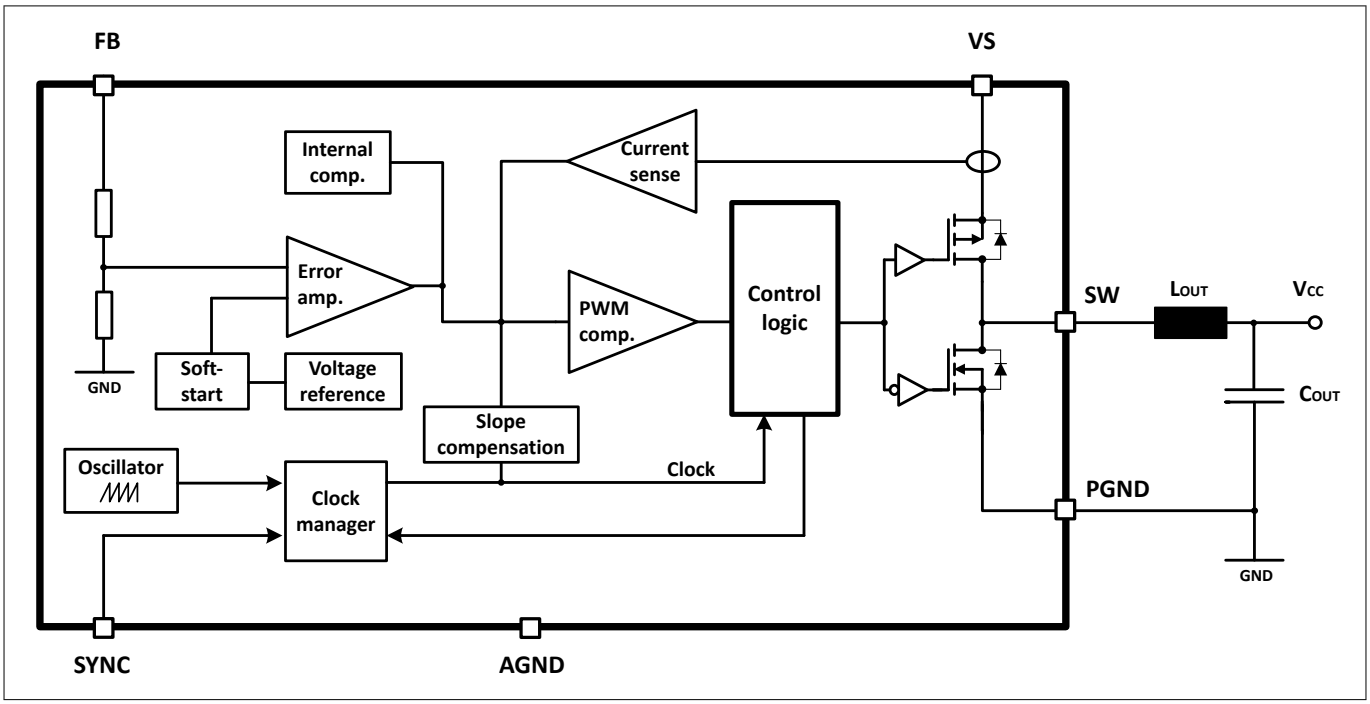



**Figure 3 Functional block diagram buck regulator**

#### 4.1.1.1 PWM (Pulse Width Modulation) mode

At high load the TLS4125D0EPV33 operates with the configured switching frequency $f_{OSC}$ in PWM mode. In PWM mode the device modulates the duty cycle to achieve a regulated output voltage. The nominal switching frequency can be set using one of the following methods, see ***Oscillator***:

- by an external resistor connected at pin FREQ
- from a synchronization signal applied at the SYNC pin

The pulse width modulation is based on peak current mode detection to achieve a fast reaction time and an optimized feedback accuracy. The PWM comparator processes the current signal detected at the high side power stage as well as the current signals of the slope compensation and the error amplifier to adjust the switching duty cycle to regulate the output voltage accordingly. With a duty cycle above 50% the slope compensation ensures system stability. This is achieved by avoidance of subharmonic oscillations of the output inductor current.

Due to a current sense signal inaccuracy at the beginning of each high side switch conduction phase, a short blanking time is required to mask the output of the current sense before processing it. The blanking time defines the minimum allowed on-time $t_{on,min}$ of the high side PMOS power stage and therefore the point of transition from PWM to PFM operation.

### 4.1.1.2 PFM (Pulse Frequency Modulation) mode

The device can operate at constant on-time $t_{on,min}$ of the high side PMOS power stage to achieve a stable output voltage at light load or high input voltage conditions. In PFM mode the device operates at a constant on-time and modulates the switching frequency to regulate the output voltage. The switching frequency is lower than in PWM mode. For further information about the PFM boundary condition and the frequency modulation depending on load and on input voltage, see ***Typical performance characteristics buck regulator***.

In PFM mode with light load the device offers optimized efficiency with reduced current consumption.

### 4.1.1.3 Continuous conduction mode and discontinuous conduction mode

#### Continuous conduction mode (CCM)

The device operates at a continuously rising or falling triangular positive inductor current. The on-time and the switching duty cycle mainly depend on the ratio of output voltage to input voltage.

#### Boundary condition for CCM → DCM transition

With a decrease of the load current during continuous conduction mode, the minimum valley inductor current can obtain approximately zero, which is the boundary condition for the discontinuous conduction mode. Further reduction of the load current leads to discontinuous conduction mode.

#### Discontinuous conduction mode (DCM)

The device turns off the low side power stage to avoid a negative inductor current. Further reduction of the load current reduces the on-time and leads to transition from PWM into PFM when obtaining the minimum on-time.

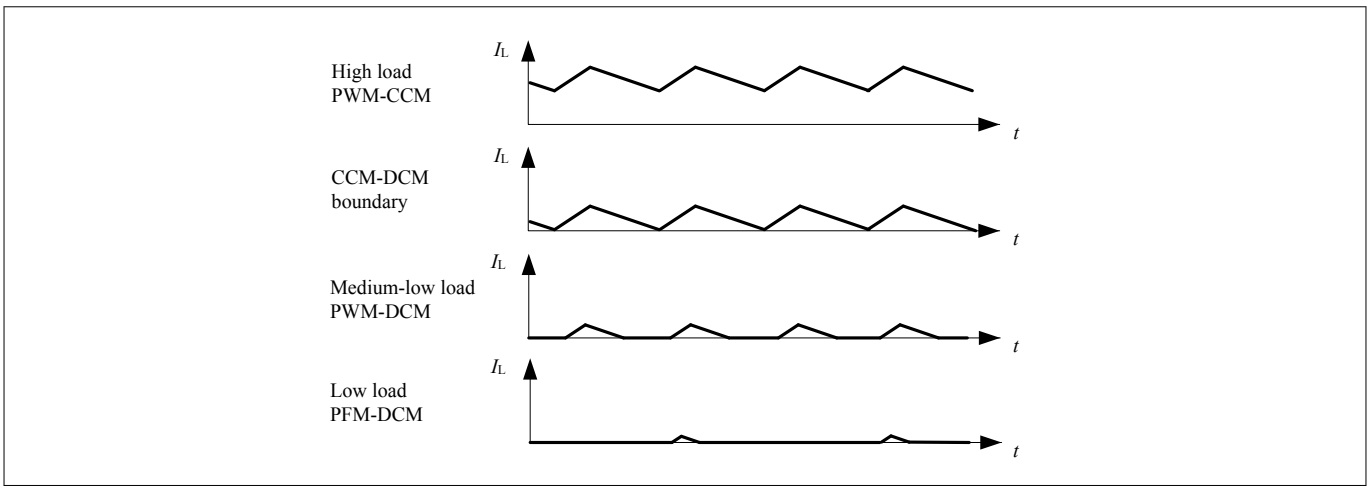



**Figure 4 Typical example inductor current waveforms for CCM and DCM**

### 4.1.1.4 High duty cycle operation

In 100% duty cycle mode the high side PMOS power stage constantly conducts current. If the input voltage is close to the nominal output voltage or lower, then the device enters this operation mode, see ***Figure 5***.

If the input voltage is decreased (for example during a battery cranking scenario) and the device moves from regulation to the 100% duty cycle mode, then the output voltage tracks the input voltage as accurate as possible down to an input voltage $V_{VS}$ of 3.7 V. During steady state operation, the difference of the output voltage and the tracked input voltage as well as the entry point into 100% duty cycle mainly depend on the voltage drop at the resistance $R_{on,hs}$ of the high side PMOS power stage, which in turn depends on the load current $I_{CC}$. Parasitic elements of external application circuitry and components, such as the output inductor series resistance, increase the voltage drop.

At high duty cycles close to 100%, the loop might not propagate very short off-times and compensates this by skipping switching cycles to ensure a smooth transition to 100% duty cycle with a stable output voltage.

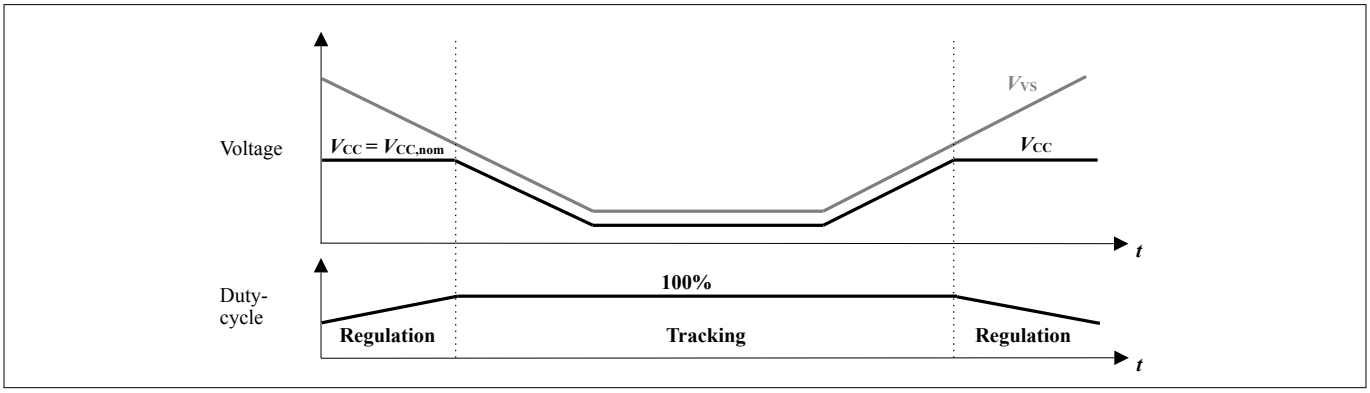



**Figure 5 Typical 100% duty cycle mode tracking behavior**

### 4.1.2 Power-up and power-down control

The following features of the device control power up and power down, see ***Table 4*** for electrical characteristics:

- Startup with soft-start
- Active output discharge

#### 4.1.2.1 Startup procedure with soft-start

The soft-start function of the TLS4125D0EPV33 controls the ramp-up of the output voltage with defined timing $t_{start}$ during startup, see ***Figure 6***. If $V_{VS} > V_{VS,on}$, then a "high" signal $V_{EN,hi}$ at pin EN triggers the startup procedure. During startup the internal supply establishes a stable state and the device initializes the switching frequency and the reset function according to the configuration. The regulator then increases the output voltage $V_{cc}$ by ramping up the internal voltage reference connected to the error amplifier.

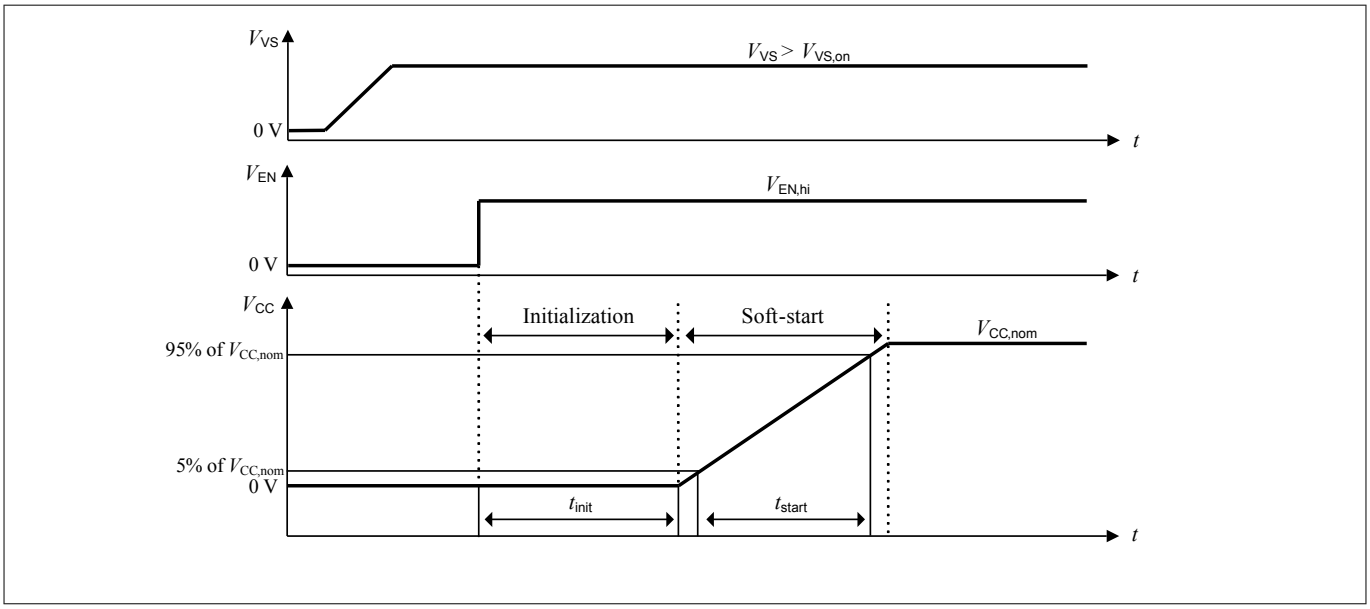



**Figure 6 Typical startup procedure**

#### 4.1.2.2 Active output discharge

The active output discharge function of the TLS4125D0EPV33 controls the ramp-down of the output voltage during power down, see ***Figure 7***. If the device detects a "low" signal $V_{EN,lo}$ at the EN pin, then it switches on the integrated discharge transistor connected to the SW pin in order to discharge the output capacitor $C_{OUT}$ via the output inductor $L_{OUT}$. The typical on-resistance $R_{dc}$ of the discharge transistor is 55 Ω.

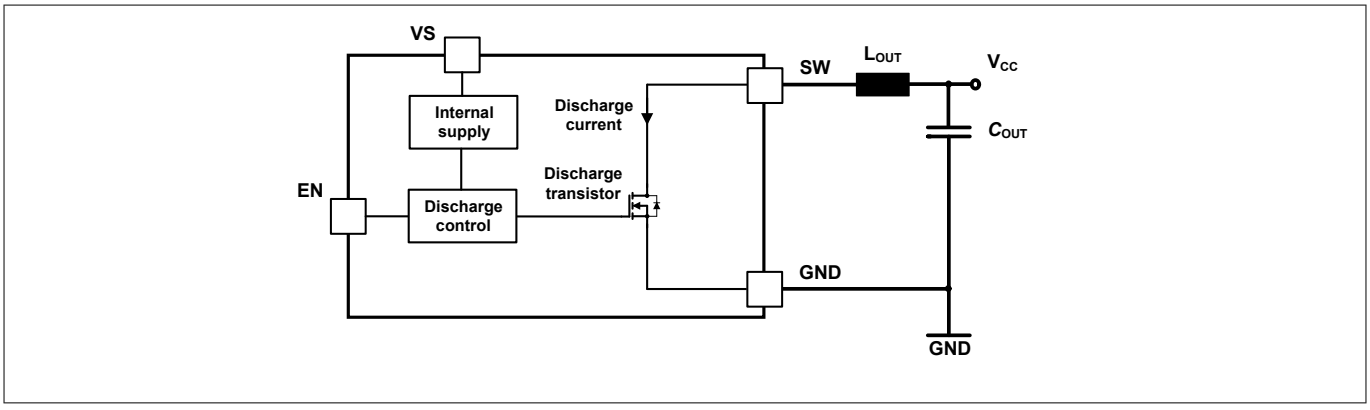



**Figure 7 Active output discharge block diagram**

### 4.1.3 Protection features

The device offers features that are designed to protect it from fault events such as overcurrent, overload, input undervoltage and overtemperature, see ***Table 4***.

#### 4.1.3.1 Overcurrent protection and overload protection

If the sensed current through the high side PMOS power stage exceeds the buck peak overcurrent limit $I_{BUOC}$ after the blanking time of the current sense, then the device switches off the high side power stage for the remaining time of the current cycle. Active current limitation can decrease the output voltage level.

If the sensed freewheeling current through the low side NMOS power stage exceeds the overload limit $I_{BUOL}$, then the device prevents the high side PMOS power stage from switching on in the subsequent clock cycles to avoid overheating. The overload threshold level is set to a higher value than the overcurrent threshold level.

If an overload condition and an undervoltage condition occur for longer than 3 ms typically, then the device detects a short circuit at the output voltage node and shuts down. After a waiting time of typically 1 s, the device restarts with a soft-start.

#### 4.1.3.2 Input undervoltage shutdown

The device incorporates an undervoltage shutdown function. If the input voltage $V_{VS}$ drops below the input undervoltage shutdown threshold $V_{VS,off}$, then the device shuts down.

#### 4.1.3.3 Overtemperature protection

The integrated overtemperature protection turns off the device in case of a too high junction temperature. The typical junction thermal shutdown temperature is 175°C. After the device has cooled down by the amount of the typical junction temperature hysteresis 10 K and a subsequent waiting time of typically 1 s, the device restarts with a soft-start to resume normal operation. The thermal shutdown is an integrated protection function to prevent the immediate destruction of the device during fault conditions. However, a junction temperature above 150°C is outside of the maximum ratings and reduces the lifetime of the device.

## 4.2 Electrical characteristics buck regulator

**Table 4 Electrical characteristics buck regulator**

$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Feedback voltage accuracy** | | | | | | | |
| Feedback voltage accuracy | $V_{FB,PWM}$ | -1.5 | – | +1.5 | % | 6 V ≤ $V_{VS}$ ≤ 35 V; PWM mode | P_4.2.1 |
| Feedback voltage accuracy | $V_{FB,PFM,1}$ | -2 | – | +3.5 | % | 6 V ≤ $V_{VS}$ ≤ 35 V; PFM mode | P_4.2.2 |
| Feedback voltage $V_{FB}$ | $V_{FB}$ | – | 3.3 | – | V | – | P_4.2.4 |
| **MOSFETs** | | | | | | | |
| High side MOSFET on-resistance | $R_{on,hs}$ | – | 120 | 240 | mΩ | $I_{CC}$ = 100 mA | P_4.2.7 |
| Low side MOSFET on-resistance | $R_{on,ls}$ | – | 70 | 150 | mΩ | $I_{CC}$ = 100 mA | P_4.2.9 |
| **Regulation loop** | | | | | | | |
| Maximum duty cycle | $D_{max}$ | – | – | 100 | % | [10] | P_4.2.11 |
| Minimum on-time, high frequency | $t_{on,min,hf}$ | – | 78 | – | ns | [11] $I_{CC}$ = 1.5 A; valid for high frequency operation range | P_4.2.12 |
| Minimum on-time, low frequency | $t_{on,min,lf}$ | – | 308 | – | ns | [11] $I_{CC}$ = 1.5 A; valid for low frequency operation range | P_4.2.13 |
| **Startup and active discharge** [12] | | | | | | | |
| Soft-start time | $t_{start}$ | 0.8 | 1 | 1.2 | ms | $V_{CC}$ rising from 5% to 95% of nominal $V_{CC}$ level | P_4.2.14 |
| Startup initialization time | $t_{init}$ | – | – | 2.6 | ms | time from rising edge of $V_{EN}$ (0 V to $V_{EN,hi}$ ) until soft-start | P_4.2.15 |
| Input voltage startup threshold | $V_{VS,on}$ | 2.6 | – | 6.0 | V | $V_{VS}$ increasing; $V_{EN}$ ≥ 2 V | P_4.2.16 |
| Output discharge resistance | $R_{dc}$ | – | 55 | – | Ω | $V_{EN}$ = 0 V; $V_{VS}$ = 13.5 V; $V_{SW}$ = 100 mV | P_4.2.17 |
| **Current limitation** | | | | | | | |
| Buck peak overcurrent limit | $I_{BUOC}$ | 3.3 | 3.9 | 4.5 | A | – | P_4.2.19 |

10 See ***Functional range*** and ***High duty cycle operation***.
11 Specified by design, not subject to production test.
12 See ***Power-up and power-down control***

**Table 4 Electrical characteristics buck regulator (continued)**

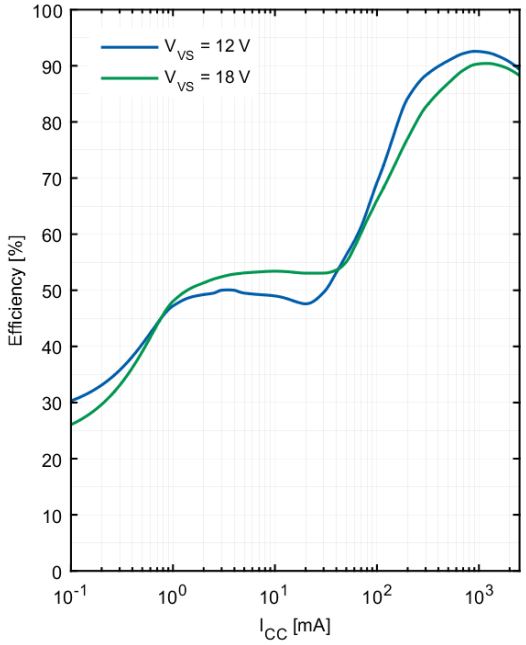
$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Overload current limit | $I_{BUOL}$ | 3.9 | 4.4 | 5.1 | A | – | P_4.2.21 |
| Overload overcurrent gap | $I_{BUOL,gap}$ | 0.05 | 0.5 | – | A | Overload current limit is typically 0.5 A above buck peak overcurrent limit | P_4.2.22 |
| **Undervoltage shutdown** | | | | | | | |
| Input undervoltage shutdown threshold | $V_{VS,off}$ | 3.3 | – | 3.55 | V | $V_{VS}$ decreasing | P_4.2.23 |
| Input undervoltage shutdown hysteresis | $V_{VS,hys}$ | 180 | 280 | 420 | mV | – | P_4.2.24 |

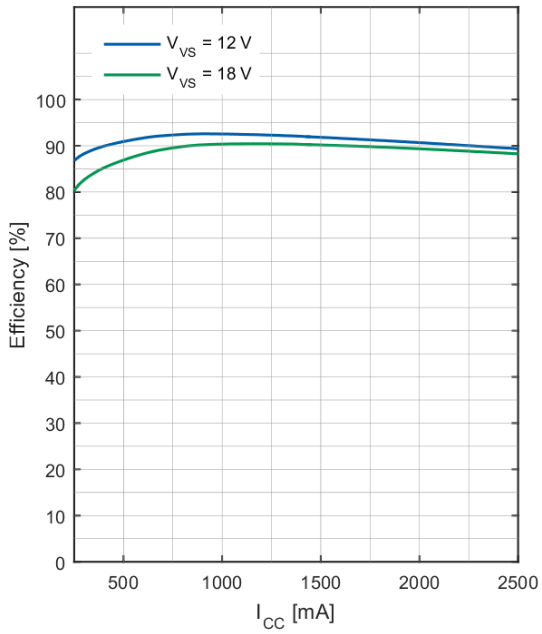
## 4.3 Typical performance characteristics buck regulator

FREQ: 2.2 MHz; $V_{VS}$ = 13.5 V; $T_j$ = 25°C (if not otherwise specified). The shown performance characteristics was measured on a 4 layer FR4 printed circuit board with external components as recommended in ***Application information***.

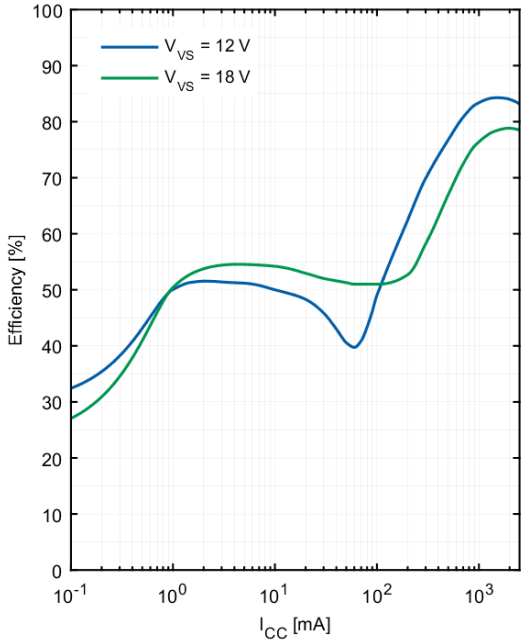
Efficiency
FREQ: 440 kHz; $T_j$ = 25°C



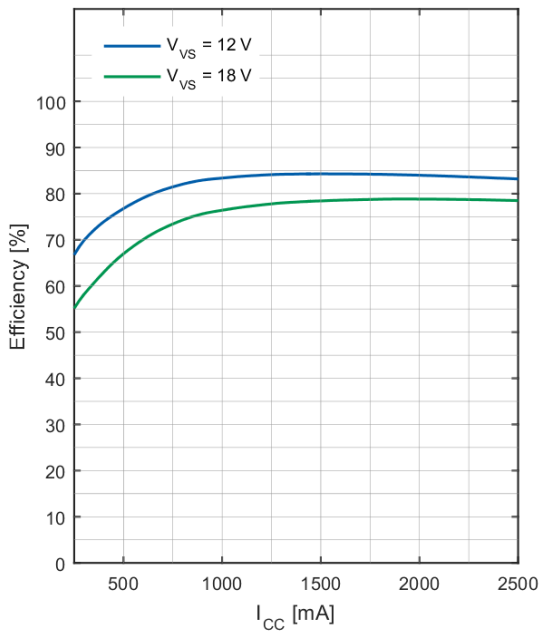

Efficiency
FREQ: 440 kHz; $T_j$ = 25°C




Efficiency
FREQ: 2.2 MHz; $T_j$ = 25°C



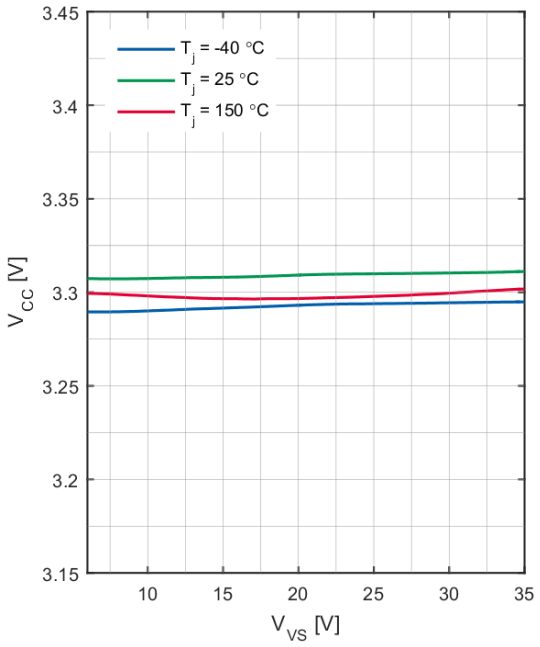

Efficiency
FREQ: 2.2 MHz; $T_j$ = 25°C



## Buck regulator

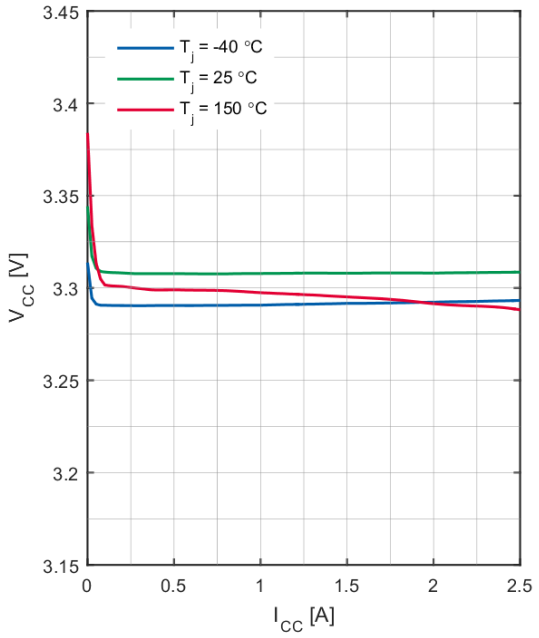
Line regulation

$I_{CC}$ = 1 A



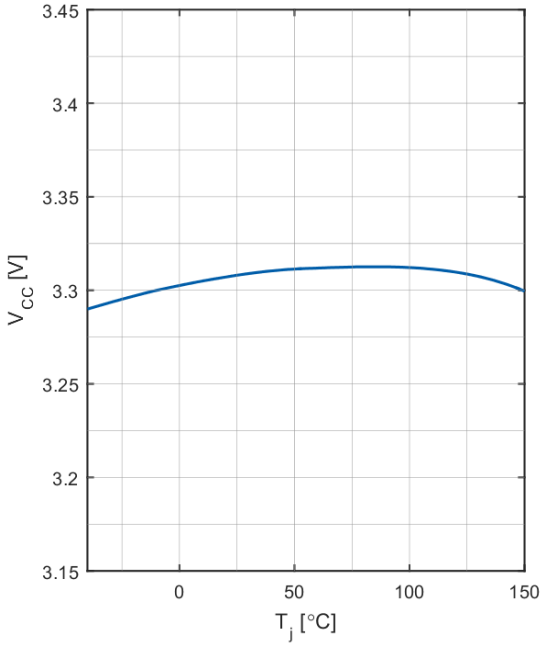

Load regulation

$V_{VS}$ = 13.5 V



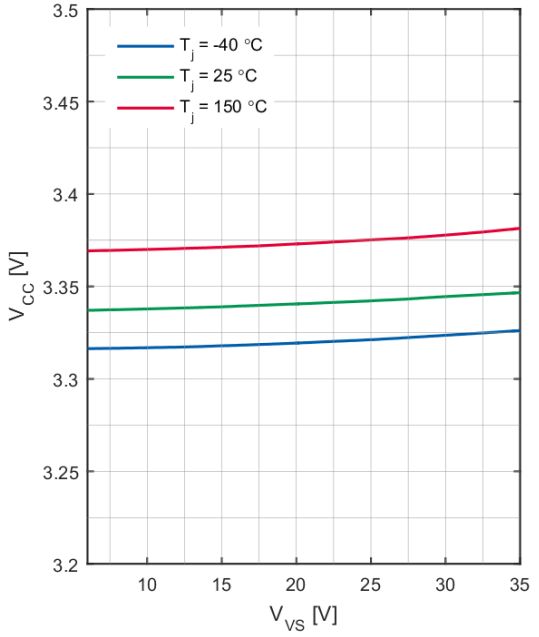

Output voltage precision

$I_{CC}$ = 200 mA



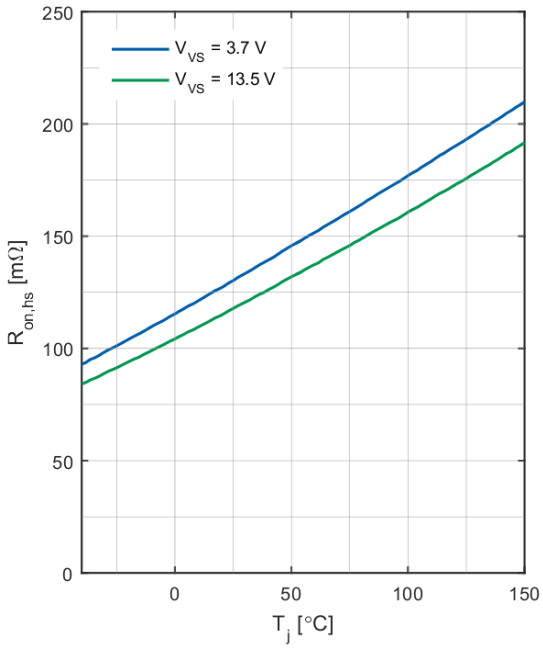

Line regulation (low load)

$I_{CC}$ = 100 µA

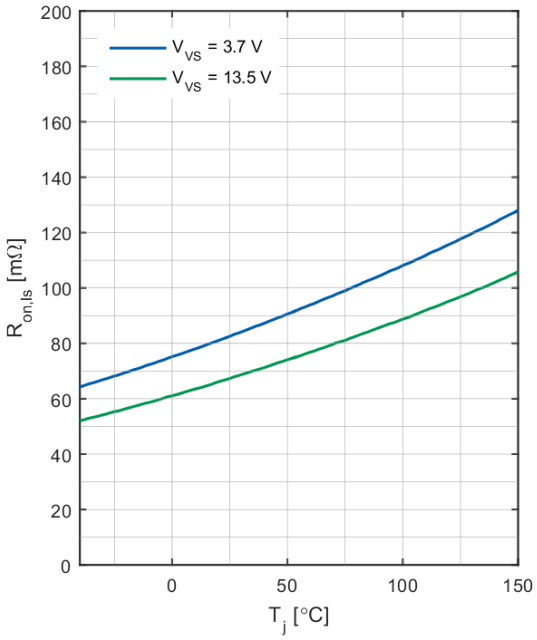


## Buck regulator

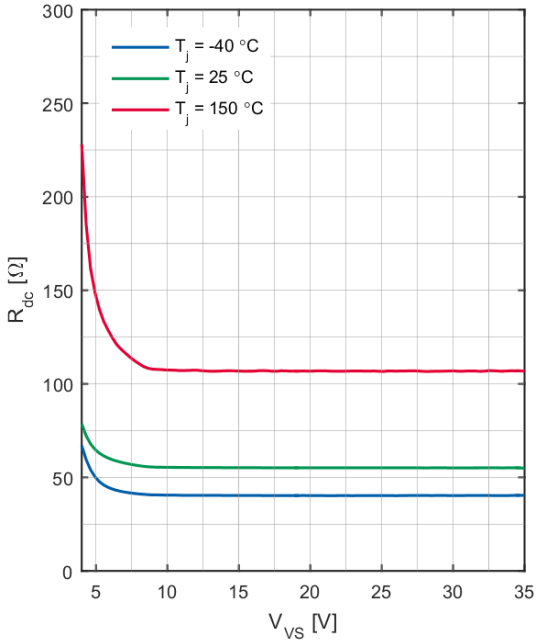
High side MOSFET on-resistance
$I_{CC}$ = 100 mA



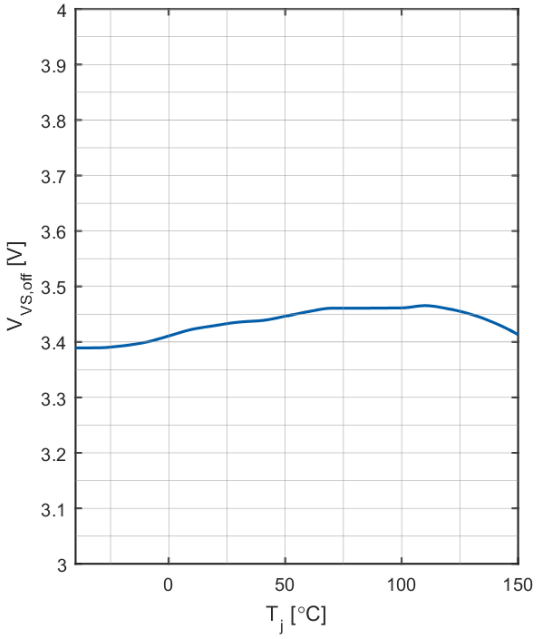

Low side MOSFET on-resistance
$I_{CC}$ = 100 mA



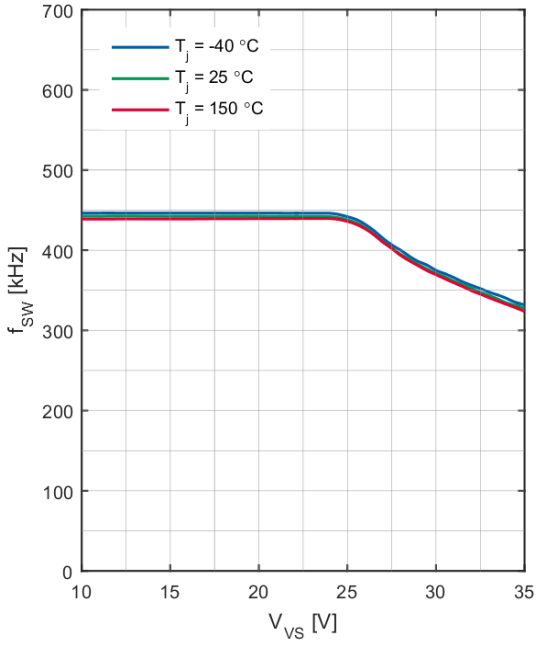

Output discharge resistance
$V_{EN}$ = 0 V; $V_{SW}$ = 100 mV



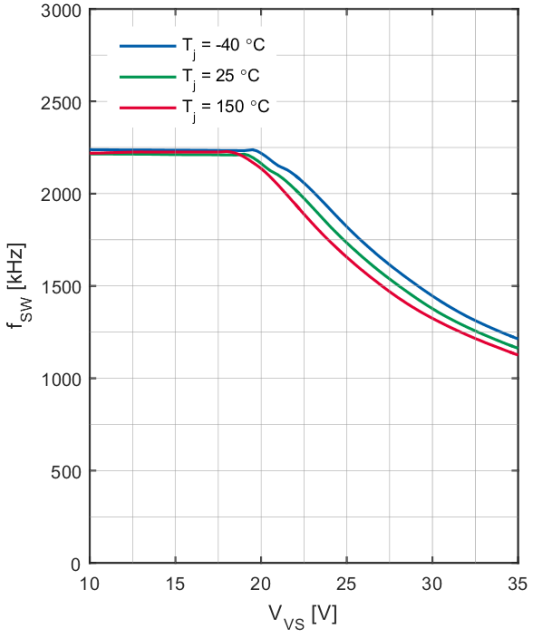

Input undervoltage shutdown threshold
$V_{VS}$ decreasing



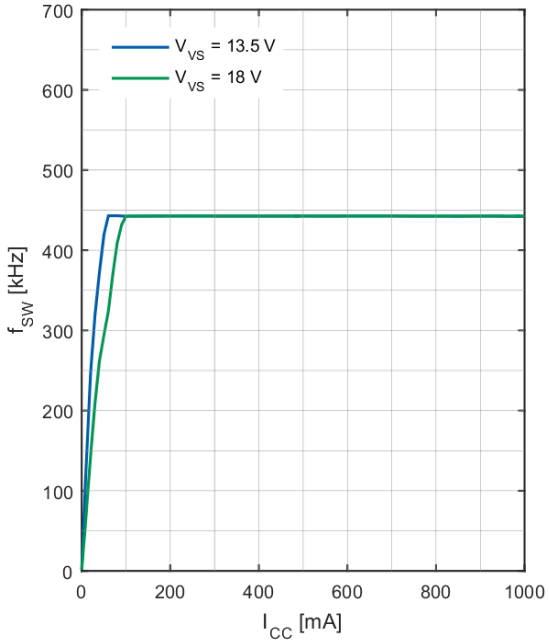
PFM frequency modulation (CCM)
FREQ: 440 kHz; $I_{CC}$ = 1.5 A



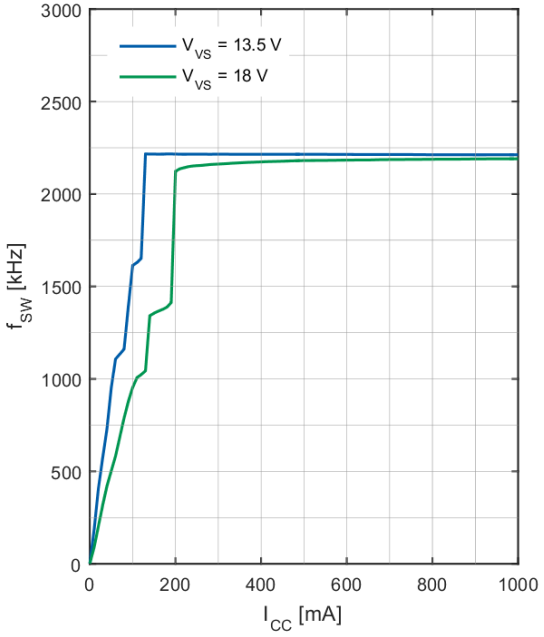

PFM frequency modulation (CCM)
FREQ: 2.2 MHz; $I_{CC}$ = 1.5 A




PFM frequency modulation (DCM)
FREQ: 440 kHz; $T_j$ = 25°C

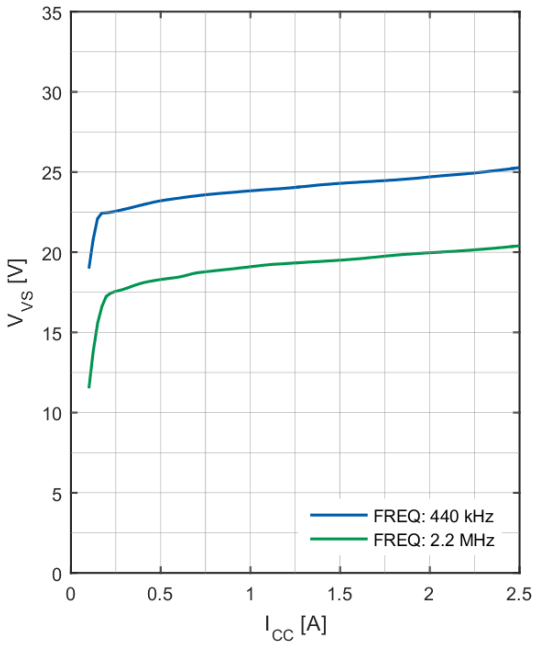



PFM frequency modulation (DCM)
FREQ: 2.2 MHz; $T_j$ = 25°C

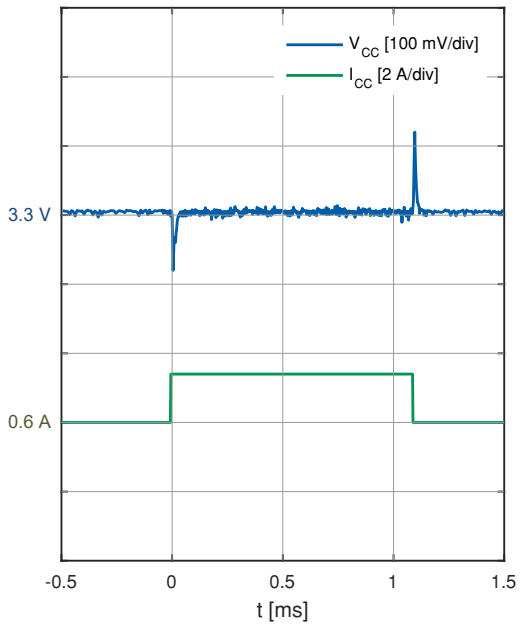


## Buck regulator

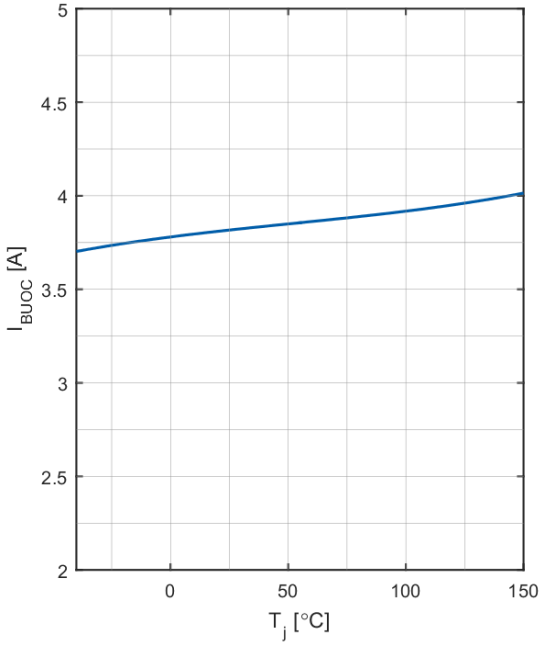
PFM boundary
$T_j$ = 25°C



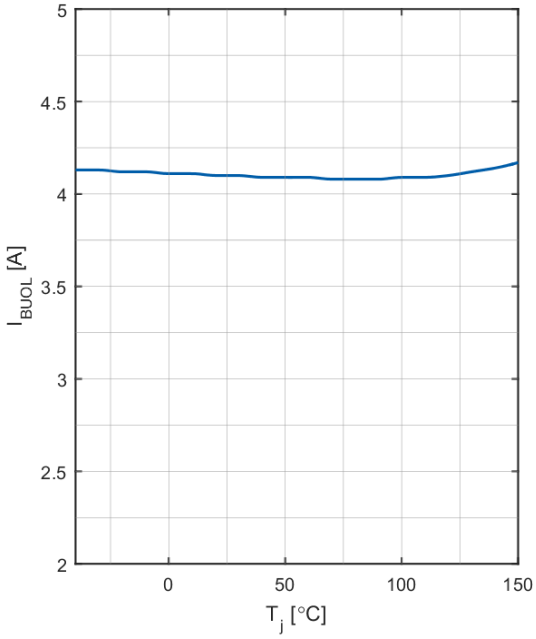

Load step response
$I_{CC}$: 0.6 A to 2 A to 0.6 A




Buck peak overcurrent limit
$V_{VS}$ = 13.5 V




Overload current limit
$V_{VS}$ = 13.5 V



# 5 Oscillator

## 5.1 Functional description oscillator

The integrated clock provides a constant frequency to the regulation loop. In PWM mode the device switches on and off the high side and low side power stages at the oscillator frequency $f_{OSC}$.

The oscillator frequency can be set by connecting a resistor $R_{FREQ}$ between the FREQ pin and ground, see ***Table 5***, ***Table 6*** and ***Table 7***. The device sets the selected switching frequency during startup.

**Table 5 FREQ configuration for typical oscillator frequencies in the low frequency range**

| $R_{FREQ}$ [kΩ][13] | $f_{OSC}$ [kHz] |
|---|---|
| 2.2 | 320 |
| 3.3 | 360 |
| 4.7 | 400 |
| ≤ 1.0 (or connect FREQ pin directly to GND) | 440[14] |
| 6.8 | 480 |
| 10 | 520 |
| 15 | 560 |

**Table 6 FREQ configuration for typical oscillator frequencies in the high frequency range**

| $R_{FREQ}$ [kΩ][15] | $f_{OSC}$ [MHz] |
|---|---|
| 22 | 1.6 |
| 33 | 1.8 |
| 47 | 2.0 |
| ≥ 200 (or leave FREQ pin open) | 2.2[16] |
| 68 | 2.4 |
| 100 | 2.6 |
| 150 | 2.8 |

### 5.1.1 Synchronization input

In PWM mode the device can synchronize the switching frequency to an external oscillator connected to the SYNC pin. The internal clock manager triggers at the falling edge of the external signal. The phase shift towards the switching frequency can be adjusted with the duty cycle of the external oscillator. 50% duty cycle of the external oscillator corresponds to a phase shift of approximately zero. A suitable setting of $R_{FREQ}$ is required so that the internal operation frequency is equal to the corresponding external synchronization frequency or above it. This is a prerequisite for the automatic transitions between PWM mode and PFM mode.

As soon as the startup is completed and the device accepts the external signal at the SYNC pin, the synchronization turns active.

13 Resistor tolerance ≤ 5%.
14 Default oscillator low frequency.
15 Resistor tolerance ≤ 5%.
16 Default oscillator high frequency.

### 5.1.2 Spread spectrum

In PWM mode, when used without an external clock at the SYNC pin, the TLS4125D0EPV33 can apply spread spectrum to optimize EMI performance. The device modulates the switching frequency up and down by a triangle waveform with a typical frequency of 8.3 kHz within a range of typically ±7.5% of the selected oscillator frequency. The logical signal on the SSON pin switches spread spectrum on or off.

## 5.2 Electrical characteristics oscillator

**Table 7 Electrical characteristics oscillator**

$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Frequency setting** | | | | | | | |
| Default oscillator low frequency | $f_{osc,1}$ | 396 | 440 | 484 | kHz | $R_{FREQ}$ ≤ 1.0 kΩ or connect FREQ pin directly to GND | P_5.2.1 |
| Default oscillator high frequency | $f_{osc,2}$ | 1.98 | 2.2 | 2.42 | MHz | $R_{FREQ}$ ≥ 200 kΩ or leave FREQ pin open | P_5.2.2 |
| Oscillator frequency | $f_{osc,3}$ | 288 | 320 | 352 | kHz | $R_{FREQ}$ = 2.2 kΩ | P_5.2.3 |
| Oscillator frequency | $f_{osc,4}$ | 324 | 360 | 396 | kHz | $R_{FREQ}$ = 3.3 kΩ | P_5.2.4 |
| Oscillator frequency | $f_{osc,5}$ | 360 | 400 | 440 | kHz | $R_{FREQ}$ = 4.7 kΩ | P_5.2.5 |
| Oscillator frequency | $f_{osc,6}$ | 432 | 480 | 528 | kHz | $R_{FREQ}$ = 6.8 kΩ | P_5.2.6 |
| Oscillator frequency | $f_{osc,7}$ | 468 | 520 | 572 | kHz | $R_{FREQ}$ = 10 kΩ | P_5.2.7 |
| Oscillator frequency | $f_{osc,8}$ | 504 | 560 | 616 | kHz | $R_{FREQ}$ = 15 kΩ | P_5.2.8 |
| Oscillator frequency | $f_{osc,9}$ | 1.44 | 1.6 | 1.76 | MHz | $R_{FREQ}$ = 22 kΩ | P_5.2.9 |
| Oscillator frequency | $f_{osc,10}$ | 1.62 | 1.8 | 1.98 | MHz | $R_{FREQ}$ = 33 kΩ | P_5.2.10 |
| Oscillator frequency | $f_{osc,11}$ | 1.8 | 2.0 | 2.2 | MHz | $R_{FREQ}$ = 47 kΩ | P_5.2.11 |
| Oscillator frequency | $f_{osc,12}$ | 2.16 | 2.4 | 2.64 | MHz | $R_{FREQ}$ = 68 kΩ | P_5.2.12 |
| Oscillator frequency | $f_{osc,13}$ | 2.34 | 2.6 | 2.86 | MHz | $R_{FREQ}$ = 100 kΩ | P_5.2.13 |
| Oscillator frequency | $f_{osc,14}$ | 2.52 | 2.8 | 3.08 | MHz | $R_{FREQ}$ = 150 kΩ | P_5.2.14 |
| **Synchronization input** | | | | | | | |
| Synchronization low frequency capture range | $f_{sync,lf}$ | 320 | – | 560 | kHz | [17] valid for oscillator low frequency range | P_5.2.15 |
| Synchronization high frequency capture range | $f_{sync,hf}$ | 1.6 | – | 2.8 | MHz | [17] valid for oscillator high frequency range | P_5.2.16 |
| SYNC "high" signal | $V_{SYNC,hi}$ | 2 | – | – | V | [17] $V_{CC}$ = 3.3 V | P_5.2.19 |

17 Synchronization of PWM to the falling edge.

## Oscillator

**Table 7 Electrical characteristics oscillator (continued)**

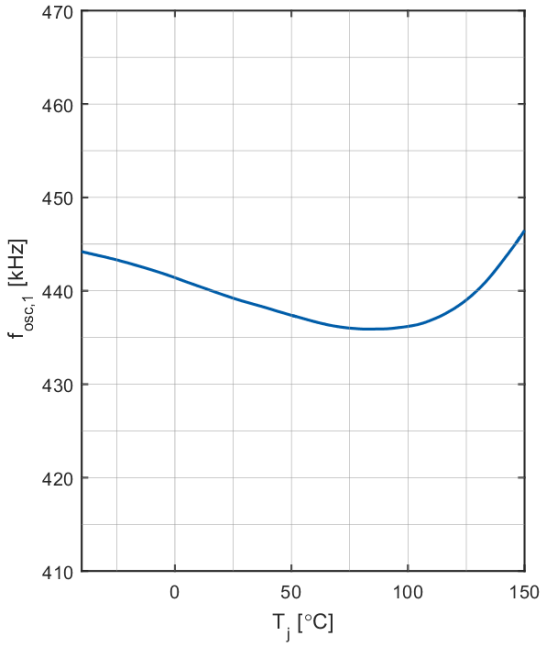
$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SYNC "low" signal | $V_{SYNC,lo}$ | – | – | 0.8 | V | 17) | P_5.2.21 |
| SYNC signal hysteresis | $V_{SYNC,hys}$ | 45 | 255 | 600 | mV | 17) | P_5.2.22 |
| SYNC "high" input current | $I_{SYNC,hi}$ | – | 0.1 | 1 | µA | $V_{SYNC}$ = 3.3 V | P_5.2.24 |
| SYNC "low" input current | $I_{SYNC,lo}$ | – | 0.1 | 1 | µA | $V_{SYNC}$ = 0 V | P_5.2.26 |
| SYNC signal duty cycle | $D_{SYNC}$ | 10 | – | 90 | % | – | P_5.2.28 |
| **Spread spectrum** | | | | | | | |
| Spread spectrum "high" signal | $V_{SSON,hi}$ | 2.0 | – | – | V | Enables spread spectrum | P_5.2.29 |
| Spread spectrum "low" signal | $V_{SSON,lo}$ | – | – | 0.8 | V | Disables spread spectrum | P_5.2.30 |
| Spread spectrum enable hysteresis | $V_{SSON,hys}$ | 100 | 250 | 1000 | mV | – | P_5.2.31 |
| Spread spectrum enable "high" input current | $I_{SSON,hi}$ | 0.7 | 1 | 1.25 | µA | $V_{SSON}$ = 5.0 V | P_5.2.32 |
| Spread spectrum modulation frequency | $f_{SS,mod}$ | 7.5 | 8.3 | 9.3 | kHz | Spread spectrum enabled | P_5.2.33 |
| Spread spectrum modulation range | $f_{SS,range}$ | – | ±7.5 | – | % | Spread spectrum enabled | P_5.2.34 |

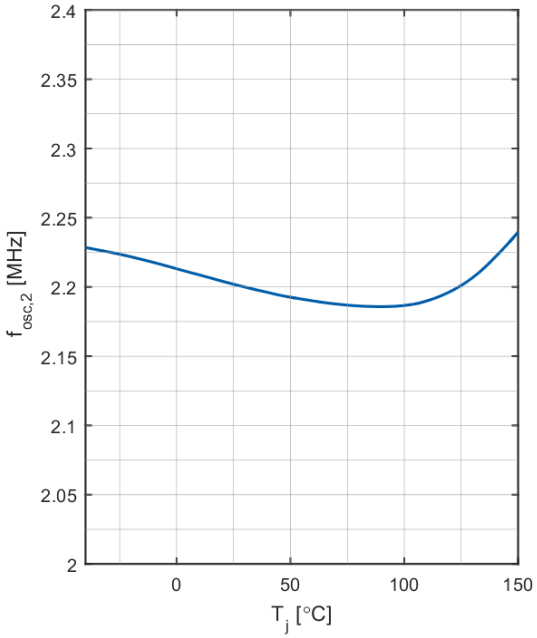
17 Synchronization of PWM to the falling edge.

## 5.3 Typical performance characteristics oscillator

Oscillator (low frequency)
$V_{VS}$ = 13.5 V; FREQ: 440 kHz




Oscillator (high frequency)
$V_{VS}$ = 13.5 V; FREQ: 2.2 MHz



# 6 Current consumption and enable

## 6.1 Functional description current consumption and enable

A "high" signal $V_{EN,hi}$ at the EN pin switches on the regulator. In on-state the device can operate at very low current consumption $I_{VS,on}$ to improve the efficiency with low load in PFM mode.

A "low" signal $V_{EN,lo}$ at the EN pin switches the regulator off. In turned off-state, the current consumption $I_{VS,off}$ of the device is 1 µA typically. If the EN pin is left open, then an internal pull-down resistor $R_{EN,int}$ ensures that the device remains switched off.

## 6.2 Electrical characteristics current consumption and enable

**Table 8 Electrical characteristics current consumption and enable**

$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

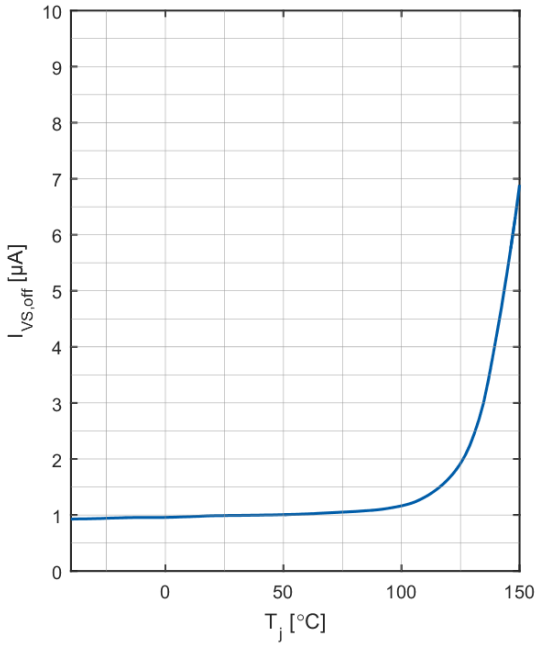
| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Current consumption** | | | | | | | |
| Current consumption in off-state | $I_{VS,off}$ | – | 1 | 2 | µA | $V_{EN}$ = 0 V; $V_{VS}$ = 13.5 V; $T_j$ < 85°C | P_6.2.1 |
| Current consumption in on-state | $I_{VS,on}$ | – | 31 | 65 | µA | $V_{EN}$ = 5.0 V; $V_{VS}$ = 13.5 V; $T_j$ < 85°C; not switching[18)] | P_6.2.2 |
| **Enable** | | | | | | | |
| Enable "high" signal | $V_{EN,hi}$ | 2.0 | – | – | V | – | P_6.2.3 |
| Enable "low" signal | $V_{EN,lo}$ | – | – | 0.8 | V | – | P_6.2.4 |
| Enable hysteresis | $V_{EN,hys}$ | 100 | 400 | 1000 | mV | – | P_6.2.5 |
| Enable "high" input current | $I_{EN,hi,1}$ | – | 0.6 | 1 | µA | $V_{EN}$ = 5.0 V | P_6.2.6 |
| Enable "high" input current | $I_{EN,hi,2}$ | – | 2.5 | 3.5 | µA | $V_{EN}$ = 13.5 V | P_6.2.7 |
| Enable, internal resistor to GND | $R_{EN,int}$ | 5.6 | 8 | 10.4 | MΩ | $V_{EN}$ = 2.0 V | P_6.2.8 |

18 The current consumption is tested while the output voltage is forced to a slightly higher value than the nominal output voltage to prevent switching activities of the regulator.

## 6.3 Typical performance characteristics current consumption and enable

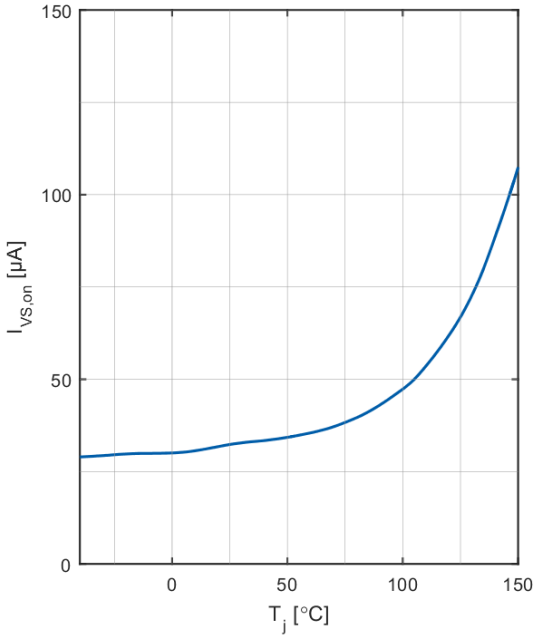
Current consumption in off-state

$V_{VS}$ = 13.5 V; $V_{EN}$ = 0 V



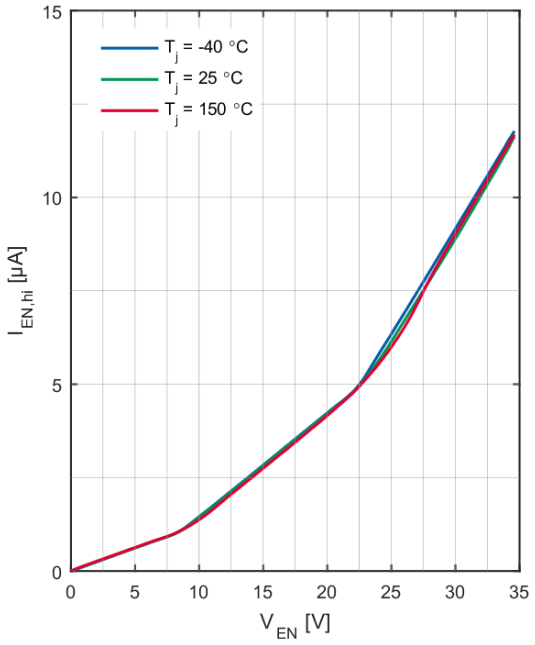

Current consumption in on-state

$V_{VS}$ = 13.5 V; $V_{EN}$ = 5 V; no switching




Enable "high" input current

$V_{VS}$ = 13.5 V



# 7 Reset

## 7.1 Functional description reset

The reset function supervises the regulator output voltage $V_{CC}$ by monitoring the feedback voltage $V_{FB}$. The device indicates the reset status at the RO pin. RO "high" indicates, that the output voltage is within the desired reset thresholds. RO "low" indicates that the output voltage is outside the desired reset thresholds. As long as the device operates within the specified range, the reset function is active, see ***Table 10*** and ***Functional range***.

### Reset output RO

The reset output pin RO is an open drain structure and needs to be pulled up to $V_{CC}$ or to a voltage rail via an external pull-up resistor $R_{RO}$, which must be chosen according to the maximum pull-up current $I_{RO,lo}$. During battery cranking conditions of the input voltage $V_{VS}$, the reset feature is active down to an input voltage $V_{VS}$ of 2.8 V.

### Power-on reset delay time

Power-on reset delay time $t_{RD,PWR-on}$ is the time period from completion of the soft-start until the device releases the reset by switching the reset output RO from "low" to "high", see ***Figure 8***. An external resistor $R_{RT}$ connected to the RT pin determines the value of power-on reset delay time $t_{RD,PWR-on}$, see ***Table 9***.

### Reset undervoltage, overvoltage and delay time

In contrast to the power-on reset delay time $t_{RD,PWR-on}$, the reset delay time $t_{RD}$ refers to an output undervoltage or output overvoltage event during operation, see ***Figure 8***. If $V_{FB}$ drops below the undervoltage reset threshold $V_{RT,UV,th}$, then the device sets the reset signal at the RO to "low". When the output voltage recovers and $V_{FB}$ exceeds the undervoltage reset threshold plus the hysteresis ($V_{RT,UV,th}$ + $V_{RT,UV,hys}$), then the device sets the RO pin to "high" after the reset delay time $t_{RD}$. In accordance with the undervoltage reset delay time, the overvoltage reset delay time $t_{RD}$ considers an output overvoltage event. If case $V_{FB}$ exceeds the overvoltage reset threshold $V_{RT,OV,th}$, then the device sets the RO pin to "low". When the output voltage recovers and $V_{FB}$ drops below the overvoltage reset threshold minus the hysteresis ($V_{RT,OV,th}$ - $V_{RT,OV,hys}$), then the device sets the RO pin to "high" after the reset delay time $t_{RD}$. An external resistor $R_{RT}$ connected to the RT pin determines the value of the reset delay time $t_{RD}$ along with the reset undervoltage threshold $V_{RT,UV,th}$, see ***Table 9***. The device sets the selected reset delay time and reset threshold during initialization phase. The value of the overvoltage reset threshold $V_{RT,OV,th}$ is fixed.

### Reset reaction time

If the output voltage of the regulator drops below the output undervoltage reset threshold $V_{RT,UV,th}$ or rises above the output overvoltage reset threshold $V_{RT,OV,th}$, then this triggers the internal output voltage monitoring circuit. If that condition lasts longer than the blanking time $t_{r,blank}$ (see ***Table 10***), then the device sets the reset signal at the RO pin to "low". If the output overvoltage or undervoltage condition lasts shorter than $t_{r,blank}$, then the device keeps the reset signal "high". This prevents a microcontroller reset due to very short distortions of the output voltage, see ***Figure 8***.

**Table 9 RT configuration for typical values of power-on, undervoltage, overvoltage reset delay time and undervoltage reset threshold**

| $R_{RT}$ [kΩ][19] | $t_{RD,PWR-on}$ [ms] | $t_{RD}$ [ms] | $V_{RT,UV,th}$ [% of $V_{FB}$][20] |
|---|---|---|---|
| ≤ 1.0 (or connect to GND) | 0.06 | 0.03 | -8 |
| 2.2 | 0.06 | 0.03 | -14 |
| 3.3 | 0.06 | 0.03 | -25 |
| 4.7 | 0.06 | 0.03 | -40 |
| 6.8 | 1.9 | 1.3 | -8 |
| 10 | 1.9 | 1.3 | -14 |
| 15 | 1.9 | 1.3 | -25 |
| 22 | 1.9 | 1.3 | -40 |
| 33 | 7.7 | 5.1 | -14 |
| 47 | 7.7 | 5.1 | -25 |
| 68 | 7.7 | 5.1 | -40 |
| 100 | 15.4 | 10.2 | -8 |
| 150 | 15.4 | 10.2 | -14 |
| ≥ 200 (or leave open) | 7.7 | 5.1 | -8 |

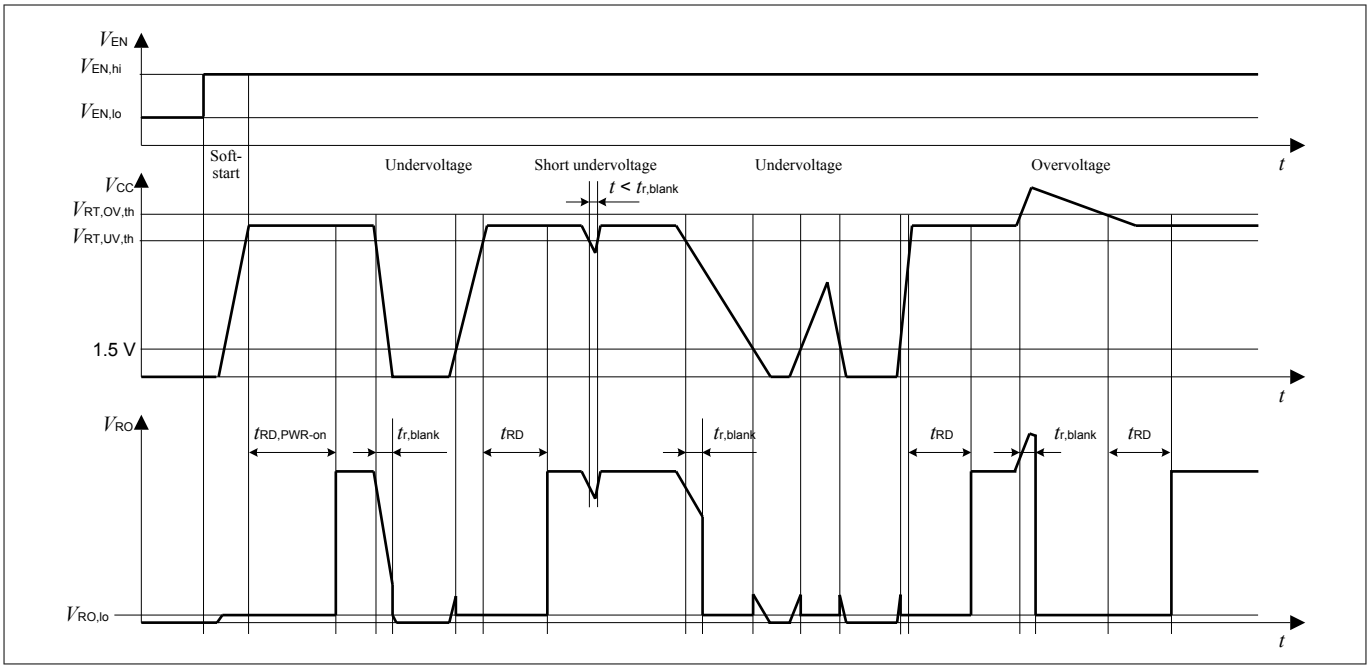



**Figure 8 Reset timing diagram[21]**

19 Resistor tolerance ≤ 5%.

20 In relation to the typical feedback voltage level 3.3 V.

21 The diagram neglects the reset undervoltage hysteresis and reset overvoltage hysteresis to improve the overview. $V_{RO}$ is connected to the output voltage $V_{CC}$ via an external pull-up resistor. The input voltage $V_{VS}$ is set to a level higher than $V_{VS,on}$.

## 7.2 Electrical characteristics reset

**Table 10 Electrical characteristics reset**

$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Reset output RO** | | | | | | | |
| Reset output "low" voltage | $V_{RO,lo}$ | – | – | 0.4 | V | $V_{CC}$ ≥ 1.5 V; $V_{EN}$ ≥ 2 V; $I_{RO}$ ≤ 1.5 mA | P_7.2.1 |
| Reset output "low" pull-up current | $I_{RO,lo}$ | – | – | 1.5 | mA | $V_{EN}$ ≥ 2 V; $V_{RO}$ = 0.4 V | P_7.2.2 |
| Reset output "high" leakage current | $I_{RO,hi}$ | – | – | 1 | µA | $V_{RO}$ = 3.3 V | P_7.2.3 |
| **Output overvoltage reset threshold** | | | | | | | |
| Output overvoltage reset threshold increasing | $V_{RT,OV,th}$ | 5 | 7 | 9 | % | percentage of $V_{FB}$ | P_7.2.4 |
| Output overvoltage reset hysteresis | $V_{RT,OV,hys}$ | – | 1 | 2 | % | percentage of $V_{FB}$ | P_7.2.5 |
| **Output undervoltage reset threshold**[22] | | | | | | | |
| Output undervoltage reset threshold decreasing -8% | $V_{RT,UV,th,1}$ | -10 | -8 | -6 | % | percentage of $V_{FB}$ | P_7.2.6 |
| Output undervoltage reset threshold decreasing -14% | $V_{RT,UV,th,2}$ | -16 | -14 | -12 | % | percentage of $V_{FB}$ | P_7.2.7 |
| Output undervoltage reset threshold decreasing -25% | $V_{RT,UV,th,3}$ | -27 | -25 | -23 | % | percentage of $V_{FB}$ | P_7.2.8 |
| Output undervoltage reset threshold decreasing -40% | $V_{RT,UV,th,4}$ | -42 | -40 | -38 | % | percentage of $V_{FB}$ | P_7.2.9 |
| Output undervoltage reset hysteresis | $V_{RT,UV,hys}$ | – | 1 | 2 | % | percentage of $V_{FB}$ | P_7.2.10 |
| **Reset delay timing**[22] | | | | | | | |
| Power-on reset delay time 60 µs | $t_{RD,PWR-on,1}$ | 15 | 60 | 90 | µs | – | P_7.2.11 |
| Power-on reset delay time 1.9 ms | $t_{RD,PWR-on,2}$ | 1.7 | 1.9 | 2.2 | ms | – | P_7.2.12 |
| Power-on reset delay time 7.7 ms | $t_{RD,PWR-on,3}$ | 6.9 | 7.7 | 8.6 | ms | – | P_7.2.13 |
| Power-on reset delay time 15.4 ms | $t_{RD,PWR-on,4}$ | 13.9 | 15.4 | 17.1 | ms | – | P_7.2.14 |

22 For RT configuration see ***Table 9***

## Reset

**Table 10 Electrical characteristics reset (continued)**

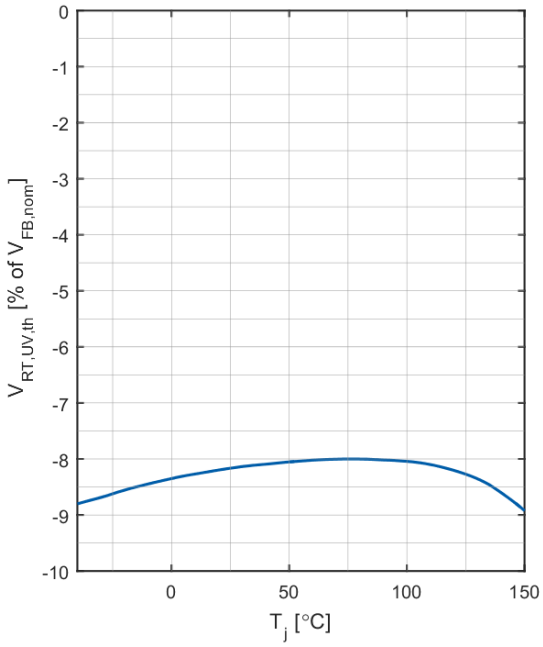
$V_{VS}$ = 6 V to 35 V; $T_j$ = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Reset delay time 30 µs | $t_{RD,1}$ | 15 | 30 | 95 | µs | – | P_7.2.15 |
| Reset delay time 1.3 ms | $t_{RD,2}$ | 1.1 | 1.3 | 1.5 | ms | – | P_7.2.16 |
| Reset delay time 5.1 ms | $t_{RD,3}$ | 4.6 | 5.1 | 5.7 | ms | – | P_7.2.17 |
| Reset delay time 10.2 ms | $t_{RD,4}$ | 9.3 | 10.2 | 11.4 | ms | – | P_7.2.18 |
| Reset blanking time | $t_{r,blank}$ | 2 | 5 | 10 | µs | – | P_7.2.19 |

## 7.3 Typical performance characteristics reset

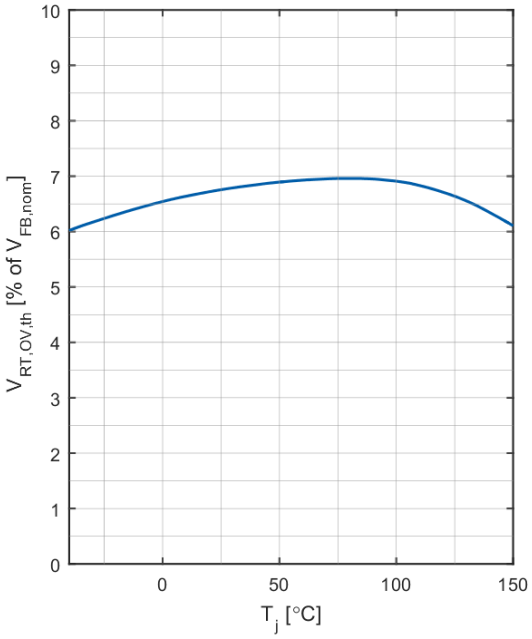
Output undervoltage reset threshold

$V_{VS}$ = 13.5 V




Output overvoltage reset threshold

$V_{VS}$ = 13.5 V



# 8 Application information

*Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

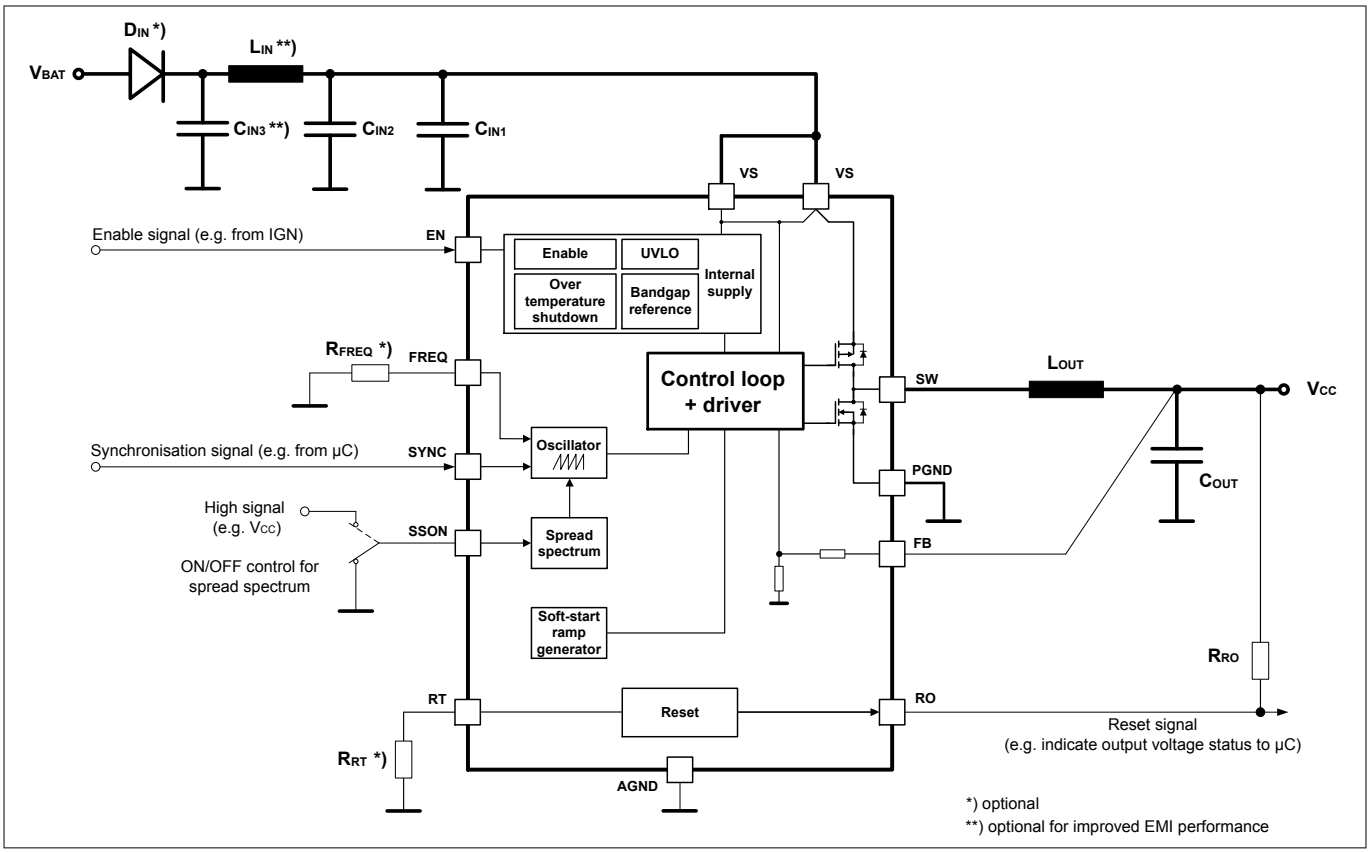



**Figure 9 Application diagram**

*Note: This figure is a simplified example of an application circuit. The function must be verified in the application.*

## Application information

**Table 11 Recommended values for components in the application diagram**

| Name | Value[23] | Switching frequency | Component type |
|---|---|---|---|
| $C_{IN1}$ | 100 nF | – | Ceramic X7R capacitor; 50 V |
| $C_{IN2}$ | 10 µF | – | Ceramic X7R capacitor; 50 V |
| $L_{OUT}$ | 22 µH | 320 kHz to 560 kHz | Shielded power inductor; $I_{SAT} > I_{BUOC}$<br>$DCR < 70$ mΩ |
| $C_{OUT}$ | 88 µF[24] | 320 kHz to 560 kHz | 22 µF (x4) ceramic X7R capacitor; 16 V |
| $L_{OUT}$ | 2.2 µH | 1.6 MHz to 2.8 MHz | Shielded power inductor; $I_{SAT} > I_{BUOC}$<br>$DCR < 70$ mΩ |
| $C_{OUT}$ | 44 µF[24] | 1.6 MHz to 2.8 MHz | 22 µF (x2) ceramic X7R capacitor; 16 V |

23 Typical condition

24 For maintenance of loop stability it is recommended to use capacitors with a limited voltage derating at the typical output voltage level. A capacitor in parallel can be added to match the recommended typical capacitance value as close as possible.

## 8.1 Layout recommendations

### Introduction

A switch mode power supply is a potential source of electromagnetic disturbance, which may affect the application environment as well as the device itself. This can lead to sporadic malfunction including regulator instability or irreversible damage depending on the amount of generated disturbance.

Main types of electromagnetic disturbance:

- Radiated emission
- Conducted emission

### Radiated emission

Radiated emission is caused by circulating currents and voltage oscillations. Alternating currents appear in so called current windows, which are defined by the area of the circulating current within the corresponding filter stage at the input or the output of the regulator. Voltage oscillations are mainly caused by resonant circuits induced by parasitic inductance and capacitance of the PCB layout.

The following PCB layout design recommendations help to minimize radiated emission:

- Place external components close to the device to reduce parasitic elements of the PCB layout and to keep the area of circulating currents small. At the same time some distance should be kept between the components to avoid coupling.
- Reduce the switching area at pin SW to minimize the inductance and especially the parasitic capacitance. The parasitic capacitance can be further reduced by removing inner GND layers below the switching area. Routing of other signal traces below the switching area should be avoided generally.
- Use GND layers to shield areas with alternating currents or voltage oscillations.

### Conducted emission

Conducted emission consists of voltage oscillations, which occur permanently or by occasion at the regulator input or output connection. Their frequency range can exceed 100 MHz and they are superimposed to the input voltage $V_{VS}$ and to the output voltage $V_{CC}$. This might disturb other components of the application.

Countermeasures against conducted disturbances are the same as against radiated emission. The following recommendations can further reduce the conducted emission:

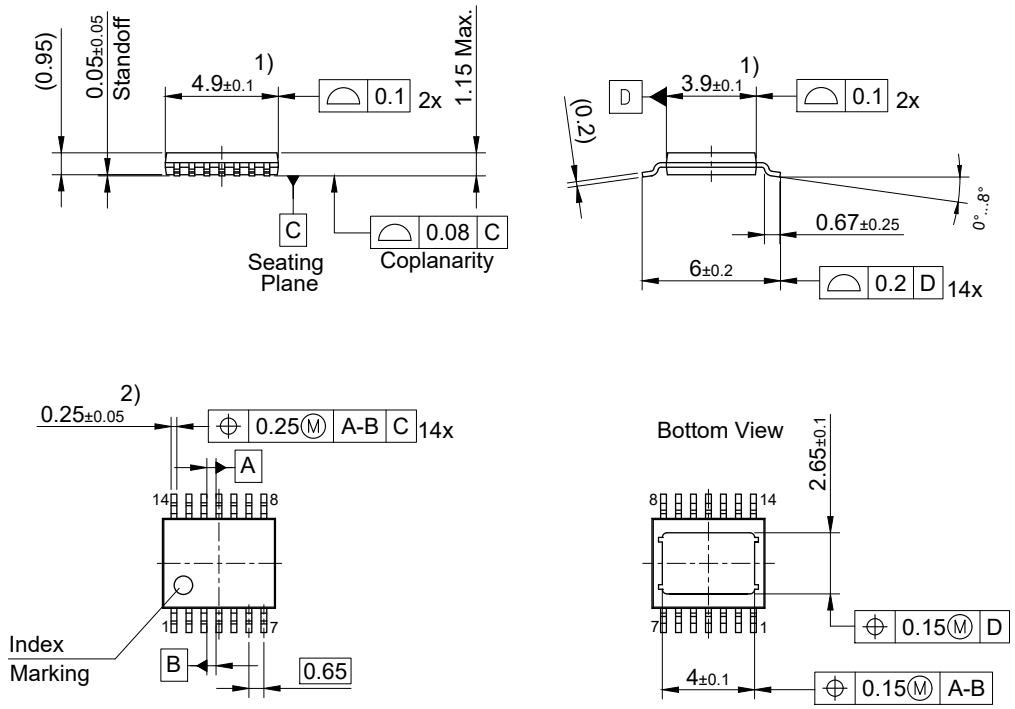
- Reduce high frequency conducted emission by placing well connected small ceramic filter capacitors (1 nF to 220 nF) with low ESR and low ESL in parallel to the input capacitors as close as possible to the input pin VS and in parallel to the output capacitor $C_{OUT}$ close to the output inductor $L_{OUT}$.
- Reduce noise injected into the battery supply line by using a π-filter, for example consisting of $C_{IN1}$, $C_{IN2}$, $C_{IN3}$ and $L_{IN}$. This requires additional capacitors and an inductor. The filter must be designed according to the requirements of the application.

## 8.2 Additional information

Please contact Infineon:

- for information regarding the pin behavioral assessment
- for application notes with more detailed information about this device
- for any further information visit ***https://www.infineon.com/***

# 9 Package information




1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

**Figure 10 PG-TSDSO-14**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Information on alternative packages

Please visit ***www.infineon.com/packages***.

# Revision history

| Version | Date | Changes |
|---|---|---|
| Rev. 1.0 | 2020-03-20 | Initial datasheet |

**Trademarks**

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2020-03-20**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2020 Infineon Technologies AG**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: erratum@infineon.com**

**Document reference**
**IFX-Z8F61444282**

**IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury