1.5 Ω On Resistance, ± 15 V / +12 V / ± 5 V, Quad SPST Switches

DESCRIPTION

The DG1411E, DG1412E, DG1413E are ± 15 V precision monolithic quad single-pole single-throw (SPST) CMOS analog switches. Built on a new CMOS process, the Vishay Siliconix DG1411E, DG1412E, and DG1413E offer low on-resistance of 1.5 Ω. The low and flat resistance over the full signal range ensures excellent linearity and low signal distortion. The new CMOS platform provides low power dissipation, minimized parasitic capacitance, and low charge injection.

The devices operate from either a single 4.5 V to 24 V power supply, or from dual ± 4.5 V to ± 15 V power supplies. The analog switches do not require a V_L logic supply, while all digital inputs have 0.8 V and 2 V logic thresholds to ensure low voltage TTL / CMOS compatibility.

The DG1411E, DG1412E, and DG1413E are bi-directional and support analog signals up to the supply voltage when on, and block them when off. The devices each feature four independently selectable SPST switches. The DG1411E is normally closed, while the DG1412E is normally open. The DG1413E has two normally open and two normally closed switches with guaranteed break-before-make operation.

Combined with fast 70 ns switching time, low and flat switch resistance. The devices are ideal for signal switching and relay replacement in data acquisition, industrial control and automation, communication, and A/V systems, in addition to medical instrumentation and automated test equipment.

The switches are available in RoHS-compliant, halogen-free TSSOP16 and QFN16 4 mm by 4 mm packages.

FEATURES

- 35 V supply max. rating
- On-resistance: 1.5 Ω
- On-resistance flatness: 0.2 Ω
- Channel to channel on-resistance match: 0.04 Ω
- Supports single and dual supply operation
- Fully specified at ± 15 V, ± 5 V, and +12 V
- Integrated V_L supply
- 3 V logic compatible
- Low parasitic capacitance: $C_{S(OFF)}$: 24 pF, $C_{D(ON)}$: 87 pF
- Rail to rail signal handling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

BENEFITS

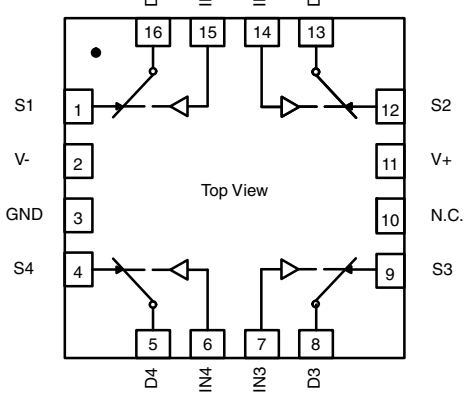
- Low insertion loss
- Low distortion
- Break-before-make switching
- Low charge injection over the full signal range

APPLICATIONS

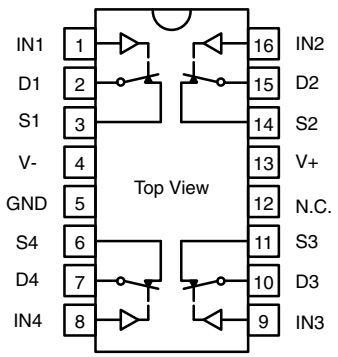
- Medical and healthcare equipment
- Data acquisition system
- Industrial control and automation
- Test and measurement equipment
- Communication systems
- Battery powered systems
- Sample and hold circuits
- Audio and video signal switching
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1411E

DG1411EEN
QFN-16 (4 mm x 4 mm)



DG1411EEQ
TSSOP



TRUTH TABLE - DG1411E	
LOGIC	SWITCH
0	On
1	Off

Notes

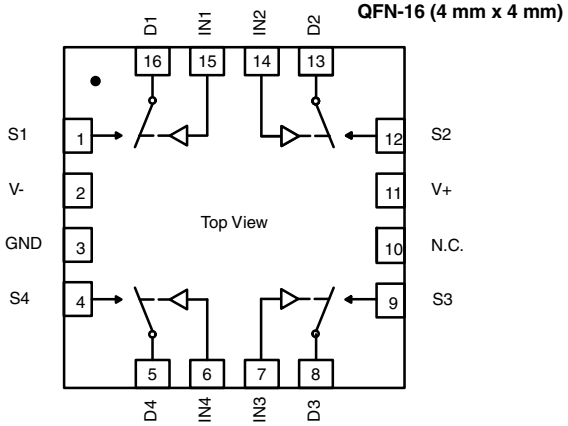
- QFN exposed pad tied to V-
- N.C. = no connect
- Switches shown for logic “0” input

For technical questions, contact: analogswitchtechsupport@vishay.com

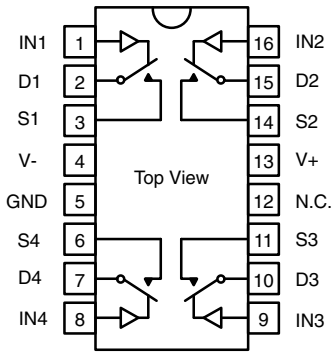
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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1412E

DG1412EEN
QFN-16 (4 mm x 4 mm)



DG1412EEQ
TSSOP

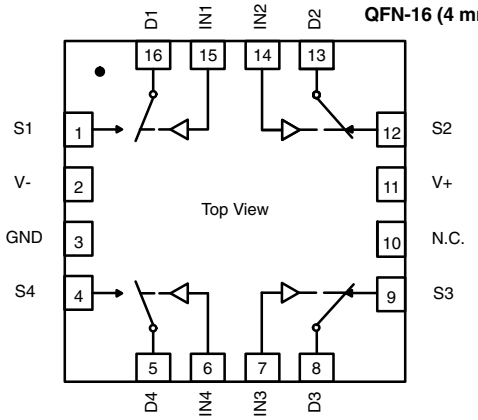


TRUTH TABLE - DG1412E	
LOGIC	**SWITCH**
0	Off
1	On

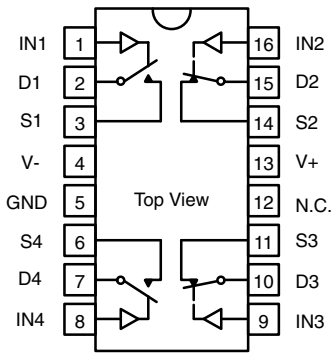
Notes
- QFN exposed pad tied to V-
- N.C. = no connect
- Switches shown for logic “0” input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1413E

DG1413EEN
QFN-16 (4 mm x 4 mm)



DG1413EEQ
TSSOP



TRUTH TABLE - DG1413E		
LOGIC	**SWITCHES 1, 4**	**SWITCHES 2, 3**
0	Off	On
1	On	Off

Notes
- QFN exposed pad tied to V-
- N.C. = no connect
- Switches shown for logic “0” input

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DEVICE OPTIONS

PART NUMBER	CONFIGURATION	SWITCH FUNCTION	TEMPERATURE RANGE	PACKAGE
DG1411EEN-T1-GE4	Quad SPST	NC	-40 °C to +125 °C	QFN (4 mm x 4 mm) 16L (variation 2)
DG1412EEN-T1-GE4	Quad SPST	NO	-40 °C to +125 °C	QFN (4 mm x 4 mm) 16L (variation 2)
DG1413EEN-T1-GE4	Quad SPST	NC / NO	-40 °C to +125 °C	QFN (4 mm x 4 mm) 16L (variation 2)
DG1411EEQ-T1-GE4	Quad SPST	NC	-40 °C to +125 °C	TSSOP-16
DG1412EEQ-T1-GE4	Quad SPST	NO	-40 °C to +125 °C	TSSOP-16
DG1413EEQ-T1-GE4	Quad SPST	NC / NO	-40 °C to +125 °C	TSSOP-16

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETER	CONDITIONS	LIMITS	UNIT
V+	Reference to GND	-0.3 to +25	V
V-	Reference to GND	+0.3 to -25	
V+ to V-		+35	
Analog inputs (S or D)		(V-) - 0.3 to (V+) + 0.3	
Digital inputs		GND - 0.3 to (V+) + 0.3	
Maximum continuous switch current	TSSOP-16, T_A = 25 °C	190	mA
	QFN (4 mm x 4 mm) 16L, T_A = 25 °C	250	
	TSSOP-16, T_A = 125 °C	90	
	QFN (4 mm x 4 mm) 16L, T_A = 125 °C	100	
Maximum pulse switch current	Pulse at 1 ms, 10 % duty cycle	500	
Thermal resistance	TSSOP-16	130	°C/W
	QFN (4 mm x 4 mm) 16L	32	
ESD / HBM	JS-001	2000	V
ESD / CDM	JS-002	750	
Latch up	JESD78	300	mA
Temperature			
Operating temperature		-40 to +125	°C
Max. operating junction temperature		150	
Operating junction temperature		125	
Storage temperature		-65 to +150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS - ± 15 V supply							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 15 V, V- = -15 V V_{INH} = 2 V, V_{INL} = 0.8 V	**+25 °C**	**-40 °C to +85 °C**	**-40 °C to +125 °C**	**TYP. / MAX.**	**UNIT**
Analog Switch							
Analog signal range	V_{ANALOG}		V- to V+			-	V
Drain-source on-resistance	$R_{DS(on)}$	V_S = ± 10 V, I_S = -10 mA V+ = 13.5 V, V- = -13.5 V	1.5	-	-	Typ.	Ω
			1.8	2	2.3	Max.	
On-resistance flatness	$R_{flat(on)}$	V_S = ± 10 V, I_S = -10 mA	0.2	-	-	-	Ω
			0.42	0.45	0.48	Max.	
On-resistance matching	$\Delta R_{DS(on)}$		0.04	-	-	Typ.	
			0.22	0.23	0.24	Max.	
Switch off leakage current	$I_S/I_{d(off)}$	V+ = 16.5 V, V- = -16.5 V V_S = ± 10 V, V_D = ∓ 10 V	± 0.01	-	-	Typ.	nA
			± 0.5	± 2	± 12	Max.	
Channel on leakage current	$I_{d(on)}$	V_S = V_D = ± 10 V	± 0.05	-	-	Typ.	
			± 1	± 3	± 40	Max.	
Digital Control							
Input, high voltage	V_{INH}		-	-	2	$V_{min.}$	V
Input, low voltage	V_{INL}		-	-	0.8	$V_{max.}$	
Input leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.001	-	-	Typ.	µA
			-	-	± 0.1	Max.	
Digital input capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-before-make time	t_{OPEN}	V_{S1}= V_{S2} = 10 V R_L= 300 Ω, C_L = 35 pF	24	-	-	Typ.	ns
			-	-	10	Min.	
Turn-on time	t_{ON}	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	70	-	-	Typ.	
			110	130	140	Max.	
Turn-off time	t_{OFF}		50	-	-	Typ.	
			90	100	110	Max.	
Charge injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 0 V	-41	-	-	Typ.	pC
Off isolation	OIRR	C_L = 5 pF, R_L = 50 Ω, 100 kHz	-78	-	-	Typ.	dB
Cross talk	X_{TALK}	C_L = 5 pF, R_L = 50 Ω, 1 MHz	-104	-	-	Typ.	
Insertion loss		f = 1MHz, R_L = 50 Ω, C_L = 5 pF	-0.16	-	-	Typ.	
Total harmonic distortion	THD	R_L = 110 Ω, 15 V_{p-p}, f = 20 Hz to 20 kHz	0.0039	-	-	Typ.	%
Bandwidth, -3 dB	BW	C_L = 5 pF, R_L = 50 Ω	150	-	-	Typ.	MHz
Source off capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	24	-	-	Typ.	pF
Drain off capacitance	$C_{D(off)}$		23	-	-	Typ.	
Drain on capacitance	$C_{D(on)}$		87	-	-	Typ.	
Power Requirements							
Power supply range		GND = 0 V	± 4.5 V min. / ± 16.5 max.				V
Power supply current	I+	Digital inputs 0 or V+ V+ = 16.5 V, V- = -16.5 V	0.001	-	-	Typ.	µA
			-	-	1	Max.	
		IN1 = IN2 = IN3 = IN4 = 5 V	113	-	-	Typ.	
			-	260	290	Max.	
	I-	Digital inputs 0 or V+	0.001	-	-	Typ.	
			-	-	1	Max.	

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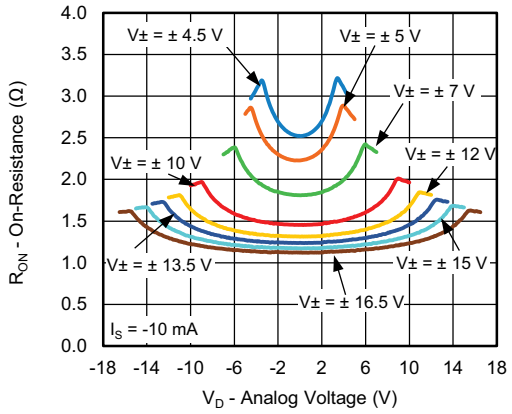
ELECTRICAL CHARACTERISTICS - Single 12 V supply							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 12 V, V- = -0 V V_{INH} = 2 V, V_{INL} = 0.8 V	**+25 °C**	**-40 °C to +85 °C**	**-40 °C to +125 °C**	**TYP. / MAX.**	**UNIT**
Analog Switch							
Analog signal range	V_{ANALOG}		0 to V+				V
Drain-source on-resistance	$R_{DS(on)}$	V_S = 0 V to 10 V, I_S = -10 mA; V+ = 10.8 V, V- = 0 V	2.5	-	-	Typ.	Ω
			3.1	3.8	4.4	Max.	
On-resistance flatness	$R_{flat(on)}$	V_S = 0 V to 10 V; I_S = -10 mA	0.7	-	-	Typ.	Ω
			0.9	1	1.1	Max.	
On-resistance matching	$\Delta R_{DS(on)}$		0.04	-	-	Typ.	
			0.19	0.22	0.25	Max.	
Switch off leakage current	$I_S/I_{d(off)}$	V+ = 10.8 V, V- = 0 V V_S = 1 V/10 V; V_D = 10 V/1 V	± 0.02	-	-	Typ.	nA
			± 0.55	± 1.2	± 10	Max.	
Channel on leakage current	$I_{d(on)}$	V_S = V_D = 3.2 V/10 V	± 0.01	-	-	Typ.	
			± 1	± 2	± 35	Max.	
Digital Control							
Input, high voltage	V_{INH}		-	-	2	Min.	V
Input, low voltage	V_{INL}		-	-	0.8	Max.	
Input leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.001	-	-	Typ.	µA
			-	-	± 0.1	Max.	
Digital input capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-before-make time	t_{OPEN}	V_{S1}= V_{S2} = 8 V R_L= 300 Ω, C_L = 35 pF	90	-	-	Typ.	ns
			-	-	50	Min.	
Turn-on time	t_{ON}	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	150	-	-	Typ.	
			190	230	260	Max.	
Turn-off time	t_{OFF}		60	-	-	Typ.	
			100	110	120	Max.	
Charge injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 6 V	6	-	-	Typ.	pC
Off isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, 100 kHz	-78	-	-	Typ.	dB
Cross talk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, 1 MHz	-106	-	-	Typ.	
Insertion loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF	-0.23	-	-	Typ.	
Bandwidth, -3 dB	BW	R_L = 50 Ω, C_L = 5 pF	150	-	-	Typ.	MHz
Source off capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 6 V	31	-	-	Typ.	pF
Drain off capacitance	$C_{D(off)}$		29	-	-	Typ.	
Drain on capacitance	$C_{D(on)}$		93	-	-	Typ.	
Power Requirements							
Power supply range		GND = 0 V, V- = 0 V	± 5 V min. / ± 16.5 max.				V
Power supply current	I+	Digital inputs 0 or V+ V+ = 13.2 V	0.001	-	-	Typ.	µA
			-	-	1	Max.	
		IN1 = IN2 = IN3 = IN4 = 5 V	54	-	-	Typ.	
			-	150	190	Max.	

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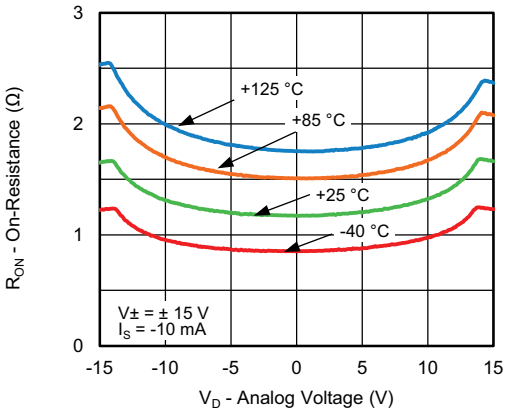
ELECTRICAL CHARACTERISTICS - ± 5 V supply							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = -5 V V_{INH} = 2 V, V_{INL} = 0.8 V	**+25 °C**	**-40 °C to +85 °C**	**-40 °C to +125 °C**	**TYP. / MAX.**	**UNIT**
Analog Switch							
Analog signal range	V_{ANALOG}		V- to V+				V
Drain-source on-resistance	$R_{DS(on)}$	V_S = ± 4.5 V, I_S = -10 mA V+ = 4.5 V, V- = -4.5 V	3	-	-	Typ.	Ω
			3.3	4	4.7	Max.	
On-resistance flatness	$R_{flat(on)}$	V_S = ± 4.5 V, I_S = -10 mA	0.7	-	-	Typ.	
			0.9	1	1.1	Max.	
On-resistance matching	$\Delta R_{DS(on)}$		0.04	-	-	Typ.	
			0.19	0.22	0.25	Max.	
Switch off leakage current	$I_S/I_{d(off)}$	V+ = 5.5 V, V- = -5.5 V V_S = ± 4.5 V, V_D = ∓ 4.5 V	± 0.004	-	-	Typ.	nA
			± 0.5	± 1.5	± 10	Max.	
Channel on leakage current	$I_{d(on)}$	V_S = V_D = ± 4.5 V	± 0.003	-	-	Typ.	
			± 0.5	± 2	± 35	Max.	
Digital Control							
Input, high voltage	V_{INH}		-	-	2	Min.	V
Input, low voltage	V_{INL}		-	-	0.8	Max.	
Input leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.001	-	-	Typ.	µA
			-	-	± 0.1	Max.	
Digital input capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-before-make time	t_{OPEN}	V_{S1}= V_{S2} = 3 V R_L= 300 Ω, C_L = 35 pF	110	-	-	Typ.	ns
			-	-	65	Min.	
Turn-on time	t_{ON}	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	280	-	-	Typ.	
			330	400	440	Max.	
Turn-off time	t_{OFF}		180	-	-	Typ.	
			220	260	280	Max.	
Charge injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 0 V	7	-	-	Typ.	pC
Off isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, 100 kHz	-78	-	-	Typ.	dB
Cross talk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, 1 MHz	-106	-	-	Typ.	
Insertion loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF	-0.26	-	-	Typ.	%
Bandwidth, -3 dB	BW	R_L = 50 Ω, C_L = 5 pF	160	-	-	Typ.	MHz
Source off capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	34	-	-	Typ.	pF
Drain off capacitance	$C_{D(off)}$		31	-	-	Typ.	
Drain on capacitance	$C_{D(on)}$		94	-	-	Typ.	
Power Requirements							
Power supply range		GND = 0 V	± 4.5 V min. / ± 16.5 max.				V
Power supply current	I+	Digital inputs 0 V or V+ V+ = 5.5 V, V- = -5.5 V	0.001	-	-	Typ.	µA
			-	-	1	Max.	
	I-	Digital inputs = 0 V or V+	0.001	-	-	Typ.	
			-	-	1	Max.	

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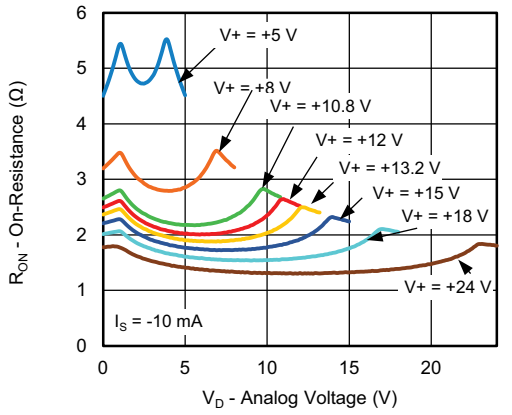
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



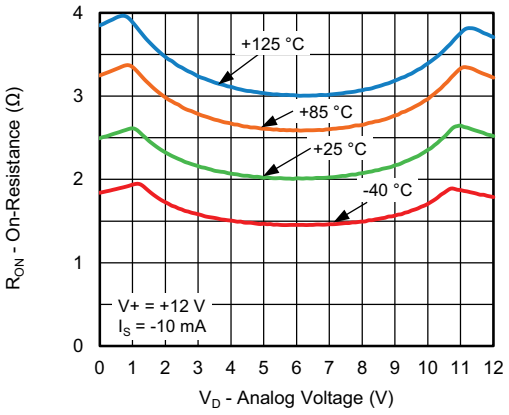
On-Resistance vs. Analog Voltage



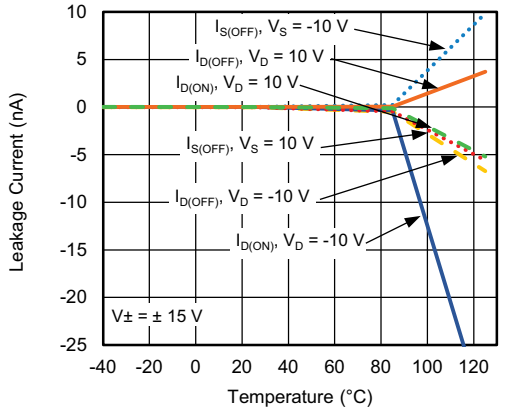
On-Resistance vs. Temperature



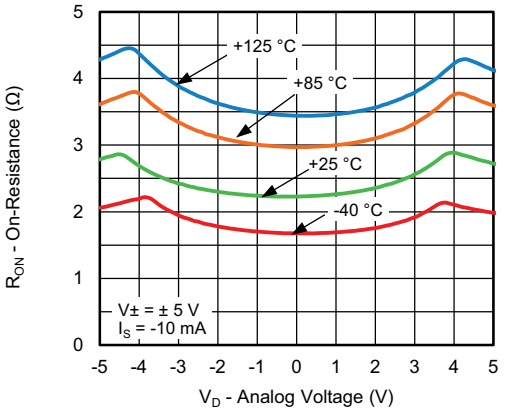
On-Resistance vs. Analog Voltage



On-Resistance vs. Temperature



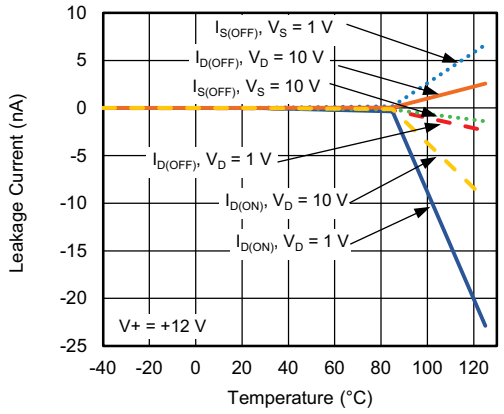
Leakage Current vs. Temperature



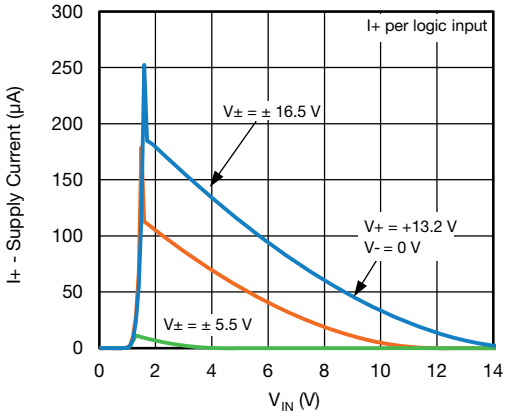
On-Resistance vs. Temperature

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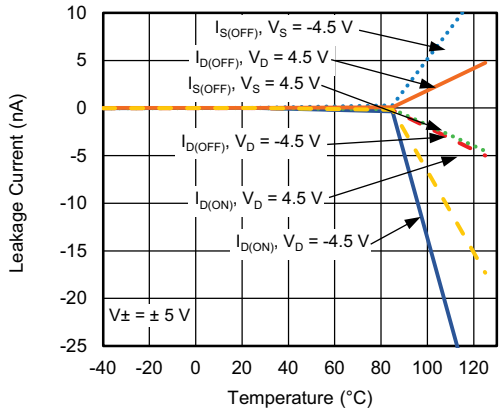
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



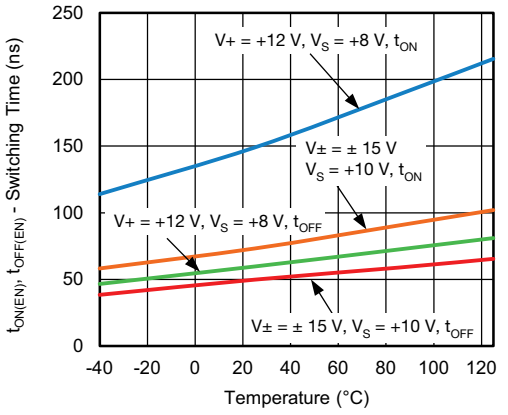
Leakage Current vs. Temperature



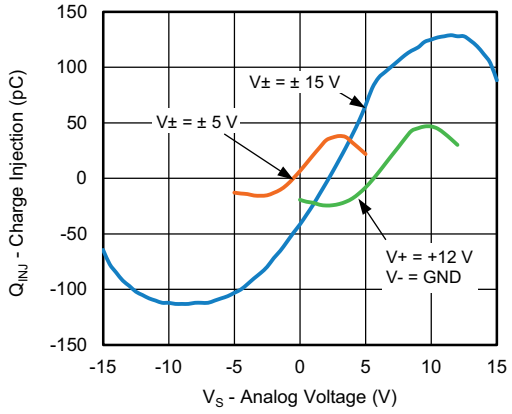
I+ - Supply Current vs. Logic Level



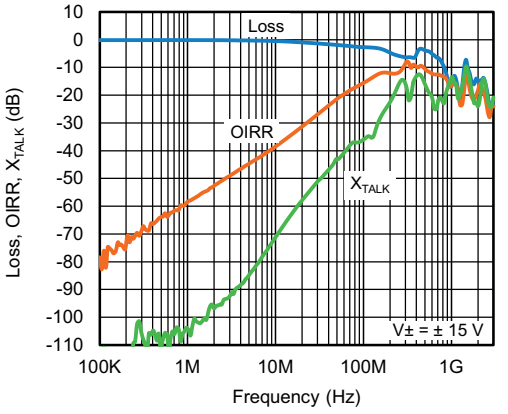
Leakage Current vs. Temperature



Switching Time vs. Temperature



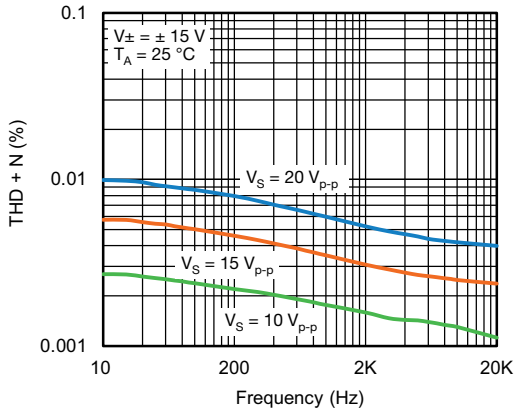
Charge Injection vs. Analog Voltage



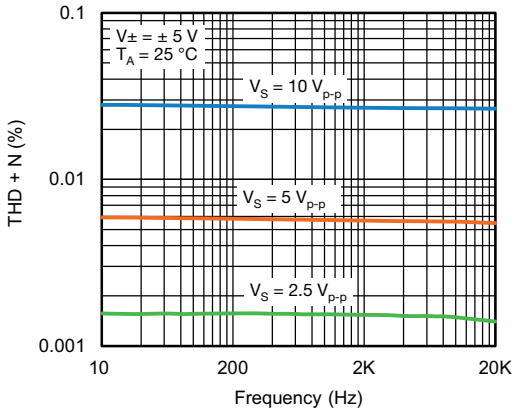
BW, OIRR, X_{TALK} vs. Frequency

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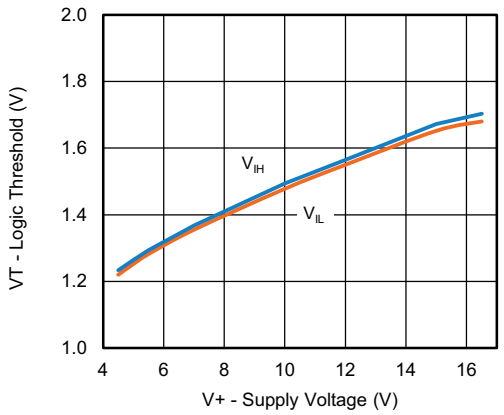
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



THD + N vs. Frequency



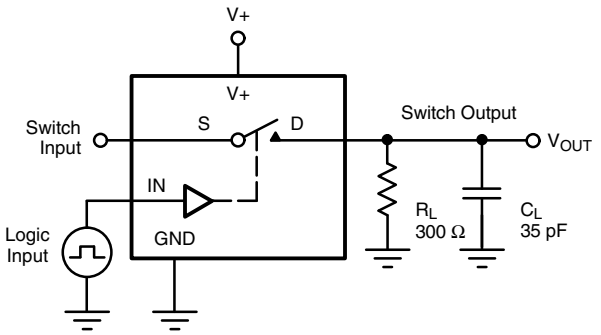
THD + N vs. Frequency



Logic Threshold vs. Supply Voltage

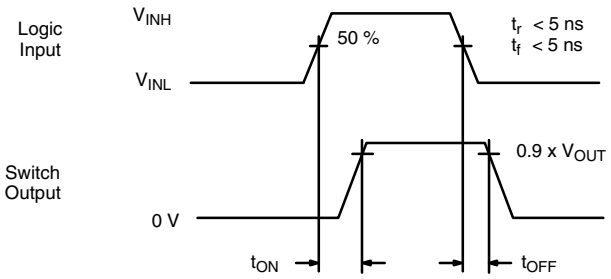
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TEST CIRCUITS



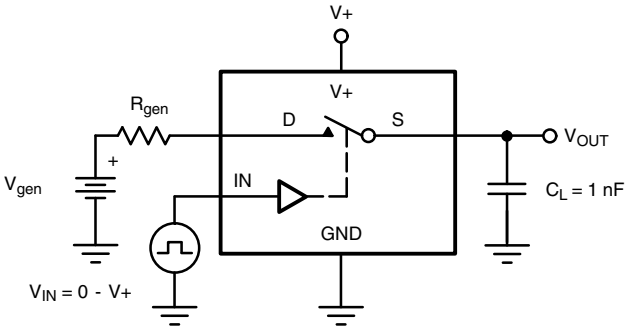
C_L (includes fixture and stray capacitance)

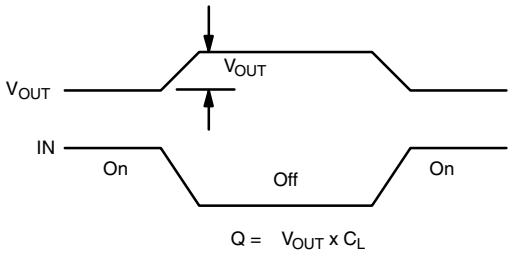
$$V_{OUT} = V_D \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time





IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 2 - Charge Injection

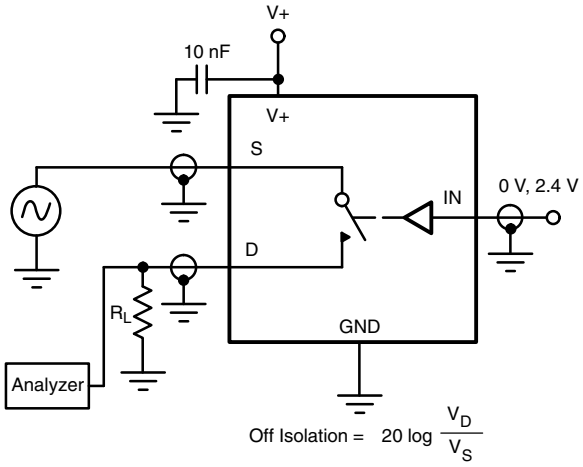


Fig. 3 - Off-Isolation

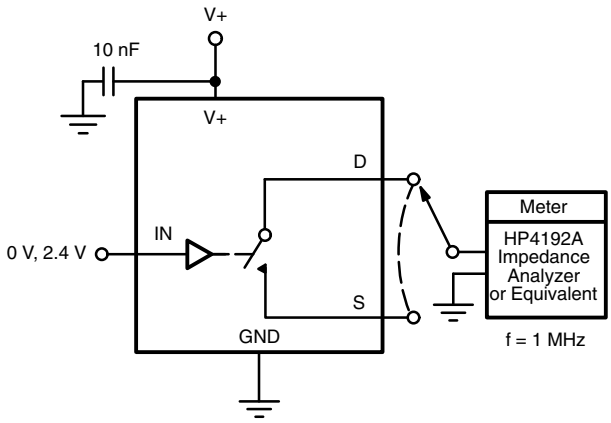
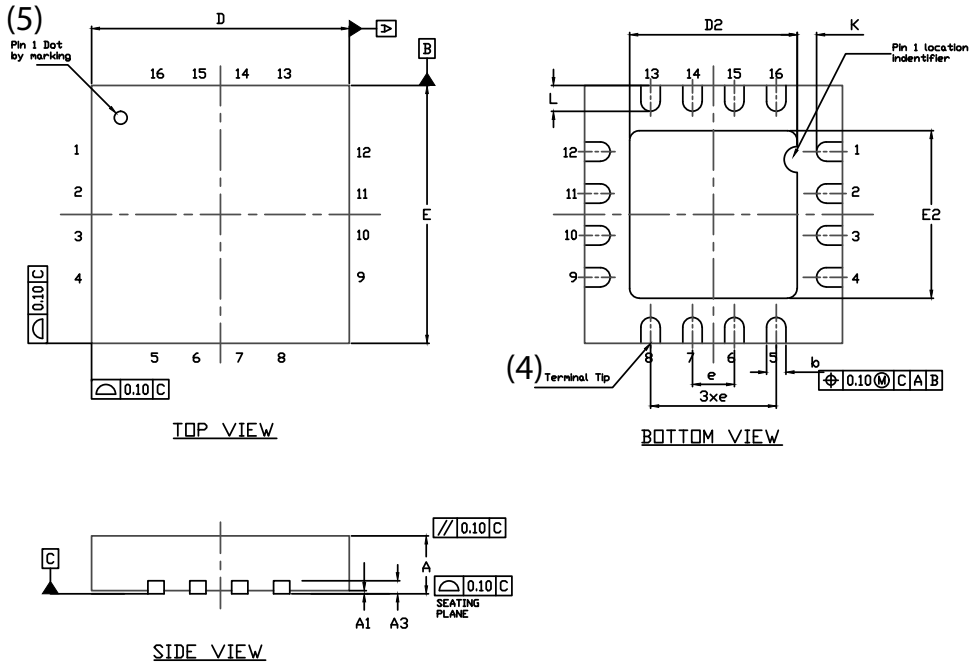


Fig. 4 - Channel Off/On Capacitance

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QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

Notes

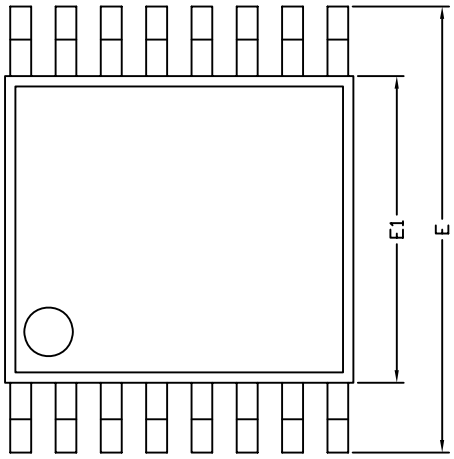
(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

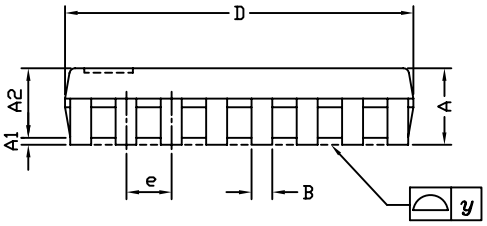
ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890

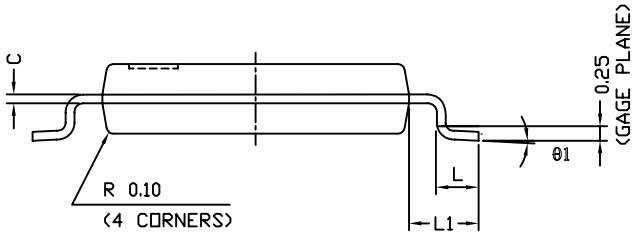
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TSSOP: 16-LEAD

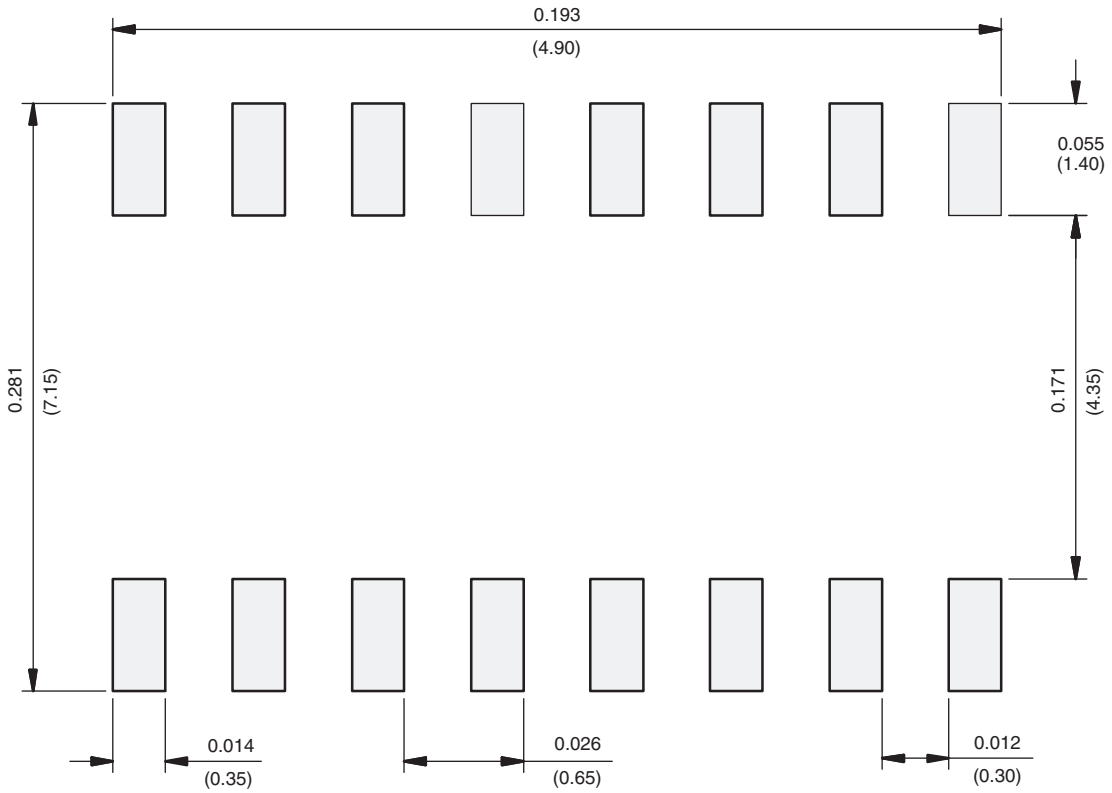






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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