TLV62150x 4-V to 17-V 1-A Step-Down Converter With DCS-Control™

1 Features

- DCS-Control™ Topology
- Input Voltage Range: 4 V to 17 V
- Up to 1-A Output Current
- Adjustable Output Voltage from 0.9 to 5 V
- Pin-Selectable Output Voltage (nominal, + 5%)
- Programmable Soft Start and Tracking
- Seamless Power Save Mode Transition
- Quiescent Current of 19 µA (Typical)
- Selectable Operating Frequency
- Power Good Output
- 100% Duty Cycle Mode
- Short Circuit Protection
- Over Temperature Protection
- For Improved Feature Set, see TPS62150
- Available in a 3-mm × 3-mm, VQFN-16 Package

2 Applications

- Standard 12-V Rail Supplies
- POL Supplies from Single or Multiple Li-Ion Batteries
- Embedded Systems
- LDO Replacements
- Mobile PC's, Tablets, Modems, Cameras

3 Description

The TLV62150x device is an easy-to-use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by use of the DCS-Control™ topology.

With their wide operating input voltage range of 4 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other batteries as well as from 12 V intermediate power rails. It supports up to 1-A continuous output current at output voltages between 0.9 V and 5 V (with 100% duty cycle mode).

The output voltage startup ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the Enable and open-drain Power Good pins.

In Power Save Mode, the devices draw quiescent current of about 19 µA from VIN. Power Save Mode, entered automatically and seamlessly if load is small, maintains high efficiency over the entire load range. In Shutdown Mode, the device is turned off and shutdown current consumption is less than 2 µA.

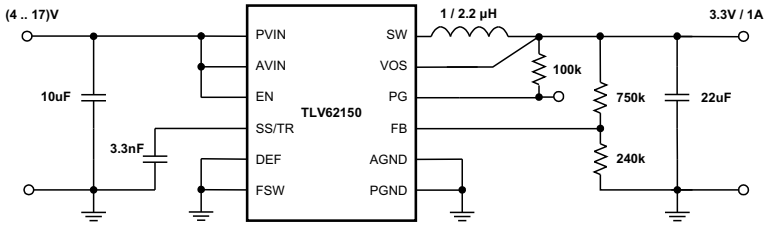
The devices is packaged in a 16-pin VQFN package measuring 3 mm × 3 mm (RGT).

Device Information(1)

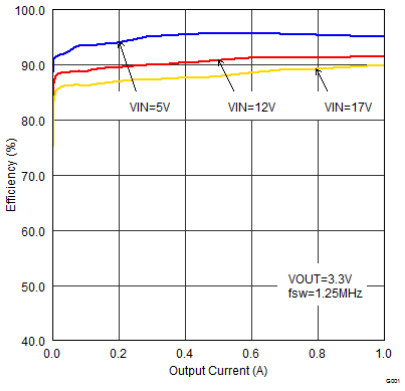
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62150	VQFN (16)	3.00 mm × 3.00 mm
TLV62150A		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D — **Page**

- Changed Power Good Threshold Voltage, Falling (%V_{OUT}) MAX spec from 93% to 94% ... 5

Changes from Revision B (June 2013) to Revision C — **Page**

- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device* and *Documentation Support section,* and *Mechanical, Packaging*, and *Orderable Information section* ... 1

Changes from Revision A (February 2013) to Revision B — **Page**

- Added new device version TLV62150A to data sheet ... 1
- Added text to Power Good section regarding the TLV62150A function. ... 8
- Added additional option to the footnote for Pin-Selectable Output Voltage (DEF) section. ... 8
- Added text to Frequency Selection (FSW) section regarding pin control. ... 8
- Added text to Tracking Function section for clarification. ... 14
- Changed schematic for Figure 38 ... 22

Changes from Original (February 2012) to Revision A — **Page**

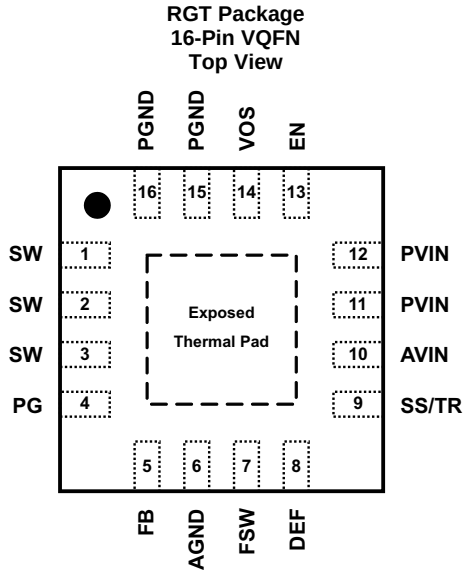
- Added text to Terminal Functions table to clarify Description for AGND, PGND, and Exposed Thermal Pad. ... 3
- Added text to Power Save Mode Operation section for clarification. ... 9
- Changed text in the Layout Considerations section for clarification. ... 25

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5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	POWER GOOD LOGIC LEVEL (EN=Low)
TLV62150	Adjustable	High Impedance
TLV62150A	Adjustable	Low

6 Pin Configuration and Functions



Pin Functions

PIN[1]		I/O	DESCRIPTION
NAME	NO.		
AGND	6	—	Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
AVIN	10	I	Supply voltage for control circuitry. Connect to same source as PVIN.
DEF	8	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%)[2]
EN	13	I	Enable input (High = enabled, Low = disabled)[2]
FB	5	I	Voltage feedback. Connect resistive voltage divider to this pin.
FSW	7	I	Switching Frequency Select (Low ≈ 2.5 MHz, High ≈ 1.25 MHz[3] for typical operation)[2]
SW	1,2,3	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	4	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor)
PGND	15,16	—	Power ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
PVIN	11,12	I	Supply voltage for power stage. Connect to same source as AVIN.
SS/TR	9	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
VOS	14	I	Output voltage sense pin and connection for the control loop circuitry.
Exposed Thermal Pad	—	—	Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane. See the *Layout Example*. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.
(2) An internal pull-down resistor keeps logic level low, if pin is floating.
(3) Connect FSW to VOUT or PG in this case.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage (2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN}+0.3	
	SW	–0.3	V_{IN}+0.3	V
	DEF, FSW, FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Operating junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge (1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIX	MAX	UNIT
Supply Voltage	4	17	V
Temperature Range, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	

7.4 Thermal Information

THERMAL METRIC (1)		TLV62150 RGT [VQFN] 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (T_A = –40°C to 85°C), typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input Voltage Range (1)		4		17	V
I_Q	Operating Quiescent Current	EN=High, I_{OUT}=0 mA, device not switching		19	27	µA
I_{SD}	Shutdown Current (2)	EN=Low		1.5	4	µA
V_{UVLO}	Undervoltage Lockout Threshold	Falling Input Voltage	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, DEF, FSW, SS/TR, PG)						
V_H	High Level Input Threshold Voltage (EN, DEF, FSW)		0.9			V
V_L	Low Level Input Threshold Voltage (EN, DEF, FSW)				0.3	V
I_{LKG}	Input Leakage Current (EN, DEF, FSW)	EN=V_{IN} or GND; DEF, FSW=V_{OUT} or GND		0.01	1	µA
V_{TH_PG}	Power Good Threshold Voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	94%	
V_{OL_PG}	Power Good Output Low	I_{PG}=-2 mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current (PG)	V_{PG}=1.8 V		1	400	nA
$I_{SS/TR}$	SS/TR Pin Source Current		2.3	2.5	2.7	µA
POWER SWITCH						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN}≥6 V		90		mΩ
	Low-Side MOSFET ON-Resistance	V_{IN}≥6 V		40		mΩ
I_{LIMF}	High-Side MOSFET Forward Current Limit (3)	V_{IN} =12 V, T_A=25°C	1.4	1.7		A
OUTPUT						
V_{REF}	Internal Reference Voltage (4)			0.8		V
I_{LKG_FB}	Input Leakage Current (FB)	V_{FB}=0.8 V		1	100	nA
V_{OUT}	Output Voltage Range	V_{IN} ≥ V_{OUT}	0.9		5	V
	DEF (Output Voltage Programming)	DEF=0 (GND)				
		DEF=1 (V_{OUT})				
	Initial Output Voltage Accuracy (5)	PWM mode operation, V_{IN} ≥ V_{OUT} +1 V	–2.5%		2.5%	
	Load Regulation (6)	V_{IN}=12 V, V_{OUT}=3.3 V, PWM mode operation		0.05		%/A
	Line Regulation (6)	4 V ≤ VIN ≤ 17 V, VOUT=3.3 V, IOUT= 1 A, PWM mode operation		0.02		%/V

(1) The device is still functional down to Under Voltage Lockout (see parameter VUVLO).
(2) Current into AVIN+PVIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection*).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included).
(6) Line and load regulation depend on external component selection and layout (see Figure 20 and Figure 21).

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7.6 Typical Characteristics

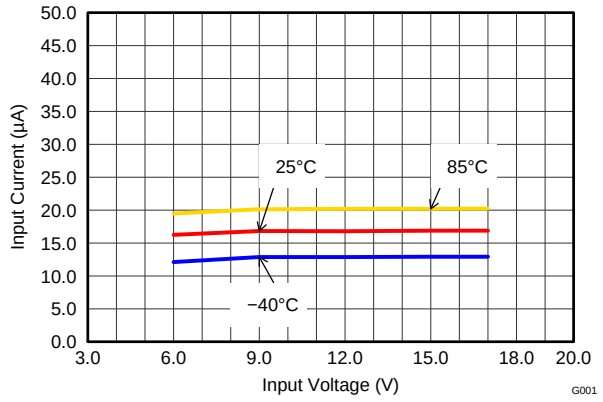


Figure 1. Quiescent Current

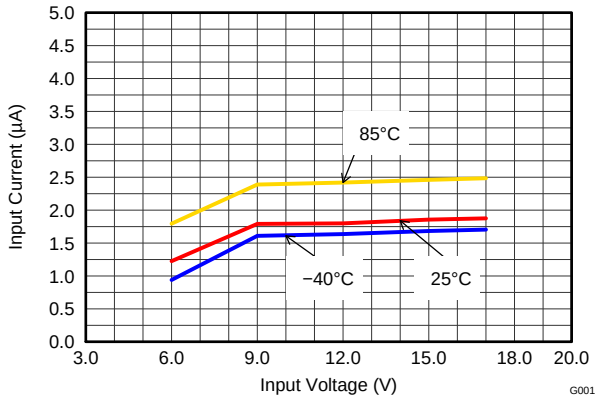


Figure 2. Shutdown Current

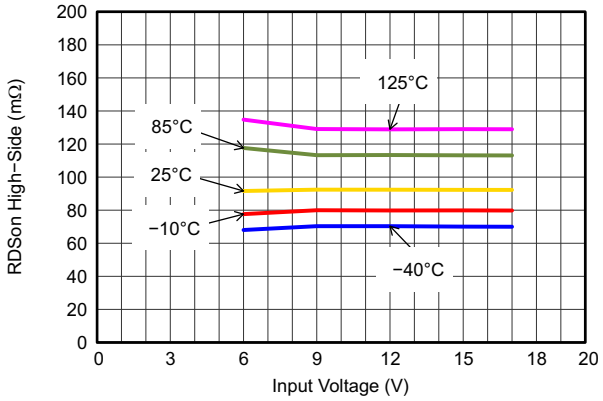


Figure 3. High-Side Switch Resistance

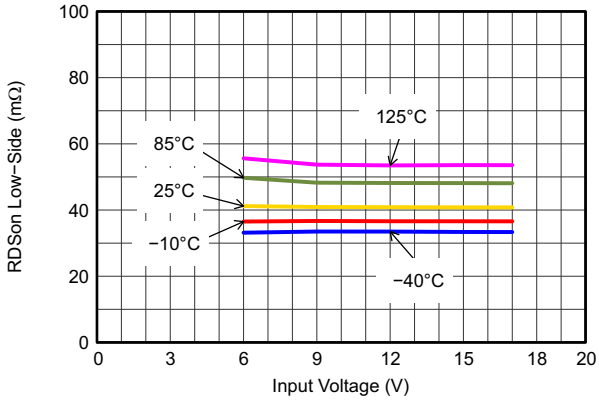


Figure 4. Low-Side Switch Resistance

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8 Detailed Description

8.1 Overview

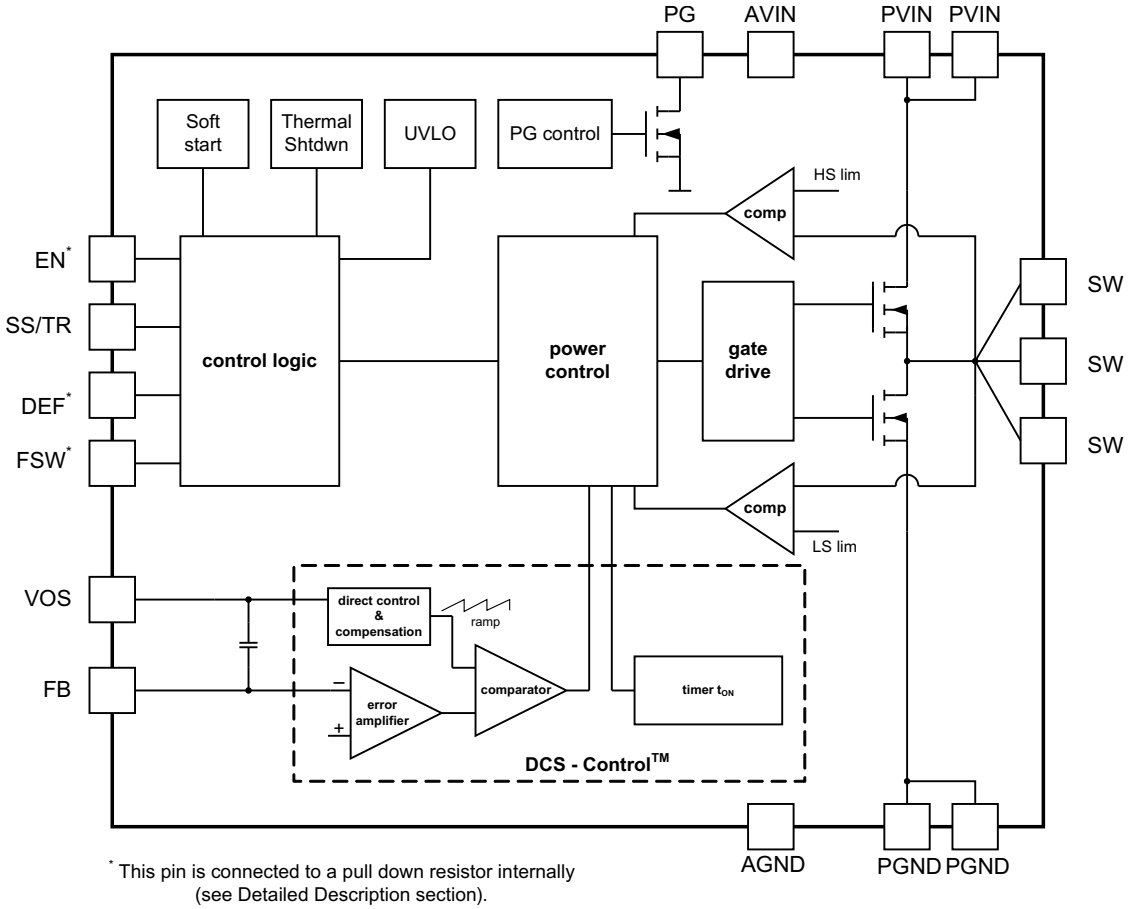
The TLV62150 synchronous switched-mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports Pulse Width Modulation (PWM) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

An internal current limit supports nominal output currents of up to 1 A.

The TLV62150 offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. An internal pull-down resistor of about 400 kΩ is connected and keeps EN logic low, if the pin is floating. It is disconnected if the pin is High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Soft Start / Tracking (SS/TR)

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 32 and Figure 33 for typical startup operation.

Using very small capacitor (or leaving SS/TR pin un-connected) provides fastest startup behavior. The TLV62150 can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage. If the device is set to shutdown (EN=GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage will follow this voltage in both directions up and down (see *Application and Implementation*).

8.3.3 Power Good (PG)

The TLV62150 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain it's specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. TLV62150A features PG=Low in this case and can be used to actively discharge Vout (see *Figure 37*). VIN must remain present for the PG pin to stay Low. See SLVA644 for application details.

8.3.4 Pin-Selectable Output Voltage (DEF)

The output voltage of the TLV62150 can be increased by 5% above the nominal voltage by setting the DEF pin to High (1). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TLV62150 can be found in SLVA489. A pull down resistor of about 400 kΩ is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

8.3.5 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typical) by pulling FSW to High. It is mandatory to start with FSW=Low to limit inrush current, which can be done by connecting to VOUT or PG. Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typical). To get low ripple and full output current at the lower switching frequency, it's recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if needed. A pull down resistor of about 400kOhm is internally connected to the pin, acting the same way as at the DEF Pin (see above).

(1) Maximum allowed voltage is 7 V. Therefore, it's recommended to connect it to VOUT or PG, not VIN.

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Feature Description (continued)

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TLV62150 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

8.4.2 Power Save Mode Operation

The built in Power Save Mode of the TLV62150 is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TLV62150 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated (for FSW=Low) as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ \text{ns} \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON} \quad (2)$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TLV62150 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D=Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, for example, for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

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Device Functional Modes (continued)

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right)$$

where

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET.
- R_L is the DC resistance of the inductor used. (3)

8.4.4 Current Limit and Short Circuit Protection

The TLV62150 devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET will be turned off. Avoiding shoot through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 1.2 A. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \times t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in the *Electrical Characteristics*.
- L is the inductor value.
- V_L is the voltage across the inductor (V_{IN} - V_{OUT}).
- t_{PD} is the internal propagation delay. (4)

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch the peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{\left(V_{IN} - V_{OUT}\right)}{L} \times 30ns \quad (5)$$

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The following information is intended to be a guideline through the individual power supply design process.

9.1 Application Information

The TLV62150 is a switched-mode step-down converter, able to convert a 4-V to 17-V input voltage into a 0.9-V to 5-V output voltage, providing up to 1 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitor, the TLV62150 (TLV62150A) needs an additional resistive divider to set the output voltage level.

9.2 Typical Application

Figure 5 shows an application for Point-of-Load Power Supply Using TLV62150.

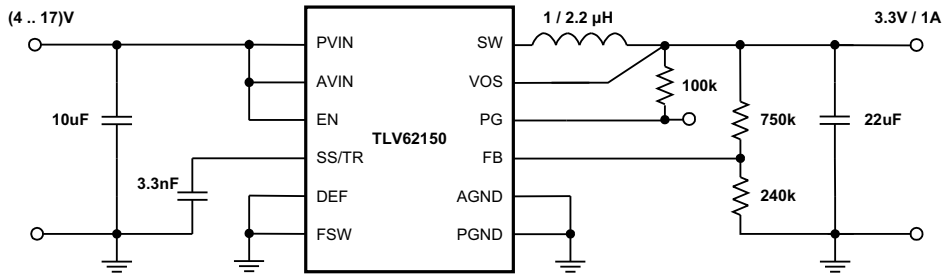


Figure 5. 3.3-V/1-A Step-Down Converter

9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set FSW=High and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set FSW=Low and the device operates with higher switching frequency. The typical values for all measurements are V_{IN} = 12 V, V_{OUT} = 3.3 V and T = 25°C, using the external components of Table 1.

9.2.2 Detailed Design Procedure

The component selection used for measurements is given as follows:

Table 1. List of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 1-A Step-Down Converter, VQFN	TLV62150RGT, Texas Instruments
L1	2.2 µH, 0.165 × 0.165 in	XFL4020-222MEB, Coilcraft
Cin	10 µF, 25 V, Ceramic	Standard
Cout	22 µF, 6.3 V, Ceramic	Standard
Cs	3300 pF, 25 V, Ceramic	
R1	depending on Vout	
R2	depending on Vout	
R3	100 kΩ, Chip, 0603, 1/16 W, 1%	Standard

(1) See *Third-Party Products* Disclaimer

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9.2.2.1 Programming the Output Voltage

The output voltage of the TLV62150 (TLV62150A) is adjustable. It can be programmed for output voltages from 0.9 V to 5 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (6)$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

9.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TLV62150 is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability* section). Table 2 can be used to simplify the output filter component selection.

Table 2. L-C Output Filter Combinations(1)

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
0.47 µH							
1 µH			yes	yes	yes	yes	
2.2 µH		yes	yes(2)	yes	yes	yes	
3.3 µH		yes	yes	yes	yes		
4.7 µH							

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

The TLV62150 can be run with an inductor as low as 1 µH or 2.2 µH. FSW should be set Low in this case. However, for applications running with the low frequency setting (FSW=High) or with low input voltages, 3.3 µH is recommended. More detailed information on further LC combinations can be found in SLVA463.

9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (8)$$

where

- I_L(max) is the maximum inductor current.
- ΔI_L is the Peak to Peak Inductor Ripple Current.
- L(min) is the minimum effective inductor value.
- f_{SW} is the actual PWM Switching Frequency.

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Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TLV62150 and are recommended for use:

Table 3. List of Inductors

Type	Inductance [µH]	Saturation Current [A](1)	Dimensions [L x B x H] mm	MANUFACTURER(2)
XFL4020-222ME_	2.2 µH, ±20%	3.5	4 × 4 × 2.1	Coilcraft
XFL3012-222MEC	2.2 µH, ±20%	1.6	3 × 3 × 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.4	3 × 3 × 1.2	Coilcraft
VLS252012T-2R2M1R3	2.2 µH, ±20%	1.3	2.5 × 2 × 1.2	TDK
LPS3015-332	3.3 µH, ±20%	1.4	3 × 3 × 1.4	Coilcraft
744025003	3.3 µH, ±20%	1.5	2.8 × 2.8 × 2.8	Wuerth
PSI25201B-2R2MS	2.2 µH, ±20%	1.3	2 × 2.5 × 1.2	Cyntec
NR3015T-2R2M	2.2 µH, ±20%	1.5	3 × 3 × 1.5	Taiyo Yuden

(1) SLVSB7156869Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) See *Third-Party Products* Disclaimer

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

9.2.2.2.2 Capacitor Selection

9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TLV62150 allows the use of tiny ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, Its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.2.2.2 Input Capacitor

For most applications, 10 µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's recommended to place a capacitance of 0.1 uF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

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9.2.2.2.2.3 Soft-Start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{1.25V} [F] \quad (10)$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin.
- t_{SS} is the desired soft-start ramp time (s).

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.3 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin will track the SS/TR pin voltage as described in Equation 11 and shown in Figure 6.

$$V_{FB} \approx 0.64 \times V_{SS/TR} \quad (11)$$

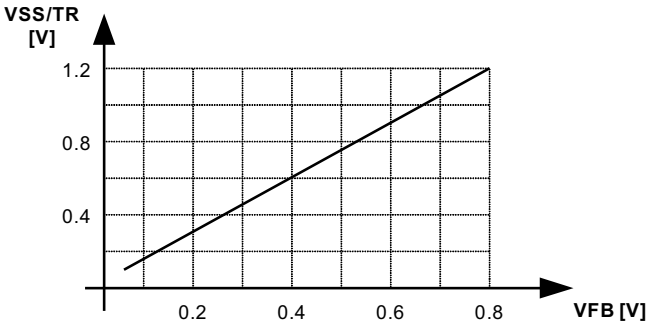


Figure 6. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device does not sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN}+0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage will go to zero, independent of the tracking voltage. Figure 7 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

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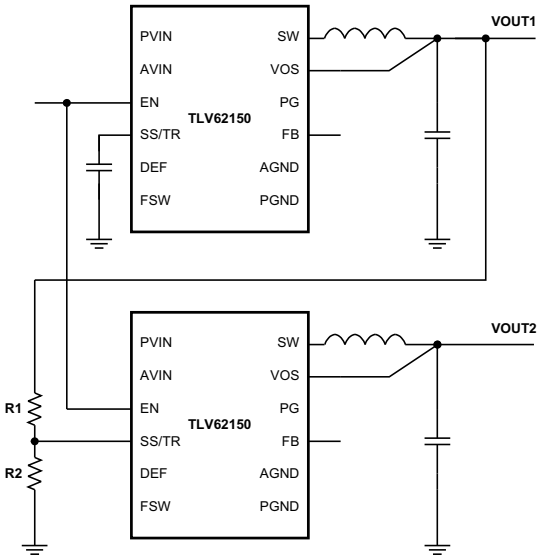


Figure 7. Sequence for Ratiometric and Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start up sequence happens if both supplies are sharing the same soft start capacitor. Equation 10 calculates the soft start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

9.2.2.4 Output Filter and Loop Stability

The TLV62150 is internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which will be affected. More information including a detailed L-C stability matrix can be found in SLVA463.

The TLV62150 includes an internal 25 pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 13 and Equation 14:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 25pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \times 25pF} \times \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

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Though the TLV62150 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in SLVA289 and SLVA466.

9.2.3 Application Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

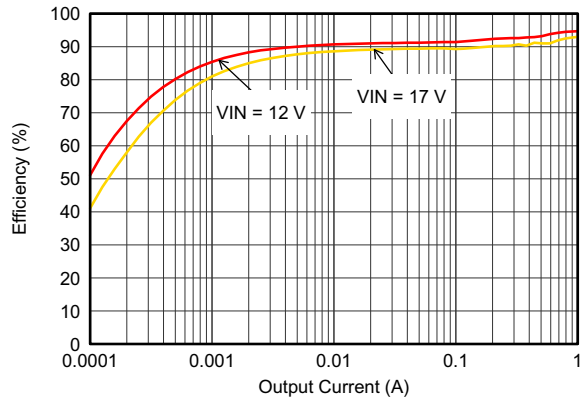


Figure 8. Efficiency With 1.25 MHz, Vout = 5 V

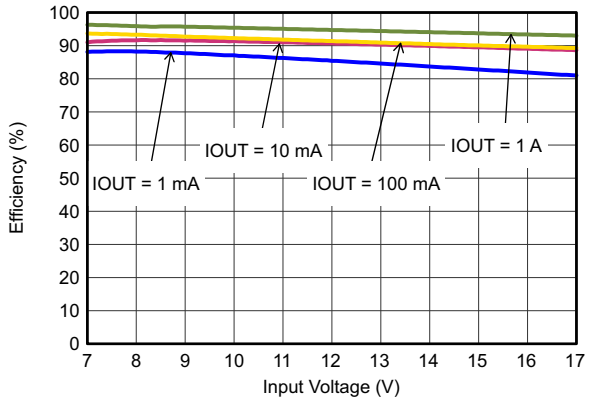


Figure 9. Efficiency With 1.25 MHz, Vout = 5 V

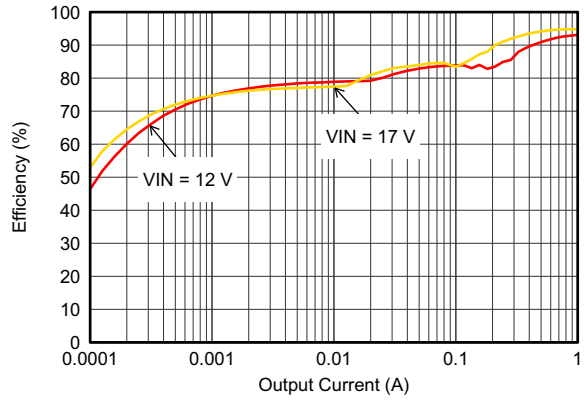


Figure 10. Efficiency With 2.5 MHz, Vout = 5 V

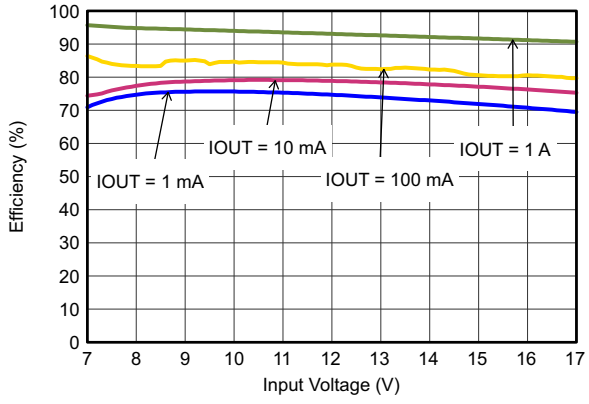


Figure 11. Efficiency With 2.5 MHz, Vout = 5 V

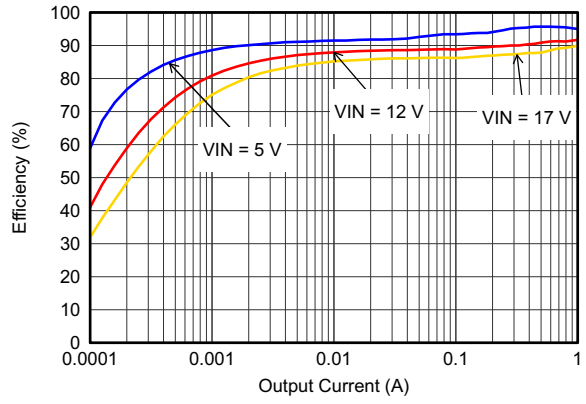


Figure 12. Efficiency With 1.25 MHz, Vout = 3.3 V

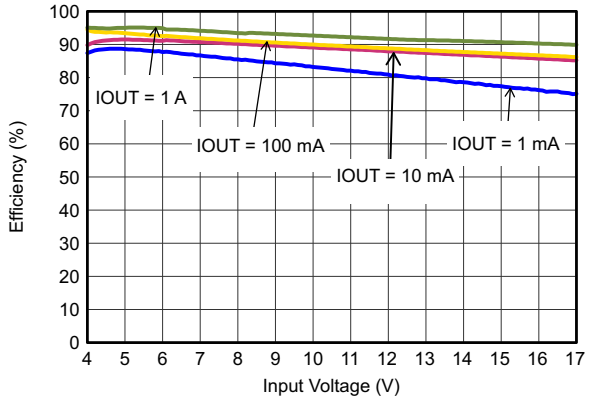


Figure 13. Efficiency With 1.25 MHz, Vout = 3.3 V

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V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

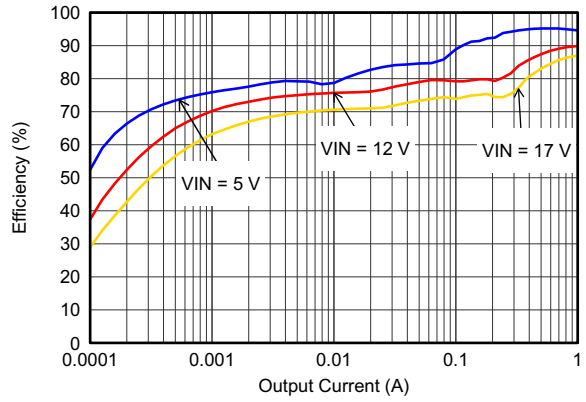


Figure 14. Efficiency With 2.5 MHz, Vout = 3.3 V

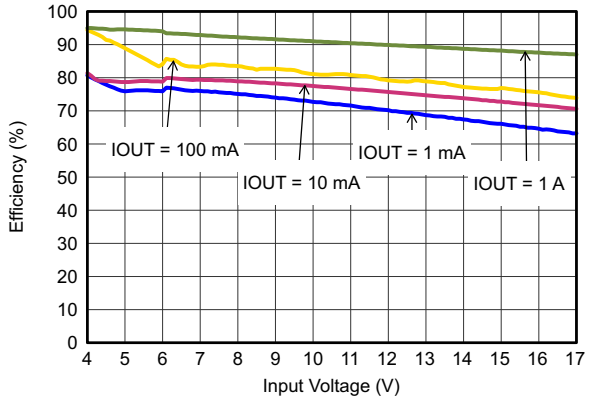


Figure 15. Efficiency With 2.5 MHz, Vout = 3.3 V

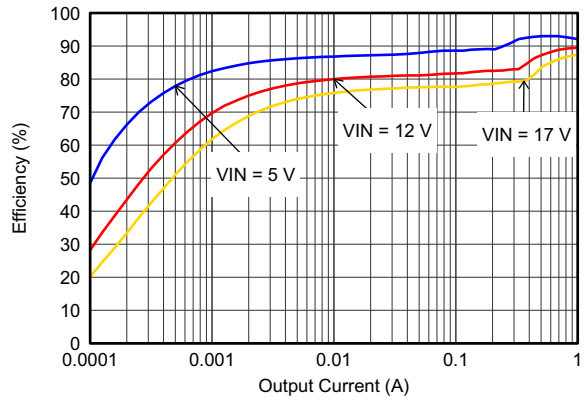


Figure 16. Efficiency With 1.25 MHz, Vout = 1.8 V

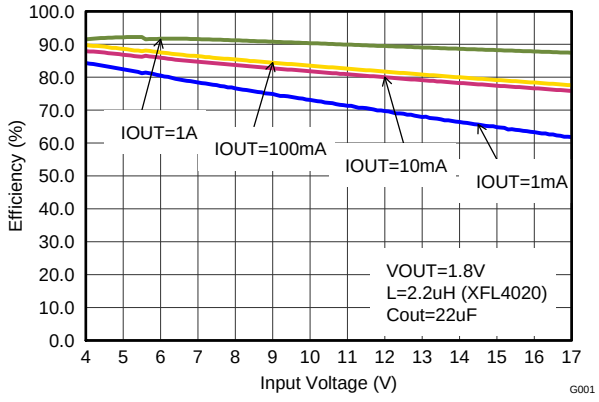


Figure 17. Efficiency With 1.25 MHz, Vout = 1.8 V

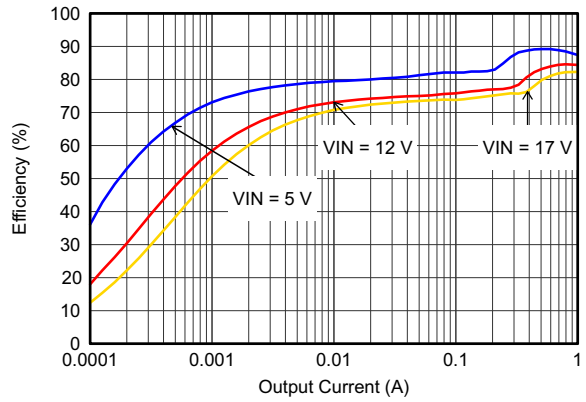


Figure 18. Efficiency With 1.25 MHz, Vout = 0.9 V

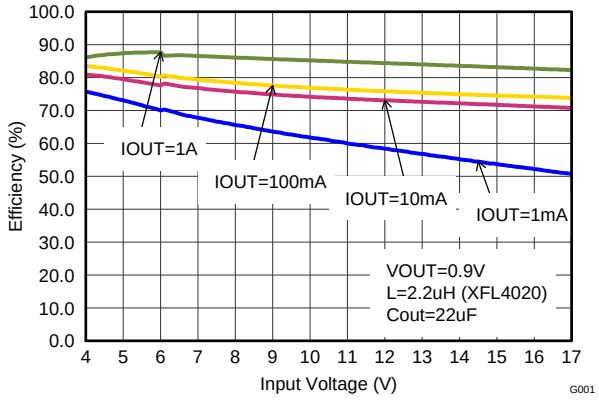


Figure 19. Efficiency With 1.25 MHz, Vout=0.9 V

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V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

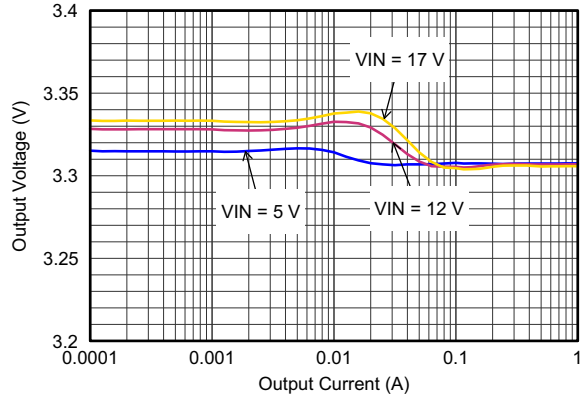


Figure 20. Output Voltage Accuracy (Load Regulation)

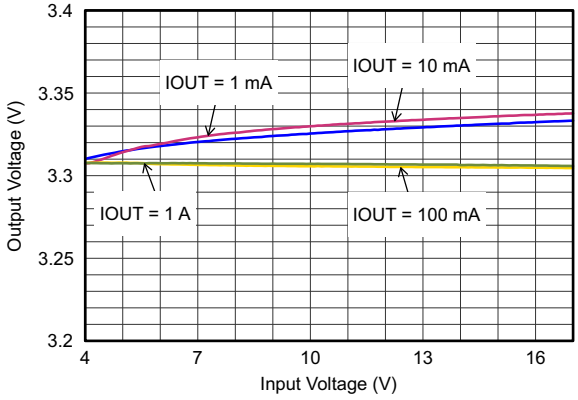


Figure 21. Output Voltage Accuracy (Line Regulation)

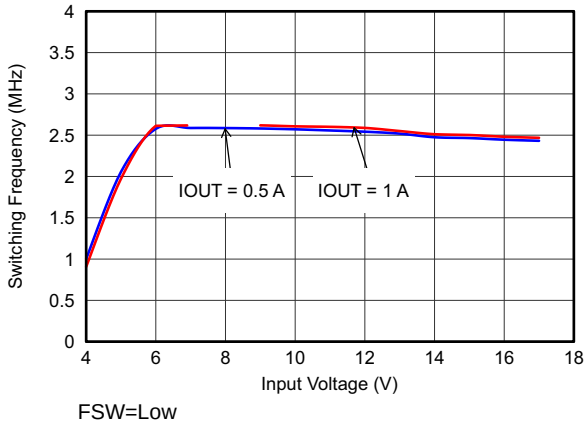


Figure 22. Switching Frequency

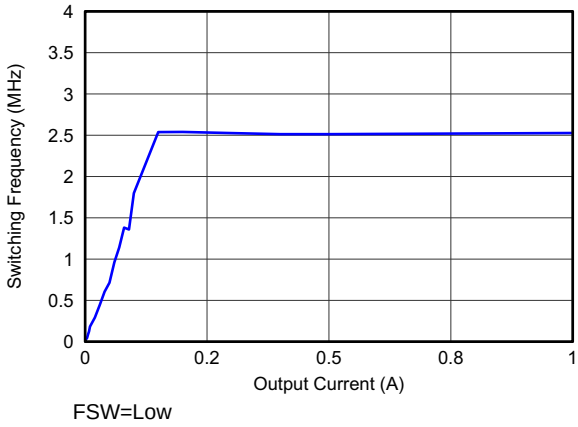


Figure 23. Switching Frequency

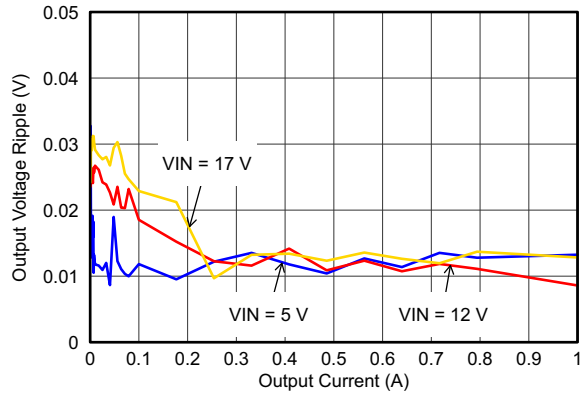


Figure 24. Output Voltage Ripple

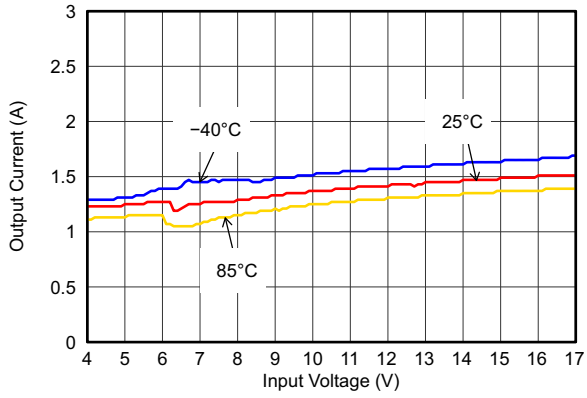
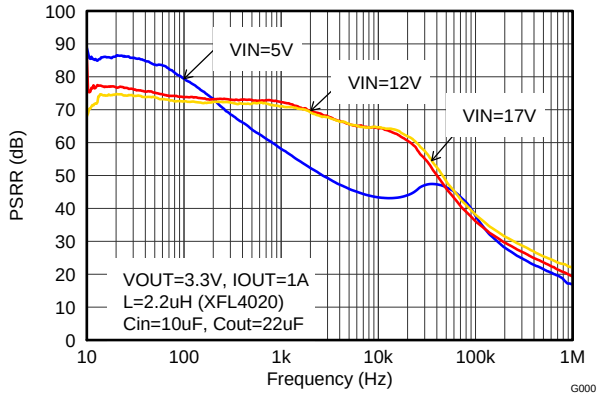


Figure 25. Maximum Output Current

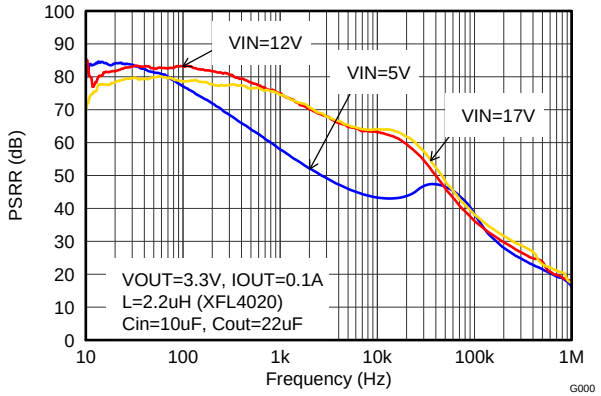
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V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



I_{OUT} = 1 A

Figure 26. Power Supply Rejection Ratio, F_{SW} = 2.5 MHz



I_{OUT} = 0.1 A

Figure 27. Power Supply Rejection Ratio, F_{SW} = 2.5 MHz

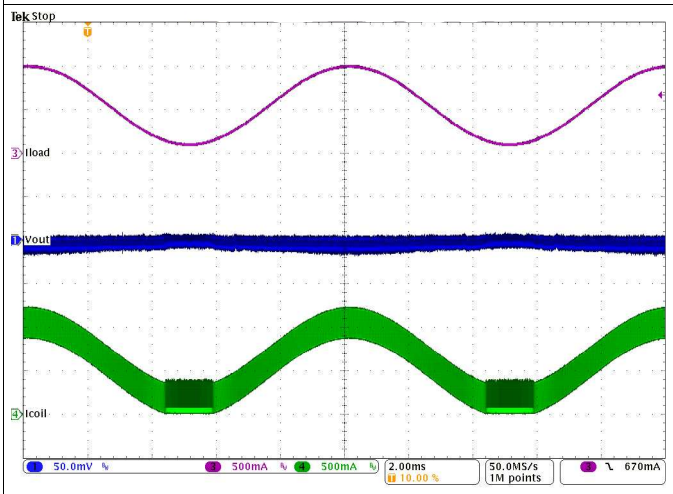


Figure 28. PWM-PSM-Transition (V_{IN} = 12 V, V_{OUT} = 3.3 V With 50 mV/div)

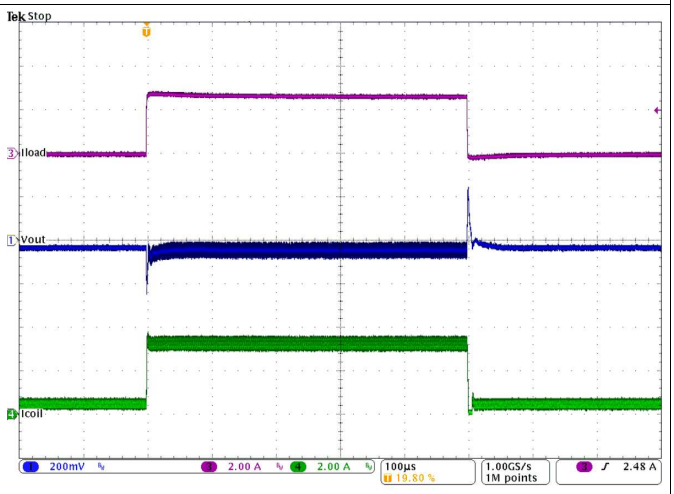


Figure 29. Load Transient Response (I_{OUT}= 0.5 to 1 to 0.5 A, V_{IN} = 12 V, V_{OUT} = 3.3 V)

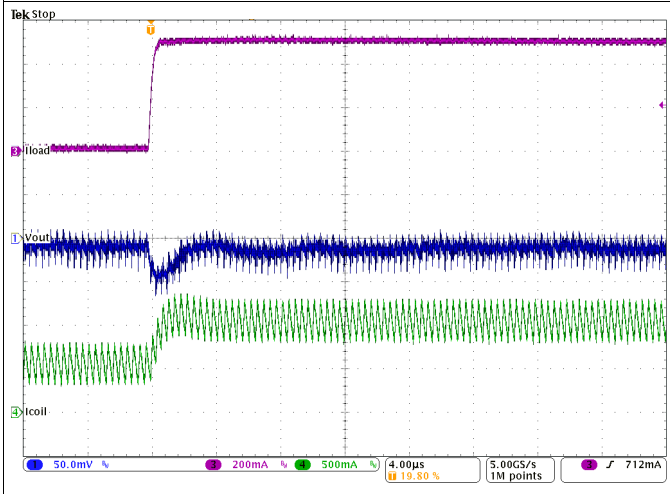


Figure 30. Load Transient Response of Figure 29, Rising Edge

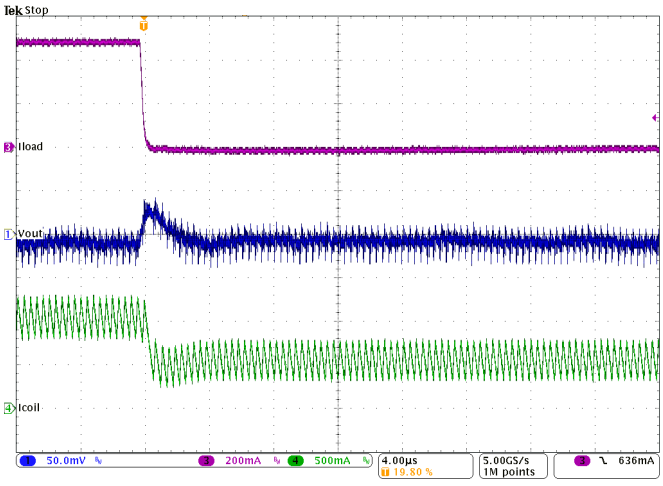


Figure 31. Load Transient Response of Figure 29, Falling Edge

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

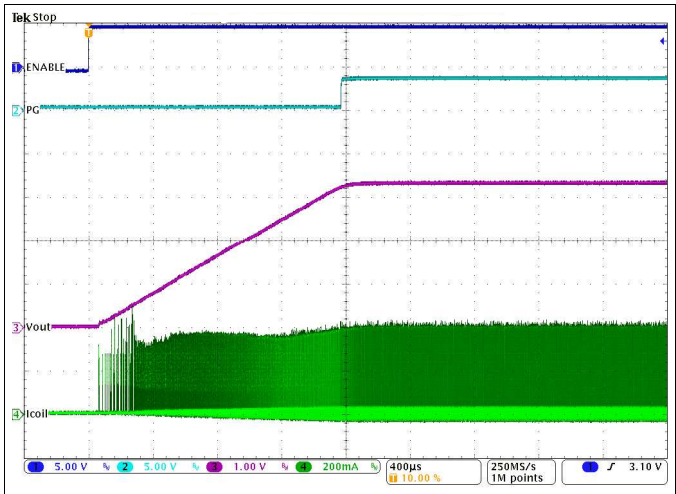


Figure 32. Startup Into 100 mA

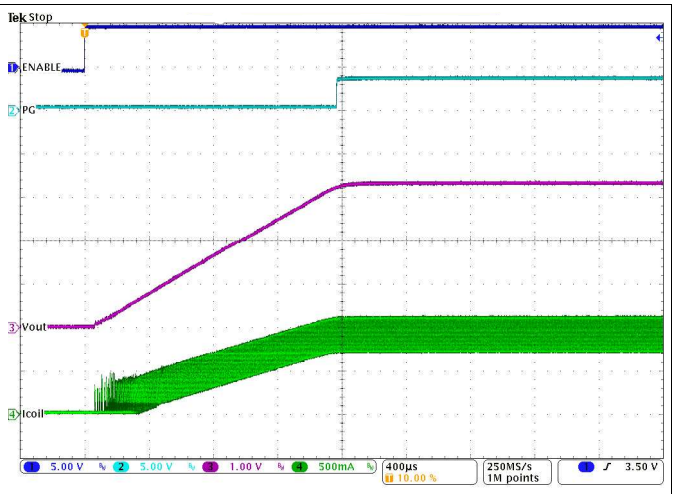


Figure 33. Startup Into 1 A

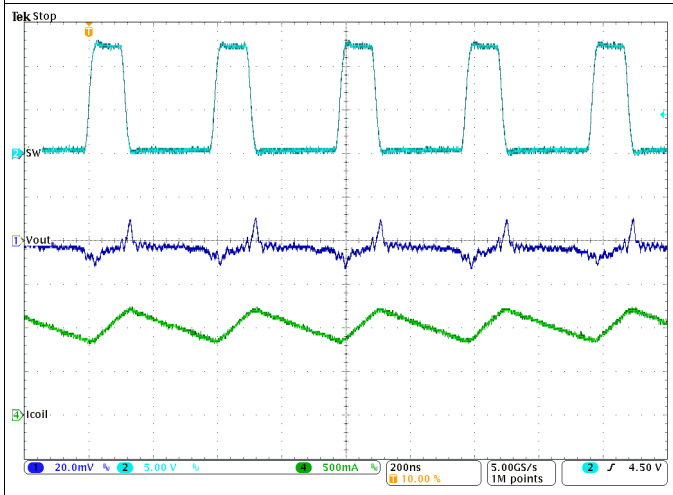


Figure 34. Typical Operation In PWM Mode (I_{OUT} = 1 A)

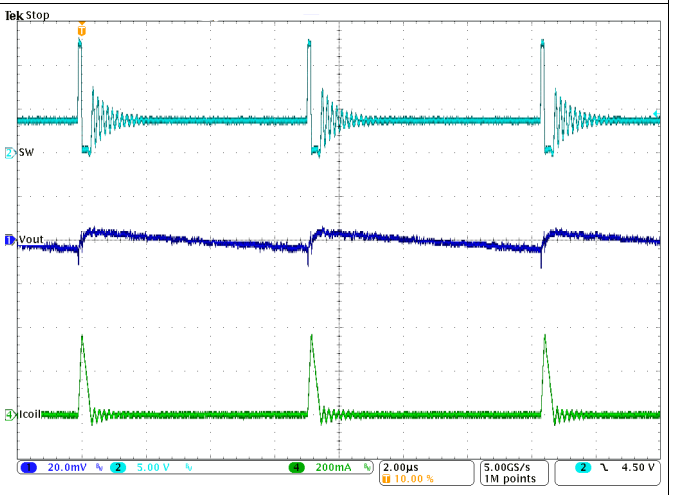


Figure 35. Typical Operation in Power Save Mode (I_{OUT} = 10 mA)

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9.3 System Examples

9.3.1 LED Power Supply

The TLV62150 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5 µA, the FB pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TLV62150. Figure 36 shows an application circuit, tested with analog dimming:

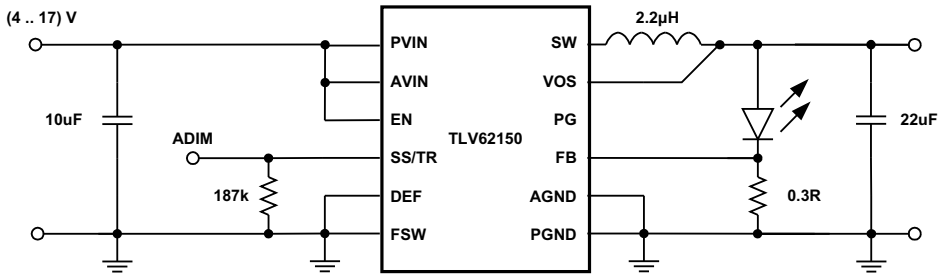


Figure 36. 1-A Single LED Power Supply

The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \times 2.5\mu A \times R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

9.3.2 Active Output Discharge

The TLV62150A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see Figure 37). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

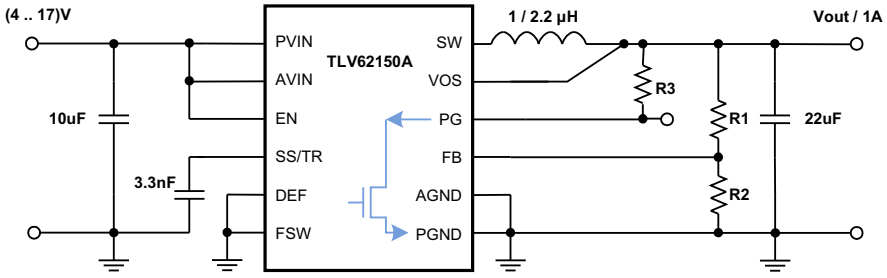


Figure 37. Discharge Vout Through PG Pin with TLV62150A

System Examples (continued)

9.3.3 Inverting Power Supply

The TLV62150 can be used as inverting power supply by rearranging external circuitry as shown in Figure 38. As the former GND node now represents a voltage level below system ground, the voltage difference between VIN and VOUT has to be limited for operation to the maximum supply voltage of 17 V (see Equation 16).

$$V_{IN} + V_{OUT} \leq V_{INmax} \quad (16)$$

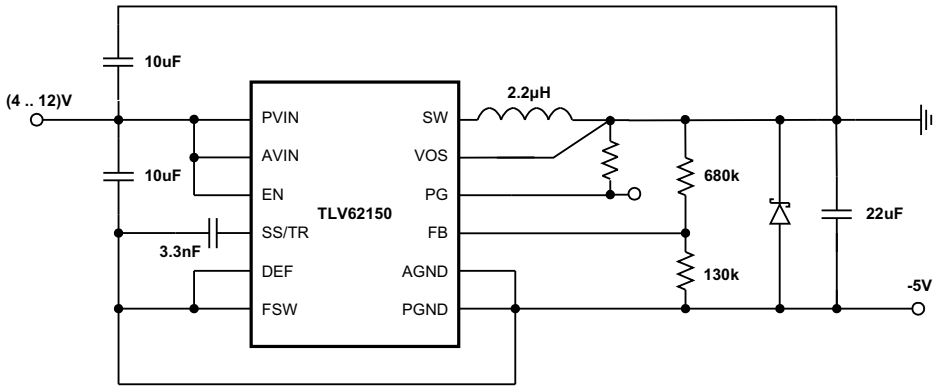


Figure 38. –5-V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

9.3.4 Various Output Voltages

The following example circuits show how to configure the external circuitry to furnish different output voltages at 1 A.

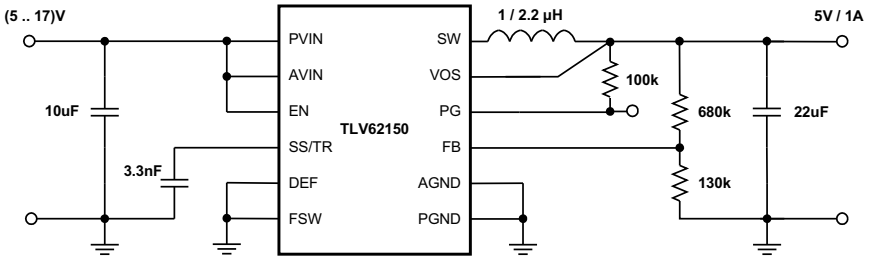


Figure 39. 5-V/1-A Power Supply

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System Examples (continued)

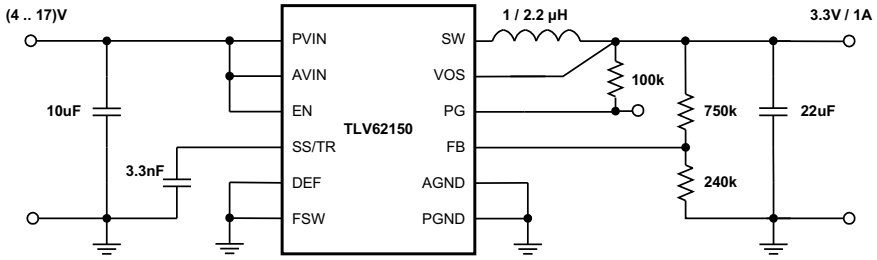


Figure 40. 3.3-V/1-A Power Supply

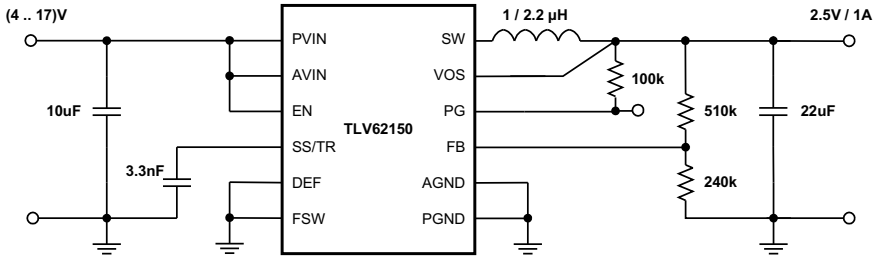


Figure 41. 2.5-V/1-A Power Supply

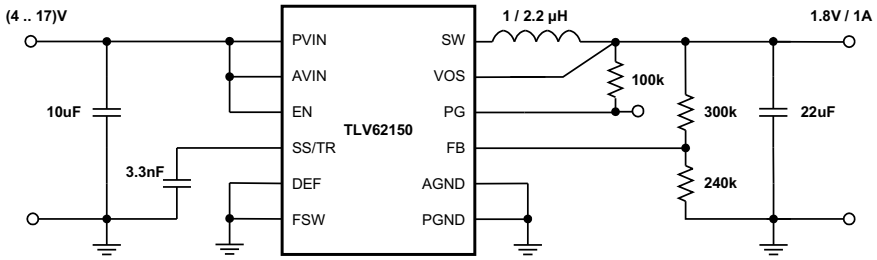


Figure 42. 1.8-V/1-A Power Supply

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System Examples (continued)

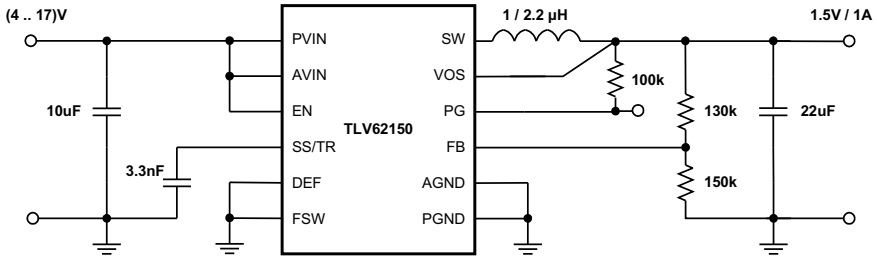


Figure 43. 1.5-V/1-A Power Supply

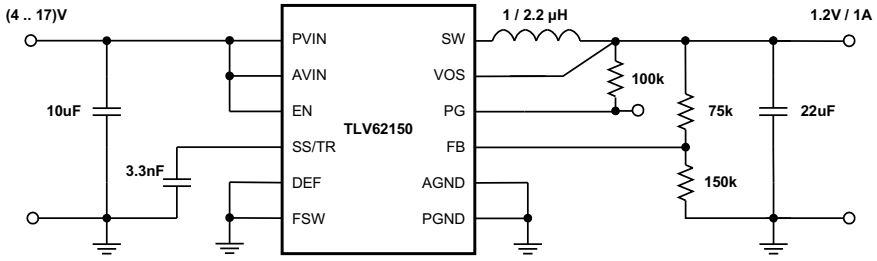


Figure 44. 1.2-V/1-A Power Supply

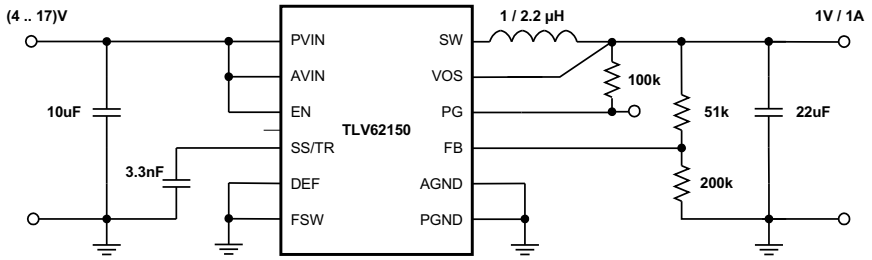


Figure 45. 1-V/1-A Power Supply

10 Power Supply Recommendations

The TLV6215X are designed to operate from a 4-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

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11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TLV62150 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

See Figure 46 for the recommended layout of the TLV62150, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to VOUT at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the VOUT power line/plane as shown in *Layout Example*.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (e.g. SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, SLAU416. Additionally, the EVM Gerber data are available for download here, SLVC394.

11.2 Layout Example

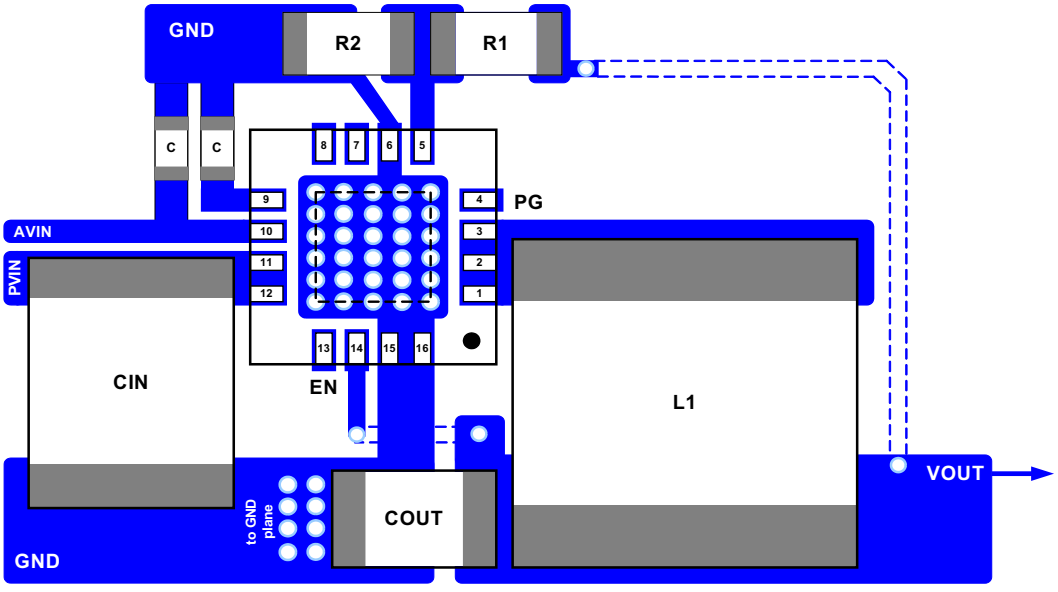


Figure 46. Layout Example Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: thermal characteristics application note (SZZA017), and (SPRA953).

The TLV62150 is designed for a maximum operating junction temperature (T_j) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV62150	Click here	Click here	Click here	Click here	Click here
TLV62150A	Click here	Click here	Click here	Click here	Click here

12.3 Documentation Support

12.3.1 Related Documentation

For related documentation, see the following:

- *TLV62130EVM-505 and TLV62150EVM-505 Evaluation Modules*, SLAU416
- EVM Gerber data, SLVC394
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017
- *Semiconductor and IC Package Thermal Metrics*, SPRA953

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62150ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUOI	Samples
TLV62150ARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUOI	Samples
TLV62150RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUCI	Samples
TLV62150RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUCI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

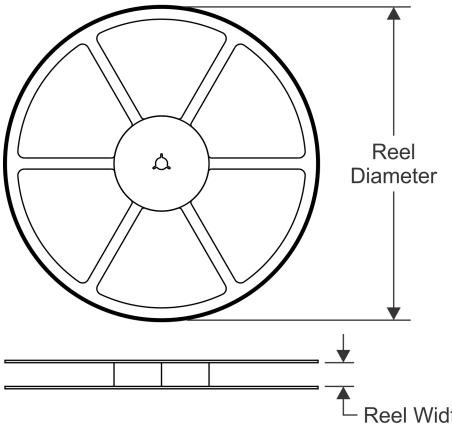
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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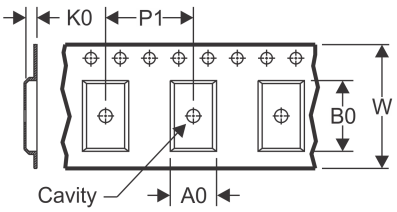
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

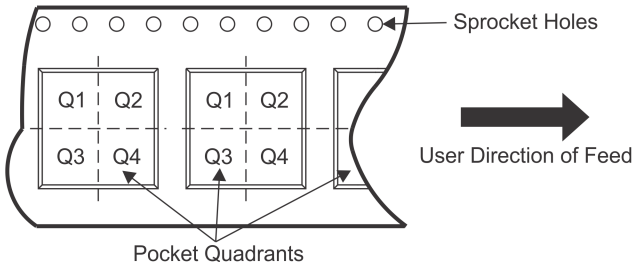


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

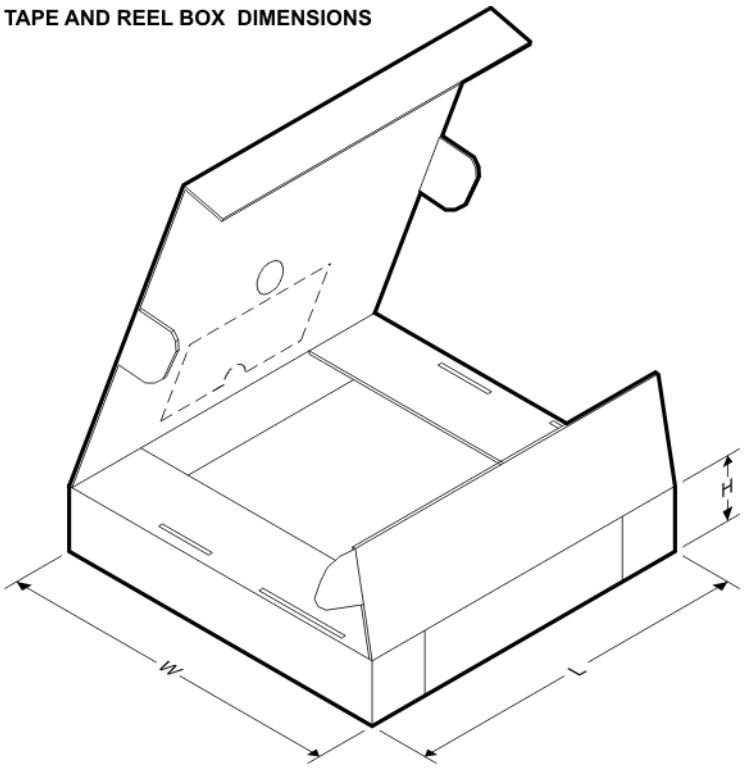
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62150ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62150ARGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62150RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62150RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62150RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62150RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

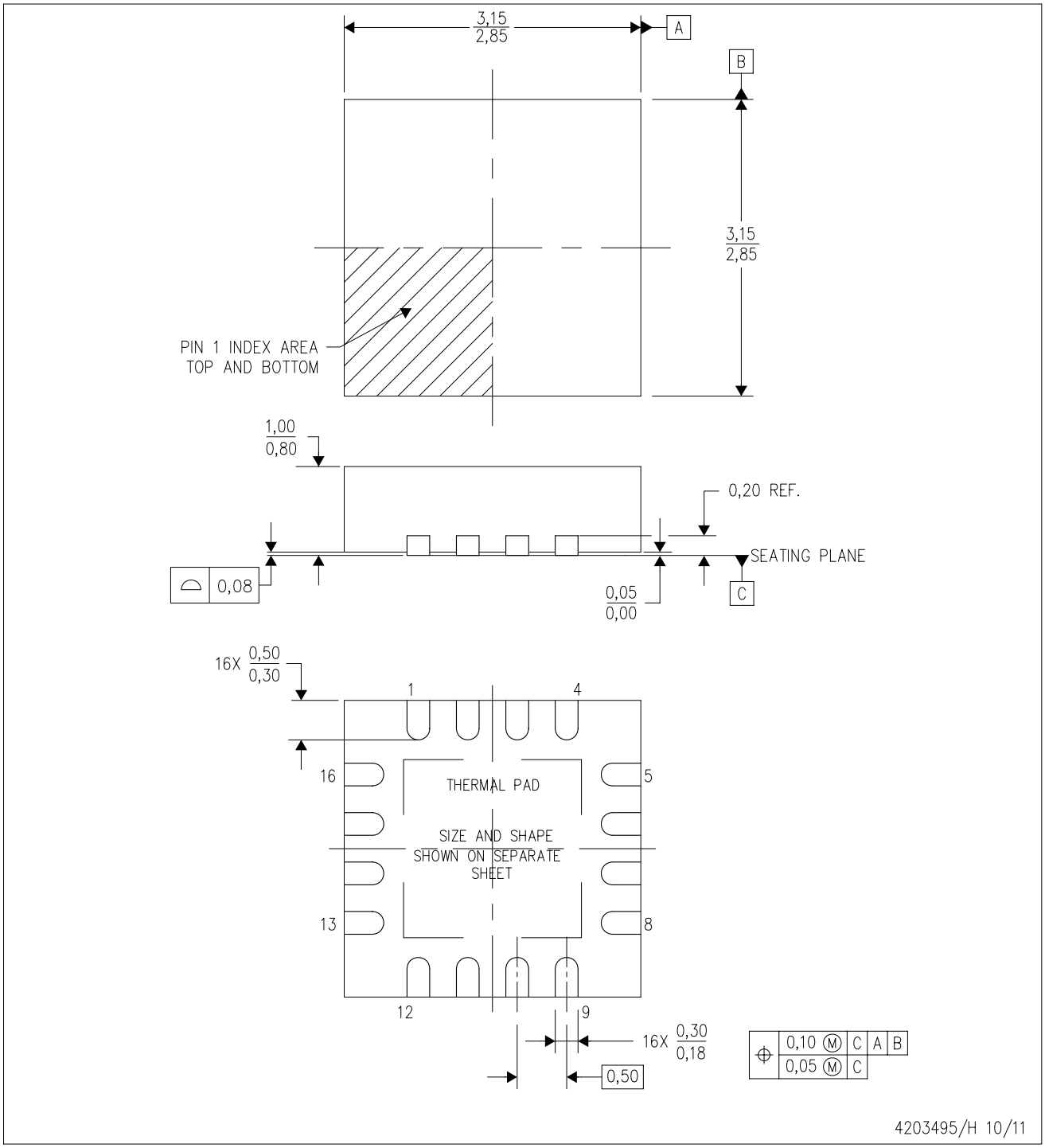
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62150ARGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TLV62150ARGTT	QFN	RGT	16	250	552.0	185.0	36.0
TLV62150RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TLV62150RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TLV62150RGTT	QFN	RGT	16	250	210.0	185.0	35.0
TLV62150RGTT	QFN	RGT	16	250	552.0	185.0	36.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

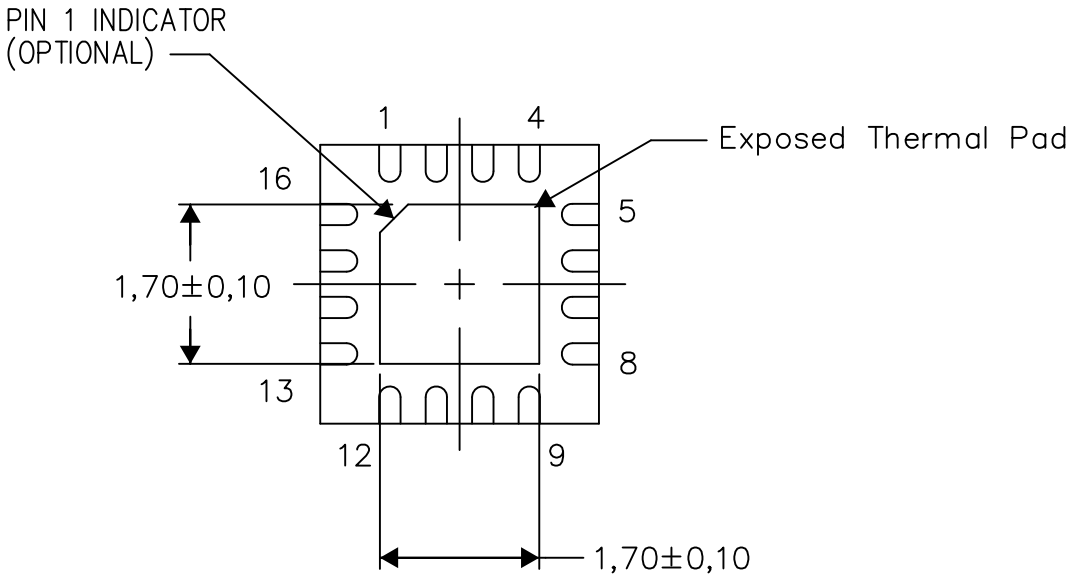
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



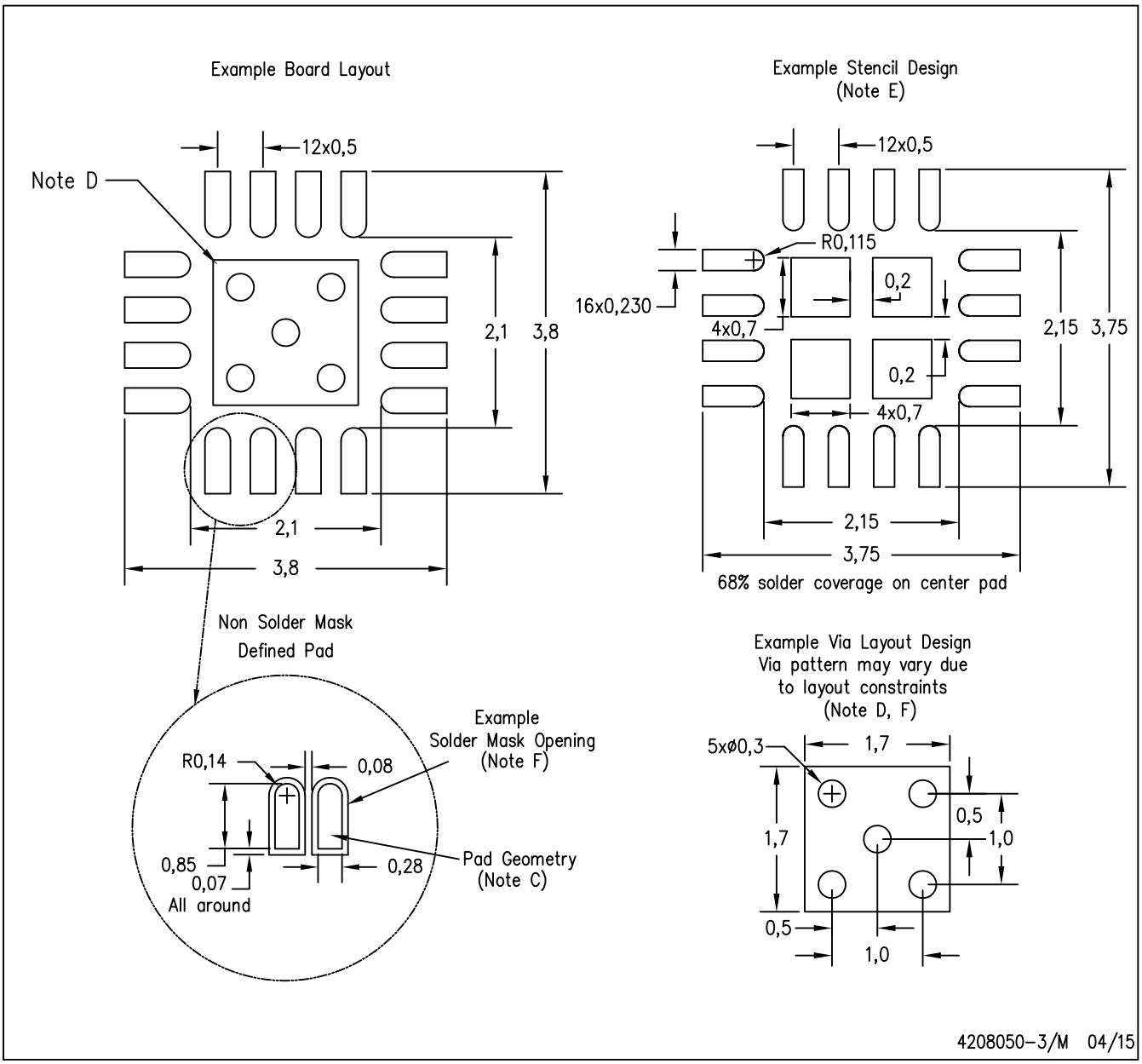
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

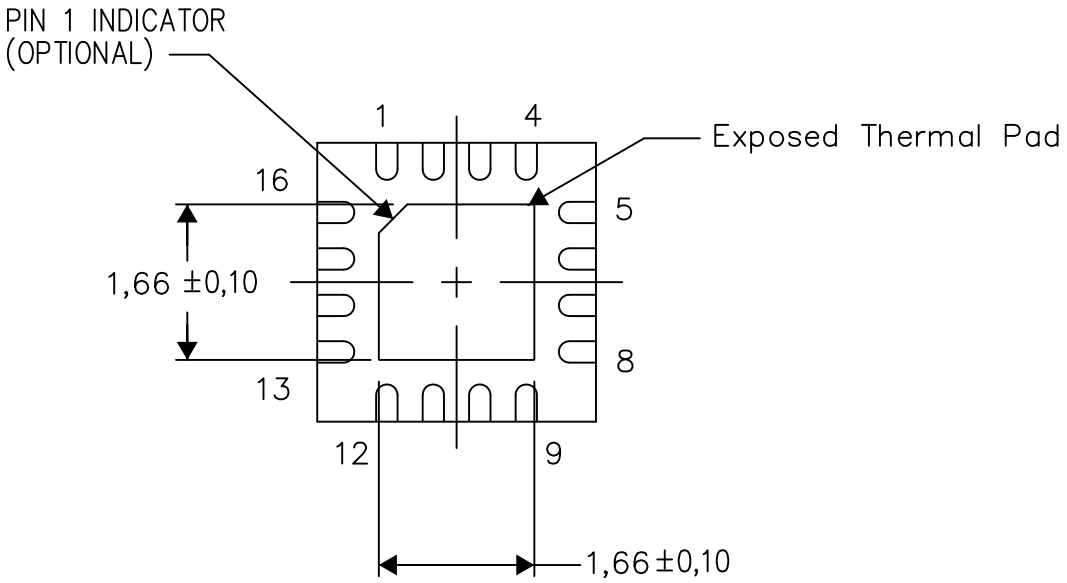
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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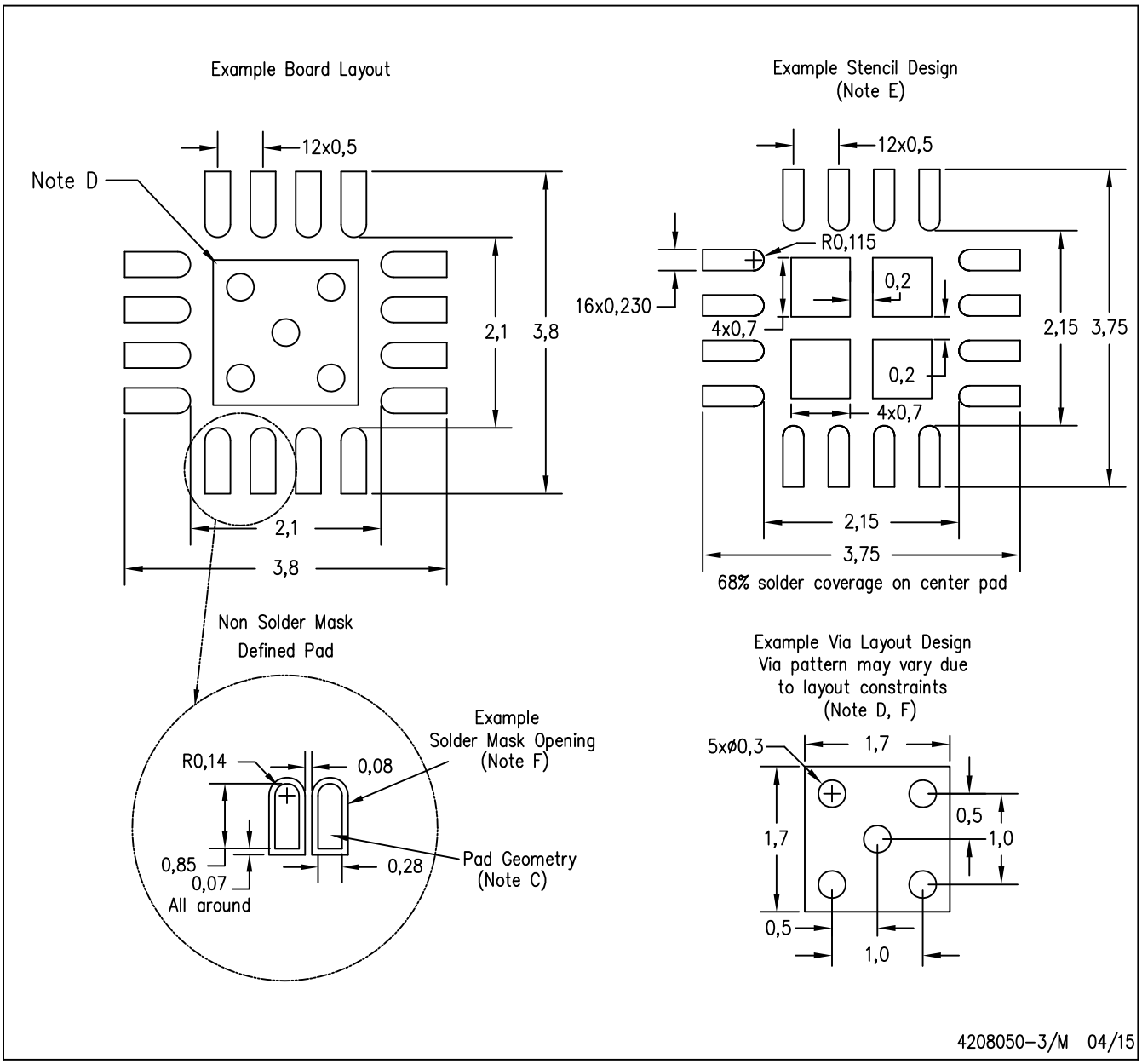
Bottom View

Exposed Thermal Pad Dimensions

4206349–10/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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