ACTT8B-800C0

AC Thyristor Triac power switch

Rev.02 - 25 April 2019 Product data sheet

1. General description

AC Thyristor Triac power switch in a TO263 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

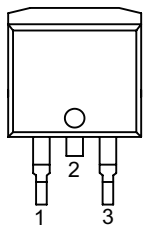
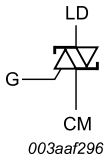
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 105$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	-	80	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	-	88	A
T_j	junction temperature			-	-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 6		-	-	2	kV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		5	-	30	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		5	-	30	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		5	-	30	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	35	mA
V_T	on-state voltage	I_T = 10 A; T_j = 25 °C; Fig. 11		-	1.3	1.5	V
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		2000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 1 V/µs; (snubberless condition); gate open circuit		8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		 003aaf296
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
ACTT8B-800C0	TO263	ACTT8B-800C0J	Reel	800	TO263E	26-May-2017

7. Marking

Table 4. Marking codes

Type number	Marking Code
ACTT8B-800C0	ACTT8B-800C0

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 105$ °C; Fig. 1; Fig. 2; Fig. 3		-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		-	80	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	88	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	32	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 60$ mA		-	100	A/µs
I_{GM}	peak gate current	$t_p = 20$ µs		-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C
V_{pp}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig 6		-	2	kV

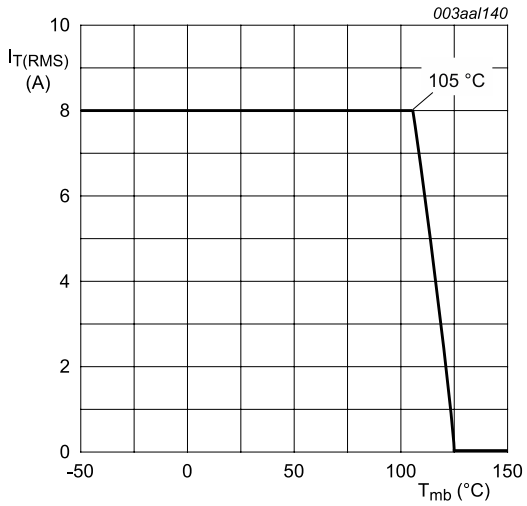
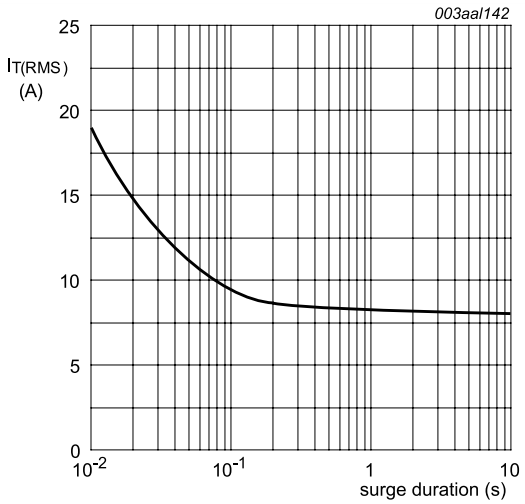


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

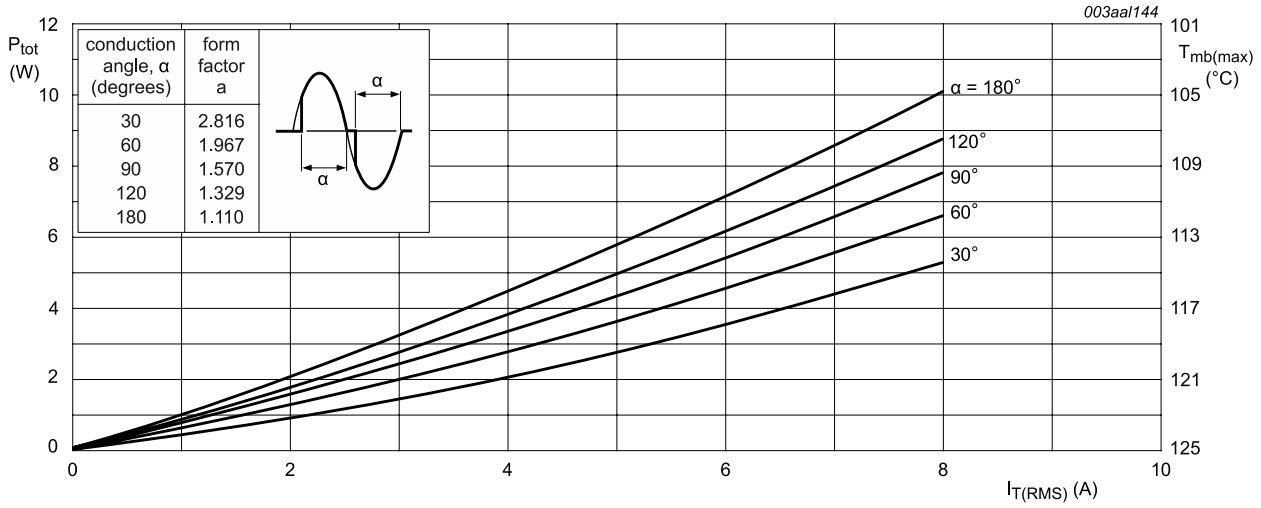


f = 50 Hz; $T_{mb} = 105$ °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values

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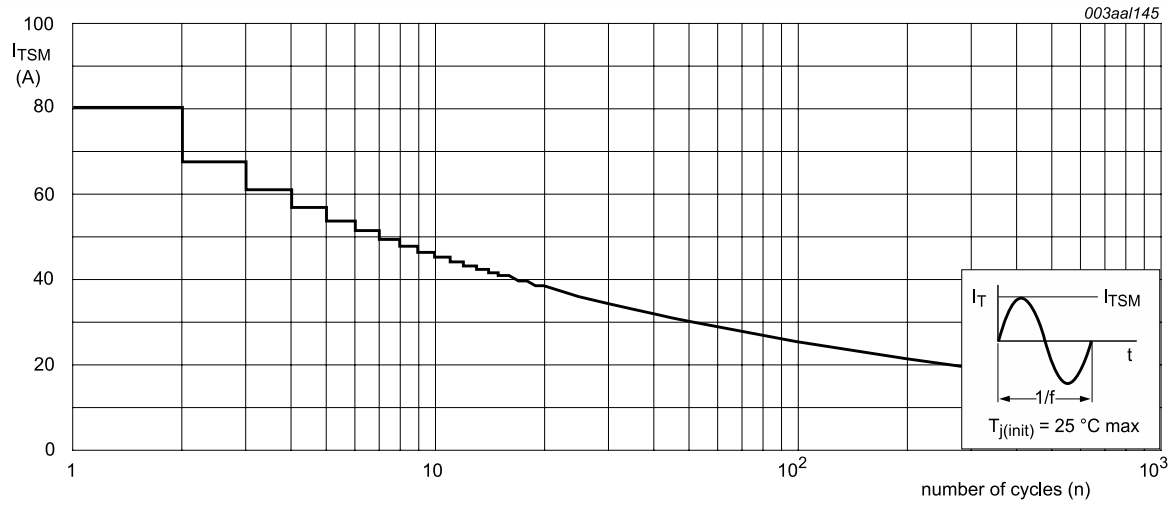
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α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

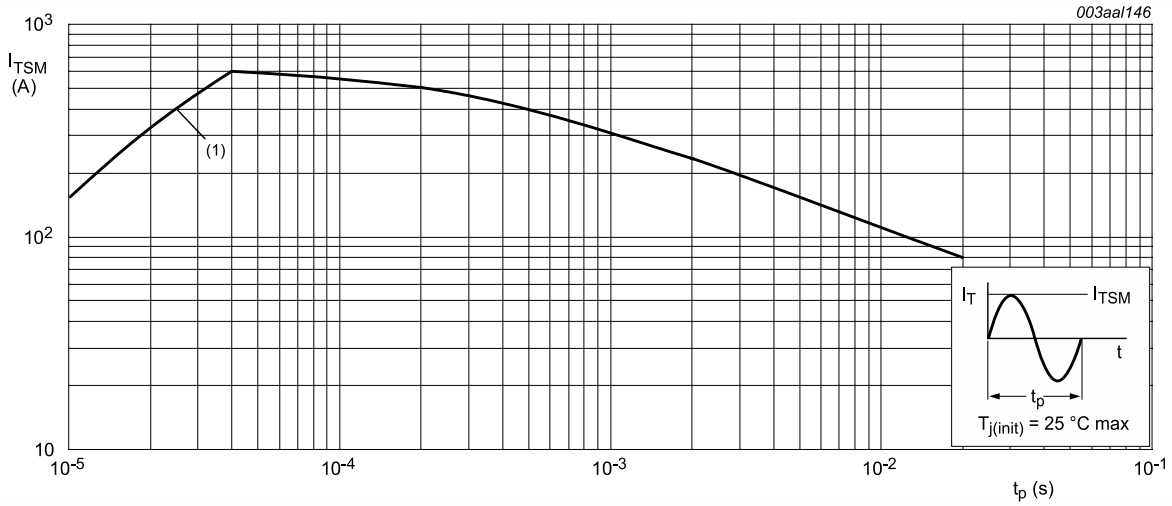


f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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$t_p \leq 20$ ms
(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

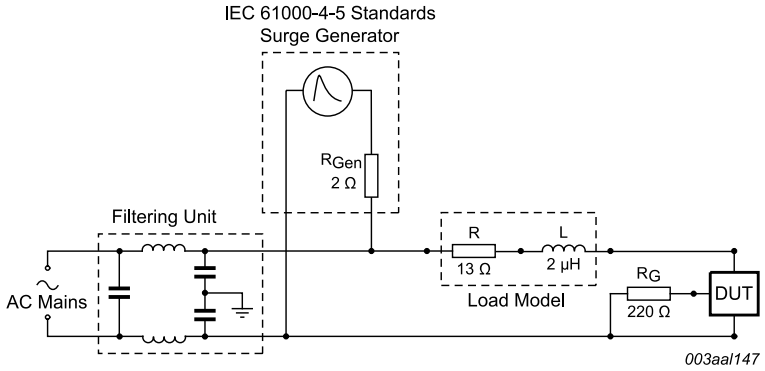


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

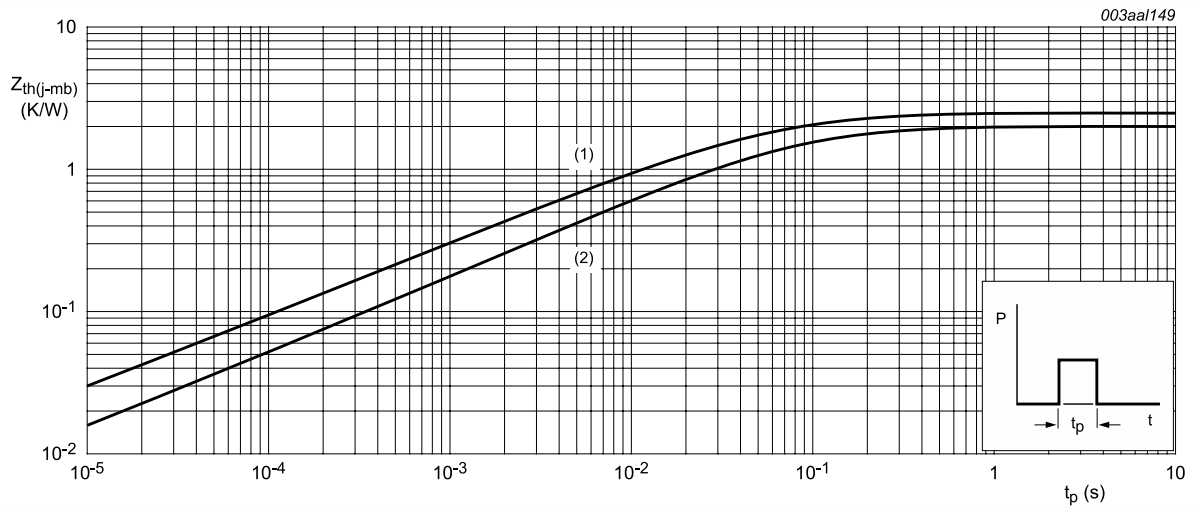
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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 7		-	-	2	K/W
		half cycle; Fig. 7		-	-	2.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air; printed circuit board (FR4) mounted		-	55	-	K/W



(1) Unidirectional (half cycle)
(2) Bidirectional (full cycle)

Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

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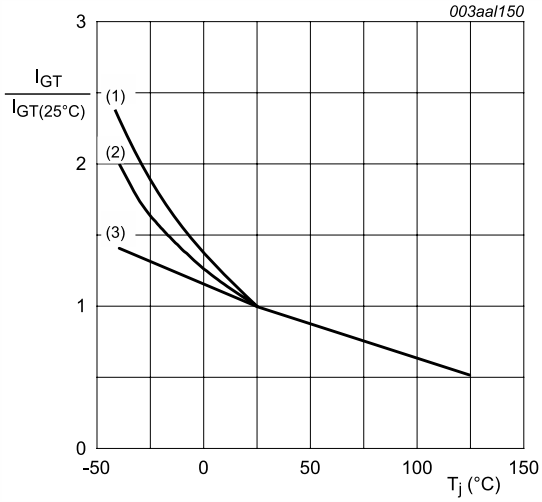
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		5	-	30	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		5	-	30	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		5	-	30	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	50	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	70	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	50	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	35	mA
V_T	on-state voltage	I_T = 10 A; T_j = 25 °C; Fig. 11		-	1.3	1.5	V
V_{GT}	gate trigger voltage	V_D = 12V; I_T = 100 mA;T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400V; I_T = 100 mA;T_j = 125 °C; Fig. 12		0.2	0.45	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		2000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		8	-	-	A/ms

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(1) LD- G-
(2) LD+ G+
(3) LD+ G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

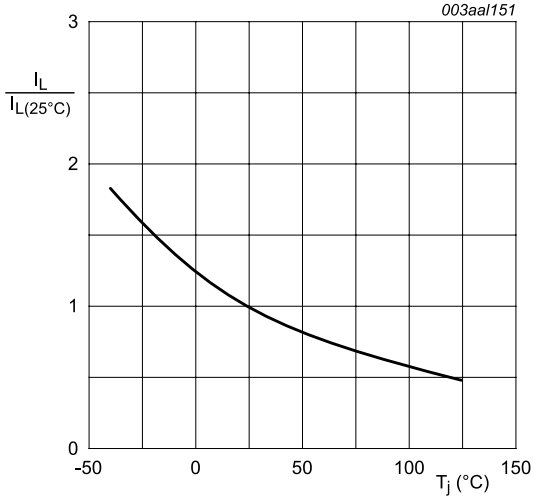


Fig. 9. Normalized latching current as a function of junction temperature

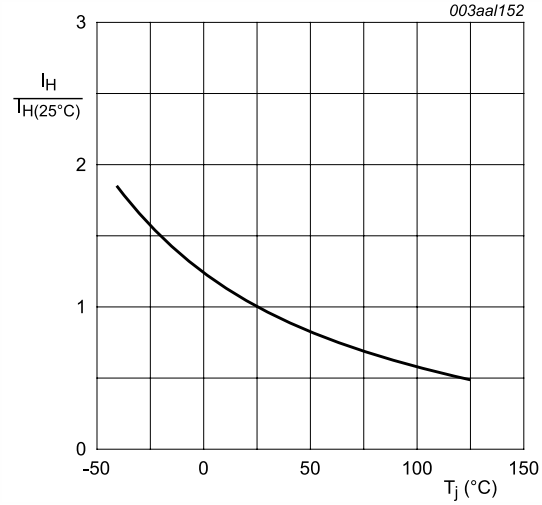
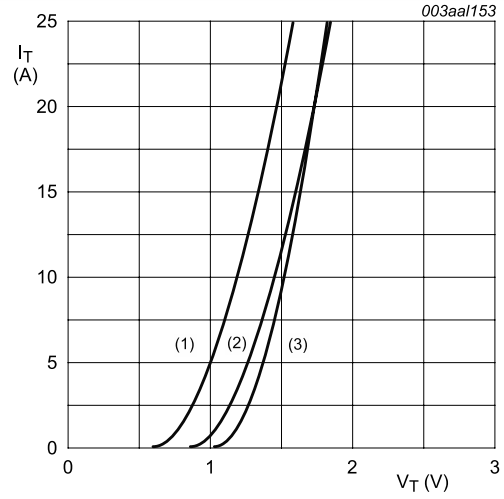


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.103 V; R_s = 0.034 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

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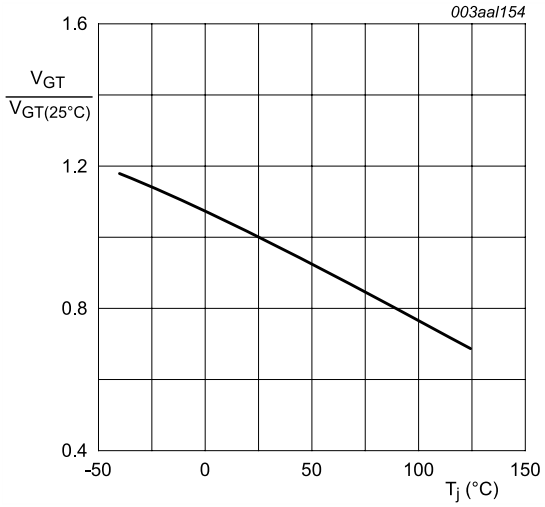


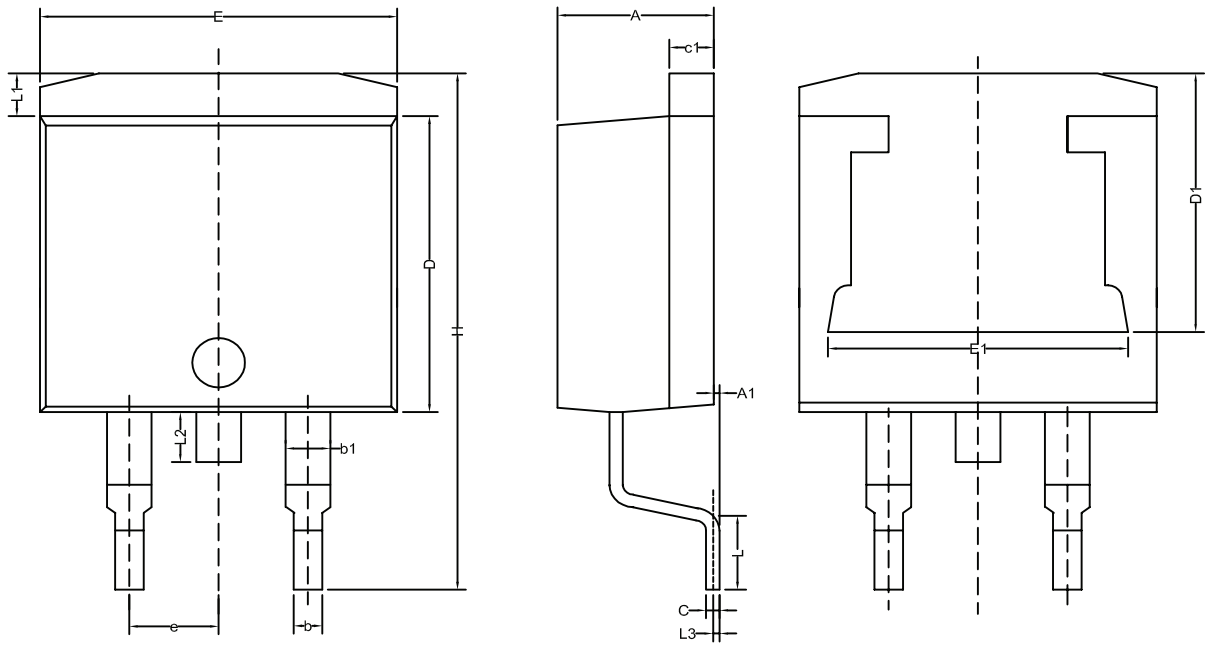
Fig. 12. Normalized gate trigger voltage as a function of junction temperature

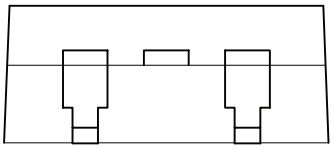
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11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) TO263





Unit		A	A1	b	b1	c	c1	D	D1	E	E1	e	H	L	L1	L2	L3
MM	min	4.35	0.00	0.69	1.14	0.38	1.14	8.50	7.50	10.00	8.25	2.54 (BSC)	14.60	2.50	1.00	1.27	0.25 (BSC.)
	max	4.75	0.15	0.99	1.73	0.61	1.40	9.02	8.00	10.40	8.80		15.60	2.79	1.65	1.78	

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Document status [1][2]	Product status [3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 25 April 2019