

100336

Low Power 4-Stage Counter/Shift Register

General Description

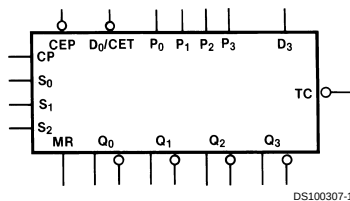
The 100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used

to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset ($\overline{MR}$) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 k Ω pull-down resistors.

Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/function compatible with 100136
- Voltage compensated operating range = -4.2V to -5.7V
- Standard Microcircuit Drawing (SMD) 5962-9230601

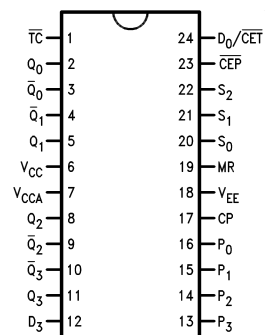
Logic Symbol



Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0 – S_2	Select Inputs
MR	Master Reset Input
P_0 – P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0 – Q_3	Data Outputs
$\overline{Q_0}$ – $\overline{Q_3}$	Complementary Data Outputs

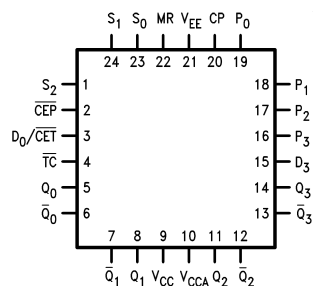
Connection Diagrams

24-Pin DIP



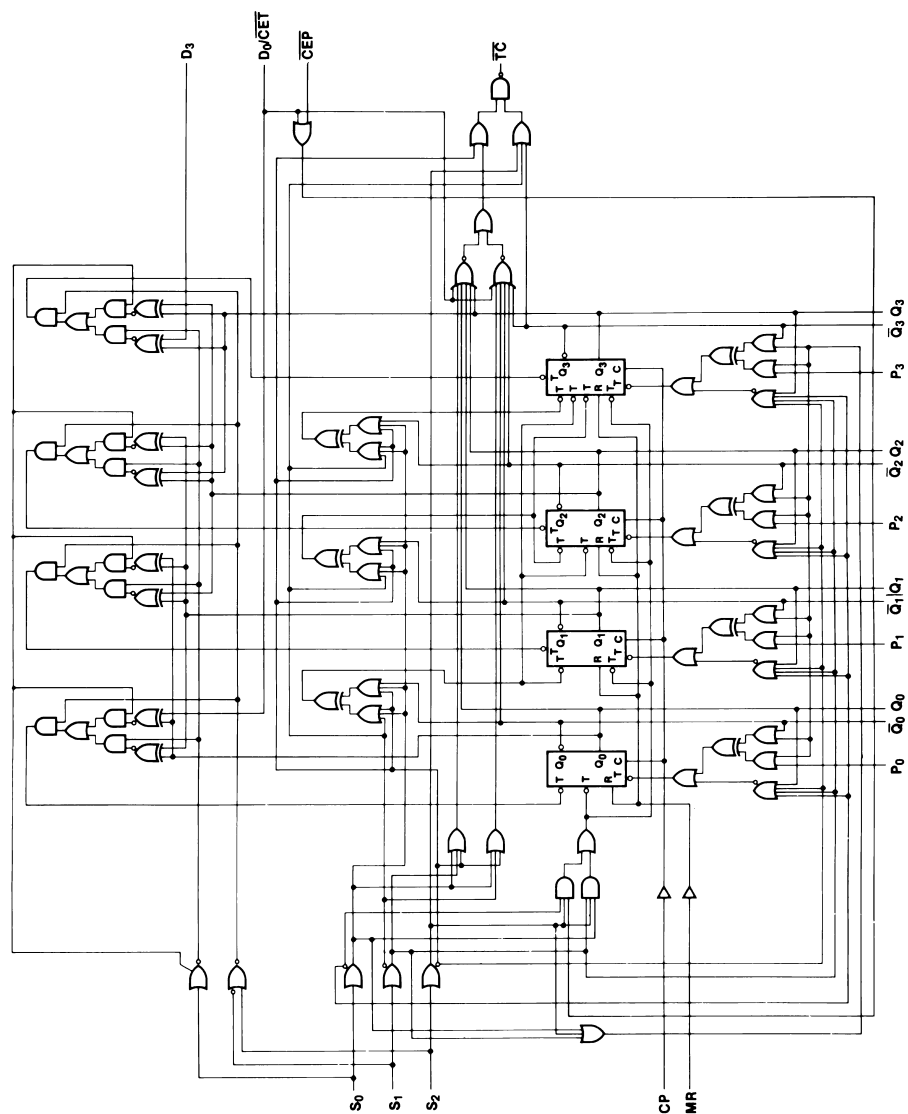
DS100307-2

24-Pin Quad Cerpak



DS100307-3

Logic Diagram



DS100307-5

Function Select Table

S ₂	S ₁	S ₀	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Truth Table

Q₀ = LSB

Inputs								Outputs				TC	Mode
MR	S ₂	S ₁	S ₀	CEP	D ₀ /CET	D ₃	CP	Q ₃	Q ₂	Q ₁	Q ₀		
L	L	L	L	X	X	X	↗	P ₃	P ₂	P ₁	P ₀	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$	L	Invert
L	L	H	L	X	X	X	↗	D ₃	Q ₃	Q ₂	Q ₁	D ₃	Shift to LSB
L	L	H	H	X	X	X	↗	Q ₂	Q ₁	Q ₀	D ₀	Q ₃ (Note 1)	Shift to MSB
L	H	L	L	L	L	X	↗	(Q ₀₋₃) minus 1				1	Count Down
L	H	L	L	H	L	X	X	Q ₃	Q ₂	Q ₁	Q ₀	1	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q ₀₋₃) plus 1				2	Count Up
L	H	H	L	H	L	X	X	Q ₃	Q ₂	Q ₁	Q ₀	2	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

1 = L if Q₀-Q₃ = LLLL

H if Q₀-Q₃ ≠ LLLL

2 = L if Q₀-Q₃ = HHHH

H if Q₀-Q₃ ≠ HHHH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↗ = LOW-to-HIGH Transition

Note 1: Before the clock, $\overline{TC}$ is Q₃

After the clock, $\overline{TC}$ is Q₂

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature (T_{STG})	–65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	–7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	–50 mA
ESD (Note 3)	≥2000V

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Recommended Operating Conditions

Case Temperature (T_C)

Military

–55°C to +125°C

Supply Voltage (V_{EE})

–5.7V to –4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	–1025	–870	mV	0°C to +125°C	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to –2.0V (Notes 4, 5, 6)
		–1085	–870	mV	–55°C		
V_{OL}	Output LOW Voltage	–1830	–1620	mV	0°C to +125°C		
		–1830	–1555	mV	–55°C		
V_{OHC}	Output HIGH Voltage	–1035		mV	0°C to +125°C	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to –2.0V (Notes 4, 5, 6)
		–1085		mV	–55°C		
V_{OLC}	Output LOW Voltage		–1610	mV	0°C to +125°C		
			–1555	mV	–55°C		
V_{IH}	Input HIGH Voltage	–1165	–870	mV	–55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 4, 5, 6, 7)
V_{IL}	Input LOW Voltage	–1830	–1475	mV	–55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 4, 5, 6, 7)
I_{IL}	Input LOW Current	0.50		μA	–55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL (Min)}$	(Notes 4, 5, 6)
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH (Max)}$	(Notes 4, 5, 6)
			340	μA	–55°C		
I_{EE}	Power Supply Current	–185	–70	mA	–55°C to +125°C	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	(Notes 4, 5, 6)
		–195	–70				

Note 4: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.

Note 5: Screen tested 100% on each device at –55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 6: Sample tested (Method 5005, Table I) on each manufactured lot at –55°C, +25°C, +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 7: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version AC Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{shift}	Shift Frequency	325		325		325		MHz	Figures 2, 3	(Note 11)
t_{PLH}	Propagation Delay	0.40	2.30	0.50	2.20	0.40	2.50	ns	Figures 1, 3	(Notes 8, 9, 10, 12)
t_{PHL}	CP to Q_n , $\overline{Q}_n$									
t_{PLH}	Propagation Delay	1.30	3.90	1.70	3.80	1.70	4.20	ns	Figures 1, 7, 8	
t_{PHL}	CP to $\overline{TC}$ (Shift)									
t_{PLH}	Propagation Delay	1.20	4.60	1.50	4.60	1.60	5.20	ns	Figures 1, 9	(Notes 8, 9, 10, 12)
t_{PHL}	CP to $\overline{TC}$ (Count)									
t_{PLH}	Propagation Delay	0.60	2.90	0.80	2.80	0.90	3.20	ns	Figures 1, 4	(Notes 8, 9, 10, 12)
t_{PHL}	MR to Q_n , $\overline{Q}_n$									
t_{PLH}	Propagation Delay	2.30	5.20	2.70	5.20	2.90	5.90	ns	Figures 1, 12	
t_{PHL}	MR to $\overline{TC}$ (Count)									
t_{PHL}	Propagation Delay	2.10	4.30	2.20	4.10	2.40	4.70	ns	Figures 1, 10, 11	(Notes 8, 9, 10, 12)
t_{PHL}	MR to $\overline{TC}$ (Shift)									
t_{PLH}	Propagation Delay	0.70	3.20	1.00	3.20	1.30	4.10	ns	Figures 1, 5	(Notes 8, 9, 10, 12)
t_{PHL}	$D_0/\overline{CET}$ to $\overline{TC}$									
t_{PLH}	Propagation Delay	1.30	4.10	1.50	4.20	1.70	4.90	ns		
t_{PHL}	S_n to $\overline{TC}$									
t_{TLH}	Transition Time	0.20	1.90	0.20	1.80	0.20	2.00	ns	Figures 1, 3	(Note 11)
t_{THL}	20% to 80%, 80% to 20%									
t_s	Setup Time									
	D_3	1.40		1.40		1.40		ns	Figure 6	(Note 11)
	P_n	1.70		1.70		1.70				
	$D_0/\overline{CET}$	1.80		1.80		1.80				
	$\overline{CEP}$	1.80		1.80		1.80				
	S_n	3.30		3.30		3.30				
	MR (Release Time)	2.60		2.60		2.60				
t_h	Hold Time									
	D_3	0.90		0.90		0.90		ns	Figure 6	(Note 11)
	P_n	1.00		1.00		1.00				
	$D_0/\overline{CET}$	0.70		0.70		0.70				
	$\overline{CEP}$	0.60		0.60		0.60				
	S_n	0.00		0.00		0.00				
$t_{pw}(H)$	Pulse Width	1.60		1.60		1.60		ns	Figures 3, 4	(Note 11)
	HIGH: CP MR	2.00		2.00		2.00				

Note 8: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

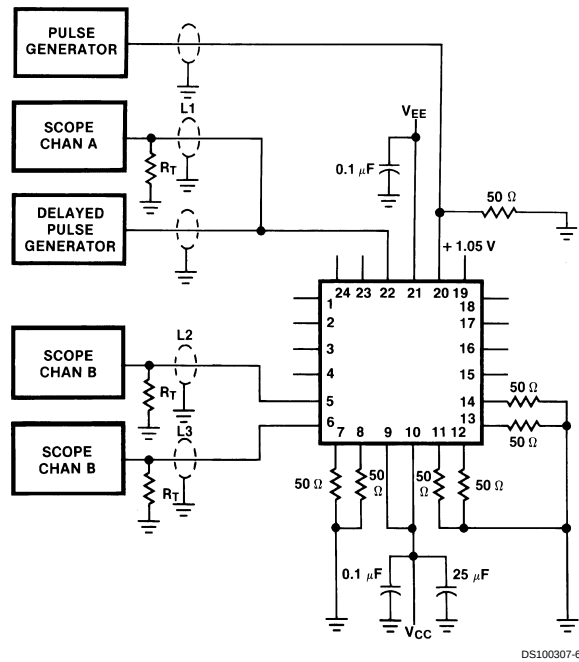
Note 9: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroups A9.

Note 10: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroups A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 11: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 12: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Test Circuitry



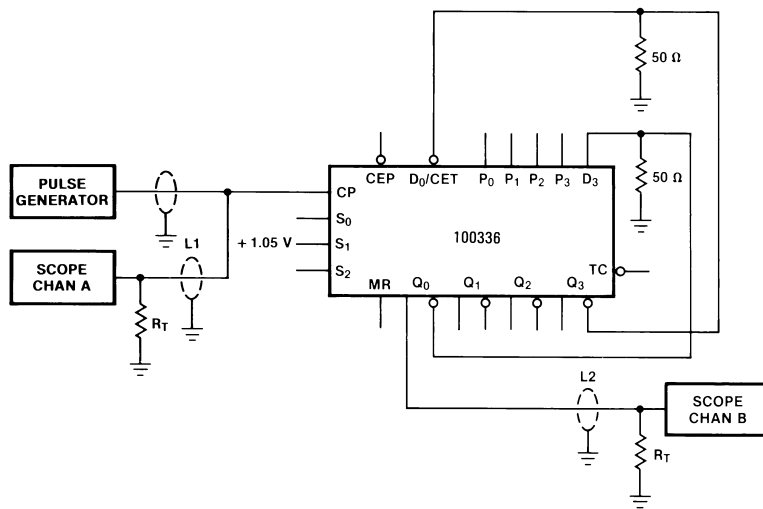
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Notes:

V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$
 $L1$, $L2$ and $L3 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3\ pF$
 Pin numbers shown are for flatpak;
 for DIP see logic symbol

FIGURE 1. AC Test Circuit

Test Circuitry (Continued)



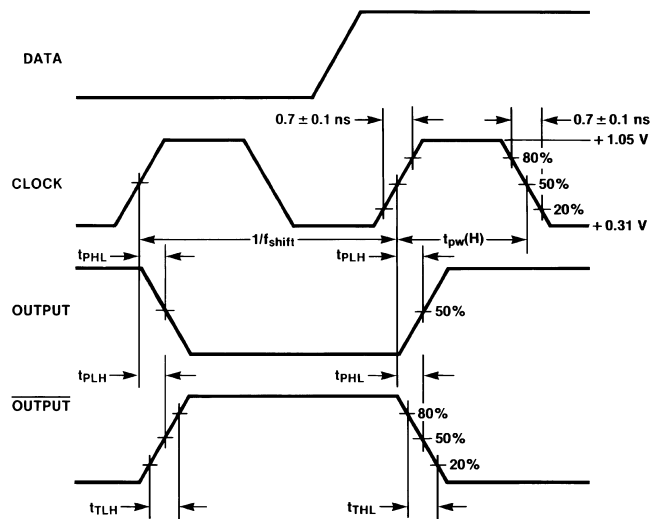
DS100307-7

Notes:

For shift right mode, +1.05V is applied at S_0 .
The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms



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FIGURE 3. Propagation Delay (Clock) and Transition Times

Switching Waveforms (Continued)

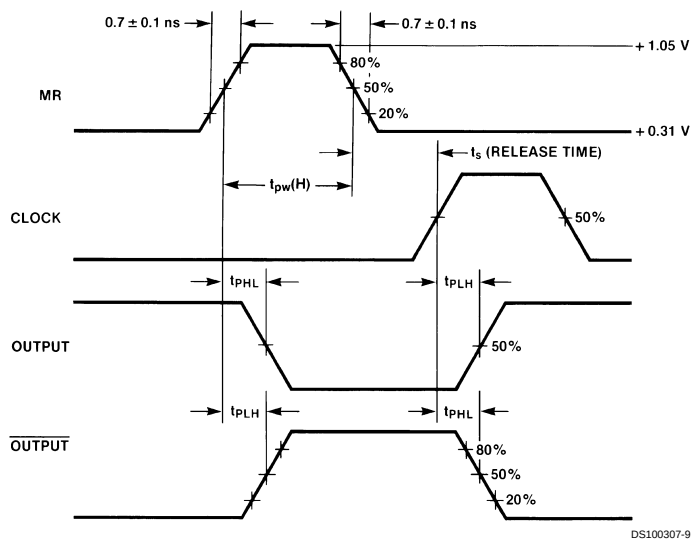


FIGURE 4. Propagation Delay (Reset)

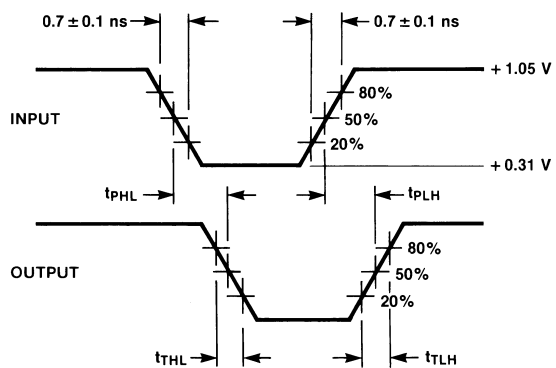
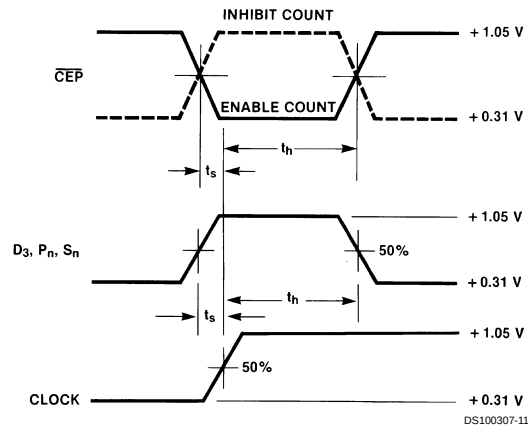


FIGURE 5. Propagation Delay (Serial Data, Selects)

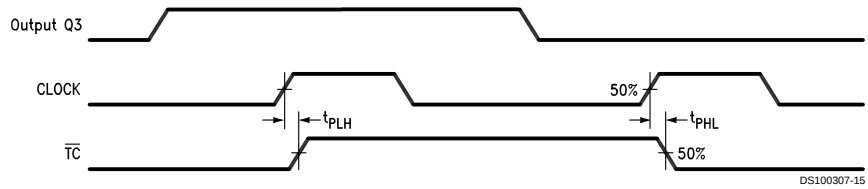
Switching Waveforms (Continued)



Notes:

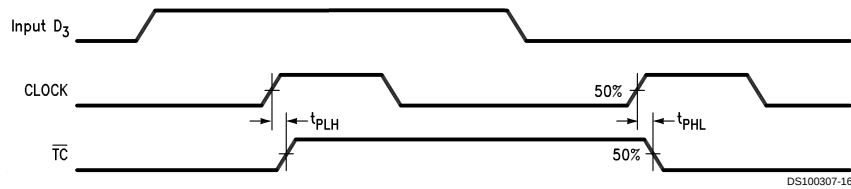
t_s is the minimum time before the transition of the clock that information must be present at the data input.
 t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time



Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

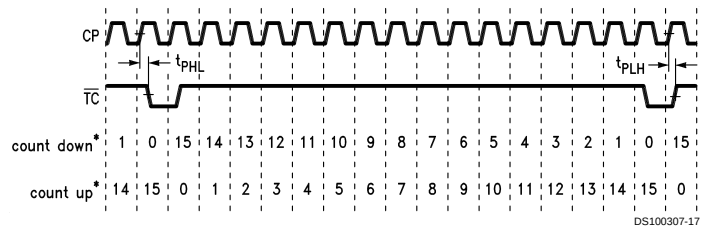
FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)



Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)

Switching Waveforms (Continued)



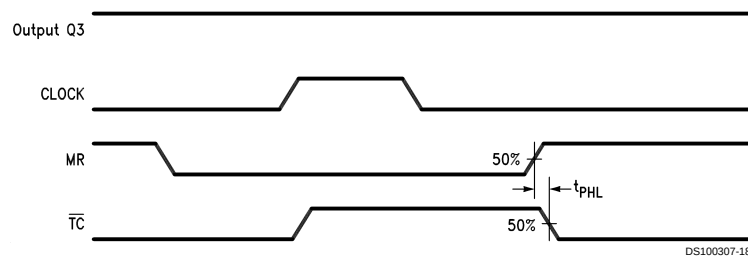
Note:

*Decimal representation of binary outputs.

Count Up: $S_0 = L, S_1 = H, S_2 = H$; Count Down: $S_0 = L, S_1 = L, S_2 = H$.

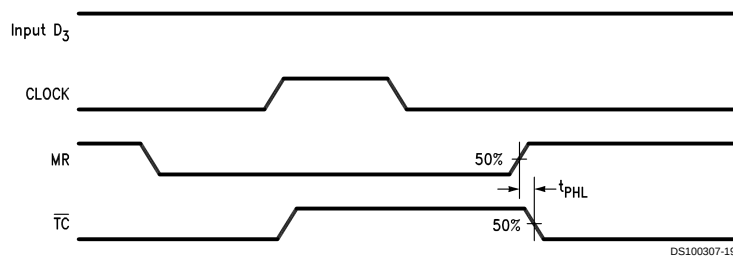
Measurement taken at 50% point of waveform.

FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)



Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

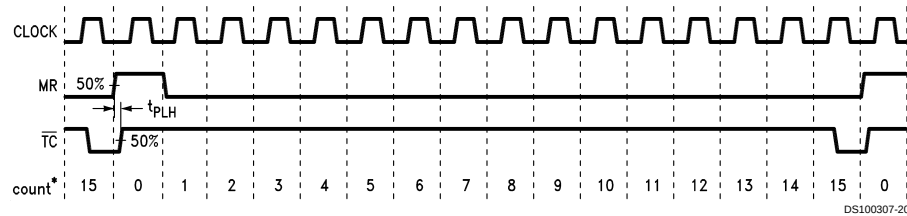
FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)



Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

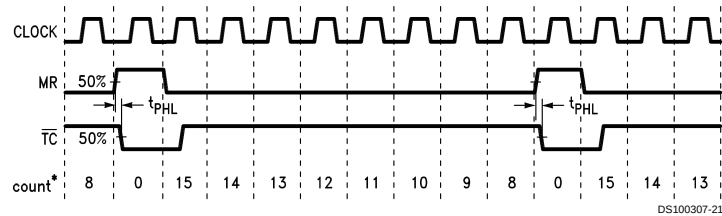
FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)

Switching Waveforms (Continued)



Note:

*Decimal representation of binary outputs. Count Up Mode: $S_0 = L$, $S_1 = H$, $S_2 = H$.



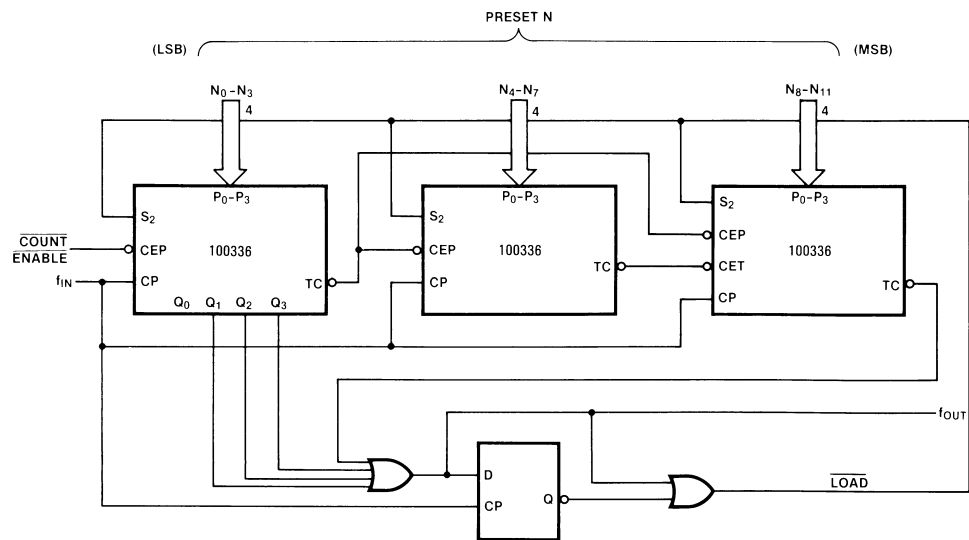
Note:

*Decimal representation of binary outputs. Count Down Mode: $S_0 = L$, $S_1 = L$, $S_2 = H$.

FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)

Applications

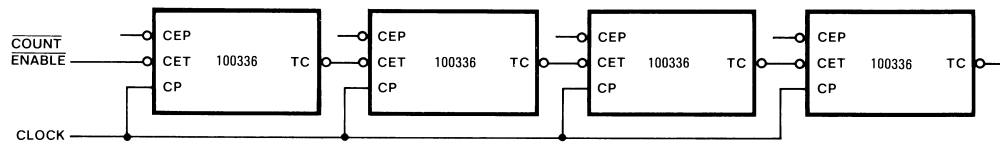
3-Stage Divider, Preset Count Down Mode



Note: If $S_0 = S_1 = S_2 = \text{LOW}$, then $T_C = \text{LOW}$

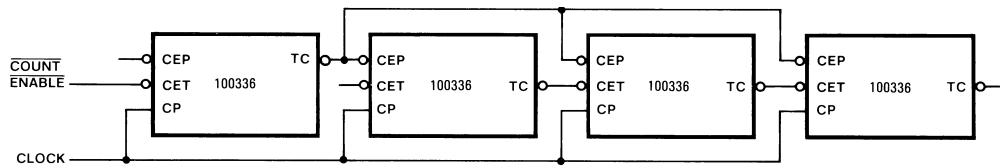
Applications (Continued)

Slow Expansion Scheme

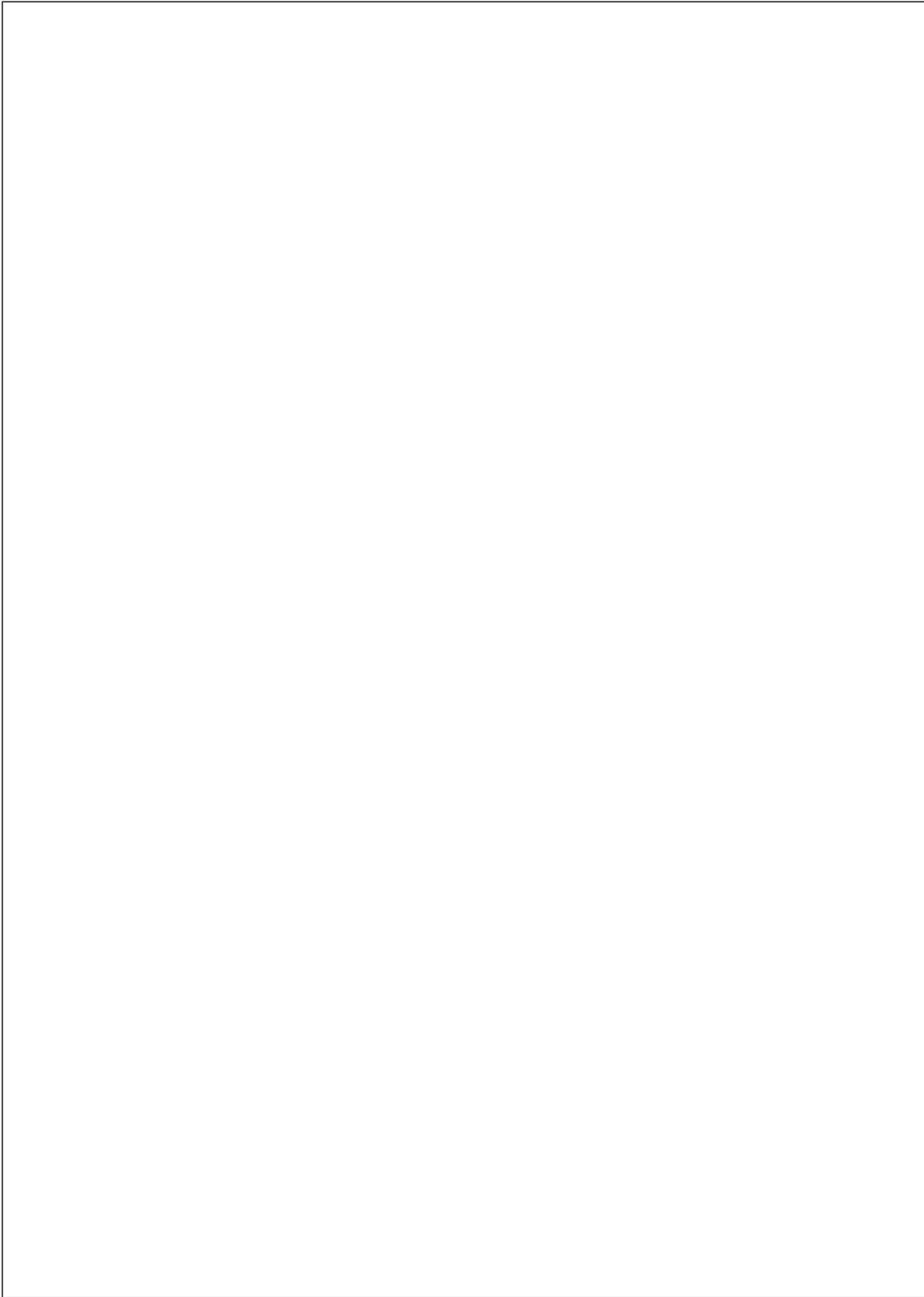


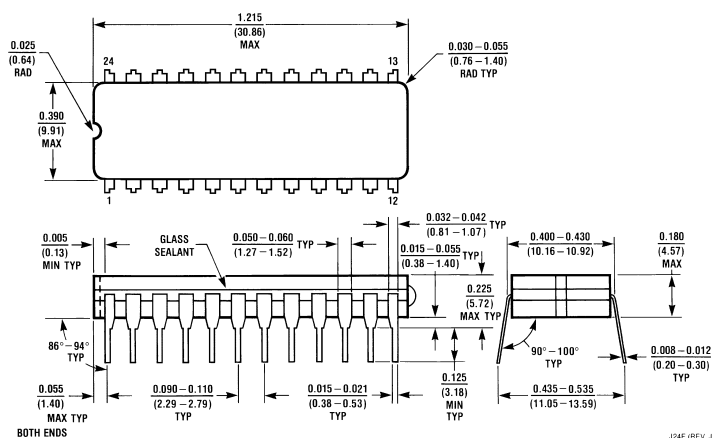
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Fast Expansion Scheme

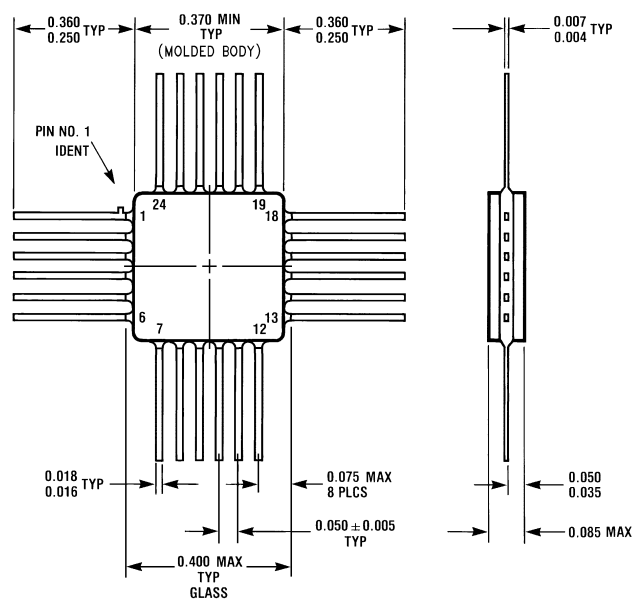


DS100307-14



Physical Dimensions inches (millimeters) unless otherwise noted

24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

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