SINGLE CHANNEL PWM CONTROLLER WITH NMOS LDO CONTROLLER AND 5V BIAS REGULATOR

ADVANCE DATA SHEET

Pb Free Product

DESCRIPTION

The NX2710 controller IC is a compact synchronous Buck controller IC with 16 lead SOIC package designed for step down DC to DC converter applications with feedforward functionality. Voltage feedforward provides fast response, good line regulation and nearly constant power stage gain under wide voltage input range. The NX2710 controller is optimized to convert single supply up to 24V bus voltage to as low as 0.8V output voltage. Internal UVLO keeps the regulator off until the supply voltage exceeds 9V where internal digital soft starts get initiated to ramp up output. The NX2710 employs programmable current limiting and FB UVLO followed by HICCUP feature. Other features include: 5V gate drive, Programmable frequency from 300kHz to 1MHz, Adaptive deadband control, Internal digital soft start; Vcc under voltage lockout and shutdown capability via comp pin.

FEATURES

- Bus voltage operation from 9V to 24V
- 5V bias regulator available
- Excellent dynamic response with input voltage feed-forward and voltage mode control
- Programmable switching frequency up to 1MHz
- Internal Digital Soft Start Function
- Programmable hiccup current limit
- Shutdown by pulling COMP pin low
- NMOS LDO controller available
- Start into precharged output
- Pb-free and RoHS compliant

APPLICATIONS

- Notebook PC
- Graphic Card on board converters
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Set Top Box and LCD Display

TYPICAL APPLICATION

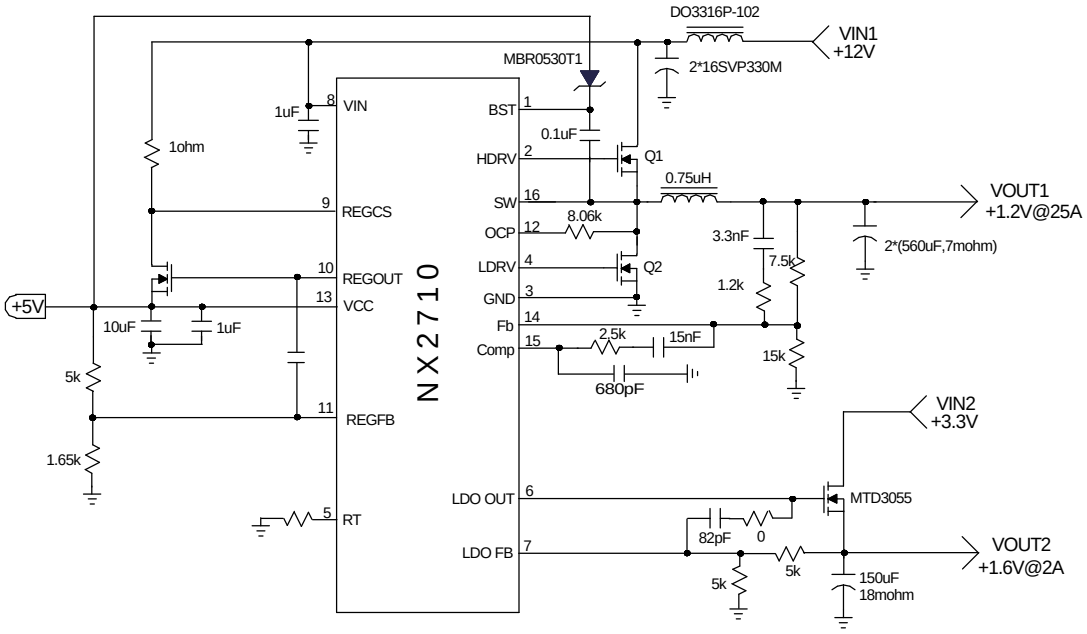


Figure1 - Typical application of NX2710

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2710CSTR	0 to 70° C	SOIC -16L	300kHz to 1MHz	Yes

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ABSOLUTE MAXIMUM RATINGS

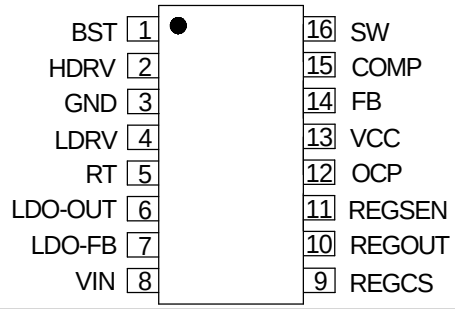
VCC to GND & BST to SW voltage ..... -0.3V to 6.5V
VIN to GND ..... -0.3V to 25V
BST, HDRV, REGCS to GND Voltage ..... -0.3V to 35V
SW to GND ..... -2V to 35V
REGOUT to GND ..... 0.2 to 16V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C
ESD Susceptibility 2kV

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

16-LEAD PLASTIC SOIC

$\theta_{JA} \approx 83^{o}C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =5V, VIN=12V and T_A = 0 to 70°C. Typical values refer to T_A = 25°C.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}			0.8		V
Ref Voltage line regulation				0.2		%
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.75		5.25	V
Operating quiescent current	I_Q	switching is off		3	5	mA
Vcc UVLO						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4.4		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		9		25	V
Input Voltage Current		Vin=24V		9	10	mA

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{in} Rising		8.8		V
V_{in}-Hysteresis	V_{in}_Hyst	V_{in} Falling		0.8		V
Oscillator (Rt)						
Frequency	F_S	RT=open		300		KHz
Frequency Over Vin			-5		5	%
Ramp-Amplitude Voltage	V_{RAMP}	Vin=20V		2		V
Ramp Offset				0.8		V
Ramp/Vin Gain				0.1		V/V
Max Duty Cycle				90		%
Min on time					150	nS
Error Amplifiers						
Transconductance				2500		umho
Input Bias Current	Ib				100	nA
Comp SD threshold				0.3		V
Vref and Soft Start						
Soft Start time	Tss	Fs=300kHz		6.8		mS
High Side Driver (CL=3300pF) Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		0.8		ohm
Rise Time	THdrv(Rise)	10% to 90%		50		ns
Fall Time	THdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		30		ns
Low Side Driver (CL=3300pF) Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		50		ns
Fall Time	TLdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		30		ns
OCP Adjust						
OCP current setting				32		uA
FBUVLO						
Feedback UVLO threshold		percent of nominal	65	70	75	%
Over temperature						
Threshold				150		°C
Hysteresis				20		°C

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
LDO Controller FB Pin- Bias Current					100	nA
LDO FB Voltage		LDO_OUT=LDO_FB		0.8		V
LDO FB UVLO		percent of nominal	65	70	75	%
High Output Voltage		VIN=12V, LDO_FB=0.7V I_{O_SOURCE}=1.4mA		10.2		V
Low Output Voltage		VIN=12V, LDO_FB=0.9V I_{O_SINK}=1.4mA		0.2		V
High Output Source Current				3		mA
5V AUX REG Current limit threshold				100		mV
FB Pin- Bias Current				0		uA
RegFb Voltage		Regout=RegFb		1.25		V
Regout Output Voltage High		VIN=12V, RegFb=1.1V I_{O_SOURCE}=1.4mA		11		V
Regout Output Voltage Low		VIN=12V, RegFb=1.4V I_{O_SINK}=1.4mA		0.2		V
Open Loop Gain		GBNT(Note1)	50			DB

Note 1: This parameter is guaranteed by design but not tested in production(GBNT).

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PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VCC	This pin supplies the internal 5V bias circuit. . A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin.
BST	This pin supplies voltage to high side FET driver. A high freq minimum 0.1uF ceramic capacitor is placed as close as possible to and connected to this pin and SW pin.
GND	Power ground.
FB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop.
SW	This pin is connected to source of high side FETs and provide return path for the high side driver.
HDRV	High side gate driver output.
LDRV	Low side gate driver output.
VIN	Bus voltage input provides power supply to oscillator, VIN UVLO signal and 5V regulator controller.
RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.
LDO FB	LDO controller feedback input. If the LDOFB pin is pulled below 0.7*Vref, an internal comparator after certain delay and pulls down LDOOUT pin and initiates the HICCUP circuitry.
LDO OUT	LDO controller output. This pin is controlling the gate of an external NCH MOSFET. The maximum rating of this pin is 16V.
REGCS	This pin is 5V regulator current limit pin. It compares the voltage drop on the resistor which is connected between Vin and REGCS pin with internal offset 100mV. 1ohm resistor sets the current limit 100mA.
REGOUT	The output of the 5V regulator controller that drives a low current low cost external bipolar transistor or an external MOSFET to regulate the voltage at Vcc pin derived from bus voltage. This eliminates an otherwise external regulator needed in applications where 5V is not available.
REGSEN	Feedback pin of the 5V regulator controller. A resistor divider is connected from the output of the 5V regulator to this pin to complete the loop.
OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on.

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BLOCK DIAGRAM

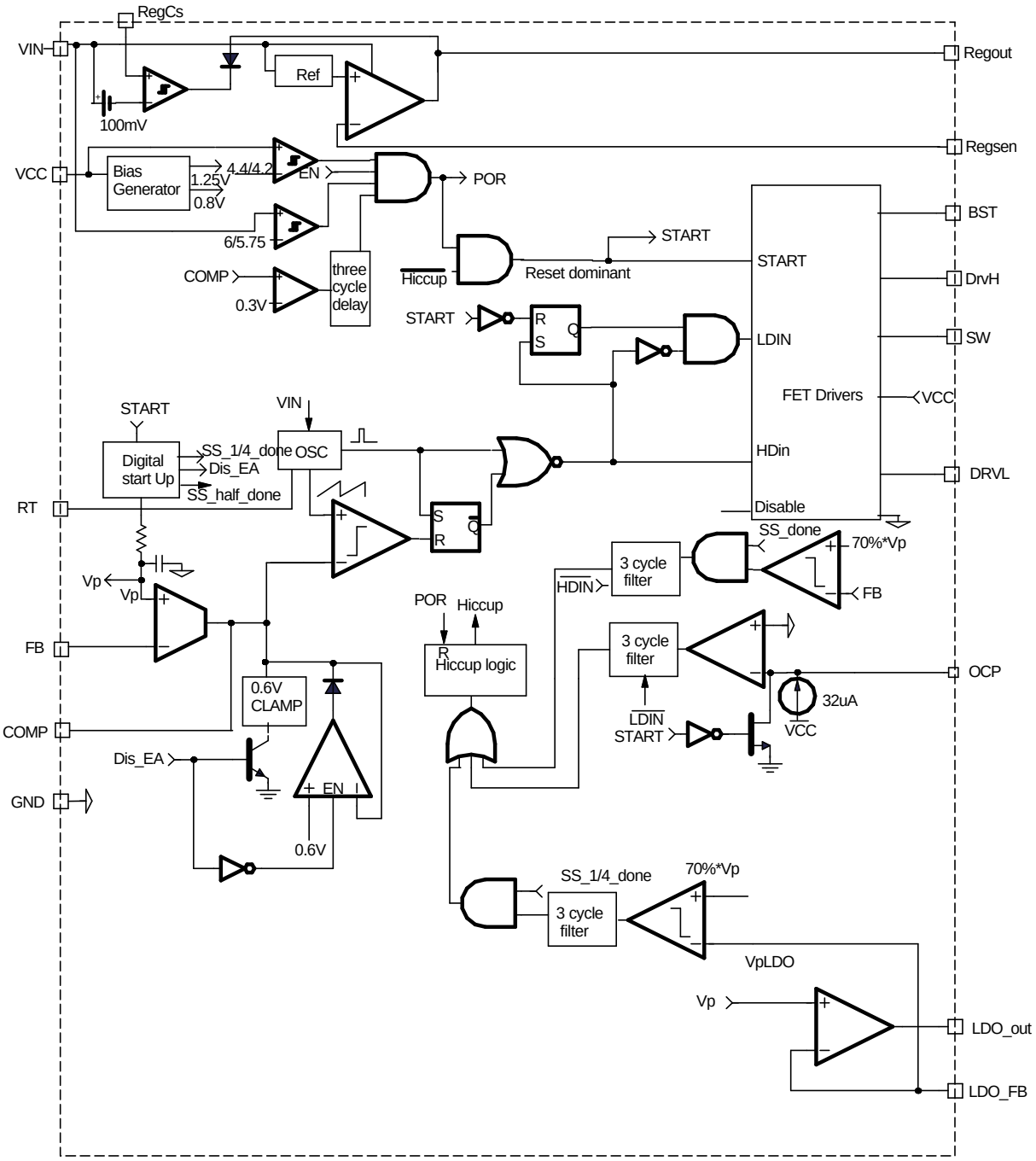


Figure 2 - Simplified block diagram of the NX2710

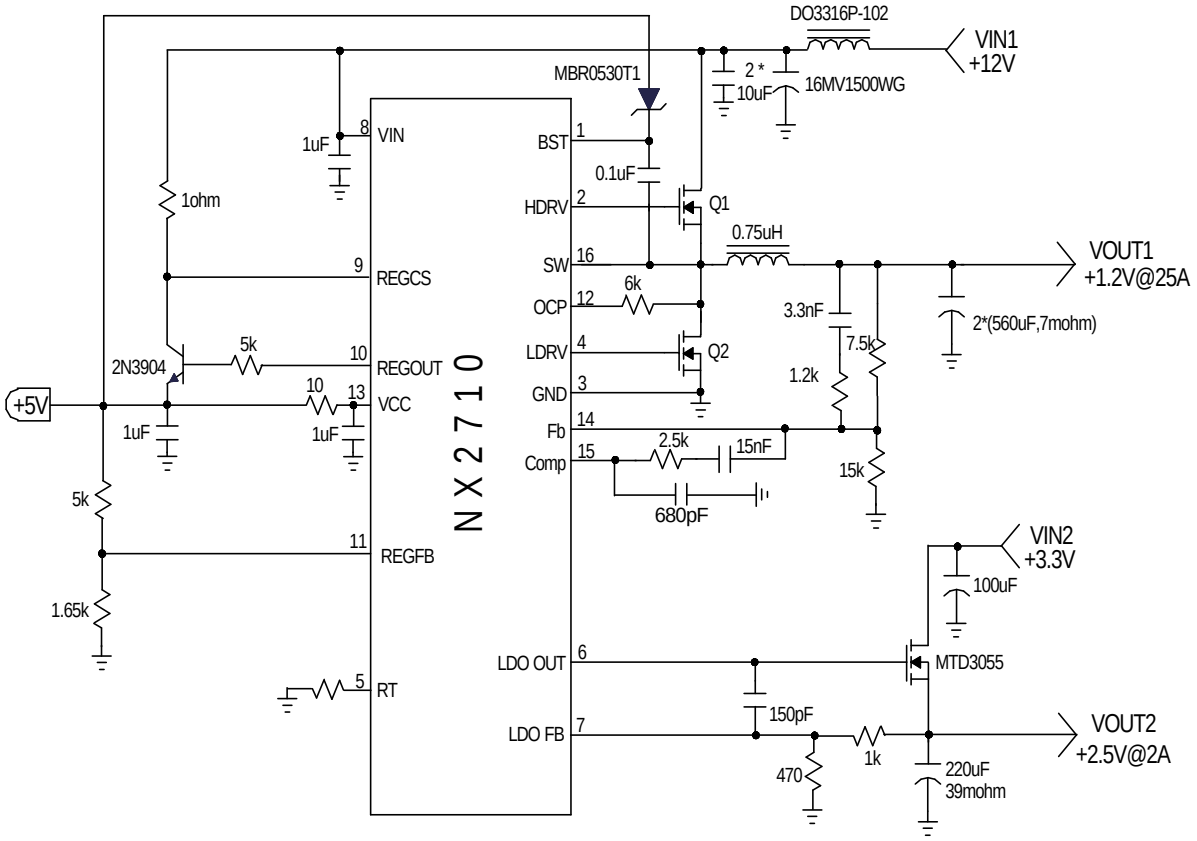


Figure 3 - Simplified Demo board schematic

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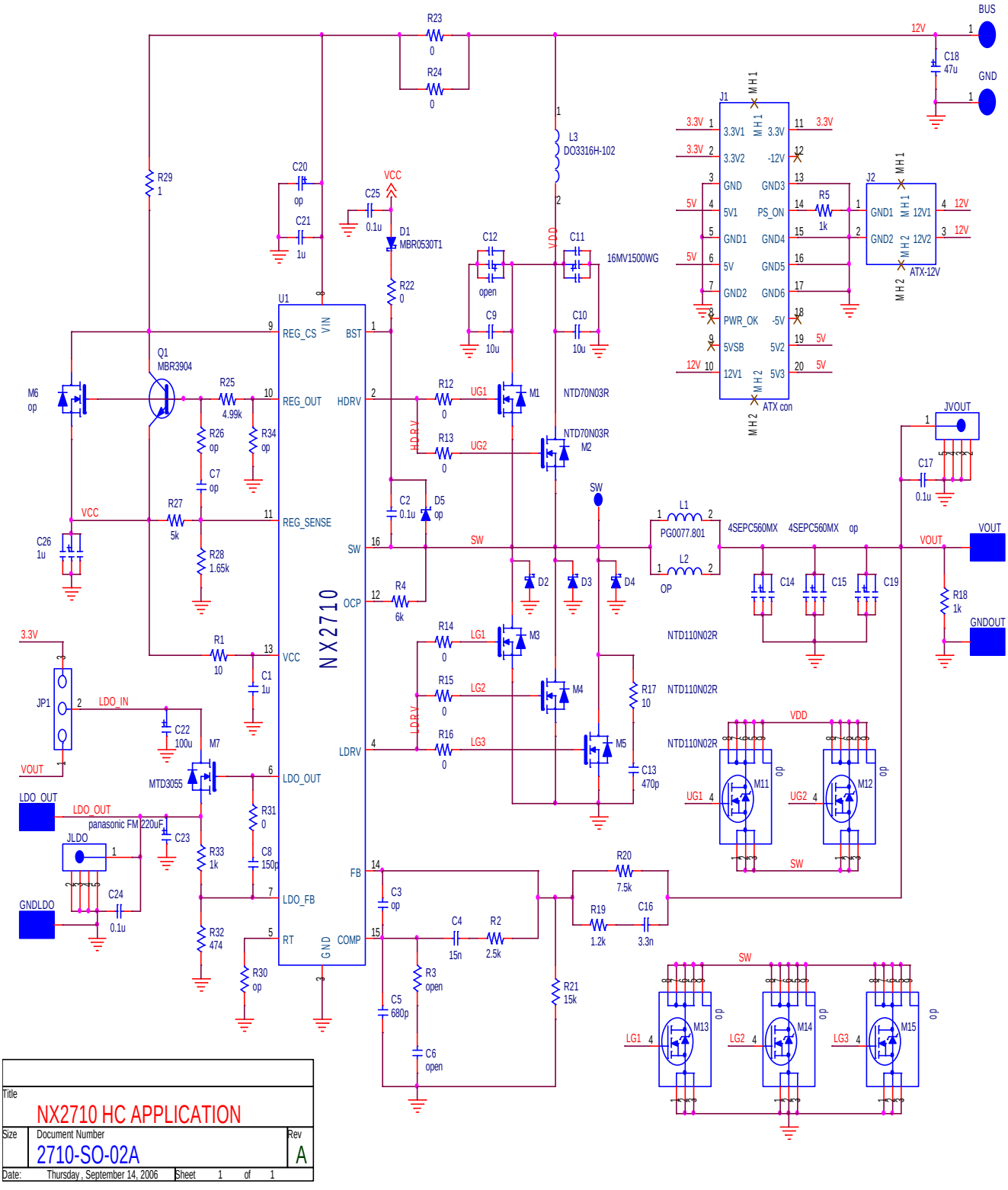


Figure 4 - Demo board schematic based on ORCAD

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Bill of Materials

Item	Quantity	Reference	Part
1	3	C1,C21,C26	1u
2	4	C2,C17,C24,C25	0.1u
3	1	C4	15n
4	1	C5	680p
5	1	C8	150p
6	2	C9,C10	10u
7	1	C11	16MV1500WG
8	1	C13	470p
9	2	C14,C15	4SEPC560MX
10	1	C16	3.3n
11	1	C18	47u
12	1	C22	100u
13	1	C23	panasonic FM 220uF
14	1	D1	MBR0530T1
15	1	L1	PG0077.801
16	1	L3	DO3316H-102
17	2	M1,M2	NTD70N03R
18	3	M3,M4,M5	NTD110N02R
19	1	M7	MTD3055
20	1	Q1	MBR3904
21	2	R1,R17	10
22	1	R2	2.5k
23	1	R4	6k
24	3	R5,R18,R33	1k
25	9	R12,R13,R14,R15,R16,R22,	0
26		R23,R24,R31	
27	1	R19	1.2k
	1	R20	7.5k
28	1	R21	15k
29	1	R25	4.99k
30	1	R27	5k
31	1	R28	1.65k
32	1	R29	1
33	1	R32	474
34	1	U1	NX2710

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Demoboard waveforms

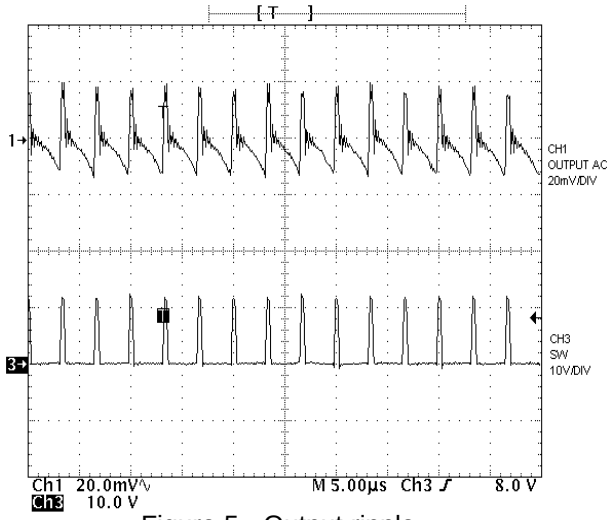


Figure 5 - Output ripple

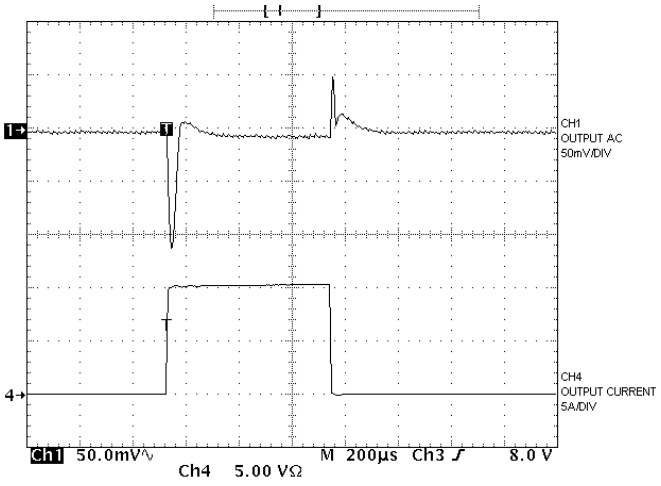


Figure 6 - Transient response @ 1.2 output

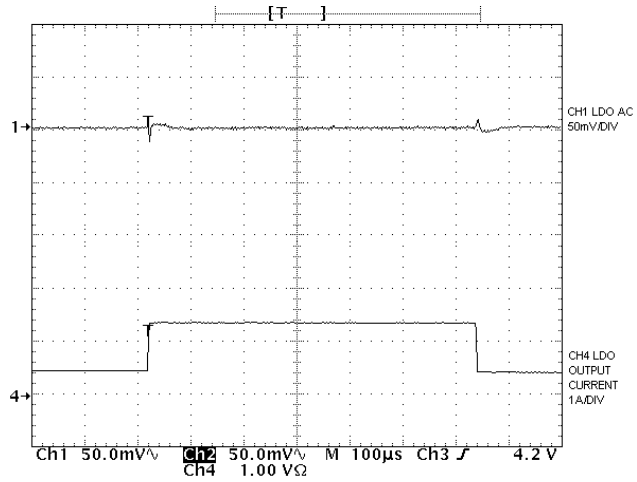


Figure 7 - Transient response @ LDO

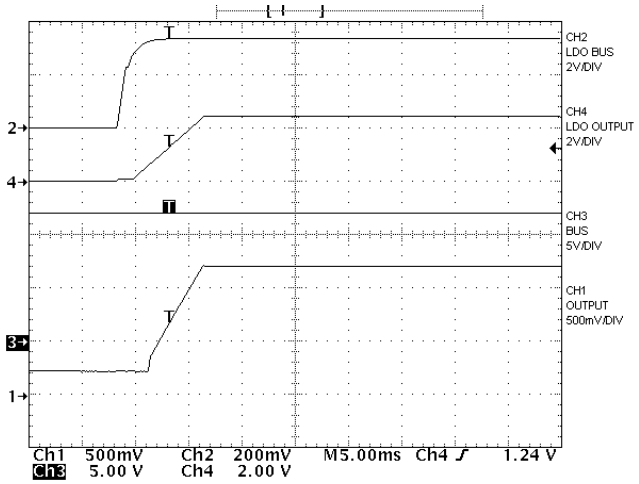


Figure 8 - Soft start

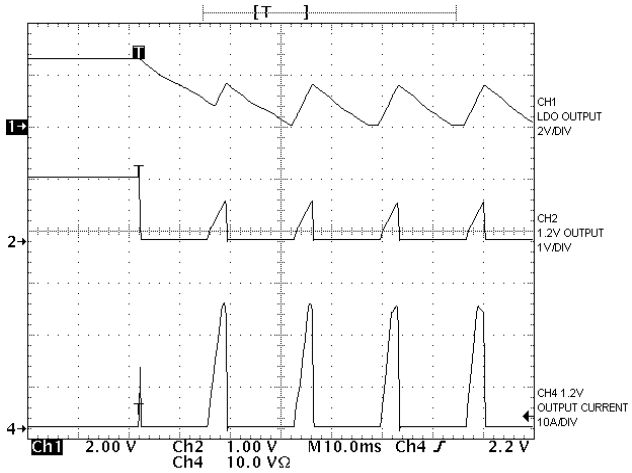


Figure 9 - 1.2V over current proteciton

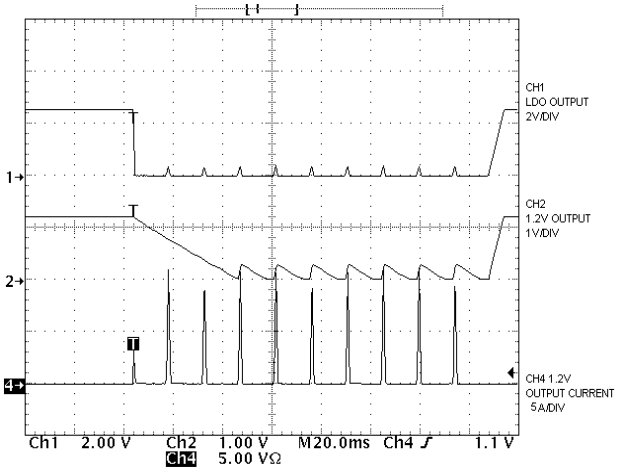


Figure 10 - LDO over current protection

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Switching frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

Power stage design requirements:
V_{IN}=12V
V_{OUT}=1.2V
I_{OUT} =25A
ΔV_{RIPPLE} <=20mV
ΔV_{TRAN}<=60mV @ 10A step
F_S=300kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.2, then

$$L_{OUT}=\frac{12V-1.2V}{0.2\times 25A}\times\frac{1.2V}{12V}\times\frac{1}{300kHz}$$

L_{OUT}=0.72uH

Choose L_{OUT}=0.75uH, then Pulse inductor PG0077.801 is a good choice.

Current Ripple is calculated as

$$I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$=\frac{12V-1.2V}{0.75uH}\times\frac{1.2V}{12V}\times\frac{1}{300kHz}=4.8A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, OSCON are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{15mV}{4.8A}=4.2m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 15mV output ripple, OSCON 4SEPC560MX with 7mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{7m\Omega\times 4.8A}{20mV}$$

N =1.68

The number of capacitor has to be round up to a integer. Choose N =2.

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If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors. The amount of ceramic capacitor output ripple is :

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times 300kHz \times C_{OUT}}$$

Using the above equations, although DC ripple spec can be met, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is

a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 60mV for 10A load step.

If the OSCON 4SEPC560MX(560uF, 7mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{7m\Omega \times 560\mu F \times 1.2V}{5A} = 0.94\mu H$$

The selected inductor is 0.75uH which is smaller than critical inductance. In that case, the output voltage transient mainly dependent on the ESR.

number of capacitor is

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} = \frac{7m\Omega \times 5A}{60mV} = 1.296$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

Voltage feedforward compensation is used in NX2710 to compensate the output voltage variation caused by input voltage changing. The feedforward funtion is realized by using VIN pin voltage to program the oscillator ramp voltage $V_{OSC}=0.1V_{IN}$, which provides nearly constant power stage gain under wide voltage input range.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R4>>2/gm. And it would be desirable if R1||R2||R3>>1/gm can be met at the same time,

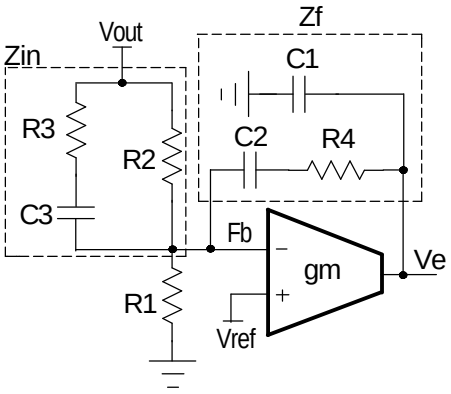


Figure 11 - Type III compensator using transconductance amplifier

Case 1: $F_{LC}<F_O<F_{ESR}$(for most ceramic or low ESR POSCAP, OSCON)

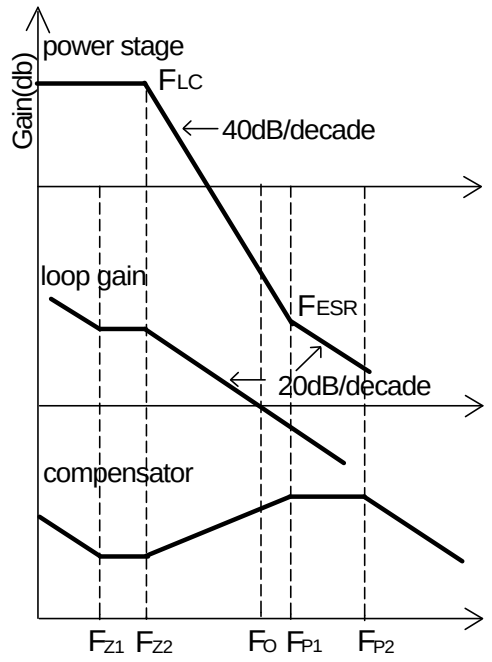


Figure 12 - Bode plot of Type III compensator ($F_{LC}<F_O<F_{ESR}$)

Typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_O<F_{ESR}$ and $F_O<=1/10F_s$ is shown as the following steps.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{0.75uH\times1120uF}}=5.5kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times3.5m\Omega\times1120uF}=40.6kHz$$

2. Set R_4 equal to 2.5kΩ.

3. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times0.75\times5.5kHz\times2.5k\Omega}=15nF$$

Choose C_2=15nF.

4. Calculate C_1 by equation (14) with pole F_{p2} at one third of the switching frequency.

$$C_1\approx\frac{1}{2\times\pi\times R_4\times F_{P2}}\approx\frac{1}{2\times\pi\times2.5k\Omega\times100kHz}\approx639pF$$

Choose C_1=680pF.

5. Calculate C_3 with the crossover frequency F_O at 15kHz.

$$C_3=\frac{V_{OSC}}{V_{IN}}\times\frac{2\times\pi\times F_O\times L\times C_{OUT}}{R_4}=\frac{1}{10}\times\frac{2\times\pi\times15kHz\times0.75uH\times1120uF}{2.5k\Omega}=3.2nF$$

Choose C_3=3.3nF.

6. Calculate R_3 by equation (13) with $F_{p1}=F_{ESR}$.

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times40.6kHz\times3.3nF}=1.18k\Omega$$

Choose R_3 =1.2kΩ.

7. Calculate R_2 by setting compensator zero F_{Z2} at the LC double pole.

$$R_2=\frac{1}{2\times\pi\times C_3}\times\left(\frac{1}{F_{Z2}}-\frac{1}{F_{P1}}\right)=\frac{1}{2\times\pi\times3.3nF}\times\left(\frac{1}{5.5kHz}-\frac{1}{40.6kHz}\right)=7.6k\Omega$$

Choose R_2 =7.5kΩ.

8. Calculate R_1 .

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} = \frac{7.5k\Omega \times 0.8V}{1.2V - 0.8V} = 15k\Omega$$

Choose R_1=15kΩ.

Case 2: F_{LC}<F_{ESR}<F_O(for electrolytic capacitors)

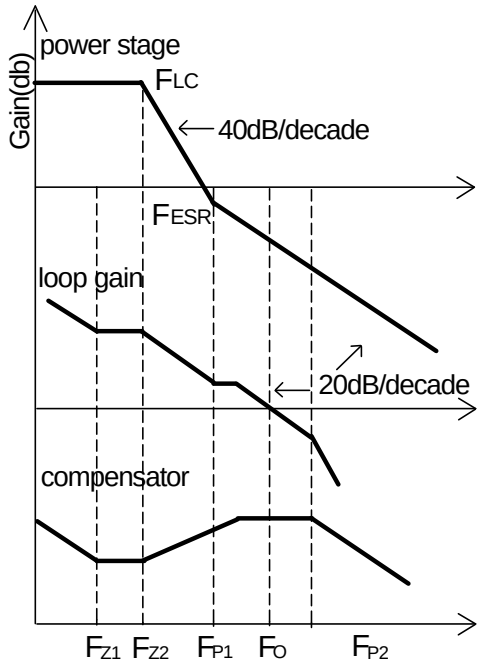


Figure 13 - Bode plot of Type III compensator (F_{LC}<F_{ESR}<F_O)

If electrolytic capacitors are used as output capacitors, typical design example of type III compensator in which the crossover frequency is selected as F_{LC}<F_{ESR}<F_O and F_O<=1/10F_s is shown as the following steps. Here two SANYO MV-WF1000 with 18 mΩ is chosen as output capacitor, output inductor is 2.2uH, output voltage is 1.2V, switching frequency is 200kHz.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = \frac{1}{2 \times \pi \times \sqrt{2.2uH \times 2000uF}} = 2.4kHz$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} = \frac{1}{2 \times \pi \times 9m\Omega \times 2000uF} = 8.8kHz$$

2. Set R_4 equal to 2.5kΩ.

3. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2 = \frac{1}{2 \times \pi \times F_{Z1} \times R_4} = \frac{1}{2 \times \pi \times 0.75 \times 2.4kHz \times 2.5k\Omega} = 35nF$$

Choose C_2=33nF.

4. Calculate C_1 by equation (14) with pole F_{p2} at one third of the switching frequency.

$$C_1 \approx \frac{1}{2 \times \pi \times R_4 \times F_{P2}} \approx \frac{1}{2 \times \pi \times 2.5k\Omega \times 66.7kHz} \approx 959pF$$

Choose C_1=1nF.

5. Calculate R_3 with the crossover frequency F_O at 15kHz.

$$R_3 = \frac{V_{IN}}{V_{OSC}} \times \frac{ESR \times R_4}{2 \times \pi \times F_O \times L} = 10 \times \frac{9mohm \times 2.5k\Omega}{2 \times \pi \times 15kHz \times 1uH} = 1.08k\Omega$$

Choose R_3=1.2kΩ.

6. Calculate C_3 by equation (13) with F_{p1} =F_{ESR}.

$$C_3 = \frac{1}{2\times\pi\times F_{P1}\times R_3}$$
$$= \frac{1}{2\times\pi\times 8.8kHz\times 1.2k\Omega}$$
$$= 14nF$$

Choose C_3 =15nF.

7. Calculate R_2 by setting compensator zero F_{Z2} at the LC double pole.

$$R_2 = \frac{1}{2\times\pi\times C_3}\times\left(\frac{1}{F_{Z2}} - \frac{1}{F_{P1}}\right)$$
$$= \frac{1}{2\times\pi\times 15nF}\times\left(\frac{1}{2.4kHz} - \frac{1}{8.8kHz}\right)$$
$$= 3.2k\Omega$$

Choose R_2 =4kΩ.

8. Calculate R_1 .

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT} - V_{REF}} = \frac{7.5k\Omega\times 0.8V}{1.2V - 0.8V} = 15k\Omega$$

Choose R_1=15kΩ.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

For this type of compensator, F_O need to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10F_s$.

Type II compensator can also be realized by simple RC circuit without feedback as shown in the following figure. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m\times\frac{R_1}{R_1+R_2}\times R_3 \quad \text{... (15)}$$

$$F_z = \frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

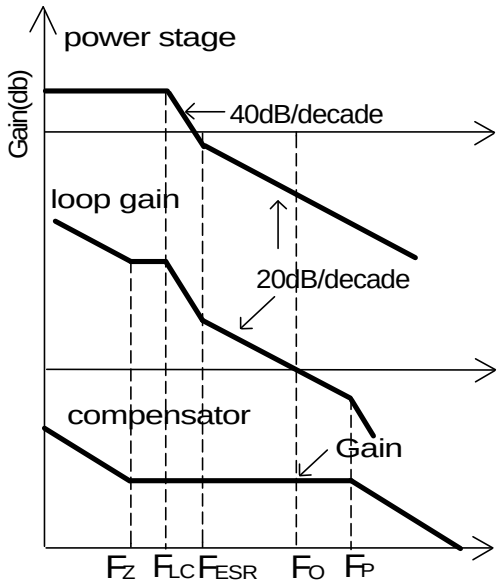


Figure 14 - Bode plot of Type II compensator

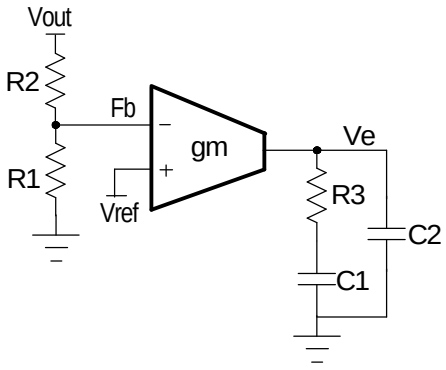


Figure 15 - Type II compensator with transconductance amplifier

The following is parameters for type II compensator design. Input voltage is 12V, output voltage is 2.5V, output inductor is 2.2uH, output capacitors are **two 680uF with 41mΩ** electrolytic capacitors.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$= \frac{1}{2\times\pi\times\sqrt{2.2uH\times 1360uF}}$$
$$= 2.9kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$= \frac{1}{2\times\pi\times 20.5m\Omega\times 1360uF}$$
$$= 5.7kHz$$

2.Set R_2 equal to10kΩ. Using equation 18, the final selection of R_1 is 4.7kΩ.

3. Set crossover frequency at 1/10 of the swithing frequency, here F_O=30kHz.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{R_{ESR}}\times\frac{1}{g_m}\times\frac{V_{OUT}}{V_{REF}}$$
$$=0.1\times\frac{2\times\pi\times 30kHz\times 2.2uH}{20.5m\Omega}\times\frac{1}{2.5mA/V}$$
$$\times\frac{2.5V}{0.8V}$$
$$=2.53k\Omega$$

Choose R_3 =2.55kΩ.

5. Calculate C_1 by setting compensator zero F_z at 75% of the LC double pole.

$$C_1 = \frac{1}{2\times\pi\times R_3\times F_z}$$
$$= \frac{1}{2\times\pi\times 2.55k\Omega\times 0.75\times 2.9kHz}$$
$$=28nF$$

Choose C_1=27nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi\times R_3\times F_s}$$
$$= \frac{1}{\pi\times 2.55k\Omega\times 300kHz}$$
$$=207pF$$

Choose C_2=220pF.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value.

The following equation applies to figure16, which shows the relationship between V_{OUT} , V_{REF} and voltage divider.

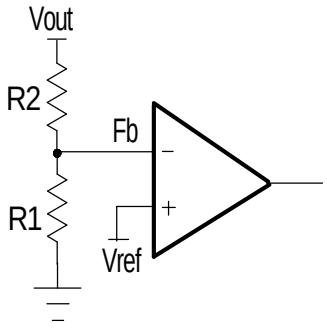


Figure 16 - Voltage Divider

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT}\times\sqrt{D}\times\sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(19)$$

V_{IN} = 12V, V_{OUT}=1.2V, I_{OUT}=25A, the result of input RMS current is 7.5A.

For higher efficiency, low ESR capacitors are recommended. Two Sanyo OS-CON 16SVP330M **16V 330uF 16mΩ** with 4.72A RMS rating are chosen as input capacitors.

Power MOSFETs Selection

The NX2710 requires at least two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In 25A output application, five IRFR3706 can be used, two for high side, three for low side. They have the following parameters: V_{DS}=30V, I_D =75A,R_{DSON} =9mΩ,Q_{GATE} =23nC.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON}=I_{OUT}^2\times D\times R_{DS(ON)}\times K$$
$$P_{LCON}=I_{OUT}^2\times(1-D)\times R_{DS(ON)}\times K \quad ...(20)$$
$$P_{TOTAL}=P_{HCON}+P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.4 at 125°C according to IRFR3706 datasheet. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW}=\frac{1}{2}\times V_{IN}\times I_{OUT}\times T_{SW}\times F_S \quad ...(21)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate}=(Q_{HGATE}\times V_{HGS}+Q_{LGATE}\times V_{LGS})\times F_S \quad ...(22)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Over Current Limit Protection

Over current protection is achieved by sensing current through the low side MOSFET. An internal current source of 32uA flows through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW}=-I_L\times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP}\times R_{OCP}+V_{SW}$$

When the voltage is below zero, the over current occurss as shown in figure 17.

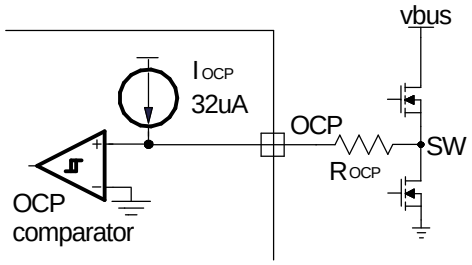


Figure 17 - Over Current Protection

The over current limit can be set by the following equation:

$$I_{SET}=\frac{I_{OCP}\times R_{OCP}}{K\times R_{DSON}}$$

If two MOSFETs R_{DSON}=6.5mΩ, the worst case thermal consideration K=1.5 and the current limit is set at 40A, then

$$R_{OCP}=\frac{I_{SET}\times K\times R_{DSON}}{I_{OCP}}=\frac{40A\times 1.5\times 6.5m\Omega}{32uA\times 2}=6.1k\Omega$$

Choose R_{OCP}=6kΩ.

For NX2710, if switching channel goes into hiccup current limit, the LDO will go to hiccup too.

LDO Selection Guide

NX2710 offers a LDO controller. The selection of MOSFET to meet LDO is more straight forward. The selection is that the Rdson of MOSFET should

meet the dropout requirement. For example.

V_{LDOIN}=3.3V

V_{LDOOUT}=2.5V

I_{Load}=2A

The maximum Rdson of MOSFET should be

$$R_{RDSON} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) / 2A = 0.4\Omega$$

Most of MOSFETs can meet the requirement. Moreimportant is that MOSFET has to be selected right package to handle the thermal capability. For LDO, maximum power dissipation is given as

$$P_{LOSS} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) \times 2A = 1.6W$$

Select IR MOSFET IRFR3706 with 9mΩ R_{DSON} is sufficient.

LDO Compensation

The diagram of LDO controller including VCC regulator is shown in the following figure.

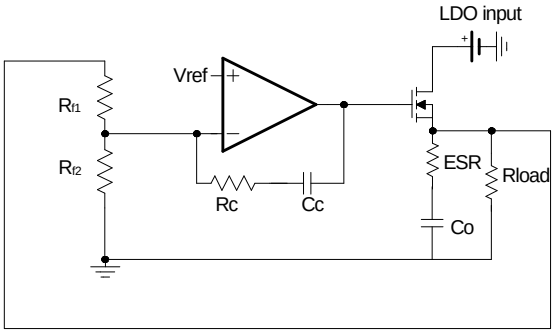


Figure 18 - NX2710 LDO controller.

For most low frequency capacitor such as electrolytic, POSCAP, OSCON, etc, the compensation parameter can be calculated as follows.

$$C_C = \frac{1}{4 \times \pi \times F_O \times R_{f1}} \times \frac{g_m \times ESR}{1 + g_m \times ESR}$$

where F_O is the desired crossover frequency.

Typically, in this LDO compensation, crossover frequency F_O has to be higher than zero caused by ESR. F_O is typically around several tens kHz to a few hundred kHz. For this example, we select Fo=100kHz.

g_m is the forward trans-conductance of MOSFET.

For IRF3706, g_m=53.

Select R_{f1}=5kohm.

Output capacitor is Sanyo POSCAP 4TPE150M with 150uF, ESR=25mohm.

$$C_C = \frac{1}{4 \times \pi \times 100kHz \times 5k\Omega} \times \frac{53 \times 25m\Omega}{1 + 53 \times 25m\Omega} = 91pF$$

Choose C_C=100pF. For electrolytic or POSCAP, R_C is typically selected to be zero.

R_{f2} is determined by the desired output voltage.

$$R_{f2} = \frac{R_{f1} \times V_{REF}}{V_{LDOOUT} - V_{REF}}$$
$$= \frac{5k\Omega \times 0.8V}{1.6V - 0.8V}$$
$$= 5k\Omega$$

Choose R_{f2}=5kΩ.

When ceramic capacitors or some low ESR bulk capacitors are chosen as LDO output capacitors, the zero caused by output capacitor ESR is so high that crossover frequency F_O has to be chosen much higher than zero caused by R_C and C_C and much lower than zero caused by ESR. For example, 10uF ceramic is used as output capacitor. We select Fo=100kHz, R_{f1}=5kohm and select MOSFET MTD3055(g_m=5S). R_C and C_C can be calculated as follows.

$$R_C = R_{f1} \times \frac{2 \times \pi \times F_O \times C_O}{0.5 \times g_m}$$
$$= 5k\Omega \times \frac{2 \times \pi \times 100kHz \times 10uF}{0.5 \times 5S}$$
$$= 12.56k\Omega$$

Choose R_C=12.7kΩ.

$$C_C = \frac{10 \times C_O}{R_C \times g_m}$$
$$= \frac{10 \times 10uF}{12.7k\Omega \times 5S}$$
$$= 16nF$$

Choose C_C=1.5nF.

Current Limit for LDO

Current limit of LDO is achieved by sensing the LDO feedback voltage. When LDO_FB pin is below 70% of V_{REF}, the IC goes into hiccup mode. The IC will turn off all the channel for 4096 cycles and start to restart system again.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

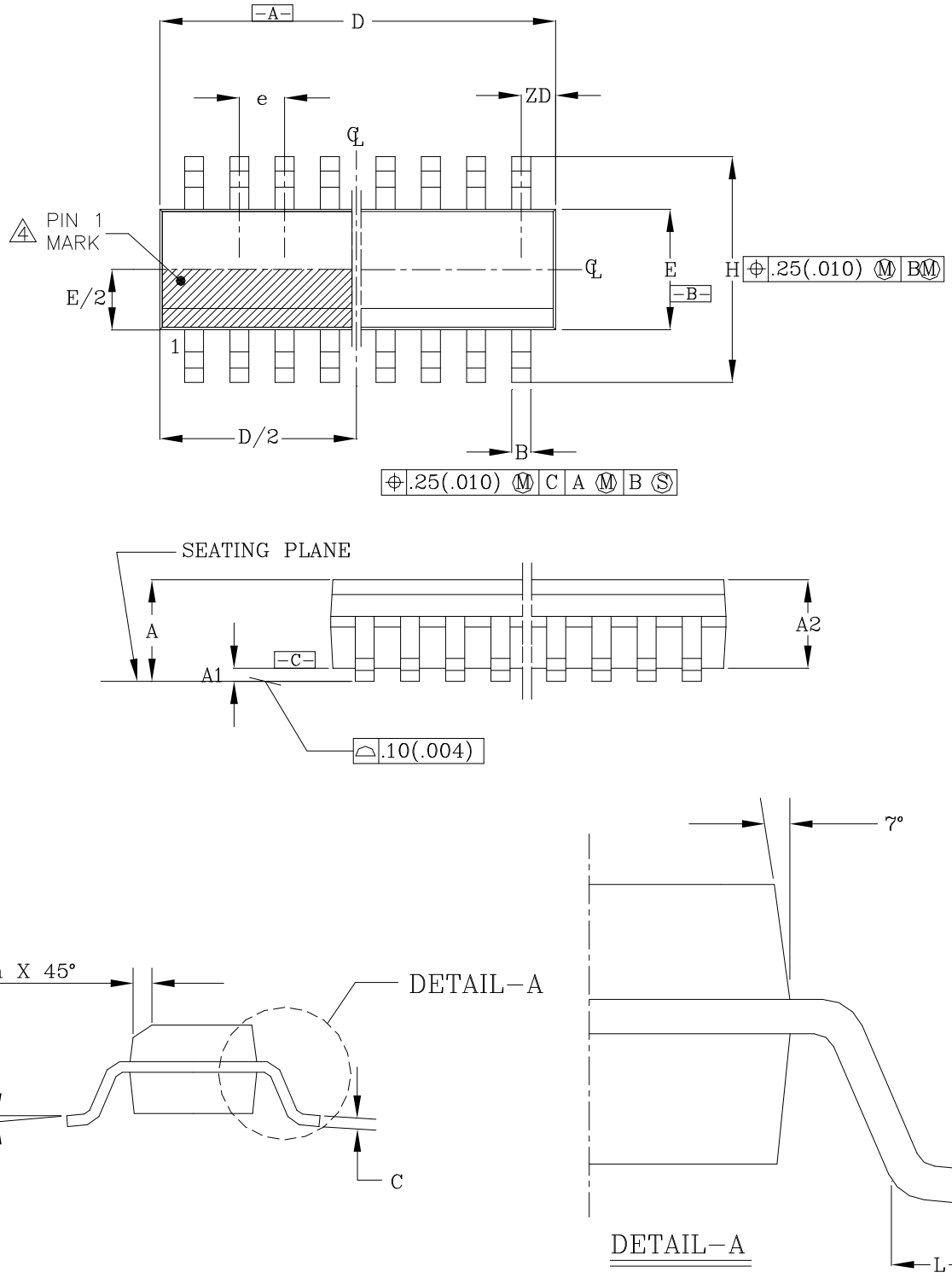
9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

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SOIC16 PACKAGE OUTLINE DIMENSIONS



SYMBOL	SOIC−16LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51 REF	
A2	1.37	1.57

SYMBOL	SOIC−16LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.

2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
   (2.2) ALL SIDES : MATTE (CHARMILLES #18~30).
   (2.3) BOTTOM : SMOOTH OR MATTE (CHARMILLES #18~30).

3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

④ DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

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