



# MX23C8100

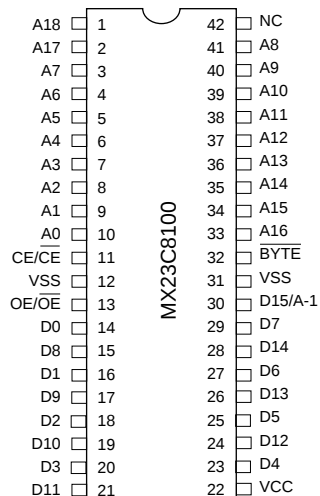
## 8M-BIT MASK ROM (8/16 BIT OUTPUT)

### FEATURES

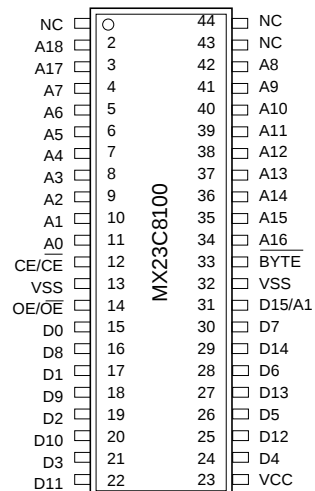
- Bit organization
  - 1M x 8 (byte mode)
  - 512K x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
- Current
  - Operating: 60mA
  - Standby: 50uA
- Supply voltage
  - 5V±10%
- Package
  - 44 pin SOP (500mil)
  - 42 pin PDIP (600mil)
  - 48 pin TSOP (20mm x 12mm)

### PIN CONFIGURATION

#### 42 PDIP



#### 44 SOP



### ORDER INFORMATION

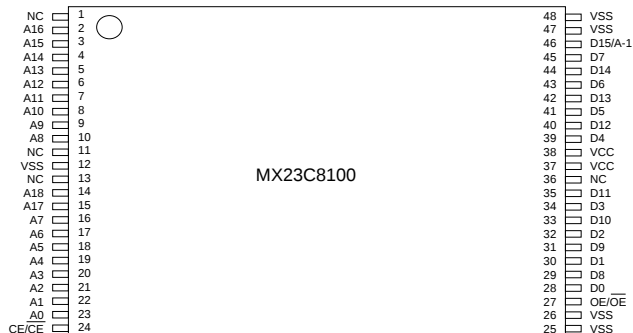
| Part No.       | Access Time | Package     |
|----------------|-------------|-------------|
| MX23C8100PC-10 | 100ns       | 42 pin PDIP |
| MX23C8100PC-12 | 120ns       | 42 pin PDIP |
| MX23C8100PC-15 | 150ns       | 42 pin PDIP |
| MX23C8100MC-10 | 100ns       | 44 pin SOP  |
| MX23C8100MC-12 | 120ns       | 44 pin SOP  |
| MX23C8100MC-15 | 150ns       | 44 pin SOP  |
| MX23C8100TC-10 | 100ns       | 48 pin TSOP |
| MX23C8100TC-12 | 120ns       | 48 pin TSOP |
| MX23C8100TC-15 | 150ns       | 48 pin TSOP |

Note: 40-TSOP and 48-RTSOP support word mode only, not for byte mode.

### PIN DESCRIPTION

| Symbol  | Pin Function                             |
|---------|------------------------------------------|
| A0~A18  | Address Inputs                           |
| D0~D14  | Data Outputs                             |
| D15/A-1 | D15 (Word Mode)/ LSB Address (Byte Mode) |
| CE/CE   | Chip Enable Input                        |
| OE/OE   | Output Enable Input                      |
| Byte    | Word/ Byte Mode Selection                |
| VCC     | Power Supply Pin                         |
| VSS     | Ground Pin                               |
| NC      | No Connection                            |

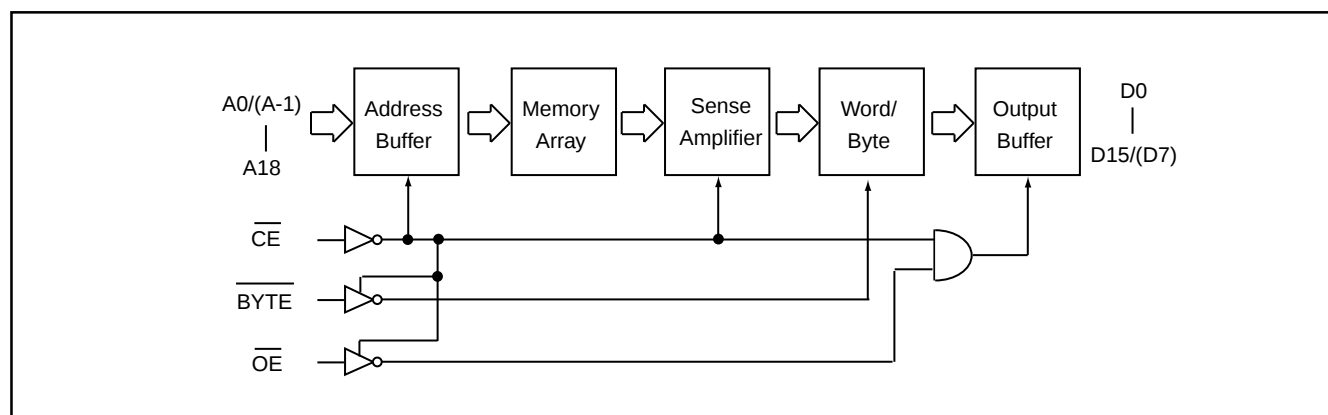
#### 48 TSOP (for word mode only)



## MODE SELECTION

| $\overline{\text{CE}}/\overline{\text{CE}}$ | $\overline{\text{OE}}/\overline{\text{OE}}$ | Byte | D15/A-1 | D0~D7  | D8~D15 | Mode | Power    |
|---------------------------------------------|---------------------------------------------|------|---------|--------|--------|------|----------|
| L/H                                         | X                                           | X    | X       | High Z | High Z | -    | Stand-by |
| H/L                                         | L/H                                         | X    | X       | High Z | High Z | -    | Active   |
| H/L                                         | H/L                                         | H    | Output  | D0~D7  | D8~D15 | Word | Active   |
| H/L                                         | H/L                                         | L    | Input   | D0~D7  | High Z | Byte | Active   |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Item                               | Symbol           | Ratings        |
|------------------------------------|------------------|----------------|
| Voltage on any Pin Relative to VSS | VCC              | -0.5V to 7.0V  |
| Ambient Operating Temperature      | T <sub>opr</sub> | 0°C to 70°C    |
| Storage Temperature                | T <sub>stg</sub> | -65°C to 125°C |

Note: minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = 0 °C ~ 70 °C, VCC = 5V±10%)

| Item                   | Symbol | MIN.  | MAX.     | Conditions                   |
|------------------------|--------|-------|----------|------------------------------|
| Output High Voltage    | VOH    | 2.4V  | -        | IOH = -1.0mA                 |
| Output Low Voltage     | VOL    | -     | 0.4V     | IOL = 2.1mA                  |
| Input High Voltage     | VIH    | 2.2V  | VCC+0.3V |                              |
| Input Low Voltage      | VIL    | -0.3V | 0.8V     |                              |
| Input Leakage Current  | ILI    | -     | 10uA     | 0V, VCC                      |
| Output Leakage Current | ILO    | -     | 10uA     | 0V, VCC                      |
| Operating Current      | ICC1   | -     | 60mA     | tRC=100ns, all output open   |
| Standby Current (TTL)  | ISTB1  | -     | 1mA      | $\overline{CE}$ =VIH         |
| Standby Current (CMOS) | ISTB2  | -     | 50uA     | $\overline{CE}$ > VCC - 0.2V |
| Input Capacitance      | CIN    | -     | 10pF     | Ta = 25 °C, f = 1MHZ         |
| Output Capacitance     | COUT   | -     | 10pF     | Ta = 25 °C, f = 1MHZ         |

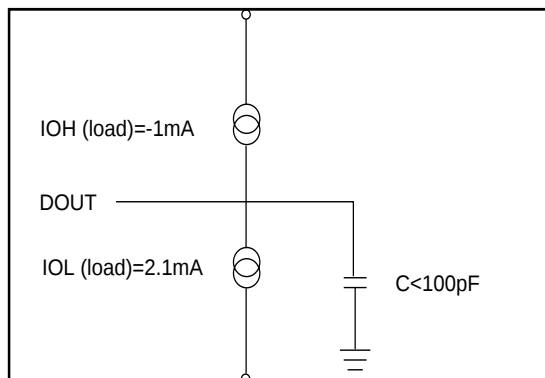
**AC CHARACTERISTICS** (Ta = 0 °C ~ 70 °C, VCC = 5V±10%)

| Item                      | Symbol | 23C8100-10 |       | 23C8100-12 |       | 23C8100-15 |       |
|---------------------------|--------|------------|-------|------------|-------|------------|-------|
|                           |        | MIN.       | MAX.  | MIN.       | MAX.  | MIN.       | MAX.  |
| Read Cycle Time           | tRC    | 100ns      | -     | 120ns      | -     | 150ns      | -     |
| Address Access Time       | tAA    | -          | 100ns | -          | 120ns | -          | 150ns |
| Chip Enable Access Time   | tACE   | -          | 100ns | -          | 120ns | -          | 150ns |
| Output Enable Time        | tOE    | -          | 50ns  | -          | 60ns  | -          | 70ns  |
| Output Hold After Address | tOH    | 0ns        | -     | 0ns        | -     | 0ns        | -     |
| Output High Z Delay       | tHZ    | -          | 20ns  | -          | 20ns  | -          | 20ns  |

Note: Output high-impedance delay (tHZ) is measured from  $\overline{OE}$  or  $\overline{CE}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

|                           |               |
|---------------------------|---------------|
| Input Pulse Levels        | 0.4V~2.4V     |
| Input Rise and Fall Times | 10ns          |
| Input Timing Level        | 1.5V          |
| Output Timing Level       | 0.8V and 2.0V |
| Output Load               | See Figure    |



Note:

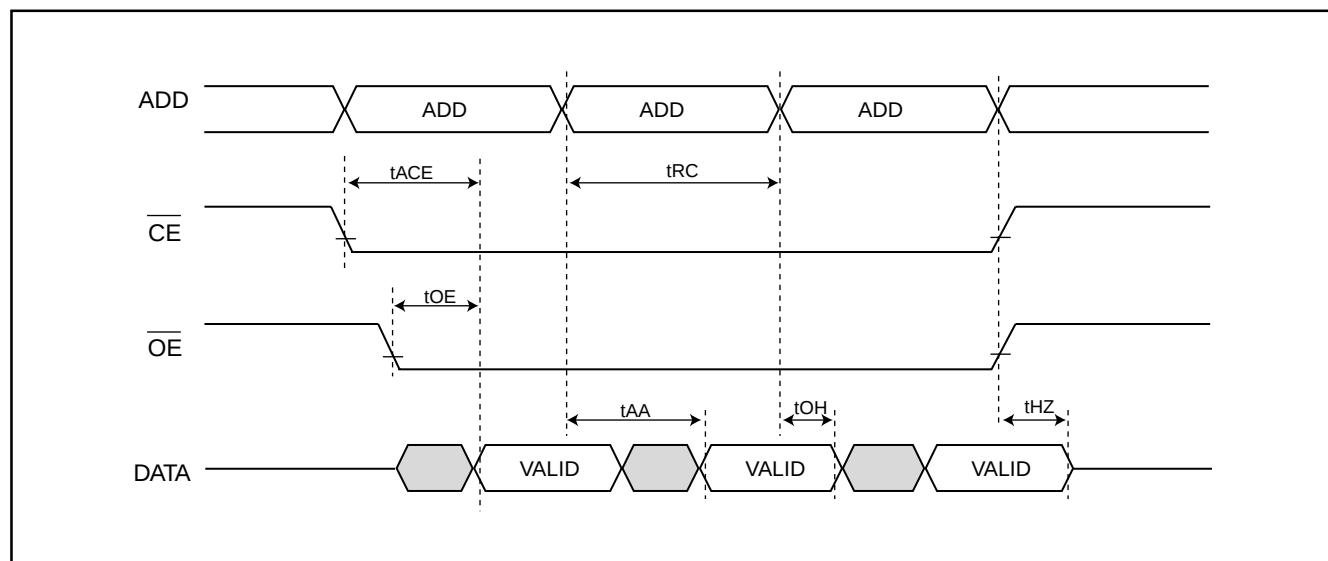
No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

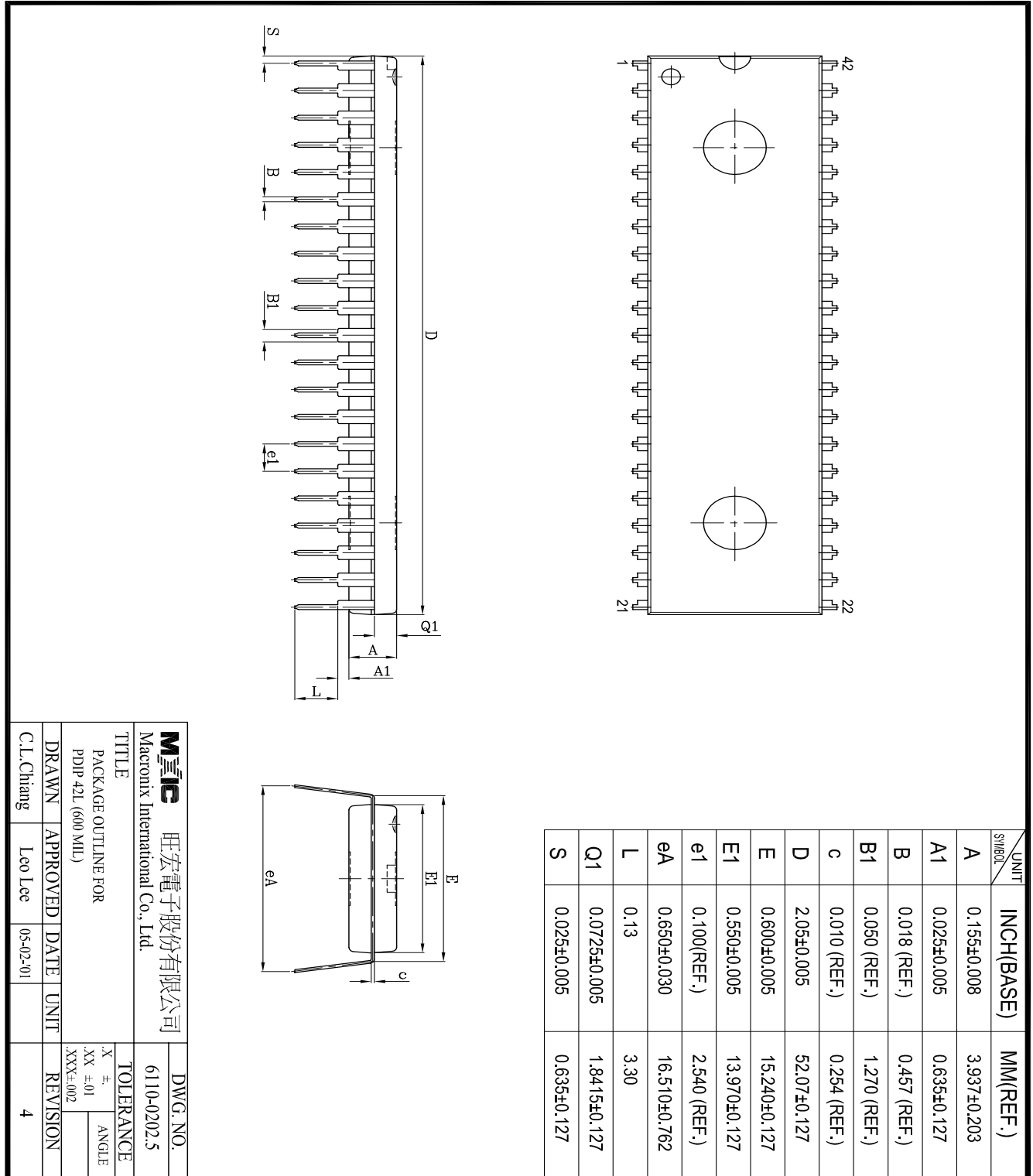
## TIMING DIAGRAM

### RANDOM READ

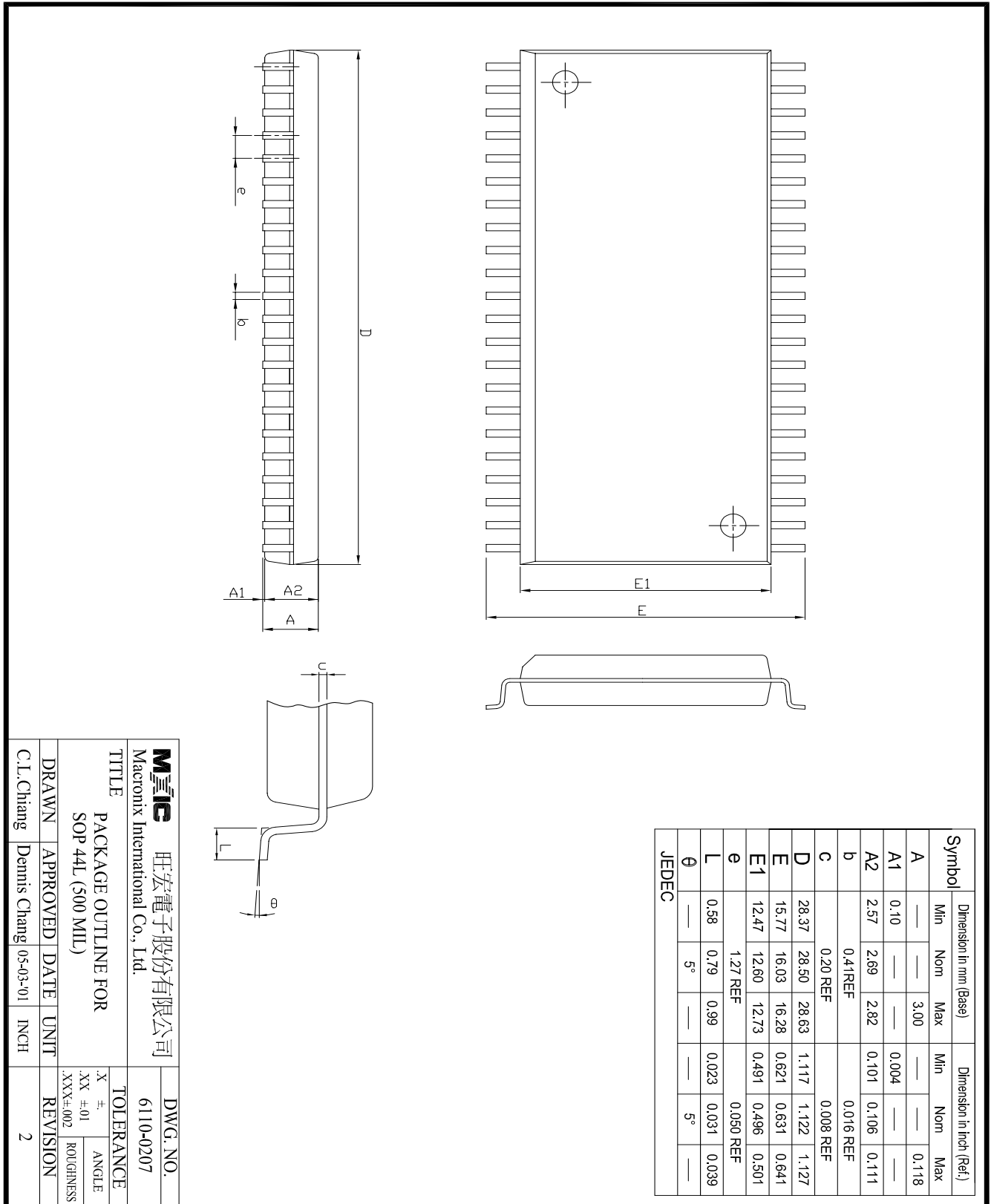


## PACKAGE INFORMATION

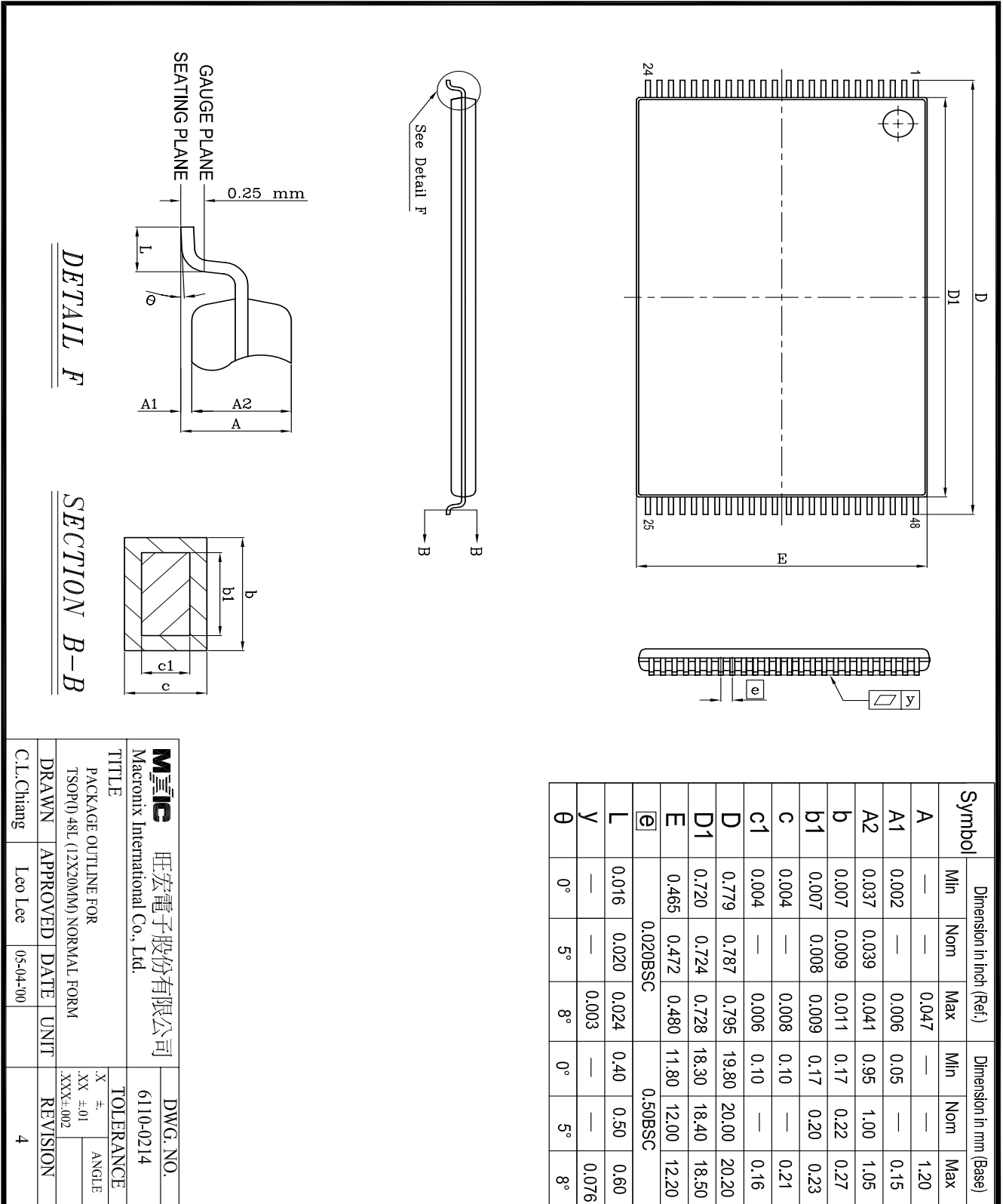
### 42-PIN PLASTIC DIP(600 mil)



## 44-PIN PLASTIC SOP



## 48-PIN PLASTIC TSOP



**REVISION HISTORY**

| Revision | Description                                                                                                                                                                                                                                                                                                                                     | Page | Date        |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------|
| 4.2      | DC Characteristics: The standby current (CMOS) ISTB2 is changed as 50us instead of 100uA.<br>AC Characteristics: Deleted 200ns grade item.<br>The output enable time (tOE) is changed as 60ns instead of 70ns in 120ns grade item, and 70ns instead of 80ns in 150ns grade item.<br>The output high Z delay is changed as 20ns instead of 70ns. |      | SEP/01/1997 |
| 4.3      | AC CHARACTERISTICS tOH 10ns-->0ns                                                                                                                                                                                                                                                                                                               | P3   | JAN/28/1999 |
| 4.4      | Undershoot -1.3V 20ns-->-2.0V 20ns                                                                                                                                                                                                                                                                                                              | P2   | AUG/04/1999 |
| 4.5      | Added Package Information                                                                                                                                                                                                                                                                                                                       | P5~7 | JUL/16/2001 |



**MX23C8100**

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