National Semiconductor

**PRELIMINARY**
October 1995

# 74VHC943
# 300 Baud Modem (5V Supply)

## General Description

The 74VHC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The 74VHC943 utilizes advanced silicon-gate CMOS technology. Switched capacitor techniques are used to perform analog signal processing.

**MODULATOR SECTION**

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

**LINE DRIVER AND HYBRID SECTION**

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at a maximum of −9 dBm.

**DEMODULATOR SECTION**

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine-pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

## Features

- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode
- Direct Pin and function replacement for the 74HC943

## Applications

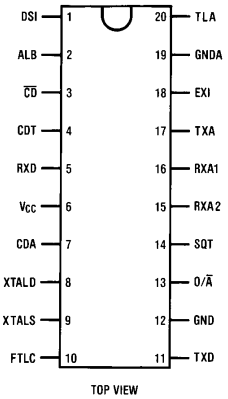
- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

| Commercial | Package Number | Package Description |
|---|---|---|
| 74VHC943WM | M20B | 20-Lead Molded JEDEC SOIC (0.300″ Wide) |
| 74VHC943N | N20A | 20-Lead Molded DIP |

**Note:** Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram

**Pin Assignments for SOIC and PDIP**



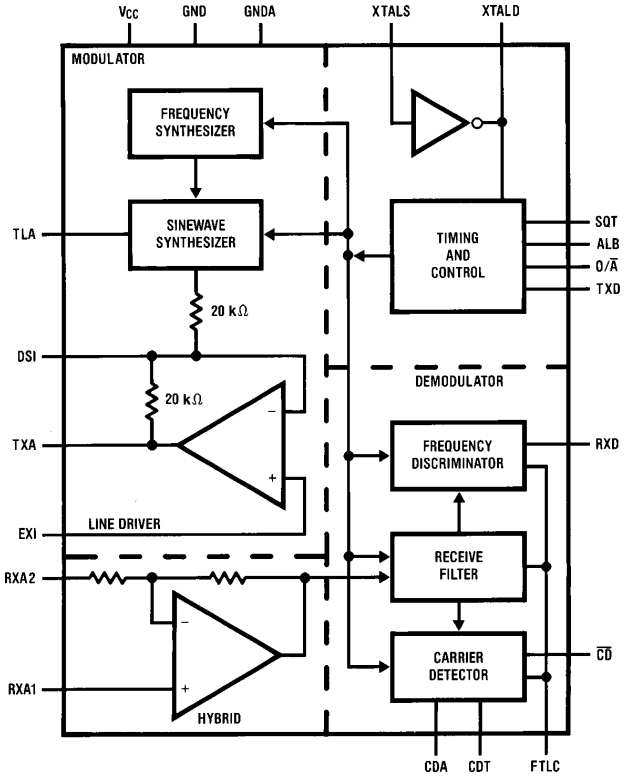

TOP VIEW

TL/F/11679–1

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## Block Diagram




TL/F/11679–2

## Description of Pin Functions

| Pin No. | Name | Function |
|---|---|---|
| 1 | DSI | Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals. |
| 2 | ALB | Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down. |
| 3 | $\overline{CD}$ | Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit. |
| 4 | CDT | Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low. |
| 5 | RXD | Received Data: This is the data output pin. |
| 6 | $V_{CC}$ | Positive Supply Pin: A +5V supply is recommended. |
| 7 | CDA | Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB. |
| 8 | XTALD | Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven. |
| 9 | XTALS | Crystal Sense: Refer to pin 8 for details. |
| 10 | FTLC | Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test.<br>For normal modem operation FTLC is AC grounded via a 0.1 $\mu$F bypass capacitor. |
| 11 | TXD | Transmitted Data: This is the data input. |
| 12 | GND | Ground: This defines the chip 0V. |
| 13 | O/$\overline{A}$ | Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation. |
| 14 | SQT | Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down. |
| 15 | RXA2 | Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600$\Omega$ hybrid. |
| 16 | RXA1 | Receive Analog #1: See RXA2 for details. |
| 17 | TXA | Transmit Analog: This is the output of the line driver. |
| 18 | EXI | External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded to GNDA. |
| 19 | GNDA | Analog Ground: Analog signals within the chip are referred to this pin. |
| 20 | TLA | Transmit Level Adjust: A resistor from this pin to $V_{CC}$ sets the transmit level. |

## Functional Description

### INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The 74VHC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The 74VHC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the 74VHC943 is capable of transmitting and receiving data simultaneously.

The tone allocation used by the 74VHC943 and other Bell 103 compatible modems is shown in Table I. The terms ''originate'' and ''answer'' which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

**TABLE I. Bell 103 Tone Allocation**

| Data | Originate Modem | | Answer Modem | |
|---|---|---|---|---|
| | Transmit | Receive | Transmit | Receive |
| Space | 1070 Hz | 2025 Hz | 2025 Hz | 1070 Hz |
| Mark | 1270 Hz | 2225 Hz | 2225 Hz | 1270 Hz |

### THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

### THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

### THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

### THE DEMODULATOR SECTION

#### The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

#### The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 $\mu$F capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

#### Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

### MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to ''look up'' the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

## Absolute Maximum Ratings (Notes 1 & 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temp. ($T_L$) (Soldering 10 seconds) | 260°C |

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 4.5 | 5.5 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temp. Range ($T_A$) | | | |
| 74VHC | −40 | +85 | °C |
| Input Rise or Fall Times ($t_r$, $t_f$) | | 500 | ns |
| Crystal frequency | | 3.579 | MHz |

## DC Electrical Characteristics $V_{CC}$ = 5V ±10% unless otherwise specified

| Symbol | Parameter | Conditions | 74VHC $T_A$ = 25°C | | 74VHC $T_A$ = −40°C to +85°C | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum High Level Input Voltage | | | 3.15 | 3.15 | V |
| $V_{IL}$ | Maximum Low Level Input Voltage | | | 1.1 | 1.1 | V |
| $V_{OH}$ | Minimum High Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ = 20 μA<br>$\|I_{OUT}\|$ = 4.0 mA, $V_{CC}$ = 4.5V | $V_{CC}$ −0.05 | $V_{CC}$ −0.1<br>3.84 | $V_{CC}$ −0.1<br>3.7 | V |
| $V_{OL}$ | Maximum Low Level Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ = 20 μA<br>$\|I_{OUT}\|$ = 4.0 mA, $V_{CC}$ = 4.5V | | 0.1<br>0.33 | 0.1<br>0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | | ±0.1 | ±1.0 | μA |
| $I_{OZ}$ | Output TRI-STATE® Leakage Current, RXD and $\overline{CD}$ Outputs | ALB = SQT = $V_{CC}$ | | | ±5 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IH}$ = $V_{CC}$, $V_{IL}$ = GND<br>ALB or SQT = GND<br>Transmit Level = −9 dBm | 8.0 | 10.0 | 10.0 | mA |
| $I_{GNDA}$ | Analog Ground Current | | 1.0 | 2.0 | 2.0 | mA |
| $I_{CC}$ | Power Down Supply Current | ALB = SQT = $V_{CC}$<br>$V_{IH}$ = $V_{CC}$, $V_{IL}$ = GND | | | 300 | μA |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

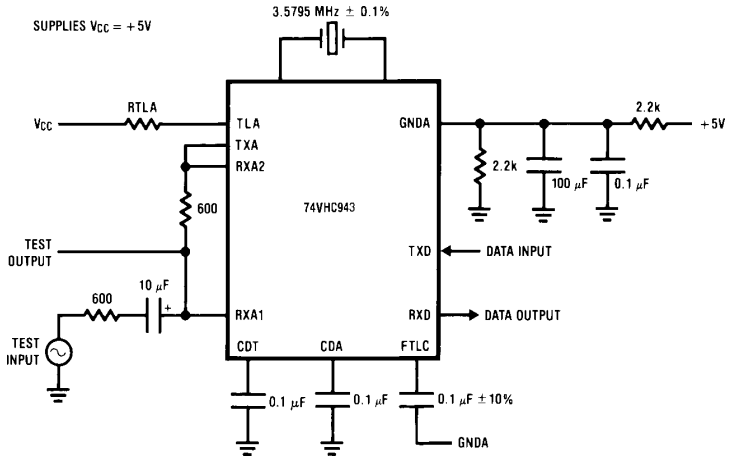
## AC Electrical Characteristics

Unless otherwise specified, all specifications apply over the range −40°C to +85°C using a $V_{CC}$ of +5V ±10%, and a 3.579 MHz ±0.1% crystal*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **TRANSMITTER** | | | | | | | |
| $F_{CE}$ | Carrier Frequency Error | | | | | 4 | Hz |
| | Power Output | $V_{CC}$ = 5.0V<br>$R_L$ = 1.2 kΩ | $R_{TLA}$ = 5490Ω | −12 | −10.5 | −9 | dBm |
| | 2nd Harmonic Energy | | $R_{TLA}$ = 5490Ω | | −62 | −56 | dBm |
| **RECEIVE FILTER AND HYBRID** | | | | | | | |
| | Hybrid Input Impedance (Pins 15 and 16) | | | 50 | | | kΩ |
| | FTLC Output Impedance | | | 5 | 10 | 50 | kΩ |
| | Adjacent Channel Rejection | RXA2 = GNDA, TXD = GND or $V_{CC}$<br>Input to RXA1 | | 60 | | | dB |
| **DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)** | | | | | | | |
| | Carrier Amplitude | | | −38 | | −12 | dBm |
| | Bit Jitter | SNR = 30 dB<br>Input = −38 dBm<br>Baud Rate = 300 Baud | | | 100 | 200 | μs |
| | Bit Bias | Alternating 1–0 Pattern | | | 5 | 10 | % |
| | Carrier Detect Trip Points | CDA = 1.2V | Off to On | −38 | −36 | −34 | dBm |
| | | $V_{CC}$ = 5.0V | On to Off | −41 | −39 | −37 | dBm |
| | Carrier Detect Hystereisis | $V_{CC}$ = 5.0V | | 2 | 3 | 4 | dB |

*The demodulator specifications apply to the 74VHC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the 74VHC943 modulator.

## AC Specification Circuit




TL/F/11679–3

## Applications Information

### TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

The transmit level is programmable by placing a resistor from TLA to $V_{CC}$. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the 74VHC943 will interface to most telephones. This arrangement is called the ''permissive arrangement.'' The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

**TABLE II. Universal Service Order Code Resistor Values**

| Line Loss (dB) | Transmit Level (dBm) | Programming Resistor ($R_{TLA}$) (Ω) |
|---|---|---|
| 0 | −12 | Open |
| 1 | −11 | 19,800 |
| 2 | −10 | 9,200 |
| 3 | −9 | 5,490 |

### CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used:

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

### CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$$T_{\overline{CDL}} \cong 6.4 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going low}$$

$$T_{\overline{CDH}} \cong 0.54 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going high}$$

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and $C_{CDT}$ is in μF.

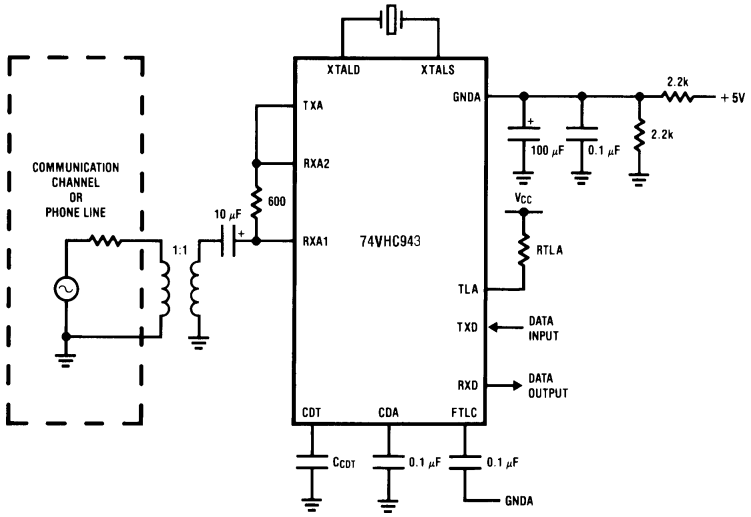
### DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the 74VHC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

## Applications Information (Continued)

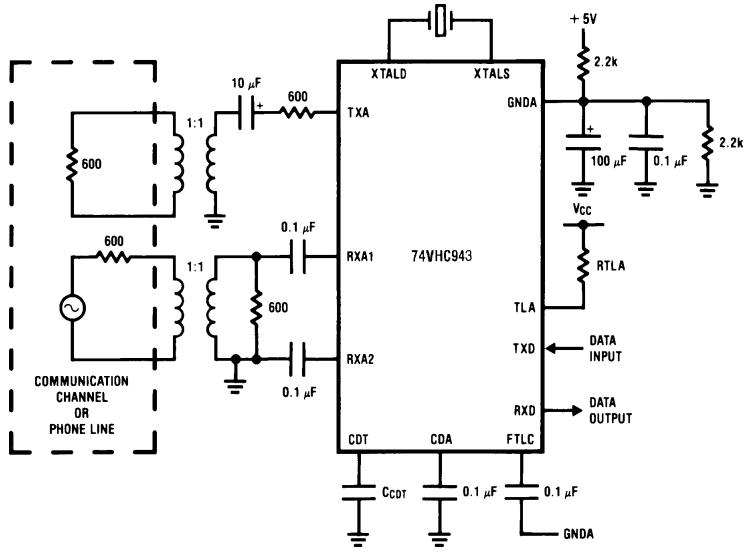
**Interface Circuits for 74VHC943 300 Baud Modem**

**2 Wire Connection**




TL/F/11679–4

**4 Wire Connection**

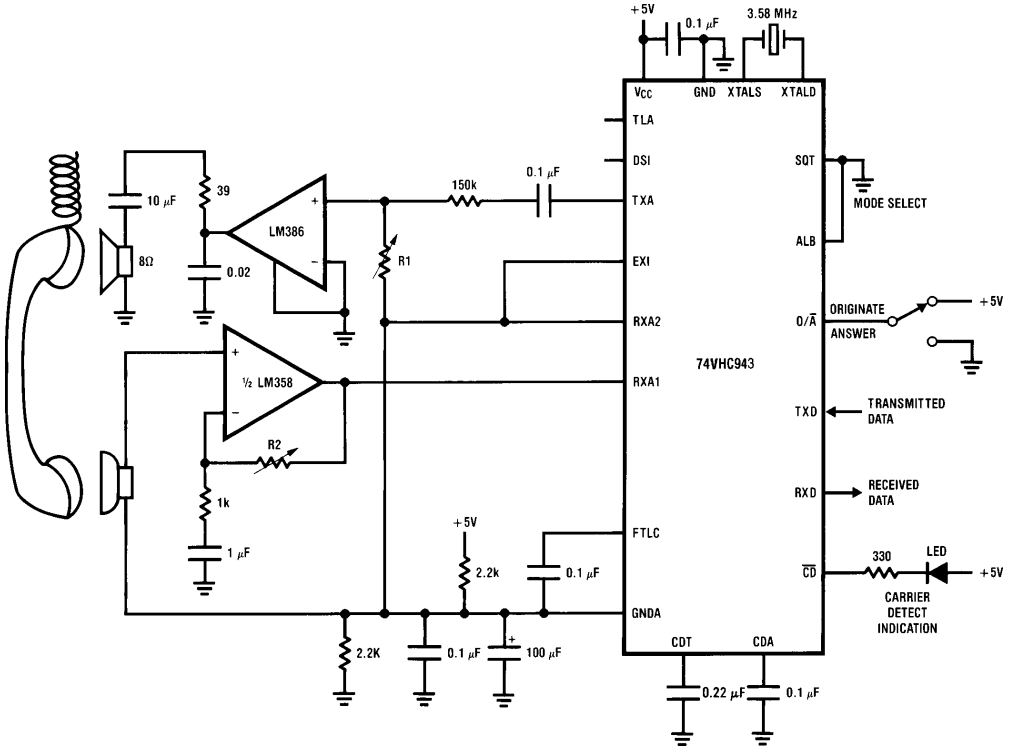



TL/F/11679–5

$C_{CDT}$ and $R_{TLA}$ should be chosen to suit the application. See the Applications Information for more details.

## Applications Information (Continued)

**Complete Acoustically Coupled 300 Baud Modem**

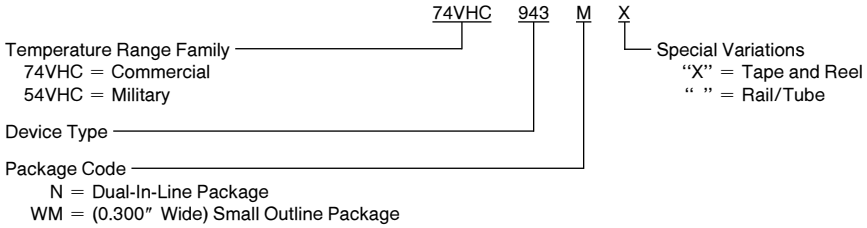



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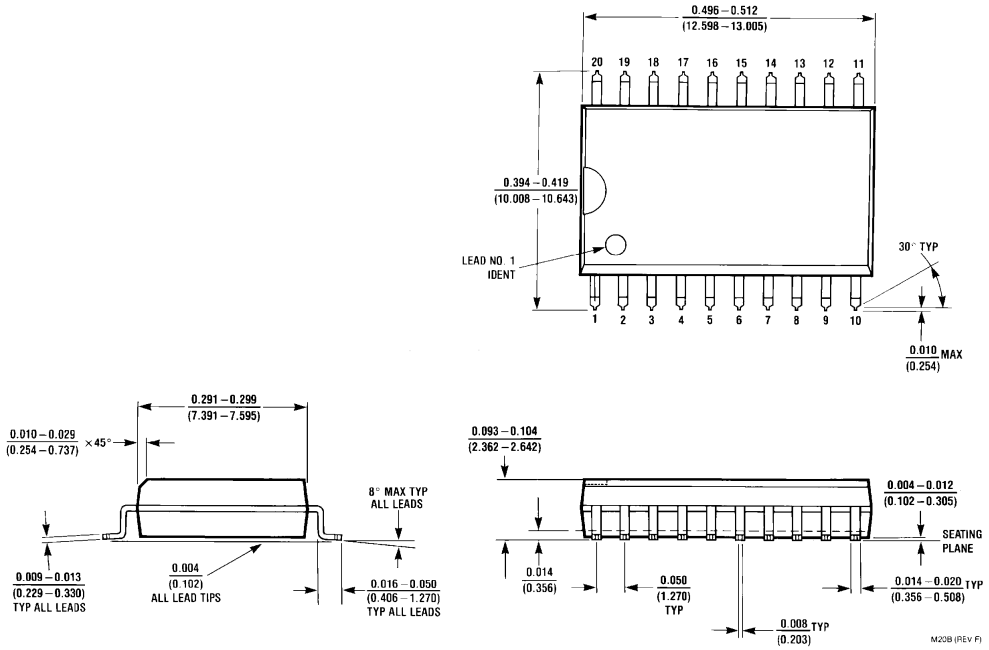
**Note:** The efficiency of the acoustic coupling will set the values of R1 and R2.

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

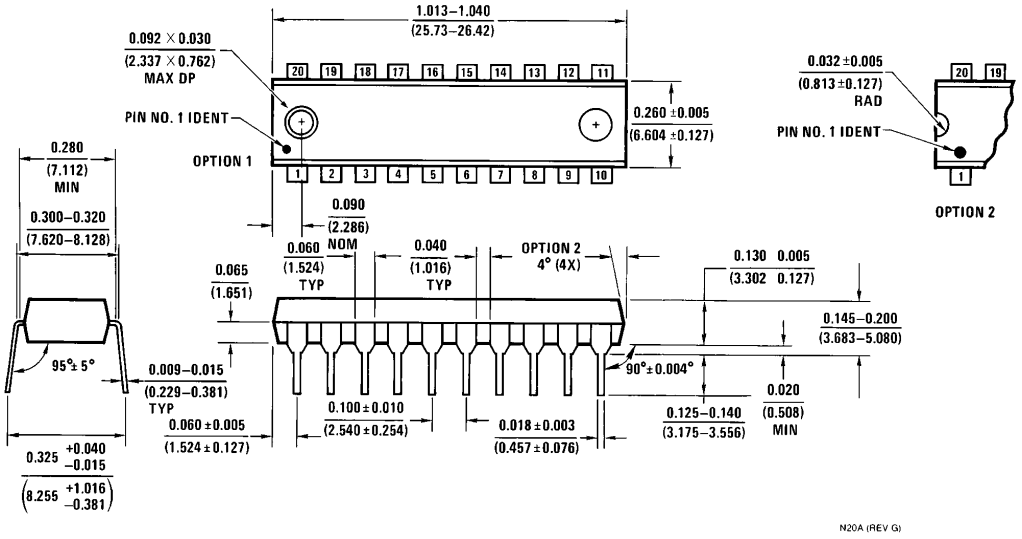


## Physical Dimensions inches (millimeters)




**20-Lead (0.300″ Wide) Molded Small Outline Package JEDEC**
**Order Number 74VHC943WM**
**NS Package Number M20B**

## Physical Dimensions inches (millimeters) (Continued)




**20-Lead (0.300″ Wide) Molded Dual-In-Line Package**
**Order Number 74VHC943N**
**NS Package Number N20A**

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