

# DATA SHEET

## **SA56606-XX** CMOS system reset

Product data  
Supersedes data of 2001 Apr 24  
File under Integrated Circuits, Standard Analog

2001 Jun 19

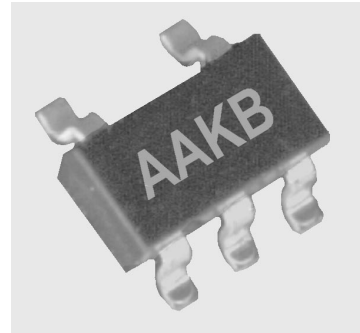
# CMOS system reset

# SA56606-XX

## GENERAL DESCRIPTION

The SA56606-XX is a CMOS device designed to generate a reset signal for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions or whenever power supply voltages sag to intolerable levels. An Open Drain output topology is incorporated for adaptability to a wide variety of logic and microprocessor applications. Several reset threshold versions of the device are available.

The SA56606-XX is available in the SOT23-5 surface mount package.



## FEATURES

- 12 V<sub>DC</sub> maximum operating voltage
- CMOS N-channel Open Drain output
- Offered in reset thresholds of 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7 V<sub>DC</sub>
- Available in SOT23-5 surface mount package

## APPLICATIONS

- Microcomputer systems
- Logic systems
- Battery monitoring systems
- Back-up power supply circuits
- Voltage detection circuits

## SIMPLIFIED SYSTEM DIAGRAM

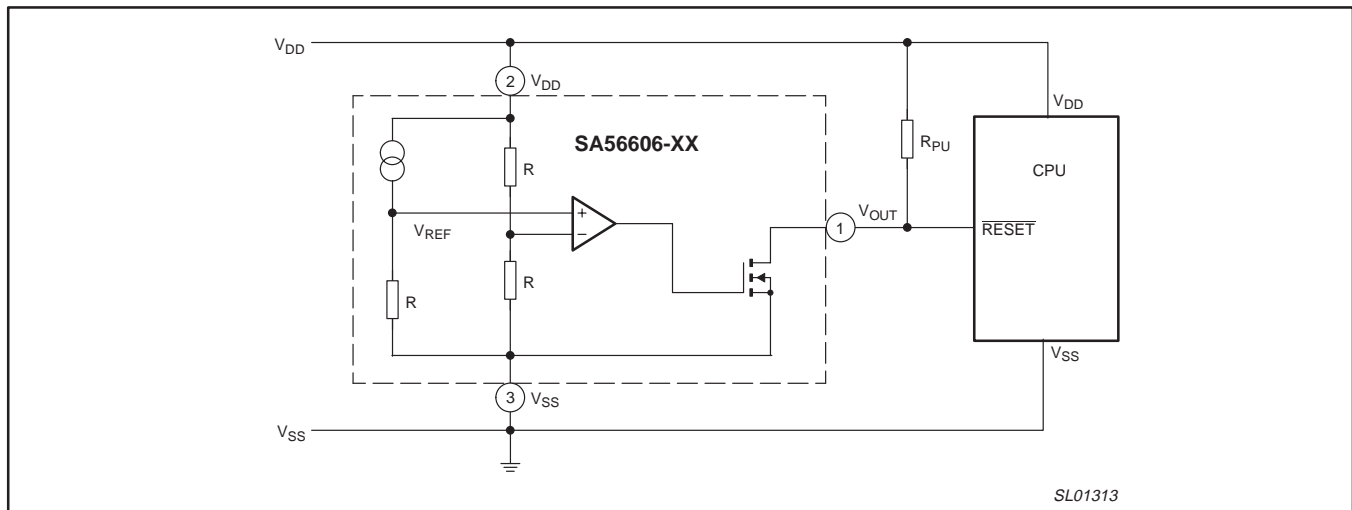


Figure 1. Simplified system diagram.

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## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
SA56606-XXGW	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	-40 to +85 °C

**NOTE:**

The device has twelve detection voltage options, indicated by the **XX** on the order code.

XX	DETECT VOLTAGE (Typical)
20	2.0 V
27	2.7 V
28	2.8 V
29	2.9 V
30	3.0 V
31	3.1 V
42	4.2 V
43	4.3 V
44	4.4 V
45	4.5 V
46	4.6 V
47	4.7 V

## Part number marking

Each package is marked with a four letter code. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code. For example, AAKB is device AAK (the SA56606-30 reset), produced in time period 'B'.

Part number	Marking
SA56606-20	AA F x
SA56606-27	AA G x
SA56606-28	AA H x
SA56606-29	AA J x
SA56606-30	AA K x
SA56606-31	AA L x
SA56606-42	AA M x
SA56606-43	AA N x
SA56606-44	AA P x
SA56606-45	AA R x
SA56606-46	AA S x
SA56606-47	AA T x

## PIN CONFIGURATION

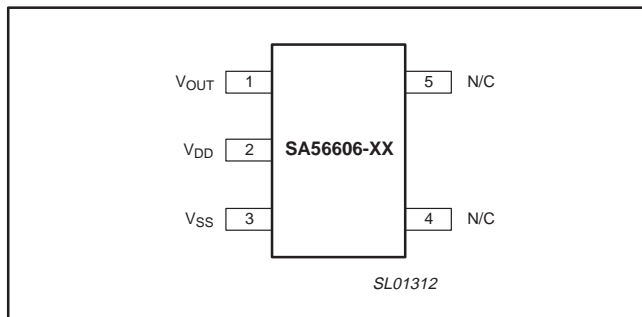


Figure 2. Pin configuration.

## PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V <sub>OUT</sub>	Reset High Output
2	V <sub>DD</sub>	Positive Supply
3	V <sub>SS</sub>	Ground. Negative Supply
4	N/C	No connection
5	N/C	No connection

## MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>DD</sub>	Power supply voltage	-0.3	12	V
V <sub>OUT</sub>	Output voltage	-	V <sub>SS</sub> - 0.3	V
I <sub>OUT</sub>	Output current	-	50	mA
T <sub>oper</sub>	Operating temperature	-40	85	°C
T <sub>stg</sub>	Storage temperature	-40	125	°C
P	Power dissipation	-	150	mW

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**DC ELECTRICAL CHARACTERISTICS**Characteristics measured with  $T_{amb} = 25\text{ °C}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT
$V_S$	Reset detection threshold		1 Fig. 17	$V_S - 2\%$	$V_S$	$V_S + 2\%$	V
$\Delta V_S$	Hysteresis	$V_{DD} = 0\text{ V} \rightarrow V_S + 1.0\text{ V} \rightarrow 0\text{ V}$		$V_S \times 0.03$	$V_S \times 0.05$	$V_S \times 0.08$	V
$V_S/\Delta T$	Threshold voltage temperature coefficient	$-40\text{ °C} \leq T_{amb} \leq +85\text{ °C}$		–	$\pm 0.01$	–	%/°C
$I_{CC}$	Supply current	$V_{DD} = V_S + 1.0\text{ V}$		–	0.25	1.0	$\mu\text{A}$
$I_{OH}$	$I_{DS}$ leakage current when OFF	$V_{DD} = V_{DS} = 10\text{ V}$	2 Fig. 18	–	–	0.1	$\mu\text{A}$
$I_{DS1}$	N-channel $I_{DS}$ output sink current 1	$V_{DS} = 0.5\text{ V}; V_{DD} = 1.2\text{ V}$		–0.23	–1.4	–	mA
$I_{DS2}$	N-channel $I_{DS}$ output sink current 2 (for $V_S > 2.6\text{ V}$ )	$V_{DS} = 0.5\text{ V}; V_{DD} = 2.4\text{ V}$		–1.6	–8.3	–	mA
$I_{DS3}$	N-channel $I_{DS}$ output sink current 3 (for $V_S > 3.9\text{ V}$ )	$V_{DS} = 0.5\text{ V}; V_{DD} = 3.6\text{ V}$		–3.2	–14.7	–	mA

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## TYPICAL PERFORMANCE CURVES

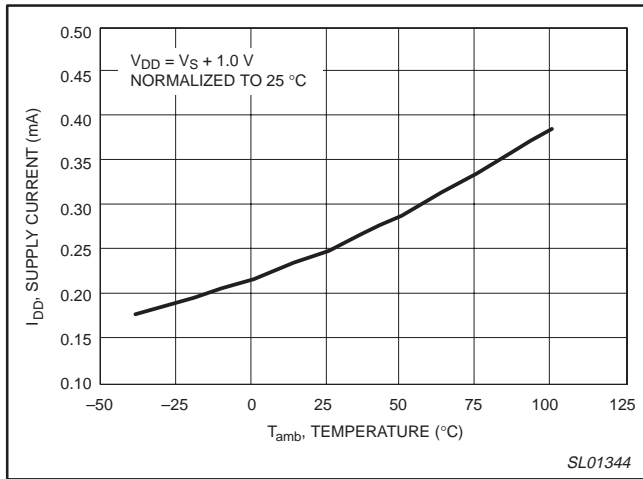


Figure 3. Supply current versus temperature.

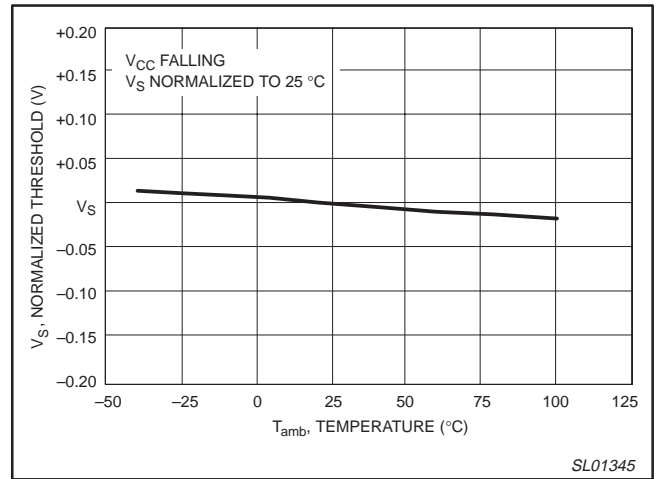


Figure 4. Detection threshold versus temperature.

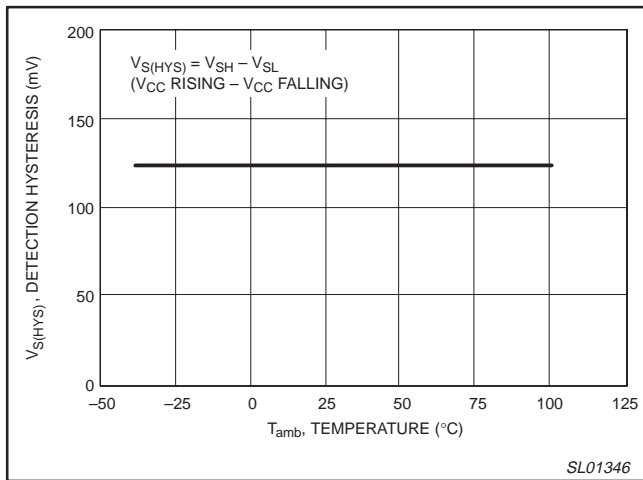


Figure 5. Detection hysteresis versus temperature.

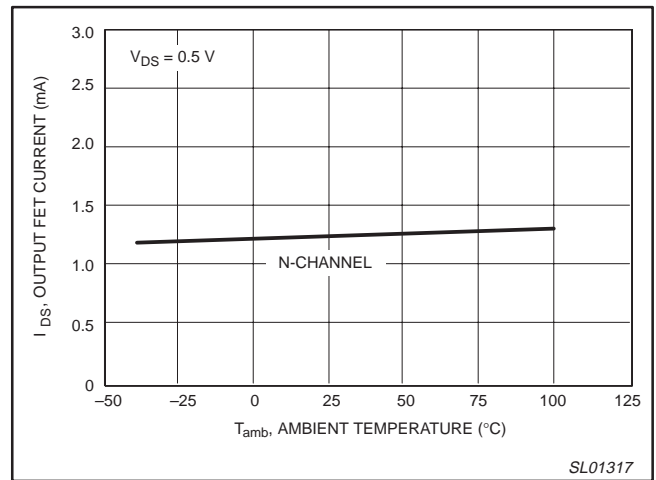


Figure 6. Output FET current versus temperature.

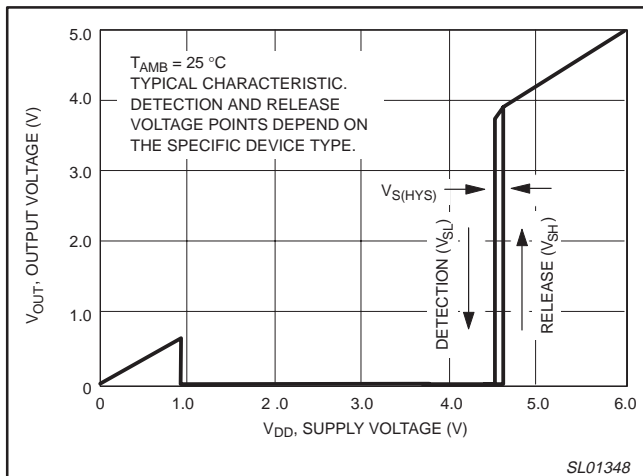


Figure 7. Output voltage versus supply voltage

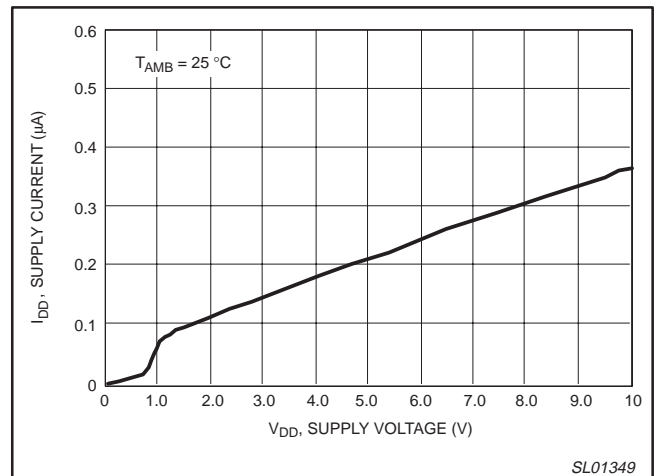


Figure 8. Supply current versus supply voltage

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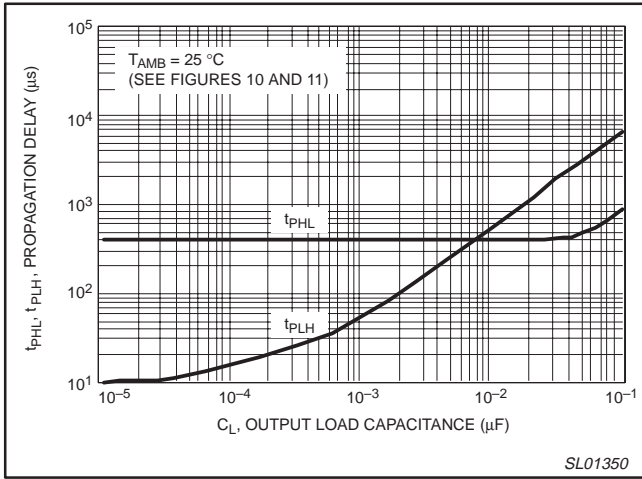


Figure 9. Propagation delay versus output load C

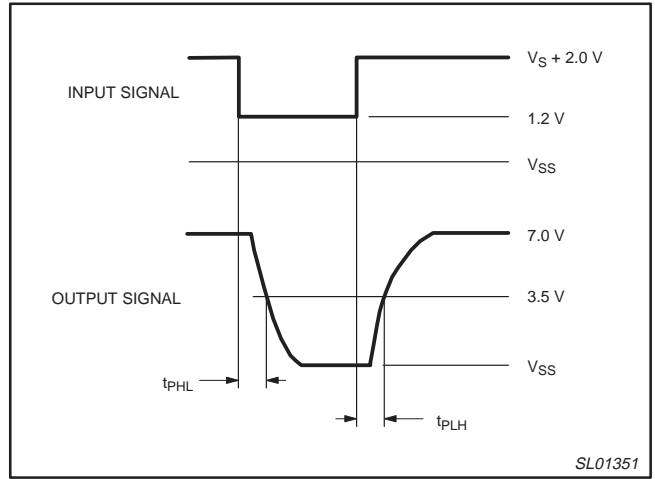


Figure 10. Propagation delay measurements

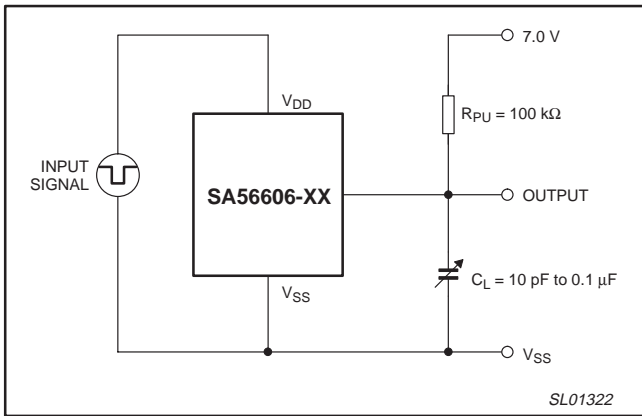


Figure 11. Propagation delay measurement circuit

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## TECHNICAL DESCRIPTION

The SA56606-XX is a CMOS device designed to provide power source monitoring and a system reset function in the event the supply voltage sags below an acceptable level for the system to reliably operate. The device is designed to generate a compatible reset signal for a wide variety of microprocessor and logic systems. The SA56606 can operate at voltages up to 12 volts. The series includes several versions providing precision threshold voltage reset values of 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.6 and 4.7 V. The reset threshold incorporates a typical hysteresis of ( $V_S \times 0.05$ ) volts to prevent erratic resets from being generated.

The output of the SA56606 utilizes a low side open drain topology, which requires an external pull-up resistor ( $R_{PU}$ ) to the  $V_{DD}$  power source. Although this may be regarded as a disadvantage, it is an advantage in many sensitive applications because the open drain output cannot source reset current to a microprocessor when both are operated from a common supply. For this reason the SA56606 offers a safe inter-connect to a wide variety of microprocessors.

The SA56606 operates at very low supply currents, typically 0.25  $\mu$ A, while offering a high precision of threshold detection ( $\pm 2\%$ ). Figure 12 is a functional block diagram of the SA56606. The internal reference source voltage ( $V_{REF}$ ) is typically 0.8 V over the operating temperature range. The reference voltage is connected to the non-inverting input of the threshold comparator, while the inverting input monitors the supply voltage through a resistor divider network made up of  $R_1$ ,  $R_2$ , and  $R_3$ . The output of the threshold comparator drives the output Open Drain N-Channel FET of the device  $TR_1$ . When the supply voltage sags to the threshold detection voltage, the resistor divider network supplies a voltage to the inverting input of the threshold comparator, which is less than that of  $V_{REF}$ , causing the output of the comparator to go to a HIGH output state. This causes the low side N-Channel FET to be active ON, pulling its drain voltage to a LOW state. The device adheres to a true input/output logic protocol: the output goes LOW when input is LOW (below threshold) and output goes HIGH when input is HIGH (above threshold).

The low side N-Channel FET ( $TR_2$ ) establishes threshold hysteresis by turning ON whenever the threshold comparator's output goes to a HIGH state (when  $V_{DD}$  sags to or below the threshold level).  $TR_2$ 's turning ON causes additional current to flow through resistors  $R_1$  and  $R_2$ , causing the inverting input of the threshold comparator to be pulled even lower. For the comparator to reverse its output polarity and turn OFF  $TR_2$ , the  $V_{DD}$  source voltage must overcome this additional pull-down voltage present on the comparator's inverting input. The differential voltage required to do this establishes the hysteresis voltage of the sensed threshold voltage. Typically it is ( $V_S \times 0.05$ ) volts.

When the  $V_{DD}$  voltage sags, and is at or below the Detection Threshold ( $V_{SL}$ ), the device will assert a Reset LOW output at or very near ground potential. As the  $V_{DD}$  voltage rises from ( $V_{DD} < V_{SL}$ ) to  $V_{SH}$  or higher, the Reset is released and the output follows  $V_{DD}$ . Conversely, decreases in  $V_{DD}$  from ( $V_{DD} > V_{SL}$ ) to  $V_{SL}$  or lower cause the output to be pulled to ground.

Hysteresis Voltage = Release Voltage – Detection Threshold Voltage

$$V_{HYS} = V_{SH} - V_{SL}$$

where:

$$V_{SH} = V_{SL} + V_{HYS} \cong V_{REF}(R_1 + R_2) / R_2$$

$$V_{SL} = V_{REF}(R_1 + R_2 + R_3) / (R_2 + R_3)$$

When  $V_{DD}$  drops to levels below the minimum operating voltage, typically less than 0.95 volts, the output is undefined and output reset LOW assertion is not guaranteed. At this level of  $V_{DD}$  the output will try to rise to  $V_{DD}$ .

The  $V_{REF}$  voltage is typically 0.8 V. The devices are fabricated using a high resistance CMOS process and utilize high resistance  $R_1$ ,  $R_2$ , and  $R_3$  values requiring very small amounts of current. This combination achieves very efficient low power performance over the full operating temperature.

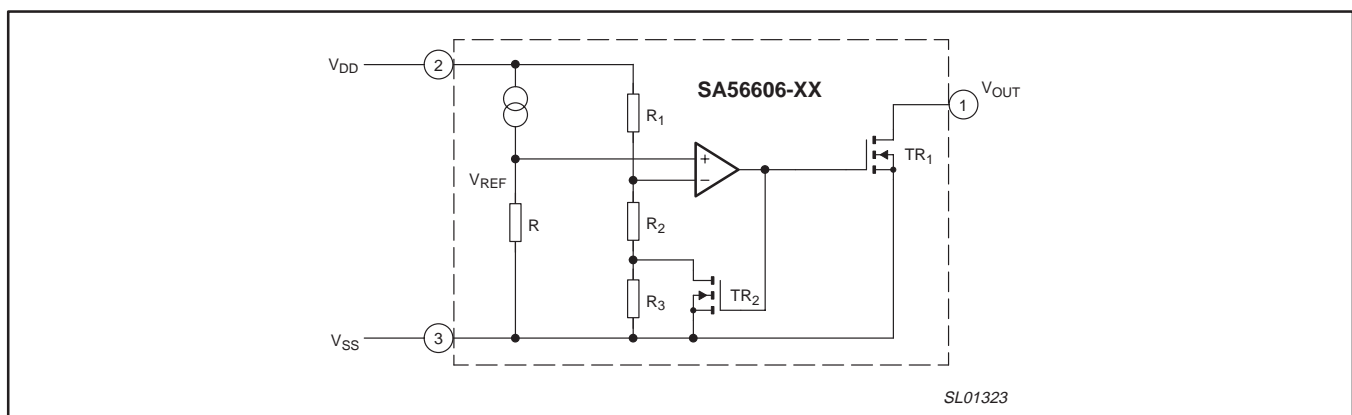


Figure 12. Functional diagram.

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## Timing diagram

The timing diagram shown in Figure 13 depicts the operation of the device. Letters A–J on the TIME axis indicate specific events.

**A:** At 'A',  $V_{DD}$  begins to increase. Also the  $V_{OUT}$  voltage initially increases but abruptly decreases when  $V_{DD}$  reaches the level (approximately 0.8 V) that activates the internal bias circuitry and **RESET** is asserted.

**B:** At 'B',  $V_{DD}$  reaches the threshold level of  $V_{SH}$ . At this point the device releases the hold on the  $V_{OUT}$  reset. The Reset output  $V_{OUT}$  tracks  $V_{DD}$  as it rises above  $V_{SH}$  (assuming the reset pull-up resistor  $R_{PU}$  is connected to  $V_{DD}$ ). In a microprocessor based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

**C–D:** At 'C',  $V_{DD}$  begins to fall, causing  $V_{OUT}$  to follow.  $V_{DD}$  continues to fall until the  $V_{SL}$  undervoltage detection threshold is reached at 'D'. This causes a reset signal to be generated ( $V_{OUT}$  Reset goes LOW).

**D–E:** Between 'D' and 'E',  $V_{DD}$  starts rising.

**E:** At 'E',  $V_{DD}$  rises to the  $V_{SH}$ . Once again, the device releases the hold on the  $V_{OUT}$  reset. The Reset output  $V_{OUT}$  tracks  $V_{DD}$  as it rises above  $V_{SH}$ .

**F–G:** At 'F',  $V_{DD}$  is above the upper threshold and begins to fall, causing  $V_{OUT}$  to follow it. As long as  $V_{DD}$  remains above the  $V_{SH}$ , no reset signal will be triggered. Before  $V_{DD}$  falls to the  $V_{SH}$ , it begins to rise, causing  $V_{OUT}$  to follow it. At 'G',  $V_{DD}$  returns to normal.

**H:** At event 'H'  $V_{DD}$  falls until the  $V_{SL}$  undervoltage detection threshold point is reached. At this level, a **RESET** signal is generated and  $V_{OUT}$  goes LOW.

**J:** At 'J' the  $V_{DD}$  voltage has decreased until normal internal circuit bias is unable to maintain a  $V_{OUT}$  reset. As a result,  $V_{DD}$  may rise to less than 0.8 V. As  $V_{DD}$  decreases further,  $V_{OUT}$  reset also decreases to zero.

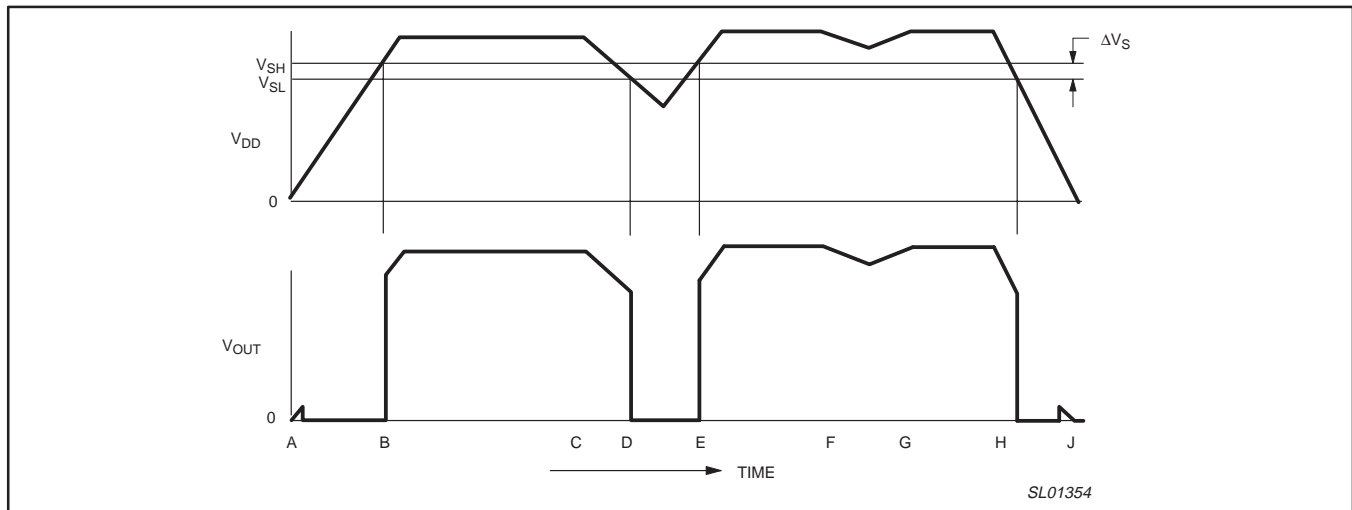


Figure 13. Timing diagram.



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## Application information

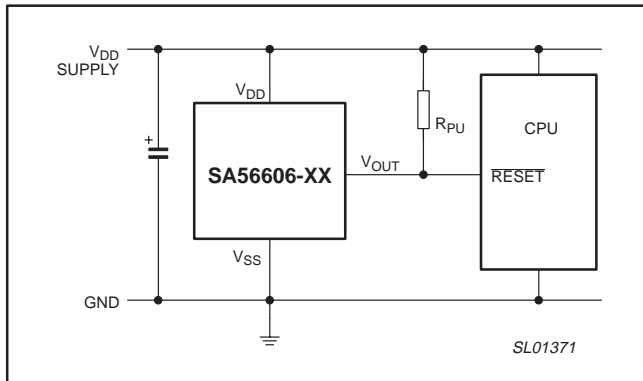


Figure 14. Conventional reset application.

The Power ON Reset Circuit shown in Figure 15 is an example of how to obtain a stable reset condition upon power-up. If the power supply voltage rises abruptly, the  $\overline{\text{RESET}}$  may go HIGH momentarily when  $V_{\text{DD}}$  is below the minimum operating voltage (0.95 V). To overcome this, a resistor (R) is placed between positive supply and the  $V_{\text{DD}}$  pin with a capacitor from the  $V_{\text{DD}}$  pin to ground.

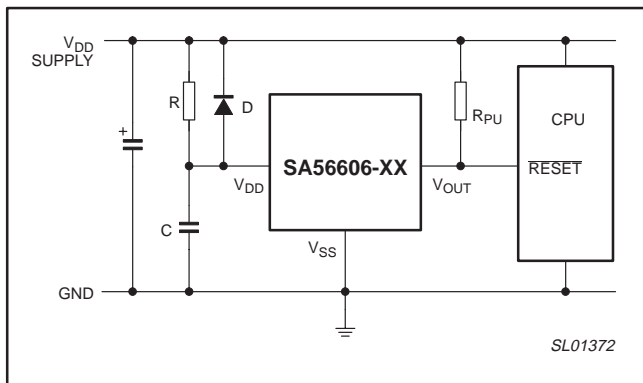


Figure 15. Power ON reset circuit.

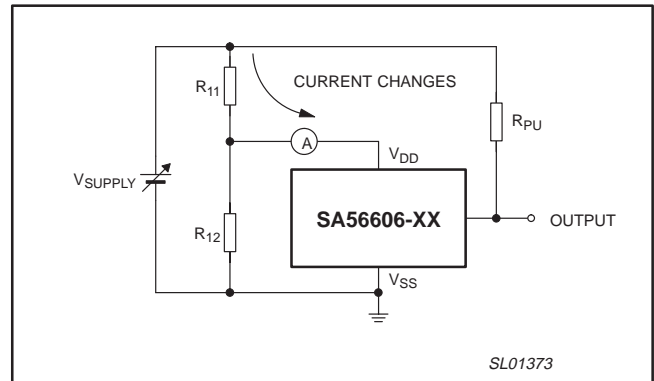


Figure 16. High impedance supply operating problems.

Significant voltage variations of  $V_{\text{DD}}$  may occur when the device is operated from high impedance power sources. When the device asserts or releases a reset,  $V_{\text{DD}}$  variations are produced as a result of the voltage drop developed across  $R_{11}$  due to the current variations through the resistor  $R_{11}$  (representing the supply impedance). If the  $V_{\text{DD}}$  variations are large, such that they exceed the Detection Hysteresis, the output of the device can oscillate from a HIGH state to a LOW state. The user should avoid using high impedance  $V_{\text{DD}}$  sources to prevent such situations.

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## Test circuits

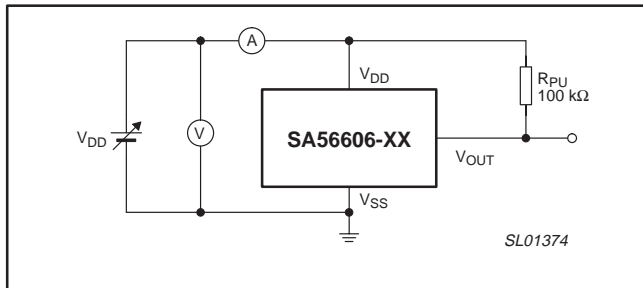


Figure 17. Test circuit 1.

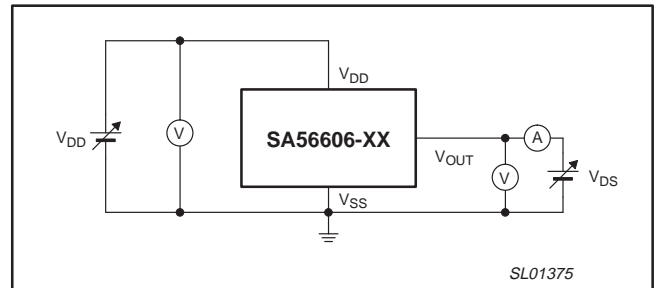


Figure 18. Test circuit 2.

## PACKING METHOD

The SA56606-XX is packed in reels, as shown in Figure 19.

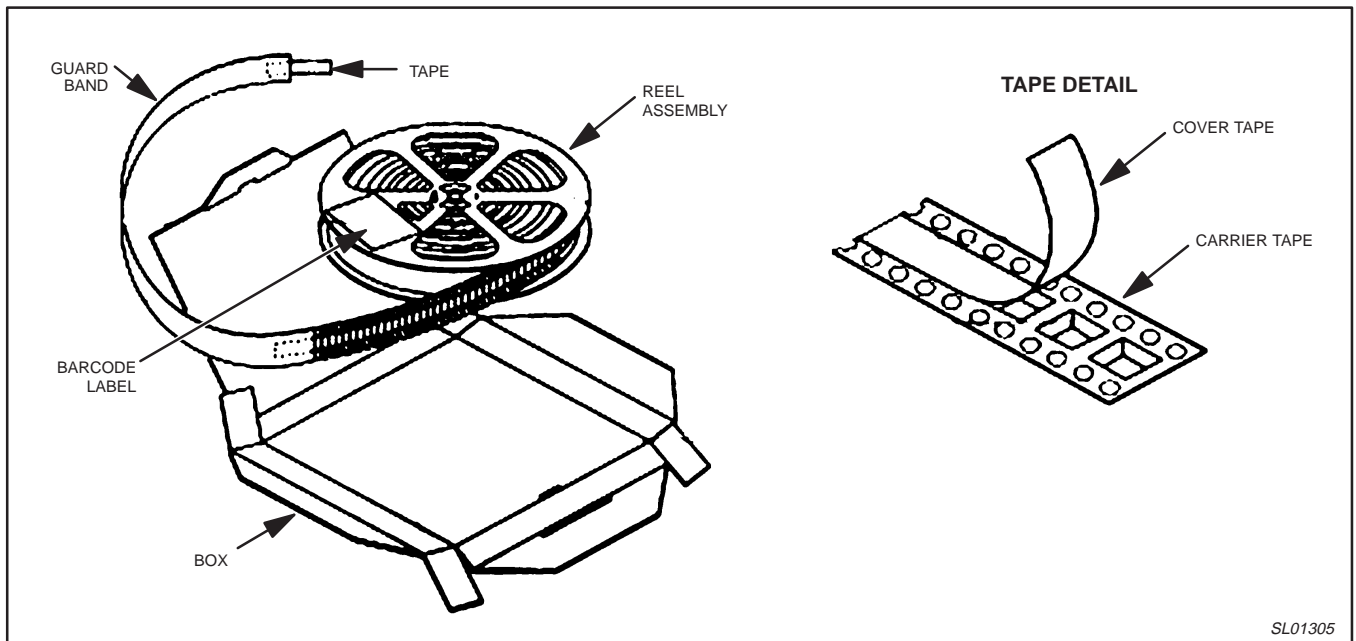
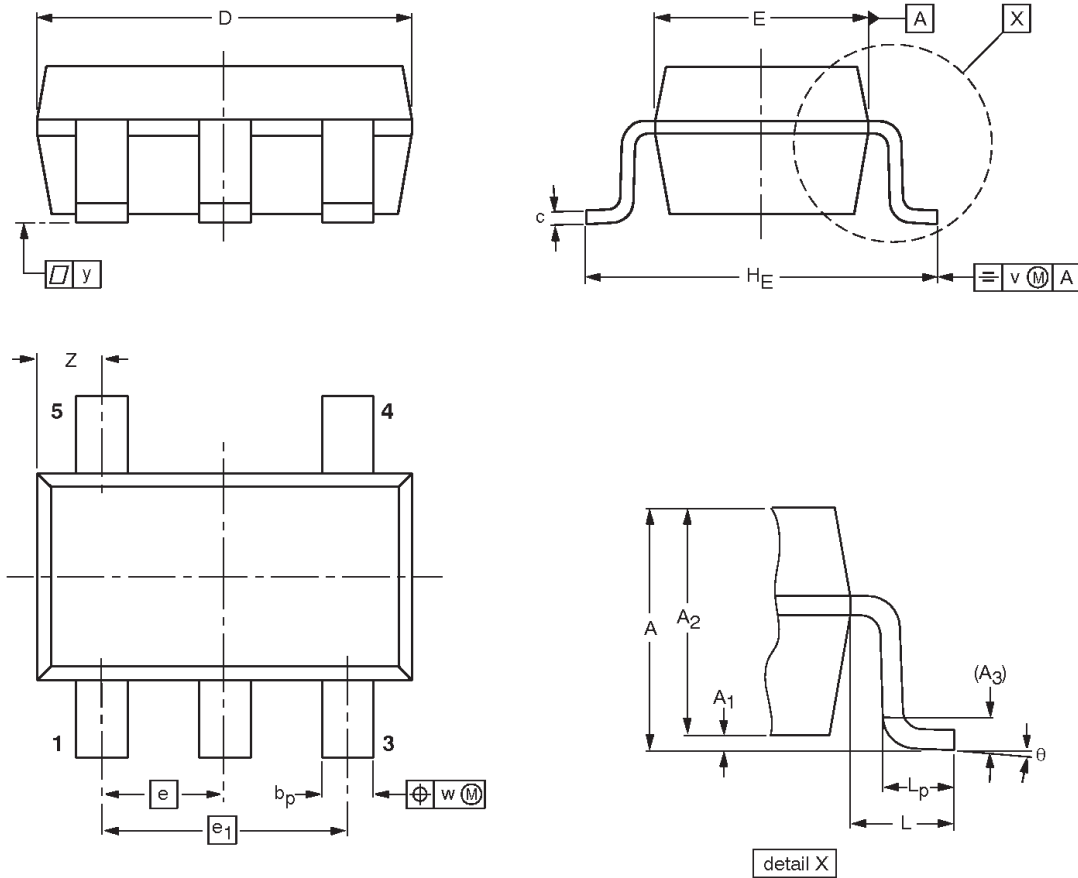


Figure 19. Tape and reel packing method

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## SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	H <sub>E</sub>	L	L <sub>p</sub>		y	θ
mm	1.35	0.05 0.15	1.2 1.0	0.025	0.55 0.41	0.22 0.08	3.00 2.70	1.70 1.50	0.95	1.90	3.00 2.60	0.60	0.55 0.35		0.1	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
		MO-178		

## CMOS system reset

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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