FAIRCHILD SEMICONDUCTOR®

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µSerDes™ FIN212AC

12-Bit Serializer Deserializer with Multiple Frequency Ranges

Features

- Low Power Consumption
- Low Power, Proprietary, CTL I/O Serial Interface
- Wide PLL Input Frequency Range
- Wide Parallel Supply Voltage Range: 1.65 to 3.6V
- Low Power Core Operation: $V_{DDS/A}$=2.5 to 3.6V
- Built-in LV-CMOS Voltage Translation Capability with no External Components
- Adjustable Parallel Edge Rate
- Operates as Serializer or Deserializer
- Standby Power-Down Mode Support
- Built-in Differential Termination

Applications

- 8-Bit LCD Displays for Cell Phones
- 8/10-Bit Cell Phone Camera Interface
- 8-Bit LCD Displays for Printers

Related Application Notes

- *AN-5058 µSerDes™ Family Frequently Asked Questions*
- *AN-5061 µSerDes™ Layout Guidelines*

Description

The FIN212AC µSerDes is a low-power serializer / deserializer optimized for use in cell phone displays and camera paths. The device reduces a 12-bit data path to four wires. The device can be configured as a serializer or deserializer through the DIRI pin, minimizing component types in the system. For camera applications, an additional master clock can be passed in the opposite direction of data flow.

The device utilizes Fairchild's proprietary ultra-low power, low-EMI technology. LV-CMOS parallel output buffers have been implemented with slew rate control to adjust for capacitive loading and to minimize EMI. The device also supports an ultra-low power-down mode for conserving power in battery-operated applications

The device is available in a 5x5mm MLP package to attach directly to a flex circuit, or in two choices of BGA, where space constraints are a concern.

Ordering Information

Order Number	Package	Pb-Free	Operating Temperature Range	Package Description	Packing Method
FIN212ACMLX	MLP032A	Yes	-30 to 70°C	32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm square	Tape & Reel
FIN212ACGFX	BGA42A	Yes	-30 to 70°C	42-Ball Ultra Small-Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5 x 4.5mm wide, 0.5mm Ball Pitch	Tape & Reel
FIN212ACBFX	BGA36A (Preliminary)	Yes	-30 to 70°C	36-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-xxx 2.5mm square, 0.4mm Ball Pitch	Tape & Reel

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Pin Definitions

Pin	I/O type	# of Pins	Description of Signals
DP[1:12]	CMOS-I/O	12	LV-CMOS Parallel I/O. Direction controlled by DIRI pin.
CKREF	CMOS-IN	1	LV-CMOS clock input and PLL reference.
STROBE	CMOS-IN	1	LV-CMOS strobe input for latching data into the serializer.
CKP	CMOS-OUT	1	LV-CMOS word clock output.
DSO+(DSI-)(1) DSO-(DSI+)	DIFF-I/O	2	CTL Differential serial I/O data signals.(2) DS(I)+: Positive signal of DS(I) pair; DS(I)-: Negative signal of DS(I) pair.
CKSI+, CKSI-	DIFF-IN	2	CTL Differential deserializer input bit clock. CKSI+: Positive signal of CKSI pair; CKSI-: Negative signal of CKSI pair.
CKSO+, CKSO-	DIFF-OUT	2	CTL Differential serializer output bit clock. CKSO+: Positive signal of CKSO pair; CKSO-: Negative signal of CKSO pair.
S0, S1	CMOS-IN	1	DIRI=1: signals are used to define frequency range for the PLL. DIRI=0: Signals are used to define the edge rate of the deserializer parallel I/Os.
PLL0(PWS0)	CMOS-IN	1	DIRI=1: PLL0 signal is used to divide or adjust the serial frequency. DIRI=0: PWS0 signal is used to set the width of the CKP output pulse.
PLL1(PWS1)	CMOS-IN	1	DIRI=1: PLL1 Signal is used to divide the serial frequency. DIRI=0: PWS1 pin controls the output pulse width.
TEST / (XTRM)	CMOS_IN	1	DIRI=1: TEST=0, Normal Operation. DIRI=0: Termination enable functionality for deserializer. XTRM=0 Internal termination. XTRM=1 External termination required. Ground this pin for serializer.
CTL_ADJ (GND)	CMOS_IN	1	Adjusts CTL drive for serializer. Ground this pin for deserializer.
DIRI	IN	1	LV-CMOS Control Input. Used to control direction of data flow: DIRI= “1” Serializer, DIRI=“0” Deserializer
/DIRO	OUT	1	LV-CMOS Output. Inversion of DIRI in normal operation mode.
VDDP	Supply	1	Power supply for parallel I/O and translation circuitry.
VDDS	Supply	1	Power supply for core and serial I/O.
VDDA	Supply	1	Power supply for analog PLL circuitry.
GND	Supply	0	Ground center pad, ground D4, E3 and NCs for 42-ball BGA. Ground B5, C2, C4 for 36-ball BGA.

Notes:

1. () Indicate deserializer functionality when DIRI=0.
2. The DS serial port pins are arranged such that when one device is rotated 180 degrees from the other device, the serial connections properly align without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.
3. All unused LV-CMOS input signals should be connected to GND or VDDP. Signals can be connected directly to the rail or through a resistor.
4. All unused LV-CMOS output signals should be allowed to float.

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Pin Assignments

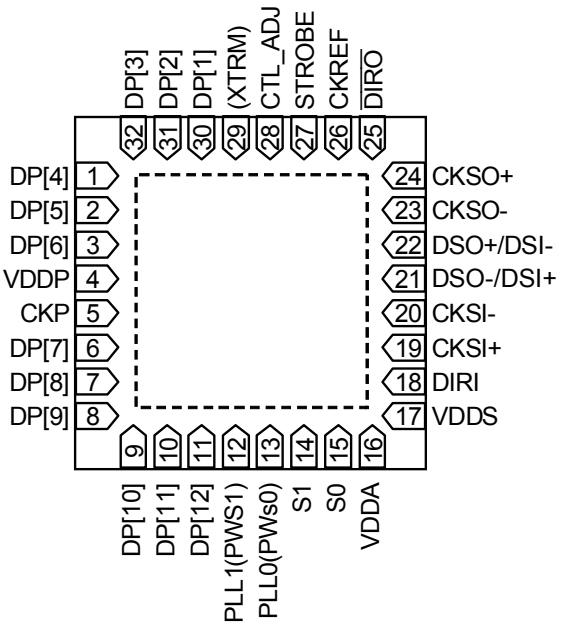
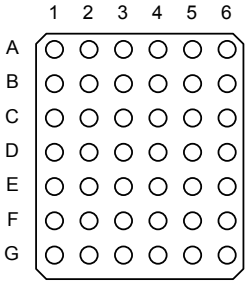
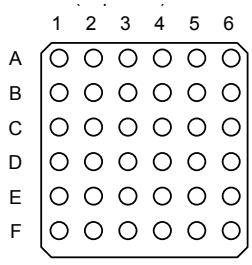


Figure 1. Pin Assignments for 32-Pin MLP (5x5mm, .5mm Pitch, Top View)



	1	2	3	4	5	6
A	DP4	DP2	XTRM	CTL_ADJ	n/c	CKREF
B	DP6	DP5	DP1	n/c	STROBE	/DIRO
C	CKP	N/C	DP3	n/c	CKSO+	CKSO-
D	N/C	DP7	VDDP	GND	DSO-/DSI+	DS0+/DSI-
E	DP8	DP9	GND	VDDS	CKSI+	CKSI-
F	DP10	DP11	n/c	VDDA	n/c	DIRI
G	DP12	n/c	PLL1(PWS1)	PLL0(PWS0)	S1	S0

Figure 2. Pin Assignments for 42 BGA (3.5x4.5mm, .5mm Pitch, Top View)



	1	2	3	4	5	6
A	DP4	DP2	DP1	(XTRM)	STROBE	CKREF
B	DP6	DP5	DP3	CTL_ADJ	GND	/DIRO
C	CKP	GND	VDDP	GND	CKSO+	CKSO-
D	DP7	DP8	GND	VDDS	DSO-/DSI+	DS0+/DSI-
E	DP9	DP10	PLL1(PWS1)	S0	CKSI+	CKSI-
F	DP11	DP12	PLL0(PWS0)	S1	VDDA	DIRI

Figure 3. Pin Assignments for 36 BGA (2.5x2.5mm, .4mm Pitch) Preliminary

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Control Logic Circuitry

Mode	PLL0	PLL1	S1	S0	DIRI	Description
0	X	X	0	0	X	Power-Down Mode
1	1	0	0	1	1	12-Bit Serializer, Standard Clocking, 20MHz to 40MHz CKREF
1	0	0	0	1	1	12-Bit Serializer, Over-Clocked PLL, 19MHz to 38.2MHz CKREF
1	X	X	0	1	0	12-Bit Deserializer
2	1	0	1	0	1	12-Bit Serializer, Standard Clocking, 5MHz to 14MHz CKREF
2	0	0	1	0	1	12-Bit Serializer, Over-0Clocked PLL, 4.7MHz to 13.3MHz CKREF
2	X	X	1	0	0	12-Bit Deserializer
3	1	0	1	1	1	12-Bit Serializer, Standard Clocking, 8MHz to 28MHz CKREF
3	0	0	1	1	1	12-Bit Serializer, Over-Clocked PLL, 9.5MHz to 26.7MHz CKREF
3	x	X	1	1	0	12-Bit Deserializer

Table 1. Control Logic Circuitry

[DIRI] Direction Logic: The FIN212 can be configured as a 12-bit serializer or deserializer based on the state of the DIRI signal. When DIRI is 1, the device is a serializer. When DIRI is 0, the device is a deserializer. The /DIRO signal is an inversion of the DIRI signal. The /DIRO signal of the master can be used to drive the DIRI signal of the slave in applications where the interface needs to be turned around.

[S0, S1] Mode Select: The mode select signals, S1 and S0, are used for different purposes when the device is a serializer or a deserializer. For the serializer, the pins need to be set to the correct value of the input CKREF Frequency range.

For the deserializer the signals are used to select an edge rate value. The fastest edge rates correspond to the highest frequency mode. This relationship is maintained for all modes.

Mode #	DIRI=0		Frequency Range
	S1	S0	
0	0	0	Power-Down
1	0	1	FAST
2	1	0	SLOW
3	1	1	MEDIUM

Table 2. Deserializer Edge Rates

[PLL0, PLL1] PLL Frequency Select Signals: The PLL1 and PLL0 signals provide additional flexibility in generating the serial clock frequency. The PLLn signals only function when the device is a serializer (DIRI=1). When the device is a slave, these pins are used for pulse width adjustment.

Over-clocking mode is used when the input reference clock has been implemented with significant spread spectrum. Over-clocking allows the serializer to tolerate a large amount of CKREF frequency spread.

No-Divide mode should be used for standard 8-bit pixel interface where the STROBE and CKREF frequencies are identical.

Divide-by-2 and Divide-by-3 modes are useful in microcontroller interfaces where the CKREF frequency is significantly higher than the required STROBE frequency.

DIRI=1		Serializer Frequency Multiplier	
PLL1	PLL0		
0	0	7.3x	Over-clocking
0	1	7x	No Divide
1	0	3.5x	Divide by 2
1	1	2.3x	Divide by 3

Table 3. Frequency Multipliers

Internal STROBE Filter: When the PLL starts, the STROBE signal is internally held off until the PLL is locked. This prevents any spurious data from being passed through the device.

[PWS0, PWS1] Pulse Width Adjust Circuitry: The word clock strobe output (CKP) pulse width can be adjusted through the PWS0 and PWS1 signals. The signals can be used to lengthen the width of the LOW pulse or invert the pulse in RGB applications with a 50% duty cycle.

DIRI=0		Low Time (Bits) No Divide	Polarity (CKP Read Edge)
PWS1	PWS0		
0	0	7	LH
0	1	7	HL
1	0	13	LH
1	1	17	LH

Table 4. Pulse Width Adjust Circuitry at Serial CLK Period

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Power-Down Functionality: When both S1 and S0 signals are 0, regardless of the state of the DIRI signal, the FIN212AC resets and powers down. The power-down mode shuts down all internal analog circuitry, disables the serial input and output of the device, and resets all internal digital logic. Table 5 indicates the state of the output buffers in Power-Down mode.

Signal Pins	DIRI=1	DIRI=0
DP[10:1]	Inputs Disabled	Outputs HIGH-Z
DP[12:11]	Inputs Disabled	Outputs HIGH-Z
CKP	HIGH	Outputs HIGH-Z
STROBE	Input Disabled	Input Disabled
CKREF	Input Disabled	Input Disabled
/DIRO	0	1

Table 5. Output States

When an input is disabled, it does not draw current, regardless of the state or level of the input signal.

All of the LV-CMOS inputs must remain driven during power-down to ensure a low-power state

Turn-Around Functionality: The device passes and inverts the DIRI signal asynchronously to the /DIRO signal. Care must be taken by the system designer to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be put into a HIGH-impedance state prior to the DIRI signal being asserted. When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned around into a deserializer and the values are overwritten.

Strobe Pass-Through Mode: For some applications, it is desirable to pass a word clock across a differential signal pair in the opposite direction of serialization. The FIN212 supports this mode of operation. The following describes how to enable this functionality.

Deserializer Configuration (DIRI=0)

1. CKREF LOW
2. Master clock connected DES to STROBE

Serializer Configuration (DIRI=1)

1. CKSI passes signal to serializer CKP

[CTL_ADJ] CTL Drive Adjustment: The drive characteristics of the CTL I/O can be adjusted through the CTL_ADJ pin. Standard-level CTL drive is provided when the CTL_ADJ pin is zero. High- level drive is provided when CTL_ADJ pin is HIGH. High-drive should be used in noisy environments or when driving cables longer than 20cm. When in high-drive mode, CTL drive increases by approximately by 50%.

CTL_ADJ	Description
0	Standard CTL Drive
1	High CTL Drive

Table 6. CTL_ADJ Functionality

[(/XTRM]] Test / XTRM Mode Functionality: For the deserializer, the (XTRM) signal can be used to enable or disable the internal termination resistor on the CKS and DS signals of the deserializer. When the internal termination is disabled, an external termination resistor is required for the CTL I/O to operate properly.

(XTRM)	DIRI=0 (/XTRM)
0	Internal Termination
1	External Termination

Table 7. (/XTRM) Functionality

Serializer Configuration (DIRI=1)

1. Master CLK transmitted out of SER CKP
2. Drive the pixel_CLK [(/XTRM)] into SER TROBE

Deserializer Configuration (DIRI=0)

1. Pixel_CLK transmitted out of DES CKP

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Serializer Operation Mode (DIRI=1)

The serializer configurations are described in the following sections. The basic serialization circuitry works similarly in all modes, but the actual data and clock streams differ if the frequency of CKREF is the same as or greater than the STROBE frequency. When CKREF equals STROBE, the CKREF and STROBE signals are physically connected together and are one signal. When CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE. For proper serialization, the PLL should be stable and locked prior to sending valid data. For the following modes, refer to Table 1.

MODE 1,2,3; PLL1=0, PLL0=1;
CKREF Equals STROBE
This mode is typically used when sending pixel data at a constant rate. Data is captured on the rising edge of the STROBE signal and serialized. The serial CLK frequency is exactly seven times the clock frequency. For example, a CKREF frequency of 10MHz results in a serial CLK frequency of 70MHz and a data transfer rate of 140Mbps. The serialized data stream is synchronized and sent source synchronously with a bit clock.

MODE 1,2,3; PLL1=0, PLL0=1;
CKREF Does Not Equal STROBE
For microcontroller interfaces, a reference clock at the same frequency as the strobe is typically not available. Data transfers are typically not synchronous. To accommodate this type of transfer, a reference clock of a higher frequency than the fastest strobe frequency must be provided to the CKREF signal. The CKREF clock signal must be continuously running for as long as data is being transferred. The actual serial transfer rate is dependent on the CKREF and the parallel transfer rate depends on the STROBE frequency. A data value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same. The exact frequency that the reference clock needs to run is dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the minimum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly if the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency. A STROBE frequency of 7MHz and a CKREF of 11MHz results in serial CLK frequency seven times the CKREF (77MHz) and a data transfer rate of 154Mbps.

MODES (1,2,3); PLL1=1,PLL0=0 (Divide-by-2) or PLL1=1,PLL0=1 (Divide-by-3)
For some microcontroller applications, the available reference frequency is significantly faster than the STROBE frequency required for the application. To more closely match the serial frequency with the strobe, the reference frequency can be divided by two or three. The serializer works identically to when CKREF is not equal to STROBE. Refer to the Deserializer Operation Mode section below for details.

Deserializer Operation Mode

The operation of the deserializer is dependent upon the data received on the DSI data signal pair and the CKSI clock signal pair. The following sections describe the operation of the deserializer under two distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device used to generate the serial data and clock signals. When operating in this mode, the internal serializer circuitry is disabled, including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks.

DIRI = 0; Serializer Source: CKREF Equals STROBE
When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserialized through a bit clock sent with the data. The falling edge of CKP occurs coincident with the parallel data transition.

DIRI=0; Serializer Source:
CKREF Does Not Equal STROBE
The logical operation of the deserializer remains the same whether CKREF is equal in frequency to STROBE or at a higher frequency than STROBE. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The average frequency of the CKP signal is equal to the STROBE frequency. The falling edge of CKP is coincident with data transition. The LOW time of the CKP signal is set by the state of the PWS1 and PWS0 signals.

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Pulse Width Calculations

Pulse Width Low Tpwl = (divOut*Pwdth)/(CKREF*14)

To meet minimum pulse width specification, divOut*Pwdth≥Tpwl*(T_{CKREF}*14).

Bit times based on PWS0, PWS1 (Pwdth = 7, 13, 17), divide by divOut = 0.954, 1, 2, 3.

Example: Tpwl=60ns CKREF=26MHz

CKP Pulsewidth = (2*13)/(26MHz*14)

if DivOut=2, Pwdth=13 bitTimes=26. Tpwl=71.4ns

Serializer Setup		Deserializer Setup		PLL DivOut	Pwidth	CKP-PWL Bit Times	CKREF Frequency	
PLL1	PLL0	PWS1	PWS0				19.2MHz	26Mhz
0	0	0	0	0.954	7	6.7	24.8	18.3
0	0	0	1	0.954	7	6.7	24.8	18.3
0	0	1	0	0.954	13	12.4	46.1	34.1
0	0	1	1	0.954	17	16.2	60.3	44.6
0	1	0	0	1	7	7	26.0	19.2
0	1	0	1	1	7	7	26.0	19.2
0	1	1	0	1	13	13	48.4	35.7
0	1	1	1	1	17	17	63.2	46.7
1	0	0	0	2	7	14	52.1	38.5
1	0	0	1	2	7	14	52.1	38.5
1	0	1	0	2	13	26	96.7	71.4
1	0	1	1	2	17	34	126.5	93.4
1	1	0	0	3	7	21	78.1	57.7
1	1	0	1	3	7	21	78.1	57.7
1	1	1	0	3	13	39	145.1	107.1
1	1	1	1	3	17	51	189.7	140.1

Table 8. CKP Pulse Widths (in nanoseconds) for Standard Cell Phone Operating Frequencies(5)

Note:

5. CKP Pwidth assumes minimal slew rate at the 50% transition point.

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Application Diagrams

The following application diagrams illustrate the most typical applications for the FIN212 device. Specific configurations of the control pins may vary based on the needs of a given system. The following recommendations are valid for all of the applications shown.

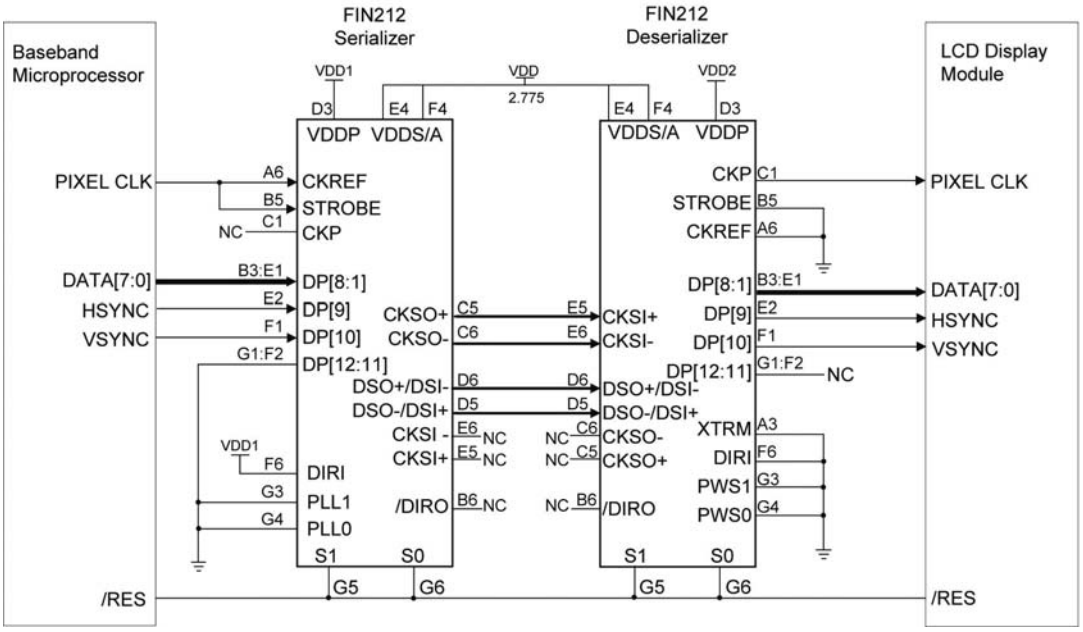


Figure 4. 8-Bit RGB Application (Example Shows BGA 42-Pin Package)

Serializer Configuration:

- PLL Frequency Mode: MODE 3 (S1=S0=1) 10-30MHz Frequency Range
- PLL Divide Mode: Over-Clocked Mode (PLL1=PLL0=0); 7.3 Serial Frequency Multiplier

Deserializer Configuration:

- Edge Rate Mode: Medium MODE 3 (S1=S0=1)
- Pulse Width Mode: Standard Non-Inverting, (PWS1=PWS0=0) Pulse Width; 3.5 x Serial CLK Period
- Pixel CLK is used to STROBE Display
- Pin number for BGA packages

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Application Diagrams (Continued)

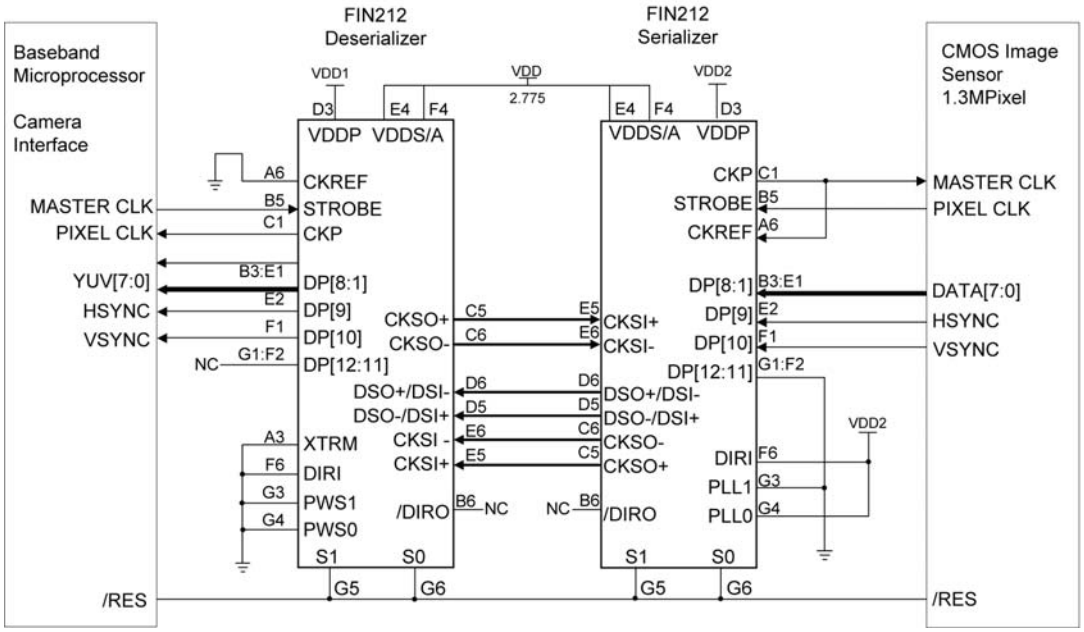


Figure 5. 8-Bit YUV 1.3MPixel CMOS Imager (Example Shows BGA 42-Pin Package)

Serializer Configuration:

- PLL Frequency Mode: MODE 3 (S1=S0=1) 10-30MHz Frequency Range
- PLL Divide Mode: Standard Not Over-Clocked (PLL1=0, PLL0=1) Multiplier 7x
- Master Clock Bypass Mode: (clock passes from CKSI to CKP)

Deserializer Configuration:

- Edge Rate Mode: Fast MODE 1 (S1=0, S0=1)
- Pulse Width Mode: Standard Non-Inverting, (PWS1=PWS0=0) Pulse Width; 3.5 x Serial CLK Period
- Master Clock Bypass Mode: Clock passes from STROBE to CKSO

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Application Diagrams (Continued)

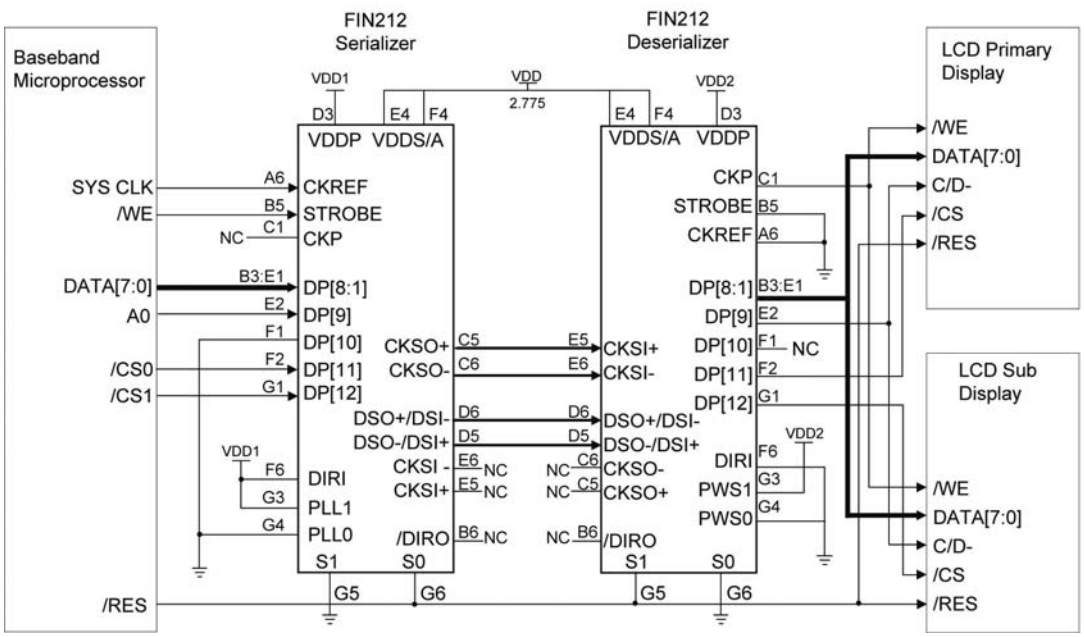


Figure 6. Dual Display with 8-Bit WRITE-Only Microcontroller Interface (Example Shows BGA 42-Pin Package)

Serializer Configuration:

- PLL Frequency Mode: MODE 1 (S1=0, S0=1) CKREF=26MHz
- STROBE Frequency = 10 MHz
- PLL Divide Mode: Divide-by 2 (PLL1=1, PLL0=0) Multiplier x 3.5

Deserializer Configuration:

- Edge Rate Mode: SLOW MODE 1 (S1=1, S0=0)
- Pulse Width Mode: 13-Bit Time Mode (PWS1=PWS0=0) (~71.4ns)

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential Serial Wires the same length.
- Do not allow noisy signals over or near differential serial wires.
  Example: No LVCMOS traces over differential serial wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Design goal of 100-ohms differential characteristic impedance.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.
- For additional applications notes or flex guidelines see your sales rep or contact Fairchild directly.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5V	+4.6	V
	All Input/Output Voltage	-0.5	V_{DD}+0.5	V
	CTL Output Short-Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature	+150		°C
T_L	Lead Temperature (Soldering, four seconds)	+260		°C
ESD	Human Body Model, 1.5KΩ, 100pF		8	kV
	Human Body Model, 1.5KΩ, Serial I/O Pins		14	kV
	Machine Model, 0Ω, 200pF		400	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	3.6	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature	-30	+70	ºC
V_{DDA-PP}	Supply Noise Voltage	100		mVp-p

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DC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.[6]	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			$0.65xV_{DDP}$		V_{DDP}	
V_{IL}	Input Low Voltage			GND		$0.35xV_{DDP}$	V
V_{OH}	Output High Voltage	I_{OH}=-2.0mA, S1=0,S0=1		$0.75xV_{DDP}$		V_{DDP}	V
		I_{OH}=-0.4mA, S1=1,S0=0					
		I_{OH}=-1.0mA, S1=1,S0=1					
V_{OL}	Output Low Voltage	I_{OL}=2.0mA, S1=0,S0=1		0		$0.25xV_{DDP}$	V
		I_{OL}=0.4mA, S1=1,S0=0					
		I_{OL}=1.0mA, S1=1,S0=1					
I_{IN}	Input Current	V_{IN}= 0V to 3.6V		-5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output HIGH Source Current	V_{OS}=1.0V	CTL_ADJ=0		-2.0		mA
			CTL_ADJ=1		-3.4		
I_{ODL}	Output LOW Sink Current	V_{OS}=1.0V	CTL_ADJ=0		1.2		mA
			CTL_ADJ=1		2.0		
V_{GO}[7]	Input Voltage Ground Offset				0		V
R_{TRM}	CKS Internal Receiver Termination Resistor	V_{ID}= 50mV, V_{IC}= 925mV, DIRI = 0		80	100	120	Ω
	DS Internal Receiver Termination Resistor	V_{ID}=50mV, V_{IC}= 925mV, DIRI = 0		80	100	120	Ω

Notes:

6. Typical values are given for V_{DD}=2.775V and T_A=25 °C. Positive current values refer to the current flowing into the device and negative values refer to the current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
7. V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

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Power Supply Currents

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD_PD}= I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S0 = 0, All Inputs at GND or VDD				0.1		µA
I_{DD_SER1}	Dynamic Serializer Power Supply Current $I_{DD_SER1}= I_{DDA}+I_{DDS}+I_{DDP}$	$f_{CKREF} = f_{STRB}$, PLL1=0,PLL0=1; CTL_ADJ=0; C_L = 0pF	S1=L S0=H	20MHz		13.0		mA
				40MHz		19.0		mA
			S1=H S0=L	5MHz		9.5		mA
				14MHz		17.0		mA
			S1=H S0=H	8MHz		11.0		mA
				28MHz		20.0		mA
I_{DD_DES1}	Dynamic Deserializer Power Supply Current $I_{DD_DES1}= I_{DDA}+I_{DDS}+I_{DDP}$	$f_{CKREF} = f_{STRB}$, PLL1=0,PLL0=1; CTL_ADJ=0; C_L = 0pF	S1=L S0=H	20MHz		10.0		mA
				40MHz		14.0		mA
			S1=H S0=L	5MHz		8.0		mA
				14MHz		9.0		mA
			S1=H S0=H	8MHz		9.0		mA
				28MHz		12.0		mA

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AC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Serializer Input Operating Conditions							
f_{CKREF}	CKREF Clock Frequency (5MHz - >40MHz)	f_{CKREF} = f_{STRB}	S1=0, S0=1	18		40	MHz
			S1=1, S0=0	5		14	
			S1=1, S0=1	10		28	
f_{STRB}	Strobe Frequency Relative to CKREF Frequency	$f_{CKREF} \neq f_{STRB}$	PLL1=0, PLL0=0			100	% of f_{CKREF}
			PLL1=0, PLL0=1			100	
			PLL1=1, PLL0=0			50	
			PLL1=1, PLL0=1			$33^{1}/_{3}$	
t_{CPWH}	CKREF DC	T=1/f_{CKREF}		0.2	0.5	0.8	T
t_{CPWL}	CKREF DC	T=1/f_{CKREF}		0.2	0.5	0.8	T
t_{CLKT}	LVCMOS Input Transition Time[8]	10-90%				20	ns
$t_{SPWH/L}$	STROBE Pulse Width HIGH/LOW	T=1/f_{CKREF}		T x $^{4}/_{14}$		T x $^{10}/_{14}$	ns
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI=1, f=5MHz See Figure 7		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE			2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay[9]	DIRI=1, f_{CKREF} = f_{STRB} See Figure 9		21a+1.5		23a+6.5	ns
Phase Lock Loop (PLL) AC Electrical Characteristics							
t_{TPLLS0}	Serializer PLL Stabilization Time	CKREF toggling and stable		200		600	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock					30.0	µs
t_{TPLLD1}	PLL Power-Down Time					20.0	ns

Notes:

8. Parameter is characterized, but not production tested.
9. The average bit time “a” is a function of the serializer CKREF frequency; a=(1/f)/14.

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AC Electrical Characteristics (Continued)

Values are provided for over-supply and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
Deserializer AC Electrical Characteristics								
t_{RCOL}	CKP OUT Low Time See Figure 8[10]		PWS1	PWS0				ns
		$f_{STRB} = f_{CKREF}$	0	0	7a-3		7a+3	
		$f_{STRB} = f_{CKREF}$	0	1	7a-3		7a+3	
		$f_{STRB} = .5x\ f_{CKREF}$	1	0	13a-3		13a+3	
		$f_{STRB} = .5x\ f_{CKREF}$	1	1	17a-3		17a+3	
t_{PDV}	Data Valid to CKP HIGH	(Rising Edge STROBE)[10], C_L=5pF See Figure 8			8a-3		8a+3	ns
t_{RFD}	Output Rise/Fall Time Data (20% to 80%)	C_L=8pF	S1=0,S0=1			3.0		ns
			S1=1,S0=0			8.0		
			S1=1,S0=1			5.0		
t_{RFC}	Output Rise/Fall Time CKP (20% to 80%)	C_L=8pF	S1=0,S0=1			2.0		ns
			S1=1,S0=0			7.0		
			S1=1,S0=1			4.0		

Notes:

10. Skew is measured from the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.
11. Signals are transmitted from the serializer source synchronously. In some cases, data is transmitted when the clock remains at a high state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew is a combination of output skew from the serializer, load variations, and ISI and jitter effects.

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Logic Timing Controls

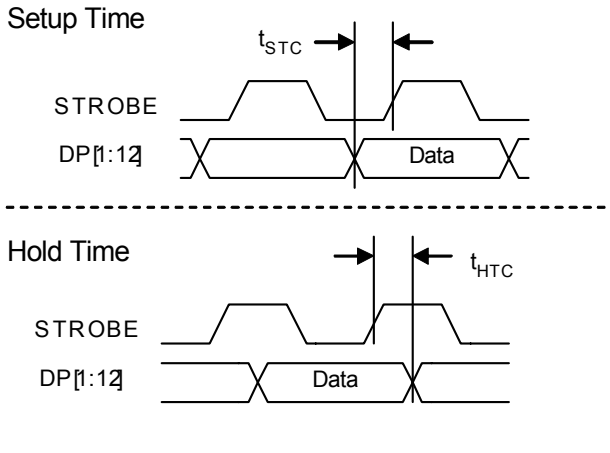
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI to /DIRO	DIRI L->H or H->L			17	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI to DP	DIRI L->H or H->L			25	ns
t_{DISDES}	Deserializer Disable Time: S0 or S1 LOW to DPTri-State	DIRI=0, See Figure 10			25	ns
t_{DISSER}	Serializer Disable Time: S0 or S1 LOW to CKP HIGH	DIRI=1; S1(0) and S0(1)=H->L			25	ns

Pin Capacitance Tables

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Capacitance of Input Only Signals	DIRI=1, S1=0, S0=0, V_{DD}=2.5V		2.0		pF
C_{IO}	Capacitance of Parallel Port Pins DP[1:12]	DIRI=1, S1=0, S0=0, V_{DD}=2.5V		2.0		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals.	DIRI=1, S1=0, S0=0, V_{DD}=2.5V		2.0		pF

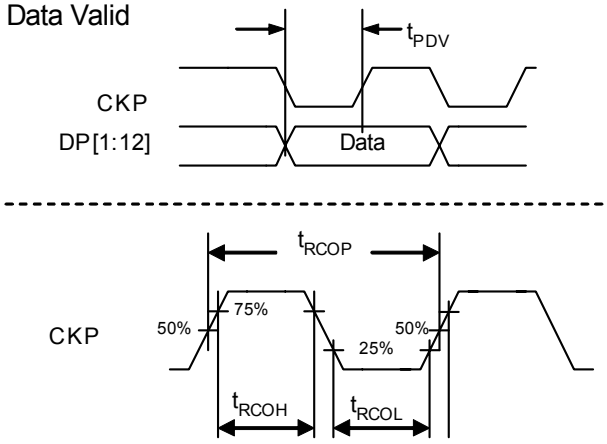
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Typical Performance Characteristics



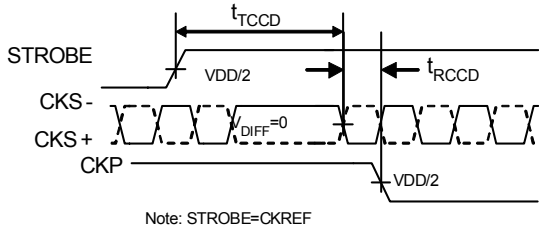
Setup: MODE0= “0” or “1”, MODE1=“1”, SER/DES=“1”

Figure 7. Serializer Setup and Hold Time



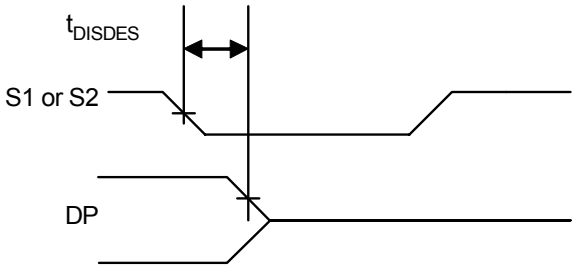
Setup: DIRI= 0, CKSI and DS are valid signals.

Figure 8. Deserializer Data Valid Time and Clock Output Parameters



Note: STROBE=CKREF

Figure 9. Clock Propagation Delay



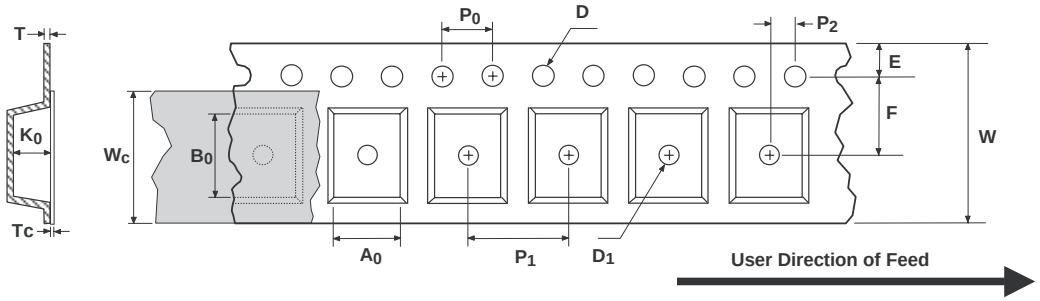
Note: If S1(2) is transitioning, S2(1) must =0 for test to be valid.

Figure 10. Deserializer Disable Timing

Tape and Reel Specifications

MLP Embossed Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



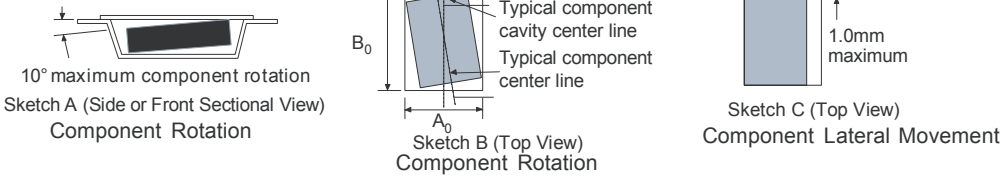
Package	A_0	B_0	D	D_1	E	F	K_0	P_1	P_0	P_2	T	T_C	W	W_C
5x5	5.35±0.1	5.35±0.1	1.55 ±0.05	1.5 min.	1.75 ±0.1	5.5 ±0.1	1.4 ±0.1	8 typ.	4 typ.	2.0 0.05±	0.3 typ.	0.07 ±0.005	12 ±0.3	9.3 typ.
6x6	6.30±0.1	6.30±0.1												

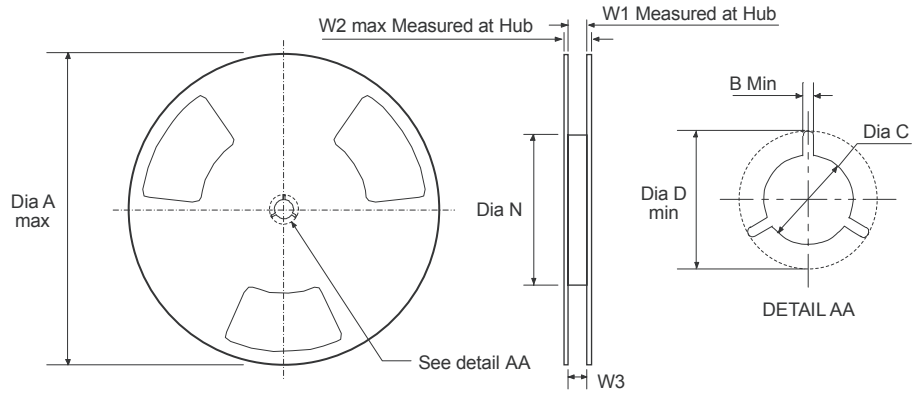
Notes:

A_0, B_0, and K_0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

MLP Shipping Reel Dimensions

Dimensions are in millimeters unless otherwise noted.





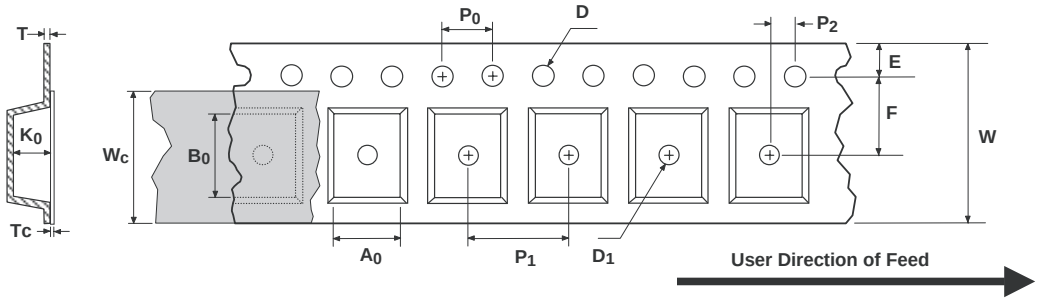
Tape Width	Dia A	Dim B	Dia C	Dia D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8	330.0 max.	1.5 min.	13.0 +0.5/-0.2	20.2 min.	178.0 min.	8.4 +2.0/-0	14.4 max.	7.9 ~ 10.4
12							18.4 max.	11.9 ~ 15.4
16							22.4 max.	15.9 ~ 19.4

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Tape and Reel Specifications (Continued)

BGA Embossed Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



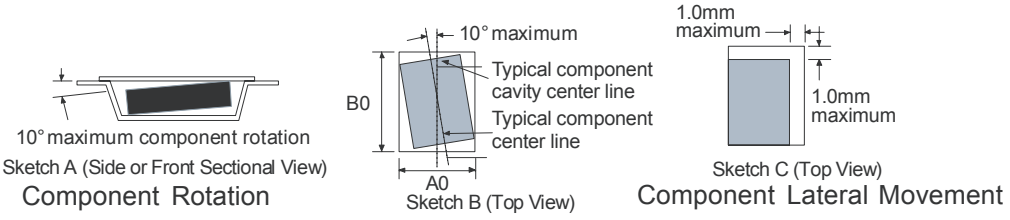
Package	A_0	B_0	D	D_1	E	F	K_0	P_1	P_0	P_2	T	T_C	W	W_C
3.5 x 4.5	TBD±0.1	TBD±0.1	1.55 ±0.05	1.5 min.	1.75 ±0.1	5.5 ±0.1	1.1 ±0.1	8.0 typ.	4.0 typ.	2.0 ±0/05	0.3 typ.	0.07 ±0.005	12 ±0.3	9.3 typ.

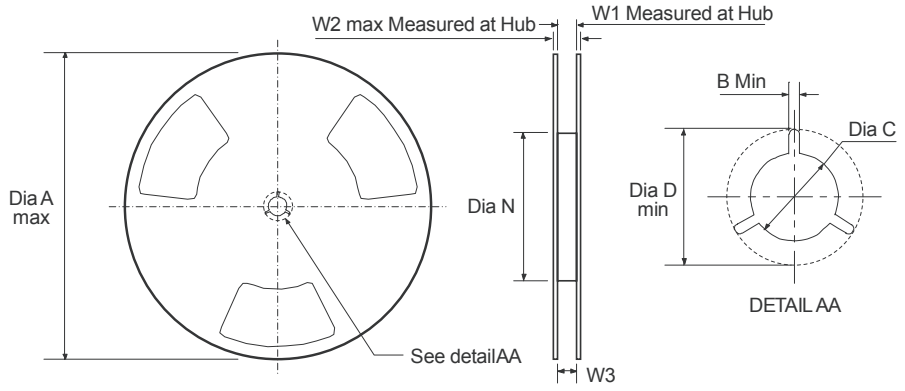
Notes:

A_0, B_0, and K_0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

BGA Shipping Reel Dimensions

Dimensions are in millimeters unless otherwise noted.



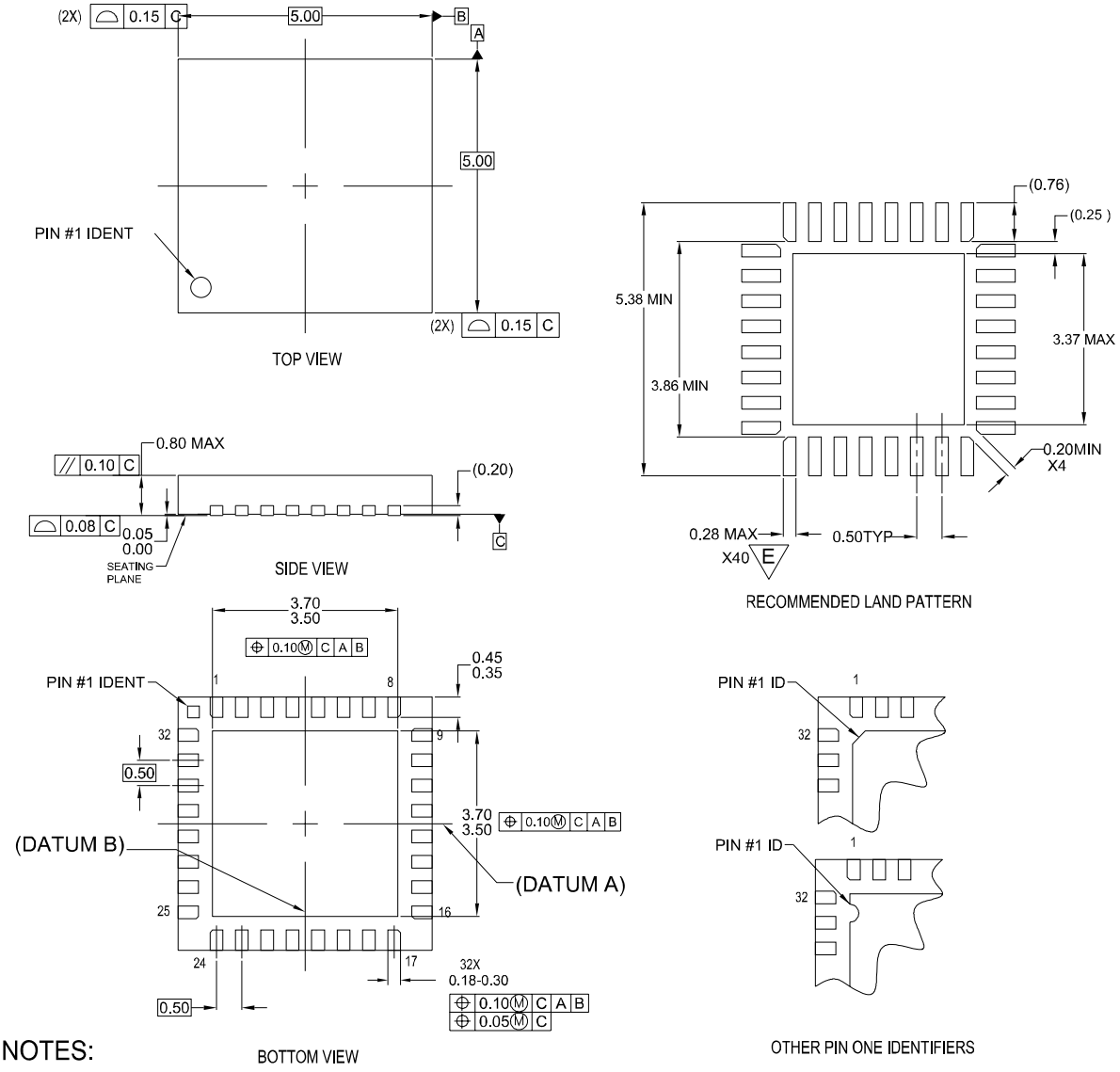


Tape Width	Dia A	Dim B	Dia C	Dia D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8	330.0 max.	1.5 min.	13.0 +0.5/-0.2	20.2 min.	178.0 min.	8.4 +2.0/-0	14.4 max.	7.9 ~ 10.4
12							18.4 max.	11.9 ~ 15.4
16							22.4 max.	15.9 ~ 19.4

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Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4
THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

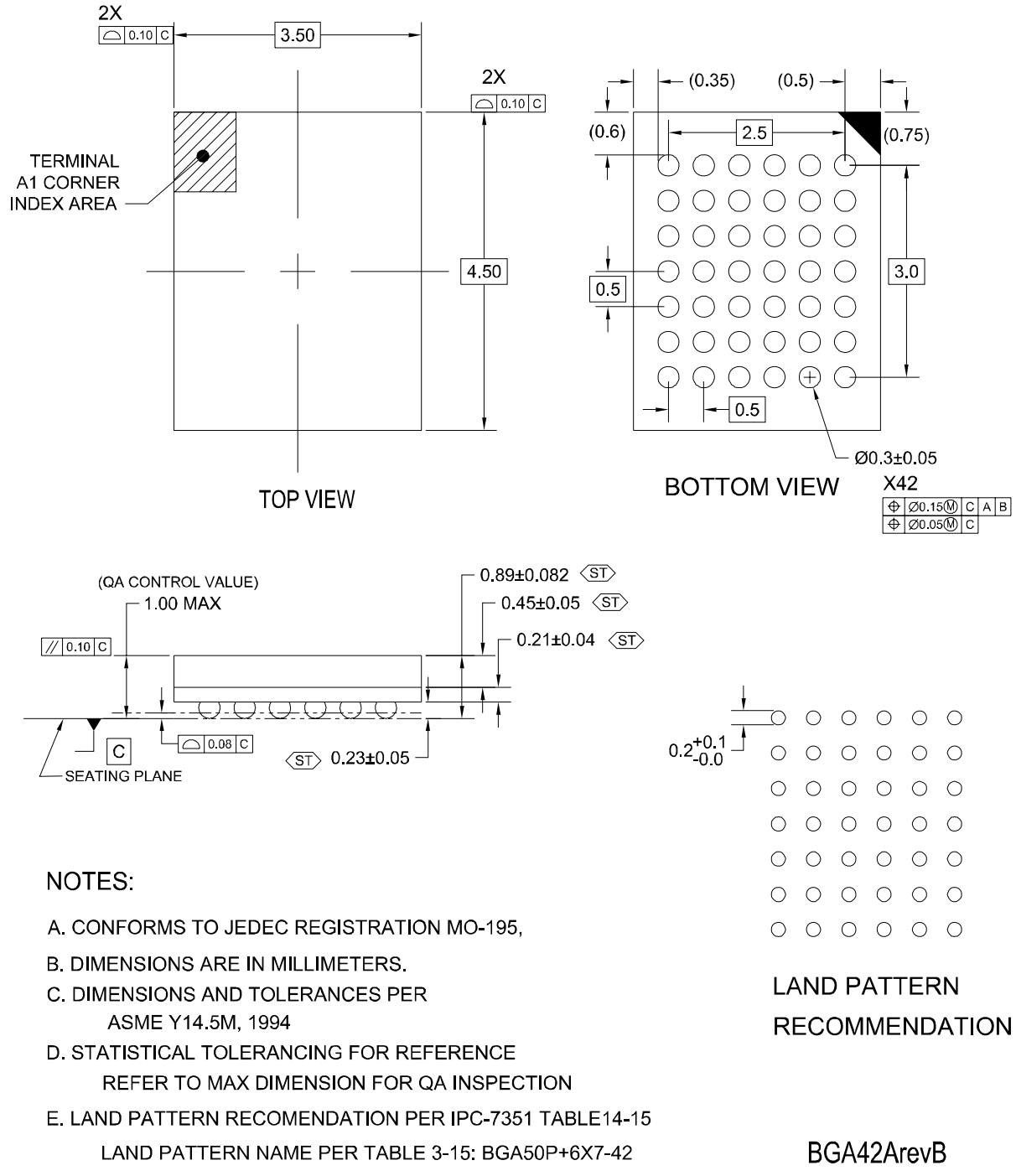
G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS,
MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP032ArevB

Figure 11. 32-Lead, Molded Leadless Package (MLP)

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE
REFER TO MAX DIMENSION FOR QA INSPECTION

E. LAND PATTERN RECOMENDATION PER IPC-7351 TABLE14-15
LAND PATTERN NAME PER TABLE 3-15: BGA50P+6X7-42

BGA42ArevB

Figure 12. 42-Ball, Ball Grid Array (BGA) Package

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