

CMLDM7002A  
CMLDM7002AG\*  
CMLDM7002AJ

SURFACE MOUNT SILICON  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
MOSFETS



SOT-563 CASE

\* Device is **Halogen Free** by design



www.centrasemi.com

#### DESCRIPTION:

These CENTRAL SEMICONDUCTOR devices are dual N-Channel enhancement-mode MOSFETs, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7002A utilizes the USA pinout configuration, while the CMLDM7002AJ utilizes the Japanese pinout configuration. These devices offer low  $r_{DS(ON)}$  and low  $V_{DS(ON)}$ .

**MARKING CODES:** CMLDM7002A: L02  
CMLDM7002AG\*: C2G  
CMLDM7002AJ: 02J

#### MAXIMUM RATINGS: ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage  
Drain-Gate Voltage  
Gate-Source Voltage  
Continuous Drain Current  
Continuous Source Current (Body Diode)  
Maximum Pulsed Drain Current  
Maximum Pulsed Source Current  
Power Dissipation (Note 1)  
Power Dissipation (Note 2)  
Power Dissipation (Note 3)  
Operating and Storage Junction Temperature  
Thermal Resistance

#### SYMBOL

$V_{DS}$  60  
 $V_{DG}$  60  
 $V_{GS}$  40  
 $I_D$  280  
 $I_S$  280  
 $I_{DM}$  1.5  
 $I_{SM}$  1.5  
 $P_D$  350  
 $P_D$  300  
 $P_D$  150  
 $T_J, T_{stg}$  -65 to +150  
 $\theta_{JA}$  357

#### UNITS

V  
V  
V  
mA  
mA  
A  
A  
mW  
mW  
mW  
 $^\circ\text{C}$   
 $^\circ\text{C/W}$

#### ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| SYMBOL               | TEST CONDITIONS                                              | MIN | MAX  | UNITS         |
|----------------------|--------------------------------------------------------------|-----|------|---------------|
| $I_{GSSF}, I_{GSSR}$ | $V_{GS}=20\text{V}, V_{DS}=0$                                |     | 100  | nA            |
| $I_{DSS}$            | $V_{DS}=60\text{V}, V_{GS}=0$                                |     | 1.0  | $\mu\text{A}$ |
| $I_{DSS}$            | $V_{DS}=60\text{V}, V_{GS}=0, T_J=125^\circ\text{C}$         |     | 500  | $\mu\text{A}$ |
| $I_{D(ON)}$          | $V_{GS}=10\text{V}, V_{DS}=10\text{V}$                       | 500 |      | mA            |
| $BV_{DSS}$           | $V_{GS}=0, I_D=10\mu\text{A}$                                | 60  |      | V             |
| $V_{GS(th)}$         | $V_{DS}=V_{GS}, I_D=250\mu\text{A}$                          | 1.0 | 2.5  | V             |
| $V_{DS(ON)}$         | $V_{GS}=10\text{V}, I_D=500\text{mA}$                        |     | 1.0  | V             |
| $V_{DS(ON)}$         | $V_{GS}=5.0\text{V}, I_D=50\text{mA}$                        |     | 0.15 | V             |
| $V_{SD}$             | $V_{GS}=0, I_S=400\text{mA}$                                 |     | 1.2  | V             |
| $r_{DS(ON)}$         | $V_{GS}=10\text{V}, I_D=500\text{mA}$                        |     | 2.0  | $\Omega$      |
| $r_{DS(ON)}$         | $V_{GS}=10\text{V}, I_D=500\text{mA}, T_J=125^\circ\text{C}$ |     | 3.5  | $\Omega$      |
| $r_{DS(ON)}$         | $V_{GS}=5.0\text{V}, I_D=50\text{mA}$                        |     | 3.0  | $\Omega$      |
| $r_{DS(ON)}$         | $V_{GS}=5.0\text{V}, I_D=50\text{mA}, T_J=125^\circ\text{C}$ |     | 5.0  | $\Omega$      |
| gFS                  | $V_{DS}=10\text{V}, I_D=200\text{mA}$                        | 80  |      | mS            |

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of  $4.0\text{mm}^2$

(2) FR-4 Epoxy PC Board with copper mounting pad area of  $4.0\text{mm}^2$

(3) FR-4 Epoxy PC Board with copper mounting pad area of  $1.4\text{mm}^2$

R8 (8-June 2015)

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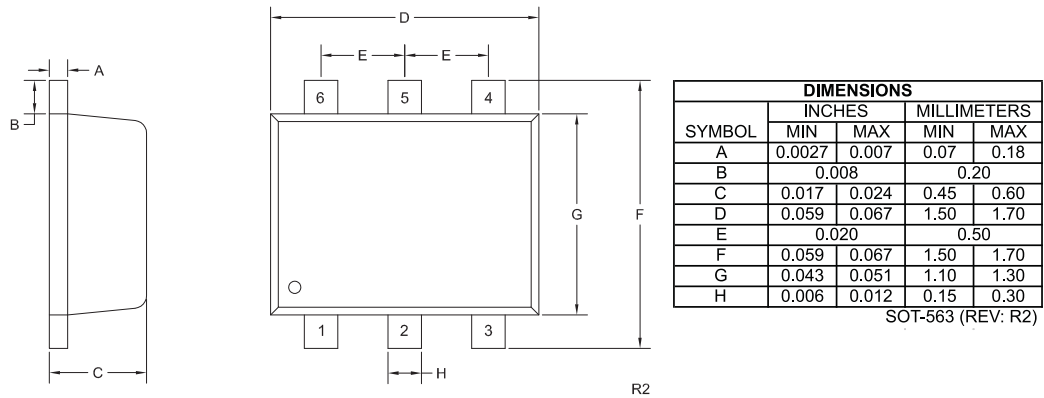
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**ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

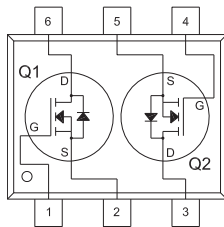
| SYMBOL               | TEST CONDITIONS                                                                                    | TYP   | MAX | UNITS |
|----------------------|----------------------------------------------------------------------------------------------------|-------|-----|-------|
| $C_{rss}$            | $V_{DS}=25\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$                                               |       | 5.0 | pF    |
| $C_{iss}$            | $V_{DS}=25\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$                                               |       | 50  | pF    |
| $C_{oss}$            | $V_{DS}=25\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$                                               |       | 25  | pF    |
| $Q_{g(tot)}$         | $V_{DS}=30\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=100\text{mA}$                                    | 0.592 |     | nC    |
| $Q_{gs}$             | $V_{DS}=30\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=100\text{mA}$                                    | 0.196 |     | nC    |
| $Q_{gd}$             | $V_{DS}=30\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=100\text{mA}$                                    | 0.148 |     | nC    |
| $t_{on}$ , $t_{off}$ | $V_{DD}=30\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=200\text{mA}$<br>$R_G=25\Omega$ , $R_L=150\Omega$ |       | 20  | ns    |

**SOT-563 CASE - MECHANICAL OUTLINE**



**PIN CONFIGURATIONS**

**CMLDM7002A (USA Pinout)  
CMLDM7002AG\***

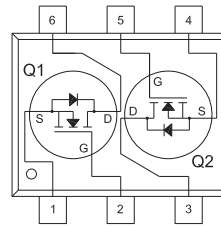


**LEAD CODE:**

- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

**MARKING CODES:**  
CMLDM7002A: L02  
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**CMLDM7002AJ (Japanese Pinout)**



**LEAD CODE:**

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

**MARKING CODE: 02J**

\* Device is **Halogen Free** by design

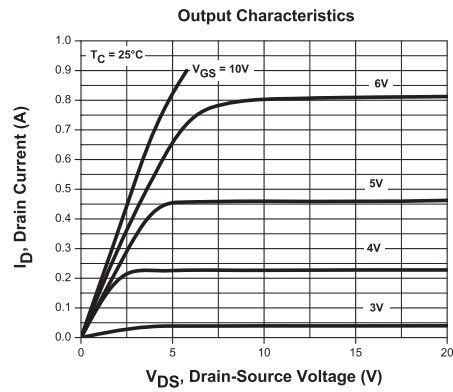
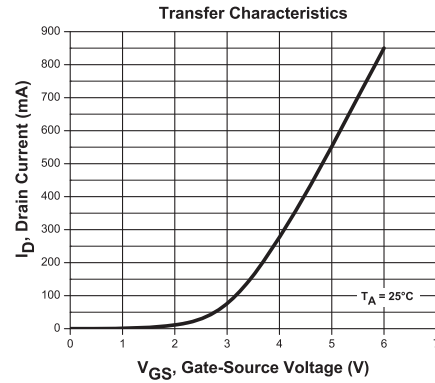
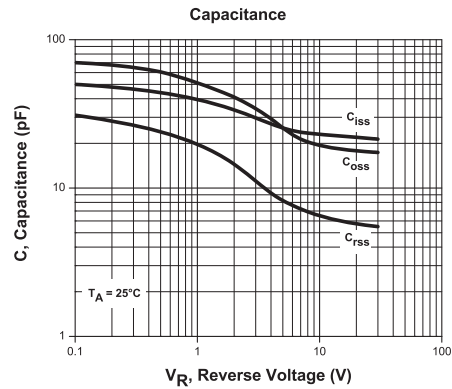
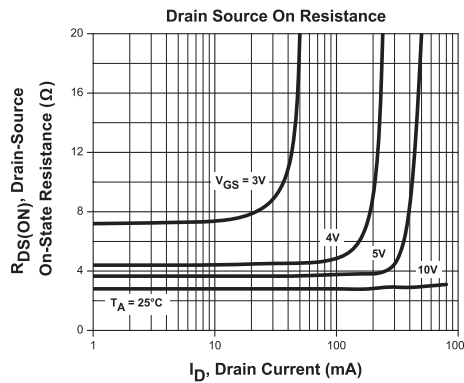
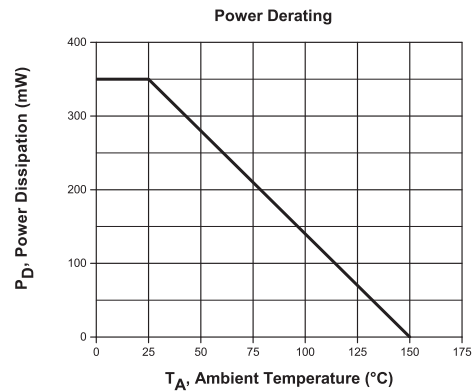
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## TYPICAL ELECTRICAL CHARACTERISTICS



R8 (8-June 2015)

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#### **SERVICES**

- Bonded Inventory
- Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development/ Multi Discrete Modules (MDM™)
- Bare Die Available for Hybrid Applications

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