

[Document Title](#)

**1M x 8 bit Low Power and Low Voltage Full CMOS Static RAM**

[Revision History](#)

<b>Revision No.</b>	<b>History</b>	<b>Draft Date</b>	<b>Remark</b>
0.0	Initial Draft	May 6, 2007	Preliminary
0.1	0.1 Revision      Add to address A19 information	May 24, 2007	
0.2	0.2 Revision      Product code table update	June 15, 2007	
0.3	0.3 Revision      Fix typo error	Nov. 12, 2007	

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The attached data sheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

### FEATURES

- Process Technology : 0.15μm Full CMOS
- Organization : 1M x 8 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V (Min.)
- Three state output and TTL Compatible
- Package Type : 44-TSOP2

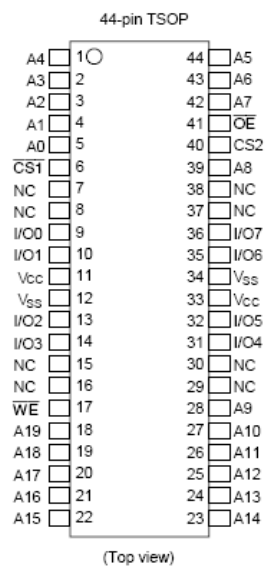
### GENERAL DESCRIPTION

The EM680FV8AU is fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC1</sub> .Max)	
EM680FV8AU-45LF	Industrial (-40 ~ 85°C)	2.7V~3.6V	45ns	2 μA	4mA	44-TSOP2
EM680FV8AU-55LF	Industrial (-40 ~ 85°C)	2.7V~3.6V	55ns	2 μA	4mA	44-TSOP2
EM680FV8AU-70LF	Industrial (-40 ~ 85°C)	2.7V~3.6V	70ns	2 μA	4mA	44-TSOP2

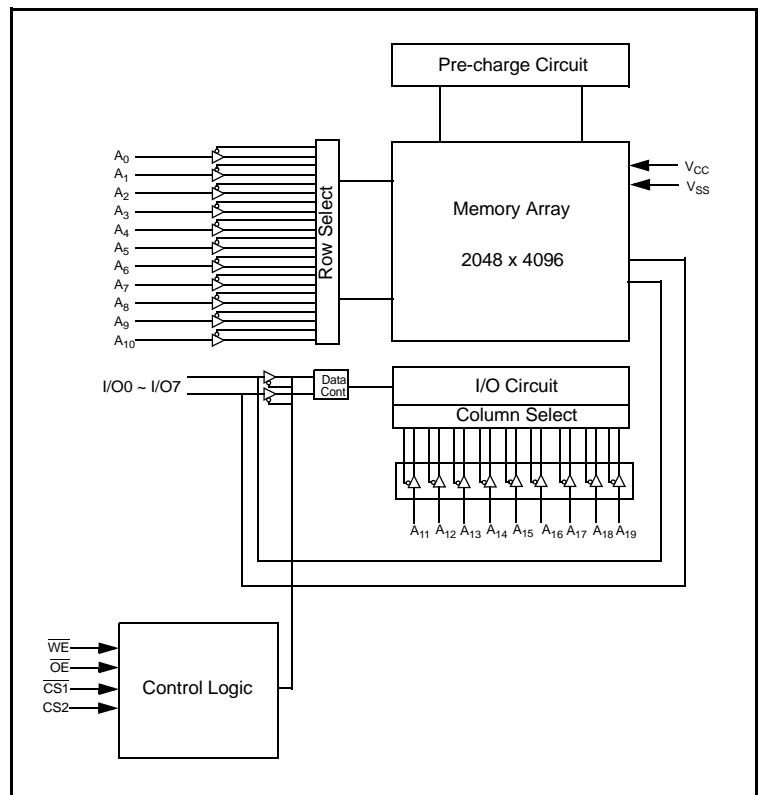
### PIN DESCRIPTION



44-TSOP2 : Top view

Name	Function	Name	Function
CS1, CS2	Chip select inputs	Vcc	Power Supply
OE	Output Enable input	Vss	Ground
WE	Write Enable input	NC	No Connected
A <sub>0</sub> -A <sub>19</sub>	Address Inputs		
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Inputs/outputs		

### FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS \***

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to Vss	$V_{IN}, V_{OUT}$	-0.2 to 4.0V	V
Voltage on Vcc supply relative to Vss	$V_{CC}$	-0.2 to 4.0V	V
Power Dissipation	$P_D$	1.0	W
Operating Temperature	$T_A$	-40 to 85	°C

\* Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**FUNCTIONAL DESCRIPTION**

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don't care. (Must be low or high state)

**RECOMMENDED DC OPERATING CONDITIONS** <sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.2^{2)}$	V
Input low voltage	$V_{IL}$	$-0.2^{3)}$	-	0.6	V

- $T_A = -40$  to  $85^\circ\text{C}$ , otherwise specified
- Overshoot:  $V_{CC} + 2.0$  V in case of pulse width  $\leq 20\text{ns}$
- Undershoot:  $-2.0$  V in case of pulse width  $\leq 20\text{ns}$
- Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE** <sup>1)</sup> ( $f = 1\text{MHz}$ ,  $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0\text{V}$	-	10	pF

- Capacitance is sampled, not 100% tested

**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$	
Output leakage current	$I_{LO}$	$\overline{CS}_1 = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{IO} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$	
Operating power supply	$I_{CC}$	$I_{IO} = 0\text{mA}$ , $\overline{CS}_1 = V_{IL}$ , $CS_2 = \overline{WE} = V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	-	-	2	mA	
Average operating current	$I_{CC1}$	Cycle time = $1\mu\text{s}$ , 100% duty, $I_{IO} = 0\text{mA}$ , $\overline{CS}_1 \leq 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	4	mA	
	$I_{CC2}$	Cycle time = Min, $I_{IO} = 0\text{mA}$ , 100% duty, $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ Others $V_{IN} = V_{IL}$ or $V_{IH}$	45ns 55ns 70ns	-	-	45 35 25	mA
Output low voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V	
Output high voltage	$V_{OH}$	$I_{OH} = -1.0\text{mA}$	2.2	-	-	V	
Standby Current (TTL)	$I_{SB}$	$\overline{CS}_1 = V_{IH}$ , $CS_2 = V_{IL}$ Other inputs = $V_{IH}$ or $V_{IL}$	-	-	0.5	mA	
Standby Current (CMOS)	$I_{SB1}$	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ ( $\overline{CS}_1$ controlled) or $0\text{V} \leq CS_2 \leq 0.2\text{V}$ ( $CS_2$ controlled) Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 3.3\text{V}$ @ $25^\circ\text{C}$ ) (Max. condition : $V_{CC} = 3.6\text{V}$ @ $85^\circ\text{C}$ )	LF	-	2	15	$\mu\text{A}$

### AC OPERATING CONDITIONS

#### Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.4V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

Output Load (See right) :  $CL^{(1)} = 100\text{pF} + 1 \text{ TTL (70ns)}$

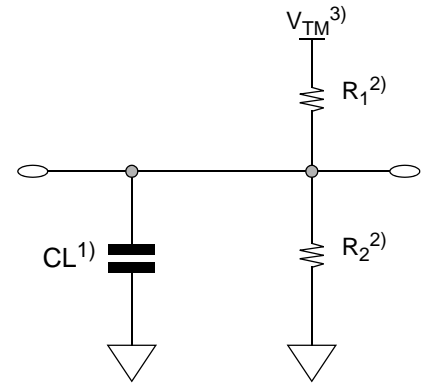
$CL^{(1)} = 30\text{pF} + 1 \text{ TTL (45ns, 55ns)}$

1. Including scope and jig capacitance

2.  $R_1=3070 \text{ ohm}$ ,  $R_2=3150 \text{ ohm}$

3.  $V_{TM}=2.8\text{V}$

4.  $CL = 5\text{pF} + 1 \text{ TTL (measurement with } t_{LZ1,2}, t_{HZ1,2}, t_{OLZ}, t_{OHZ}, t_{WHZ})$



#### READ CYCLE ( $V_{CC}=2.7 \text{ to } 3.6\text{V}$ , $Gnd = 0\text{V}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

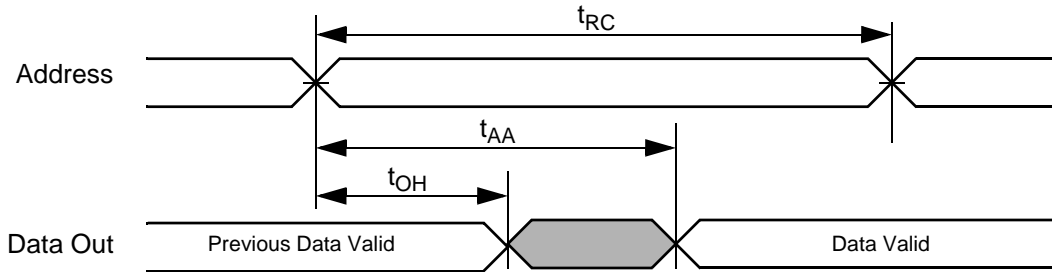
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	45	-	55	-	70	-	ns
Address access time	$t_{AA}$	-	45	-	55	-	70	ns
Chip select to output	$t_{CO1}, t_{CO2}$	-	45	-	55	-	70	ns
Output enable to valid output	$t_{OE}$	-	30	-	35	-	35	ns
Chip select to low-Z output	$t_{LZ1}, t_{LZ2}$	5	-	5	-	5	-	ns
Output enable to low-Z output	$t_{OLZ}$	5	-	5	-	5	-	ns
Chip disable to high-Z output	$t_{HZ1}, t_{HZ2}$	0	20	0	20	0	20	ns
Output disable to high-Z output	$t_{OHZ}$	0	20	0	20	0	20	ns
Output hold from address change	$t_{OH}$	10	-	10	-	10	-	ns

#### WRITE CYCLE ( $V_{CC}=2.7 \text{ to } 3.6\text{V}$ , $Gnd = 0\text{V}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

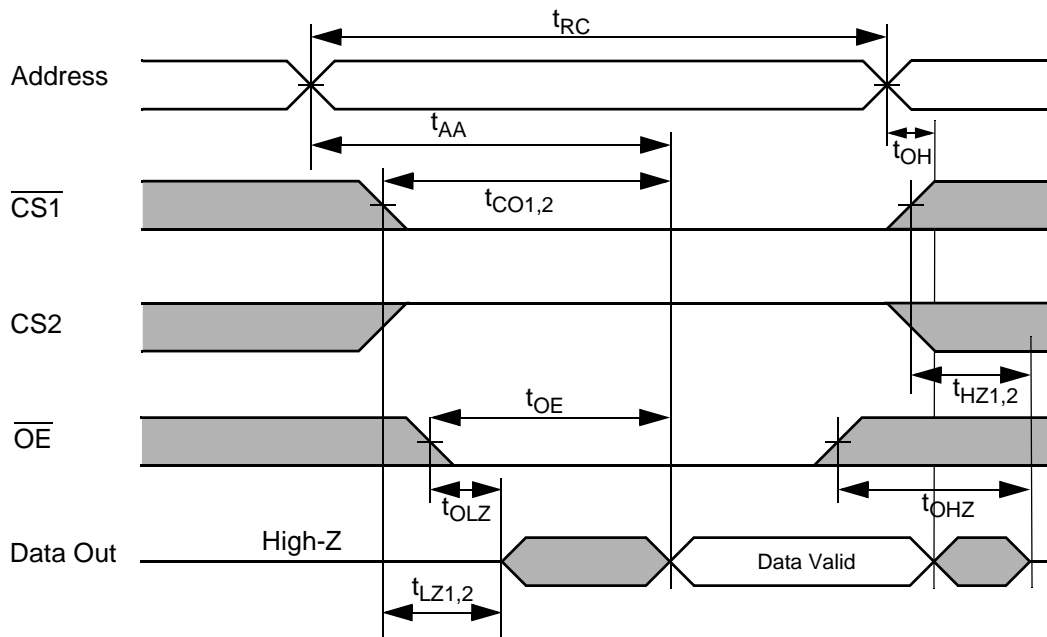
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	45	-	55	-	70	-	ns
Chip select to end of write	$t_{CW1}, t_{CW2}$	45	-	45	-	60	-	ns
Address setup time	$t_{AS}$	0	-	0	-	0	-	ns
Address valid to end of write	$t_{AW}$	45	-	45	-	60	-	ns
Write pulse width	$t_{WP}$	45	-	45	-	55	-	ns
Write recovery time	$t_{WR}$	0	-	0	-	0	-	ns
Write to output high-Z	$t_{WHZ}$	0	20	0	20	0	20	ns
Data to write time overlap	$t_{DW}$	25	-	30	-	30	-	ns
Data hold from write time	$t_{DH}$	0	-	0	-	0	-	ns
End write to output low-Z	$t_{OW}$	5	-	5	-	5	-	ns

## TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1).** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IL}$ )



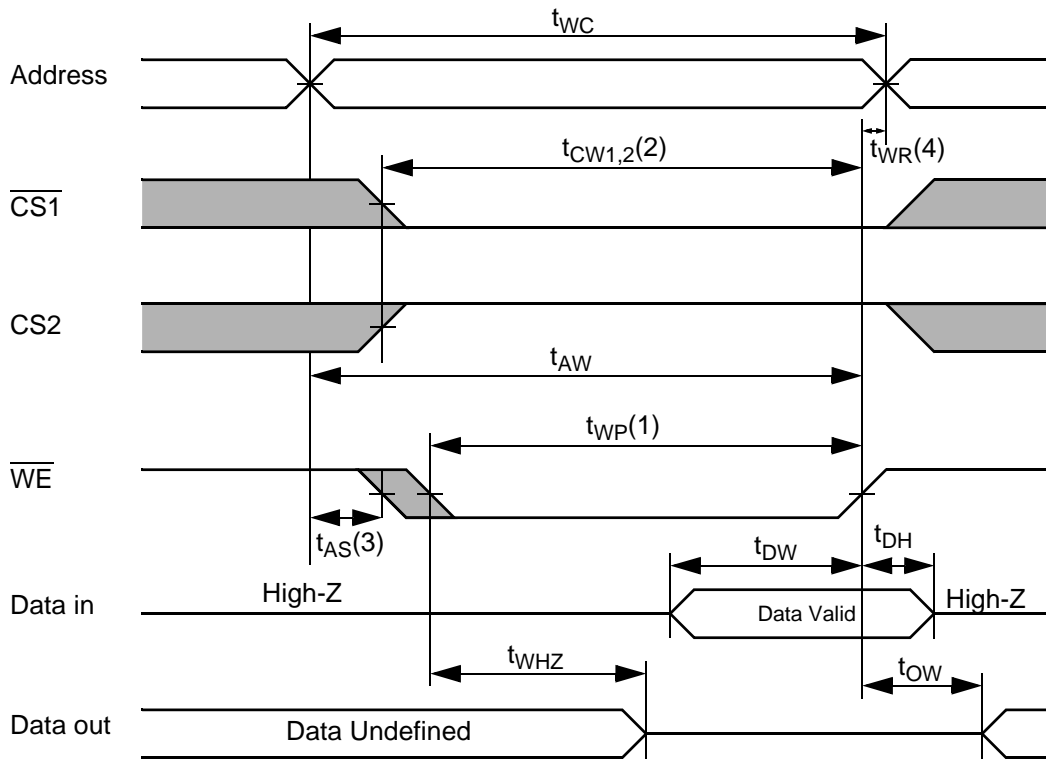
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



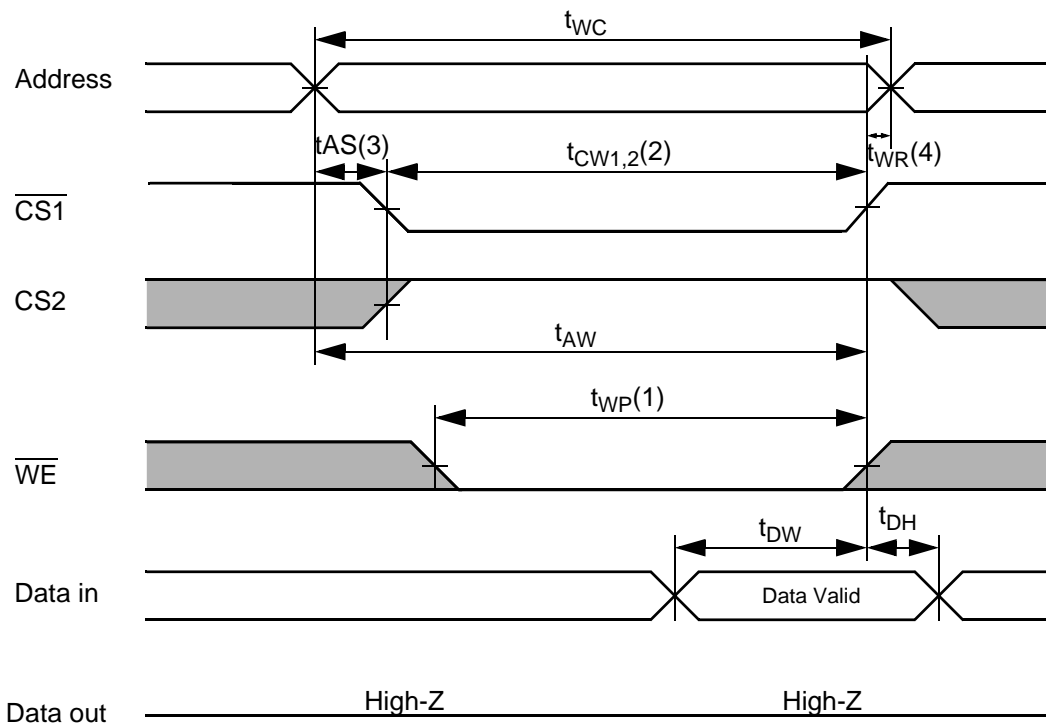
### NOTES (READ CYCLE)

1.  $t_{HZ1,2}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ1,2}(\text{Max.})$  is less than  $t_{LZ1,2}(\text{Min.})$  both for a given device and from device to device interconnection.

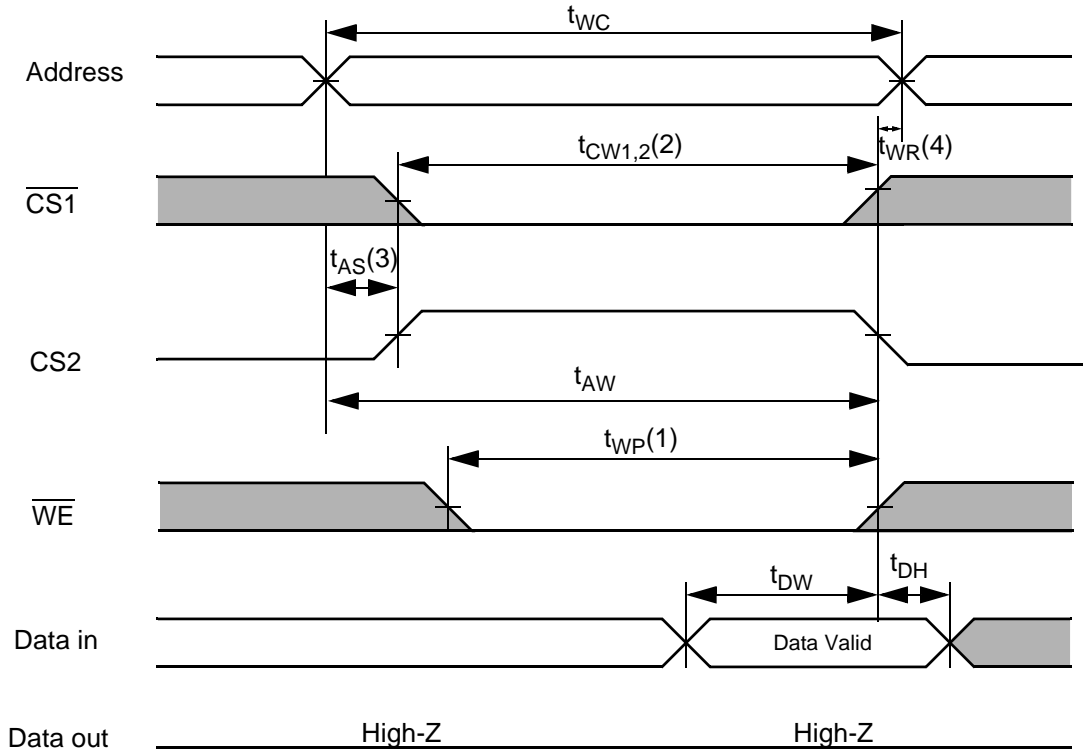
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  CONTROLLED)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  CONTROLLED)**



**TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 CONTROLLED)**



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS1}$ , a high CS2 and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  goes low, CS2 goes high and  $\overline{WE}$  goes low. A write ends at the earliest transition among  $\overline{CS1}$  goes high, CS2 goes low and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS1}$  going low or CS2 going high to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low.



**DATA RETENTION CHARACTERISTICS**

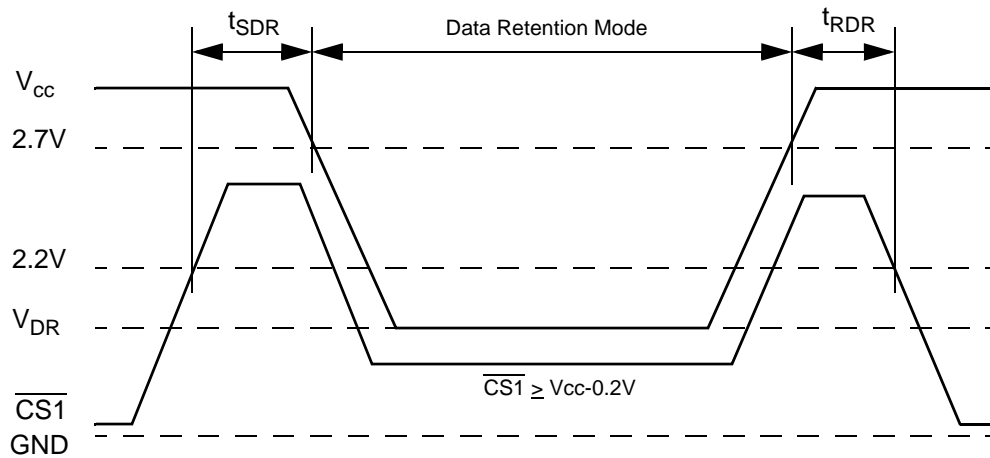
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CS1} \geq V_{CC}-0.2V$ <sup>1)</sup>	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V, $\overline{CS1} \geq V_{CC}-0.2V$ <sup>1)</sup>	-	-	4	uA
Chip Deselect to Data Retention Time	t <sub>SDR</sub>	See data retention wave form	0	-	-	ns
Operation Recovery Time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

**NOTES**

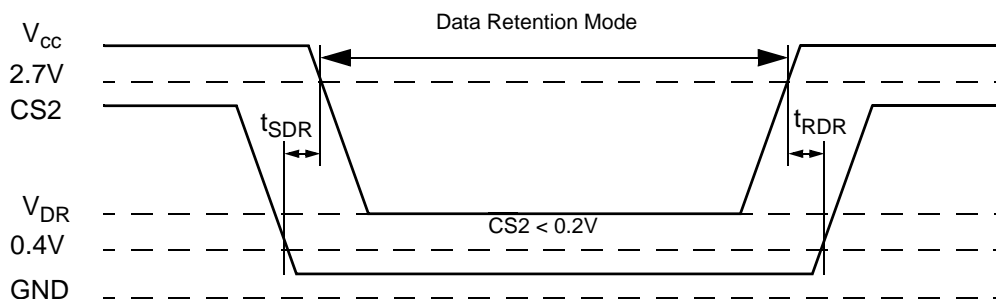
1.  $\overline{CS1} \geq V_{CC}-0.2V$  ,  $CS2 \geq V_{CC}-0.2V$  ( $\overline{CS1}$  controlled) or  $CS2 \leq 0.2V$  ( $CS2$  controlled)

**DATA RETENTION WAVE FORM**

**$\overline{CS1}$  Controlled**



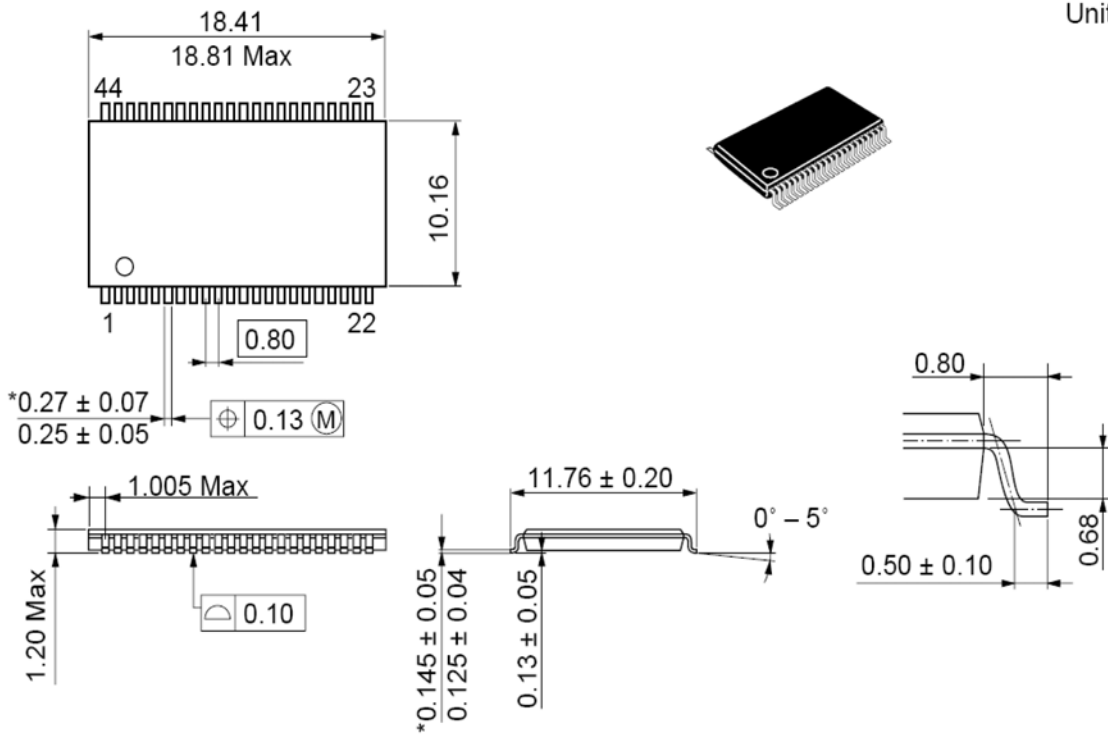
**CS2 Controlled**



**PACKAGE DIMENSION**

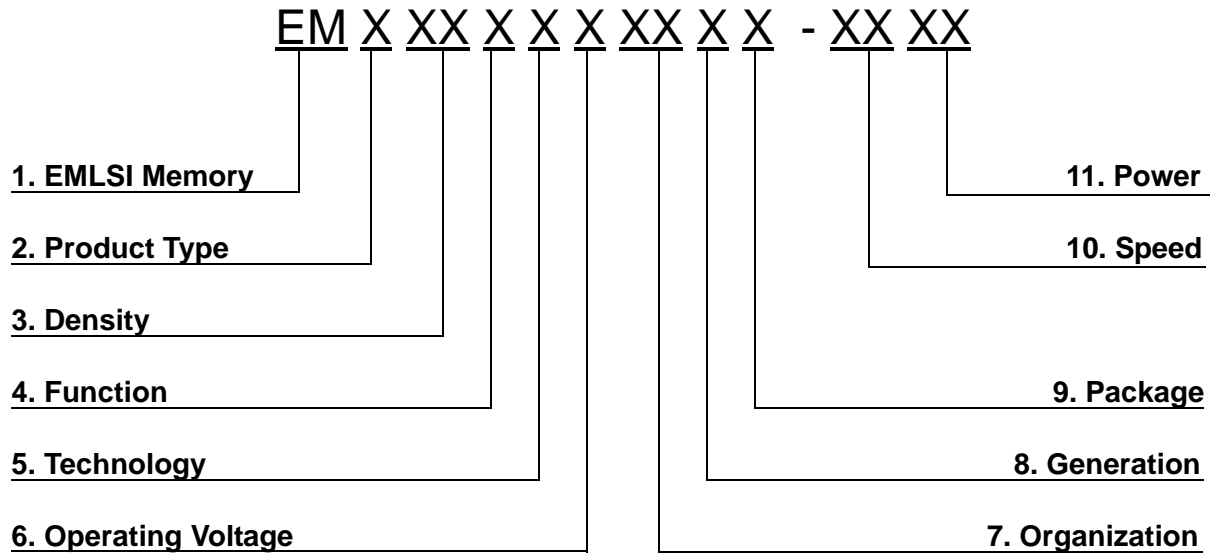
44 - TSOP2 (0.8mm pin pitch)

As of January, 2002  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

**SRAM PART CODING SYSTEM**



1. Memory Component  
EM ----- Memory

2. Product Type  
6 ----- SRAM

3. Density  
1 ----- 1M  
2 ----- 2M  
4 ----- 4M  
8 ----- 8M

4. Function  
0 ----- Dual CS  
1 ----- Single CS  
2 ----- Multiplexed  
3 ----- Single CS / LBB, UBB(tBA=tOE)  
4 ----- Single CS / LBB, UBB(tBA=tCO)  
5 ----- Dual CS / LBB, UBB(tBA=tOE)  
6 ----- Dual CS / LBB, UBB(tBA=tCO)

5. Technology  
F ----- Full CMOS

6. Operating Voltage  
T ----- 5.0V  
V ----- 3.3V  
U ----- 3.0V  
S ----- 2.5V  
R ----- 2.0V  
P ----- 1.8V

7. Organization  
8 ----- x8 bit  
16 ----- x16 bit

8. Generation  
Blank ----- 1st generation  
A ----- 2nd generation  
B ----- 3rd generation  
C ----- 4th generation  
D ----- 5th generation  
E ----- 6th generation  
F ----- 7th generation  
G ----- 8th generation

9. Package  
Blank ----- KGD, 48&36FpBGA  
S ----- 32 sTSOP1  
T ----- 32 TSOP1  
U ----- 44 TSOP2  
V ----- 32 SOP

10. Speed  
45 ----- 45ns  
55 ----- 55ns  
70 ----- 70ns  
85 ----- 85ns  
10 ----- 100ns  
12 ----- 120ns

11. Power  
LL ----- Low Low Power  
LF ----- Low Low Power(Pb-Free & Green)  
L ----- Low Power  
S ----- Standard Power