SBOS233E − MARCH 2002− REVISED MAY 2009

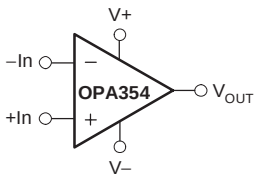
250MHz, Rail-to-Rail I/O, CMOS OPERATIONAL AMPLIFIERS

FEATURES

- UNITY-GAIN BANDWIDTH: 250MHz
- WIDE BANDWIDTH: 100MHz GBW
- HIGH SLEW RATE: 150V/μs
- LOW NOISE: 6.5nV/√Hz
- RAIL-TO-RAIL I/O
- HIGH OUTPUT CURRENT: > 100mA
- EXCELLENT VIDEO PERFORMANCE:
  Diff Gain: 0.02%, Diff Phase: 0.09°
  0.1dB Gain Flatness: 40MHz
- LOW INPUT BIAS CURRENT: 3pA
- QUIESCENT CURRENT: 4.9mA
- THERMAL SHUTDOWN
- SUPPLY RANGE: 2.5V to 5.5V
- *Micro*SIZE AND PowerPAD™ PACKAGES

APPLICATIONS

- VIDEO PROCESSING
- ULTRASOUND
- OPTICAL NETWORKING, TUNABLE LASERS
- PHOTODIODE TRANSIMPEDANCE AMPS
- ACTIVE FILTERS
- HIGH-SPEED INTEGRATORS
- ANALOG-TO-DIGITAL (A/D) CONVERTER INPUT BUFFERS
- DIGITAL-TO-ANALOG (D/A) CONVERTER OUTPUT AMPLIFIERS
- BARCODE SCANNERS
- COMMUNICATIONS



DESCRIPTION

The OPA354 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. They are unity-gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.09°. Quiescent current is only 4.9mA per channel.

The OPA354 series op amps are optimized for operation on single or dual supplies as low as 2.5V (±1.25V) and up to 5.5V (±2.75V). Common-mode input range extends beyond the supplies. The output swing is within 100mV of the rails, supporting wide dynamic range.

For applications requiring the full 100mA continuous output current, single and dual SO-8 PowerPAD versions are available.

The single version (OPA354), is available in the tiny SOT23-5 and SO-8 PowerPAD packages. The dual version (OPA2354) comes in the miniature MSOP-8 and SO-8 PowerPAD packages. The quad version (OPA4354) is offered in TSSOP-14 and SO-14 packages.

Multichannel versions feature completely independent circuitry for lowest crosstalk and freedom from interaction. All are specified over the extended −40°C to +125°C temperature range.

OPAx354 RELATED PRODUCTS

FEATURES	PRODUCT
Shutdown Version of OPA354 Family	**OPAx357**
200MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	OPAx355
200MHz GBW, Rail-to-Rail Output, CMOS	OPAx356
38MHz GBW, Rail-to-Rail Input/Output, CMOS	OPAx350/3
75MHz BW G = 2, Rail-to-Rail Output	OPAx631
150MHz BW G = 2, Rail-to-Rail Output	OPAx634
100MHz BW, Differential Input/Output, 3.3V Supply	THS412x

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V−	7.5V
Signal Input Terminals Voltage(2)	(V−) − (0.5V) to (V+) + (0.5V)
Current(2)	10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

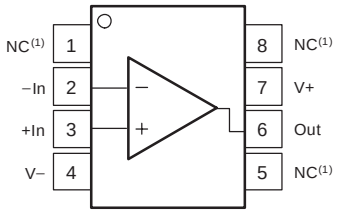
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA354	SO-8 PowerPAD	DDA	−40°C to +125°C	OPA354A	OPA354AIDDA	Rails, 97
〃	〃	〃	〃	〃	OPA354AIDDAR	Tape and Reel, 2500
OPA354	SOT23-5	DBV	−40°C to +125°C	OABI	OPA354AIDBVT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA354AIDBVR	Tape and Reel, 3000
OPA2354	SO-8 PowerPAD	DDA	−40°C to +125°C	OPA2354A	OPA2354AIDDA	Rails, 97
〃	〃	〃	〃	〃	OPA2354AIDDAR	Tape and Reel, 2500
OPA2354	MSOP-8	DGK	−40°C to +125°C	OACI	OPA2354AIDGKT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA2354AIDGKR	Tape and Reel, 2500
OPA4354	SO-14	D	−40°C to +125°C	OPA4354A	OPA4354AID	Rails, 58
〃	〃	〃	〃	〃	OPA4354AIDR	Tape and Reel, 2500
OPA4354	TSSOP-14	PW	−40°C to +125°C	OPA4354A	OPA4354AIPWT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA4354AIPWR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

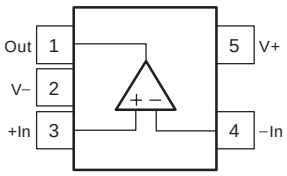
Top View

OPA354



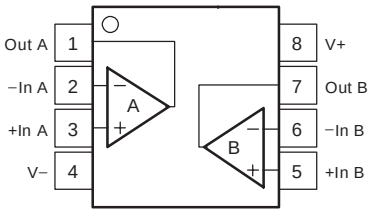
SO PowerPAD(2)

OPA354



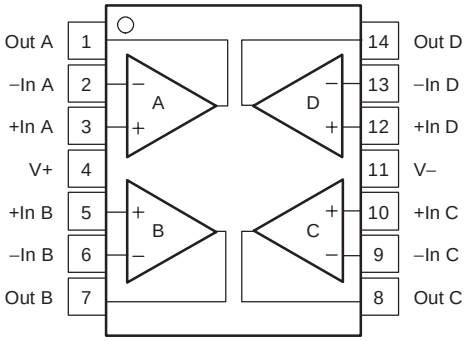
SOT23

OPA2354



SO PowerPAD(2)
MSOP

OPA4354



SO
TSSOP

NOTES: (1) NC means no internal connection. (2) PowerPAD should be connected to V− or left floating.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V Single-Supply

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C**.

At T_A = +25°C, R_F = 0Ω , R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA354AI, OPA2354AI, OPA4354AI MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V		±2	±8	mV
		Specified Temperature Range			**±10**	**mV**
vs Temperature	**dV_{OS}/dT**	**Specified Temperature Range**		**±4**		**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = (V_S/2) − 0.55V		±200	±800	µV/V
		Specified Temperature Range			**±900**	**µV/V**
INPUT BIAS CURRENT						
Input Bias Current	I_B			3	±50	pA
Input Offset Current	I_{OS}			±1	±50	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1MHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = +5.5V, −0.1V < V_{CM} < +3.5V	66	80		dB
		Specified Temperature Range	**64**			**dB**
		V_S = +5.5V, −0.1V < V_{CM} < +5.6V	56	68		dB
		Specified Temperature Range	**55**			**dB**
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 2		Ω || pF
OPEN-LOOP GAIN	A_{OL}	V_S = +5V, +0.3V < V_O < +4.7V	94	110		dB
Specified Temperature Range		**V_S = +5V, +0.4V < V_O < +4.6V**	**90**			**dB**
FREQUENCY RESPONSE						
Small-Signal Bandwidth	f_{-3dB}	G = +1, V_O = 100mV_{PP}, R_F = 25Ω		250		MHz
	f_{-3dB}	G = +2, V_O = 100mV_{PP}		90		MHz
Gain-Bandwidth Product	GBW	G = +10		100		MHz
Bandwidth for 0.1dB Gain Flatness	$f_{0.1dB}$	G = +2, V_O = 100mV_{PP}		40		MHz
Slew Rate	SR	V_S = +5V, G = +1, 4V Step		150		V/µs
		V_S = +5V, G = +1, 2V Step		130		V/µs
		V_S = +3V, G = +1, 2V Step		110		V/µs
Rise-and-Fall Time		G = +1, V_O = 200mV_{PP}, 10% to 90%		2		ns
		G = +1, V_O = 2V_{PP}, 10% to 90%		11		ns
Settling Time, 0.1%		V_S = +5V, G = +1, 2V Output Step		30		ns
0.01%				60		ns
Overload Recovery Time		V_{IN} • Gain = V_S		5		ns
Harmonic Distortion						
2nd-Harmonic		G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = 1.5V		−75		dBc
3rd-Harmonic		G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = 1.5V		−83		dBc
Differential Gain Error		NTSC, R_L = 150Ω		0.02		%
Differential Phase Error		NTSC, R_L = 150Ω		0.09		degrees
Channel-to-Channel Crosstalk						
OPA2354		f = 5MHz		−100		dB
OPA4354				−84		dB

(1) See typical characteristics *Output Voltage Swing vs Output Current*.
(2) Specified by design.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V Single-Supply (continued)

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C**.

At T_A = +25°C, R_F = 0Ω , R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

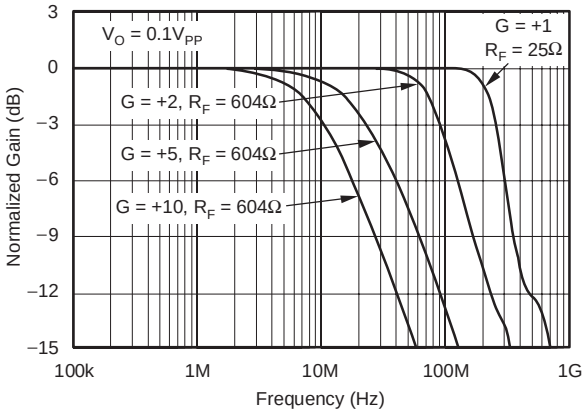
PARAMETER		CONDITIONS	OPA354AI OPA2354AI, OPA4354AI MIN	TYP	MAX	UNITS
OUTPUT						
Voltage Output Swing from Rail		V_S = +5V, R_L = 1kΩ, A_{OL} > 94dB		0.1	0.3	V
Specified Temperature Range		**V_S = +5V, R_L = 1kΩ, A_{OL} > 90dB**			**0.4**	**V**
Output Current(1)(2), Single, Dual, Quad	I_O	V_S = +5V	100			mA
		V_S = +3V		50		mA
Closed-Loop Output Impedance		f < 100kHz		0.05		Ω
Open-Loop Output Resistance	R_O			35		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.5 to 5.5		V
Quiescent Current (per amplifier)	I_Q	V_S = +5V, Enabled, I_O = 0		4.9	6	mA
		Specified Temperature Range			**7.5**	**mA**
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				+160		°C
Reset from Shutdown				+140		°C
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−55		+150	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
SOT23-5, MSOP-8				150		°C/W
TSSOP-14				100		°C/W
SO-14				100		°C/W
SO-8 PowerPAD				65		°C/W

(1) See typical characteristics *Output Voltage Swing vs Output Current*.
(2) Specified by design.

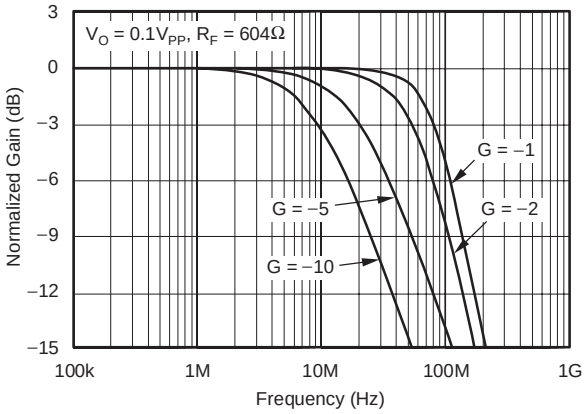
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

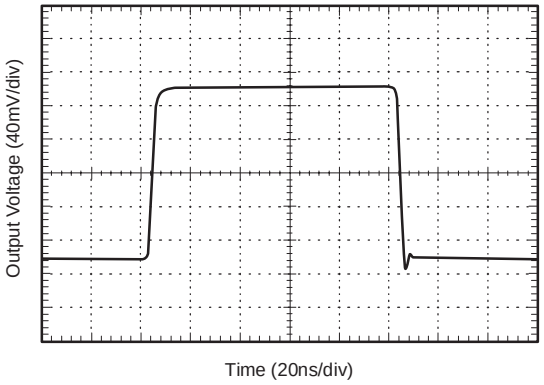
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



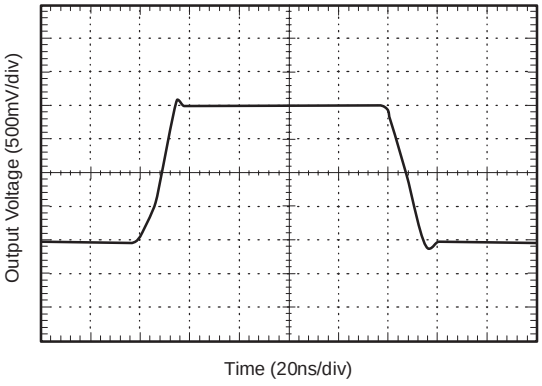
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



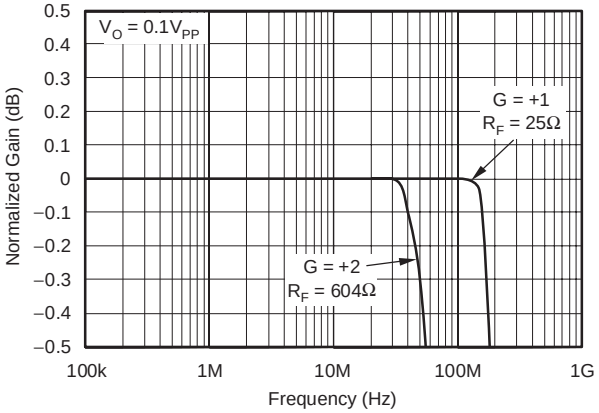
NONINVERTING SMALL−SIGNAL STEP RESPONSE



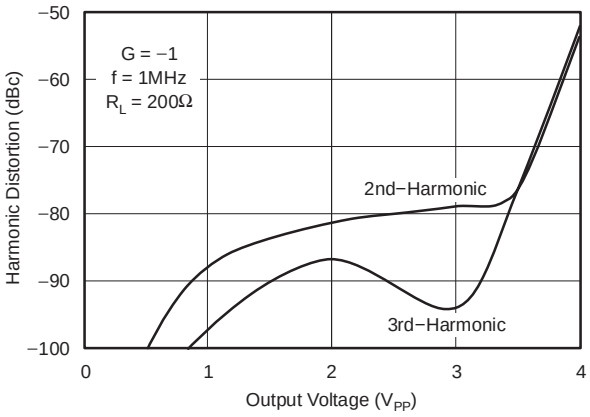
NONINVERTING LARGE−SIGNAL STEP RESPONSE



0.1dB GAIN FLATNESS



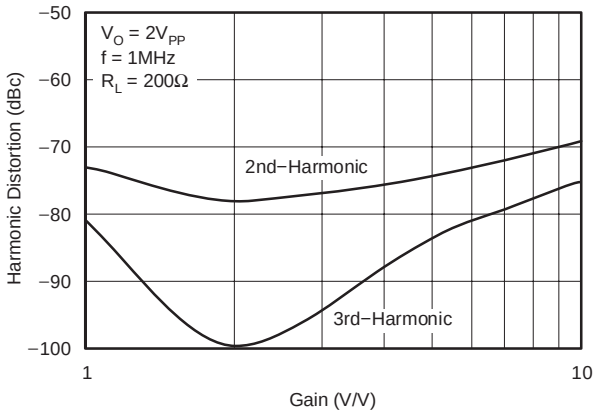
HARMONIC DISTORTION vs OUTPUT VOLTAGE



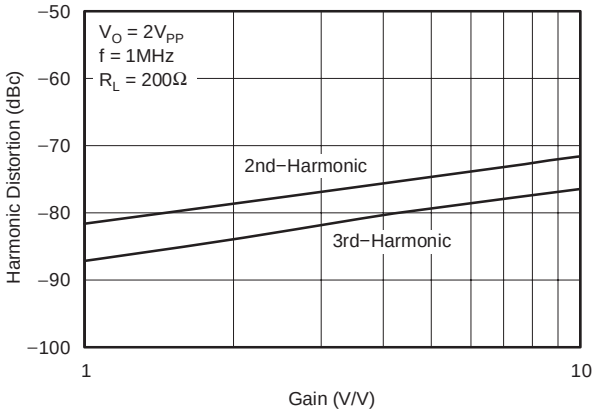
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

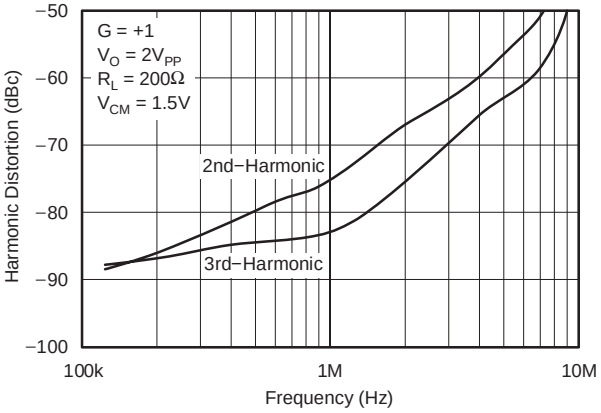
HARMONIC DISTORTION vs NONINVERTING GAIN



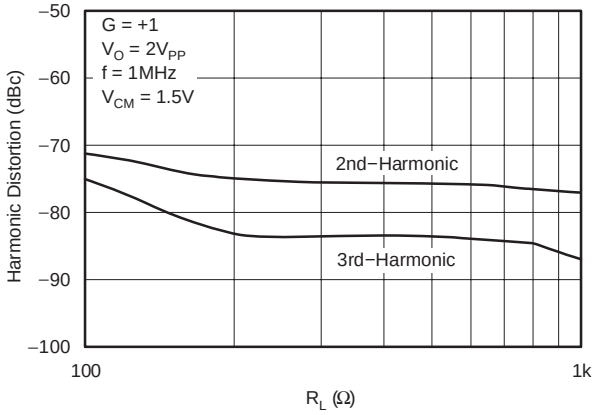
HARMONIC DISTORTION vs INVERTING GAIN



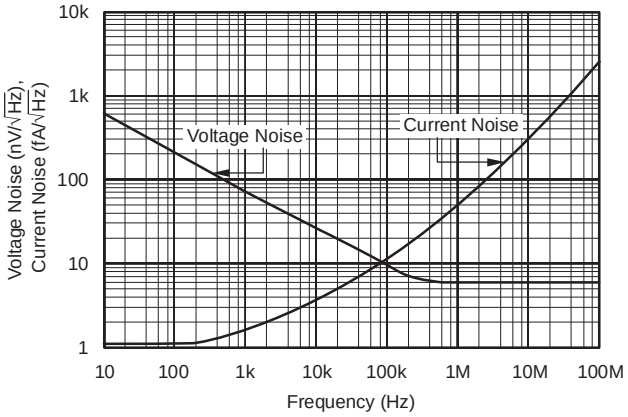
HARMONIC DISTORTION vs FREQUENCY



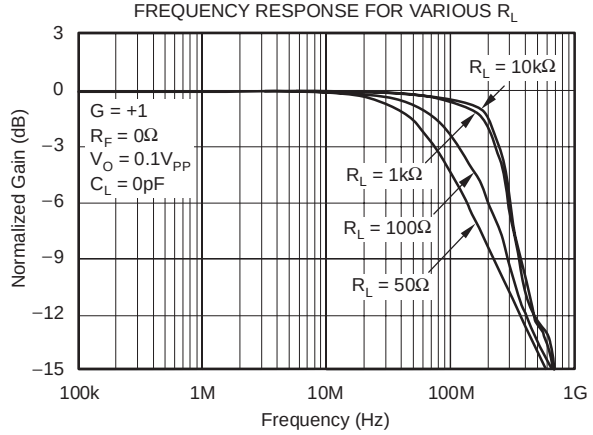
HARMONIC DISTORTION vs LOAD RESISTANCE



INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



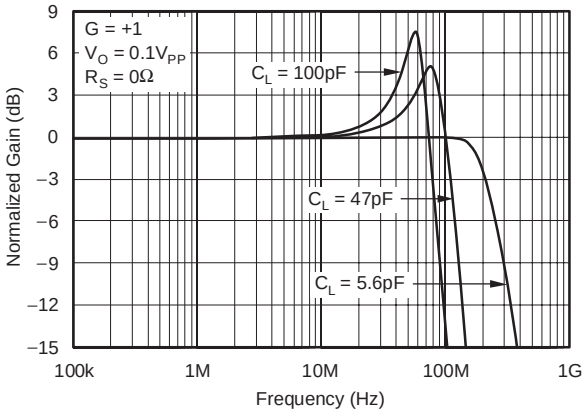
FREQUENCY RESPONSE FOR VARIOUS R_L



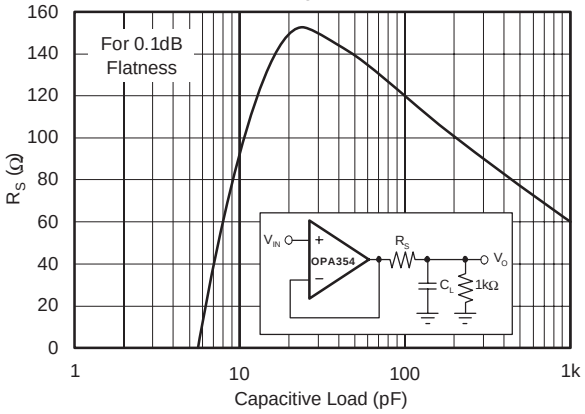
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

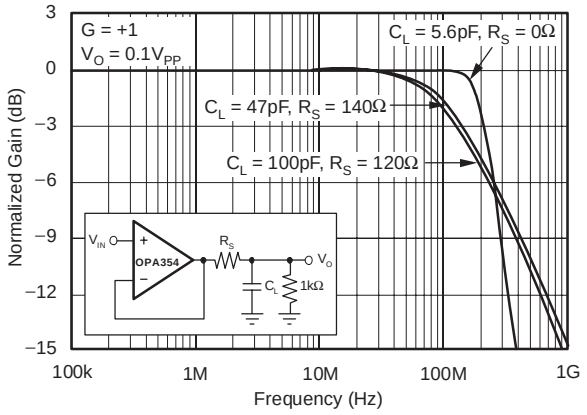
FREQUENCY RESPONSE FOR VARIOUS C_L



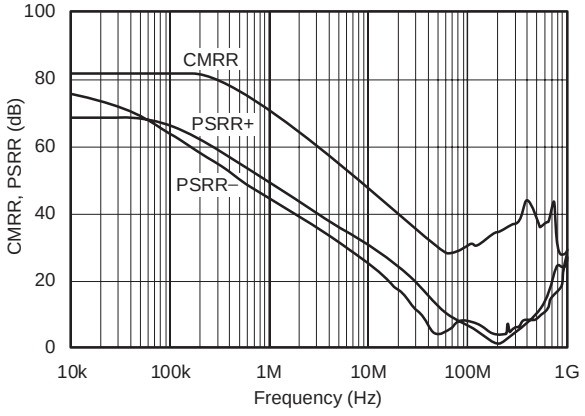
RECOMMENDED R_S vs CAPACITIVE LOAD



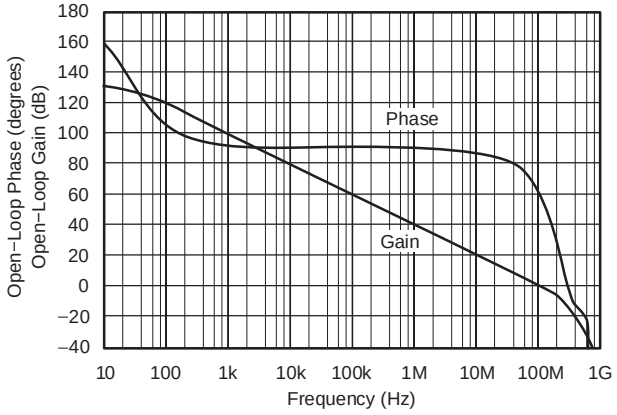
FREQUENCY RESPONSE vs CAPACITIVE LOAD



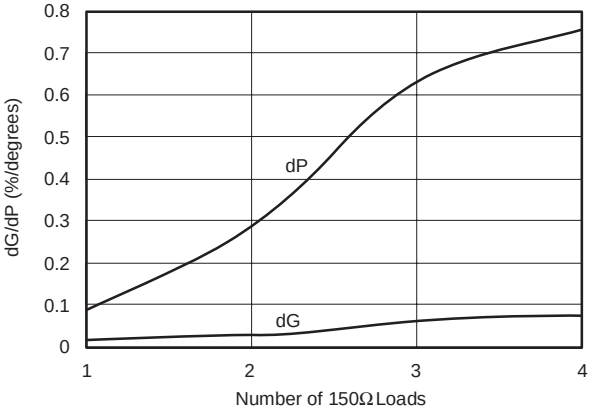
COMMON−MODE REJECTION RATIO AND
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



OPEN−LOOP GAIN AND PHASE



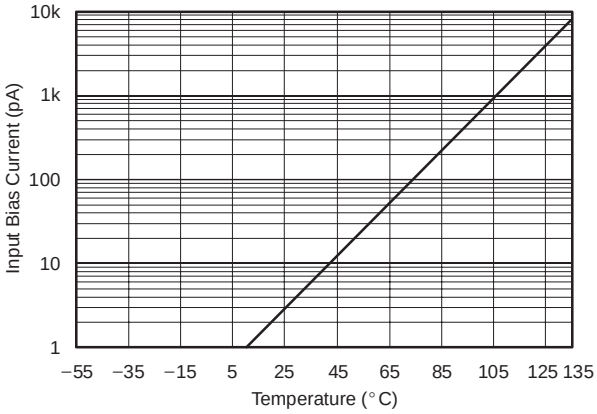
COMPOSITE VIDEO
DIFFERENTIAL GAIN AND PHASE



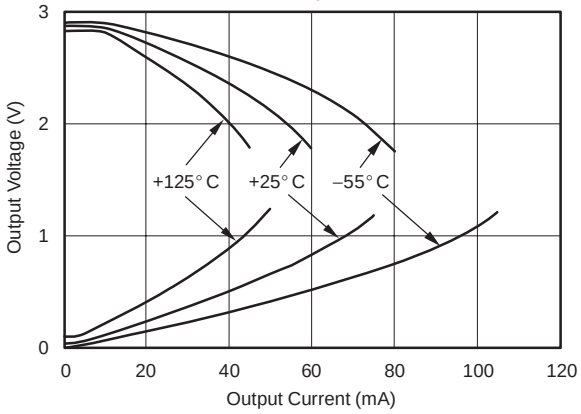
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

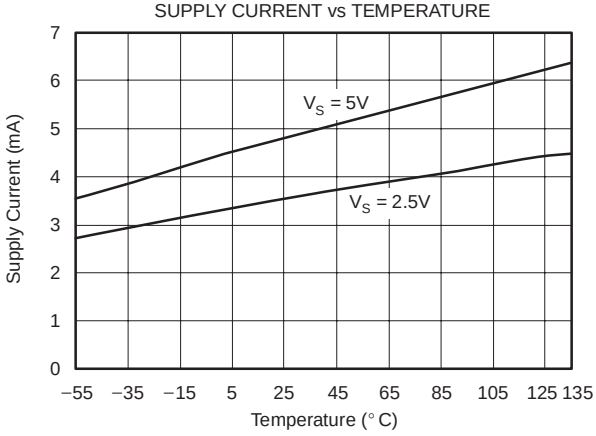
INPUT BIAS CURRENT vs TEMPERATURE



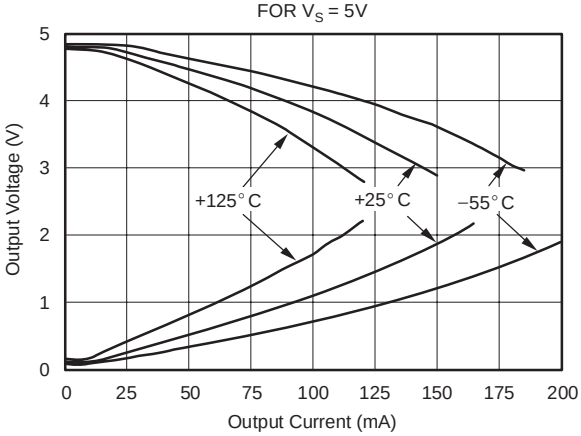
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT FOR V_S = 3V



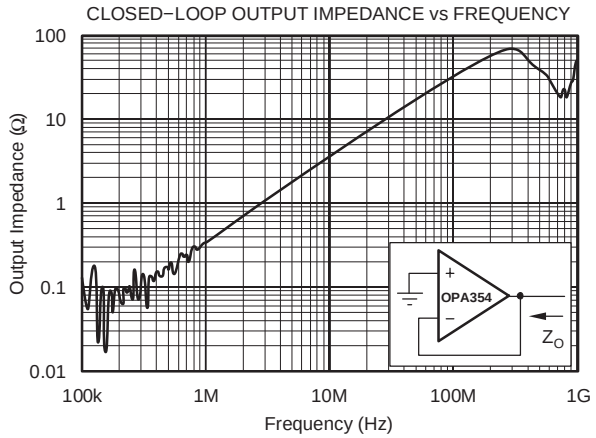
SUPPLY CURRENT vs TEMPERATURE



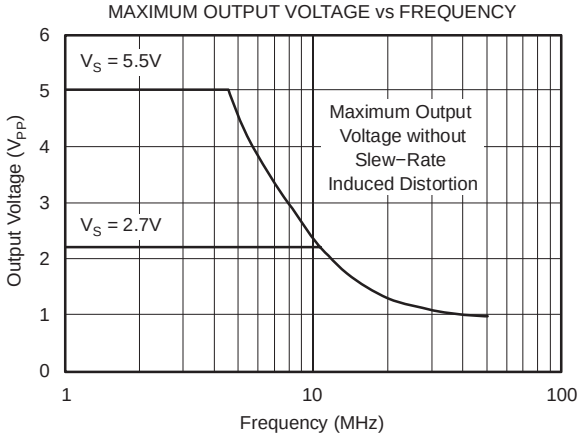
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT FOR V_S = 5V



CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



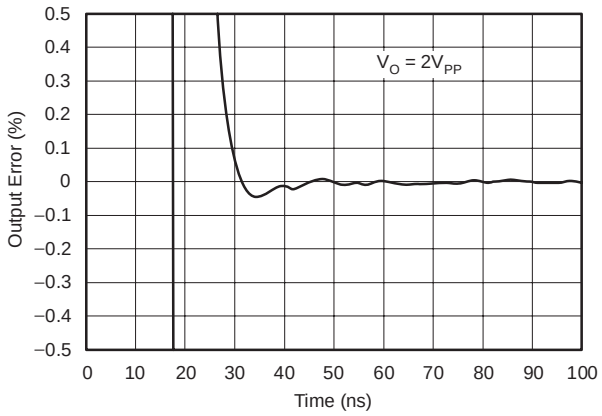
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



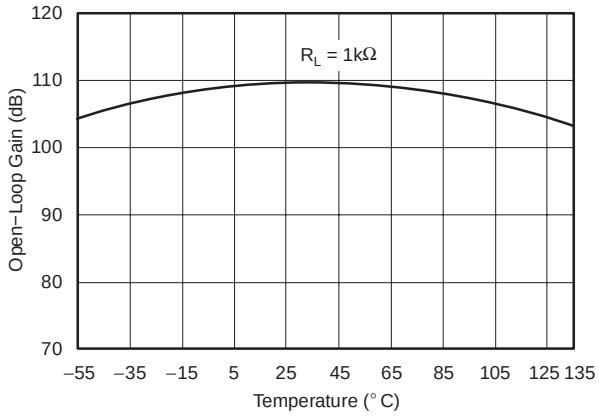
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

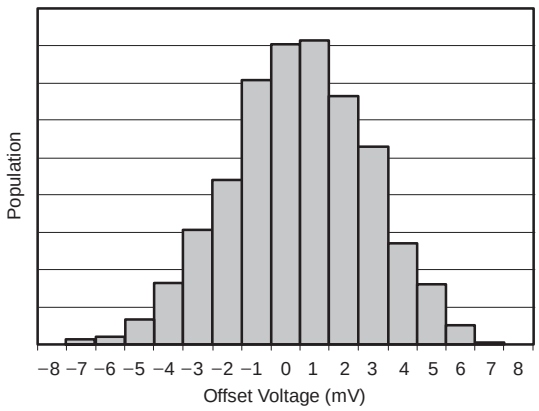
OUTPUT SETTLING TIME TO 0.1%



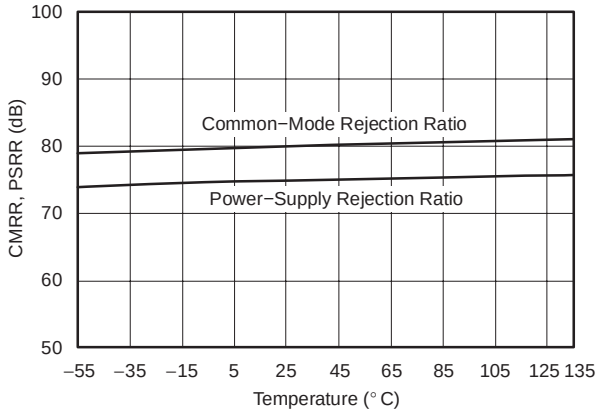
OPEN−LOOP GAIN vs TEMPERATURE



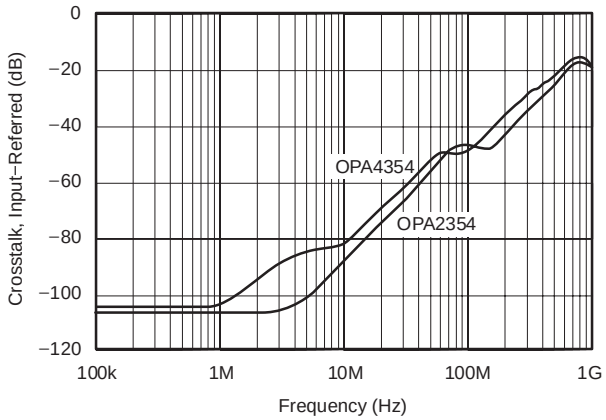
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



COMMON−MODE REJECTION RATIO AND
POWER−SUPPLY REJECTION RATIO vs TEMPERATURE



CHANNEL−TO−CHANNEL CROSSTALK



APPLICATIONS INFORMATION

The OPA354 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. It is available as a single, dual, or quad op amp.

The amplifier features a 100MHz gain bandwidth, and 150V/μs slew rate, but it is unity-gain stable and can be operated as a +1V/V voltage follower.

OPERATING VOLTAGE

The OPA354 is specified over a power-supply range of +2.7V to +5.5V (±1.35V to ±2.75V). However, the supply voltage may range from +2.5V to +5.5V (±1.25V to ±2.75V). Supply voltages higher than 7.5V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the typical characteristics section of this data sheet.

RAIL-TO-RAIL INPUT

The specified input common-mode voltage range of the OPA354 extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 1. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) − 1.2V. There is a small transition region, typically (V+) − 1.5V to (V+) − 0.9V, in which both pairs are on. This 600mV transition region can vary ±500mV with process variation. Thus, the transition region (both input stages on) can range from (V+) − 2.0V to (V+) − 1.5V on the low end, up to (V+) − 0.9V to (V+) − 0.4V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200Ω), the output voltage swing is typically 100mV from the supply rails. With 10Ω loads, a useful output swing can be achieved while maintaining high open-loop gain. See the typical characteristic curve *Output Voltage Swing vs Output Current*.

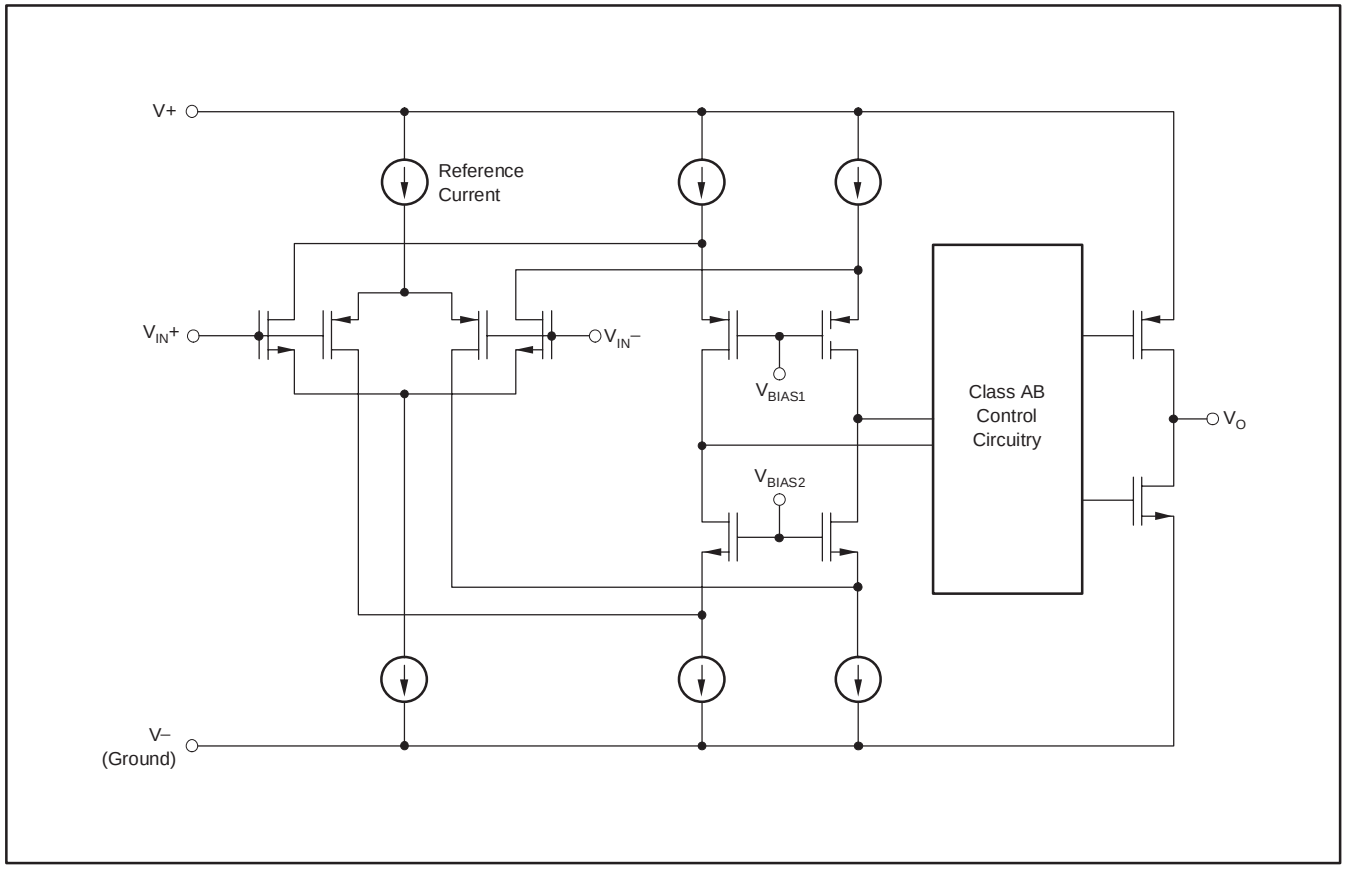


Figure 1. Simplified Schematic

OUTPUT DRIVE

The OPA354's output stage can supply a continuous output current of ±100mA and still provide approximately 2.7V of output swing on a 5V supply, as shown in Figure 2. For maximum reliability, it is not recommended to run a continuous DC current in excess of ±100mA. Refer to the typical characteristic curve *Output Voltage Swing vs Output Current*. For supplying continuous output currents greater than ±100mA, the OPA354 may be operated in parallel, as shown in Figure 3.

The OPA354 will provide peak currents up to 200mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA354 from dangerously high junction temperatures. At 160°C, the protection circuit will shut down the amplifier. Normal operation will resume when the junction temperature cools to below 140°C.

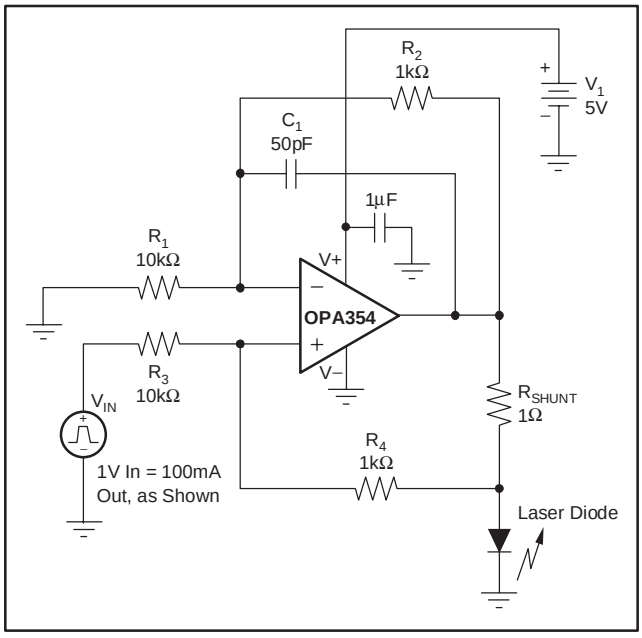


Figure 2. Laser Diode Driver

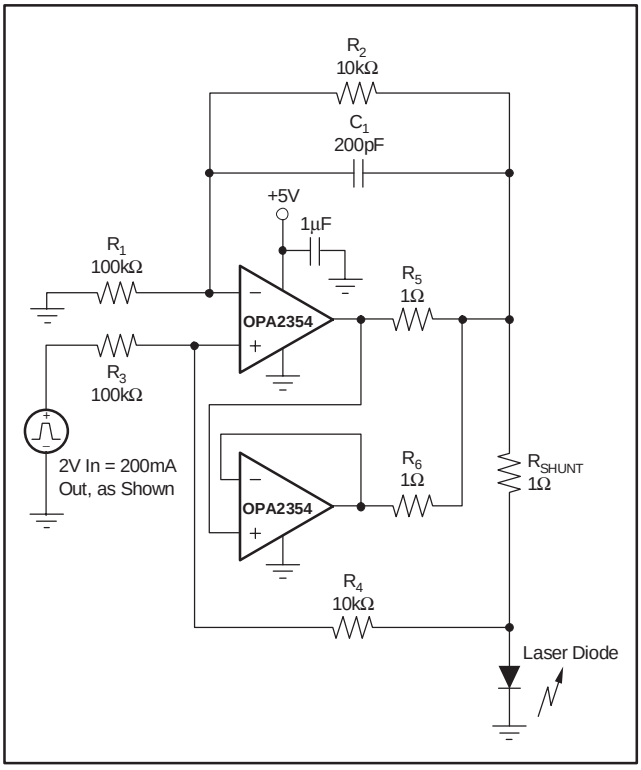


Figure 3. Parallel Operation

VIDEO

The OPA354 output stage is capable of driving standard back-terminated 75Ω video cables, as shown in Figure 4. By back-terminating a transmission line, it does not exhibit a capacitive load to its driver. A properly back-terminated 75Ω cable does not appear as capacitance; it presents only a 150Ω resistive load to the OPA354 output.

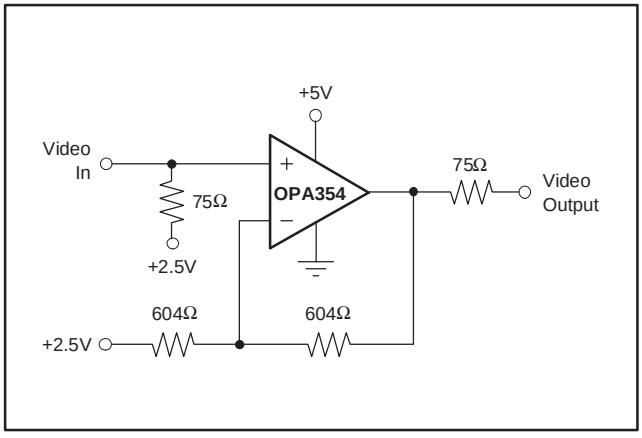


Figure 4. Single-Supply Video Line Driver

The OPA354 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 5.

DRIVING ANALOG-TO-DIGITAL CONVERTERS

The OPA354 series op amps offer 60ns of settling time to 0.01%, making them a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPA354 series provide an effective means of buffering the A/D converter's input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the OPA350 series is recommended.

Figure 6 illustrates the OPA354 driving an A/D converter. With the OPA354 in an inverting configuration, a capacitor across the feedback resistor can be used to filter high-frequency noise in the signal.

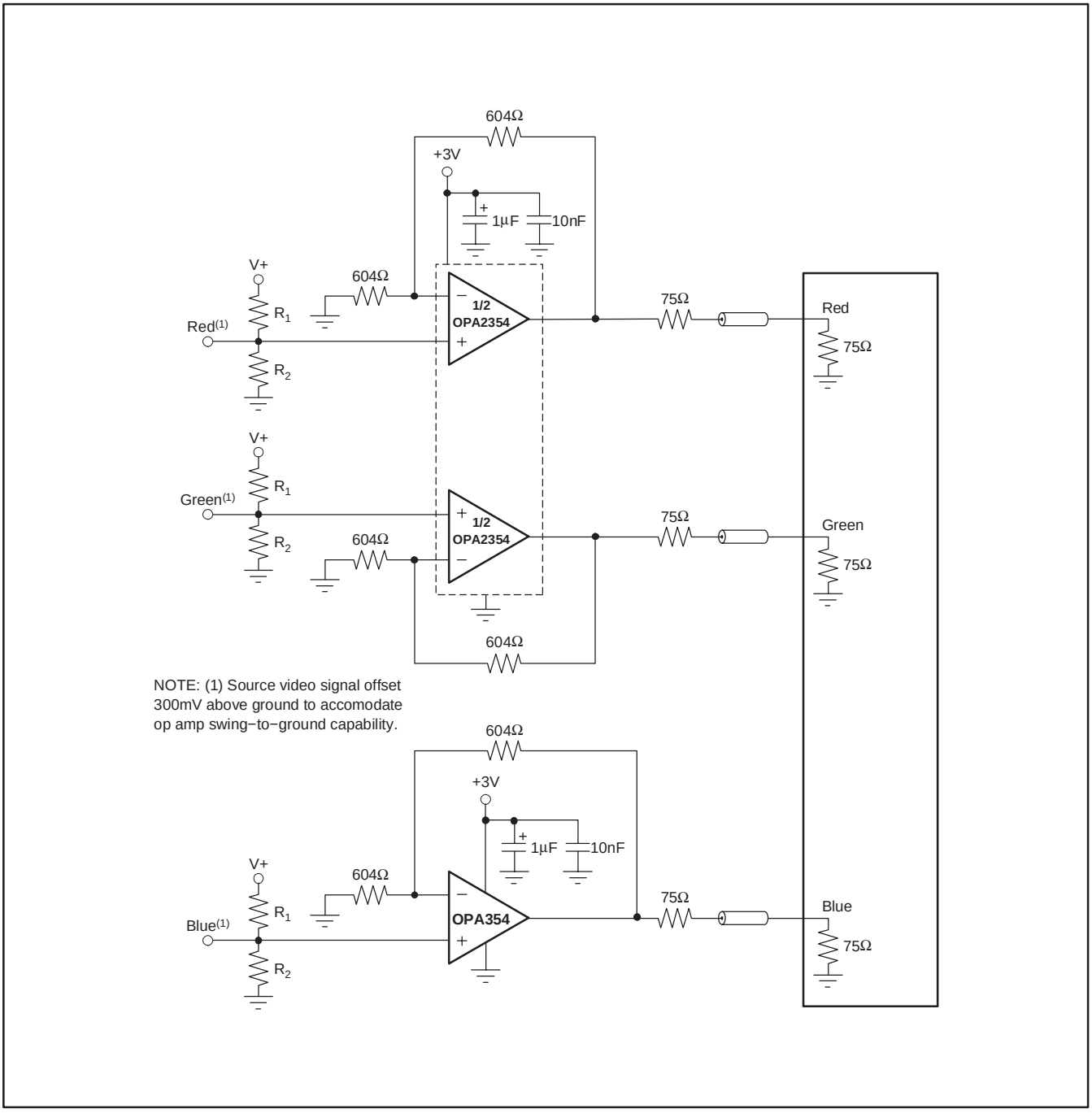


Figure 5. RGB Cable Driver

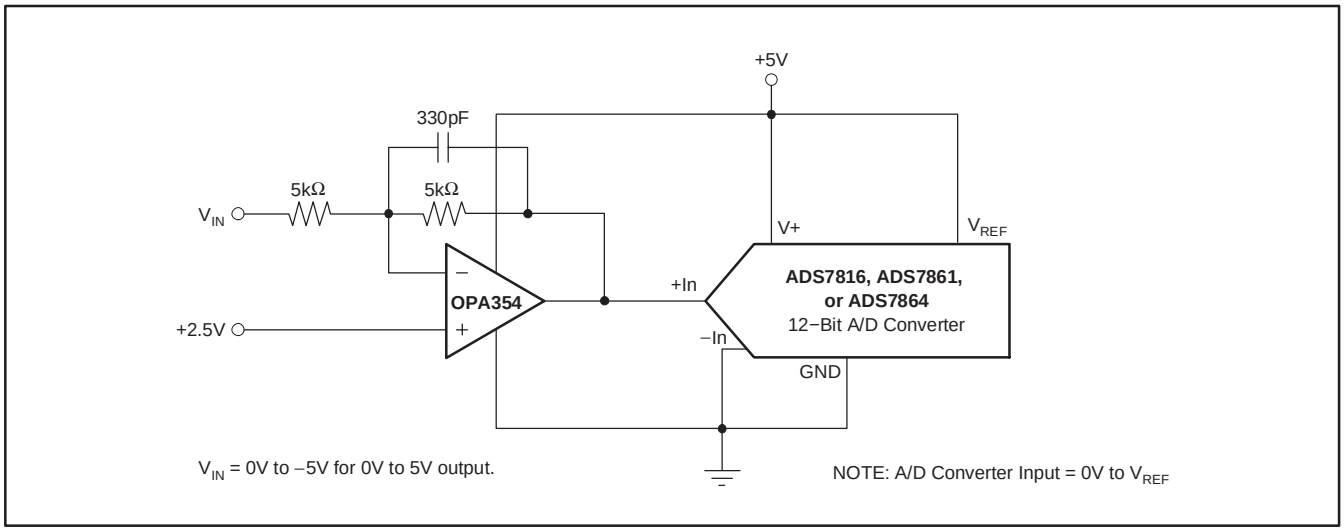


Figure 6. The OPA354 in Inverting Configuration Driving the ADS7816

CAPACITIVE LOAD AND STABILITY

The OPA354 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the op amp's output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. Refer to the typical characteristic curve *Frequency Response for Various C_L* for details.

The OPA354's topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. Refer to the typical characteristic curve *Recommended R_S vs Capacitive Load* and *Frequency Response vs Capacitive Load* for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor in series with the output, as shown in Figure 7. This significantly reduces ringing with large capacitive loads—see the typical characteristic curve *Frequency Response vs Capacitive Load*. However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10kΩ and R_S = 20Ω, there is only about a 0.2% error at the output.

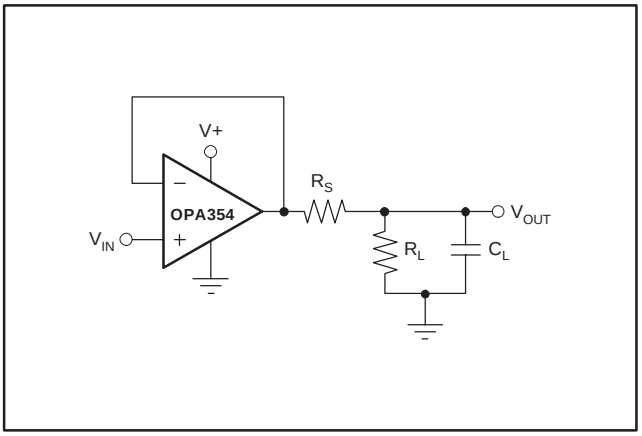


Figure 7. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

WIDEBAND TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA354 an ideal wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 8, are the expected diode capacitance (including the parasitic input common-mode and differential-mode input capacitance (2 + 2)pF for the OPA354), the desired transimpedance gain (R_F), and the Gain-Bandwidth Product (GBW) for the OPA354 (100MHz). With these 3 variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

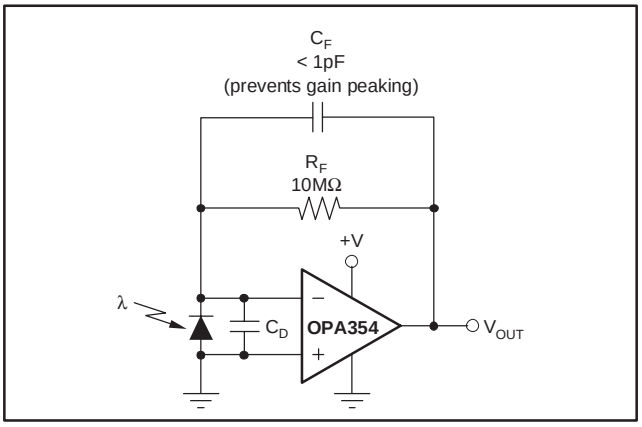


Figure 8. Transimpedance Amplifier

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of around 0.2pF that must be deducted from the calculated feedback capacitance value.

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} Hz \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200MHz GBW) or the OPA655 (400MHz GBW) may be used.

PCB LAYOUT

Good high-frequency printed circuit board (PCB) layout techniques should be employed for the OPA354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin will assure clean, stable operation. Large areas of copper also provides a means of dissipating heat that is generated in normal operation.

Sockets are definitely not recommended for use with any high-speed amplifier.

A 10nF ceramic bypass capacitor is the minimum recommended value; adding a 1μF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

POWER DISSIPATION

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application Bulletin AB-039 (SBOA022), *Power Amplifier Stress and Power Handling Limitations*, explains how to calculate or measure power dissipation with unusual signals and loads, and can be found at www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application.

PowerPAD THERMALLY ENHANCED PACKAGE

Besides the regular SOT23-5 and MSOP-8, the single and dual versions of the OPA354 also come in SO-8 PowerPAD. The SO-8 PowerPAD is a standard-size SO-8 package where the exposed leadframe on the bottom of the package can be soldered directly to the PCB to create an extremely low thermal resistance. This will enhance the OPA354's power dissipation capability significantly and eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques. NOTE: Since the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in Figure 9. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

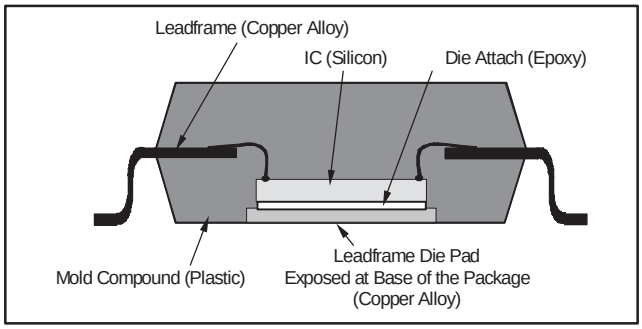


Figure 9. Section View of a PowerPAD Package

PowerPAD ASSEMBLY PROCESS

1. The PowerPAD must be connected to the device's most negative supply voltage, which will be ground in single-supply applications, and V− in split-supply applications.

2. Prepare the PCB with a top-side etch pattern, as shown in Figure 10. The exact land design may vary based on the specific assembly process requirements. There should be etch for the leads as well as etch for the thermal land.

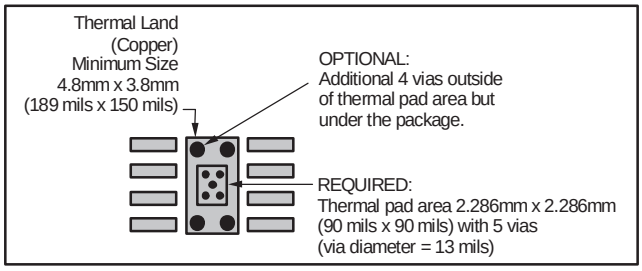


Figure 10. 8-Pin PowerPAD PCB Etch and Via Pattern

3. Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is 5, as shown in Figure 10.

4. It is recommended, but not required, to place a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This is illustrated in Figure 10.

5. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V− for split-supply applications.

6. When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in Figure 11. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

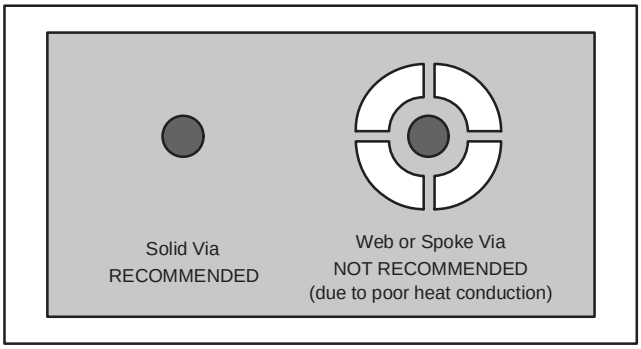


Figure 11. Via Connection

7. The top-side solder mask should leave the pad connections and the thermal pad area exposed. The thermal pad area should leave the 13 mil holes exposed. The larger holes outside the thermal pad area may be covered with solder mask.

8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

9. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, please see Technical Brief SLMA002, *PowerPAD Thermally Enhanced Package*, located at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDARG3	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA2354AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA2354AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA2354AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA354AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA4354AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples
OPA4354AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4354AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples
OPA4354AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples
OPA4354AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples
OPA4354AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples
OPA4354AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples
OPA4354AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

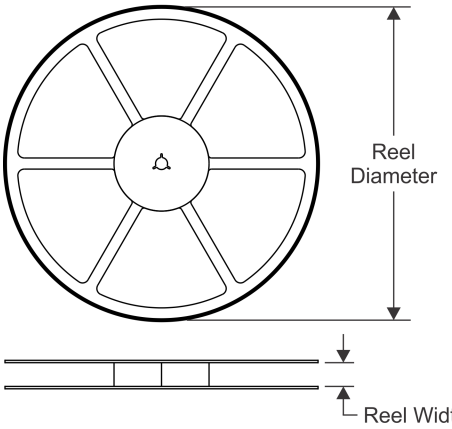
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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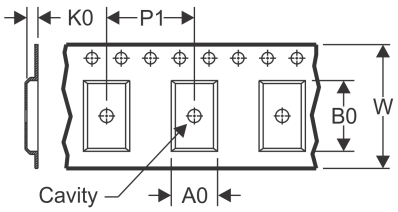
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

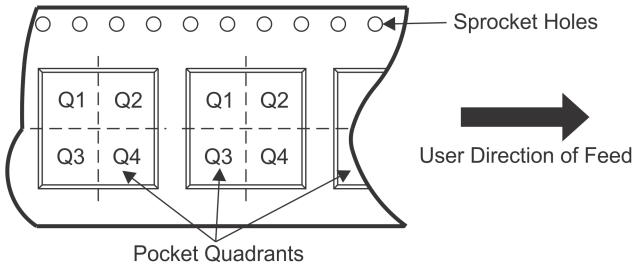


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

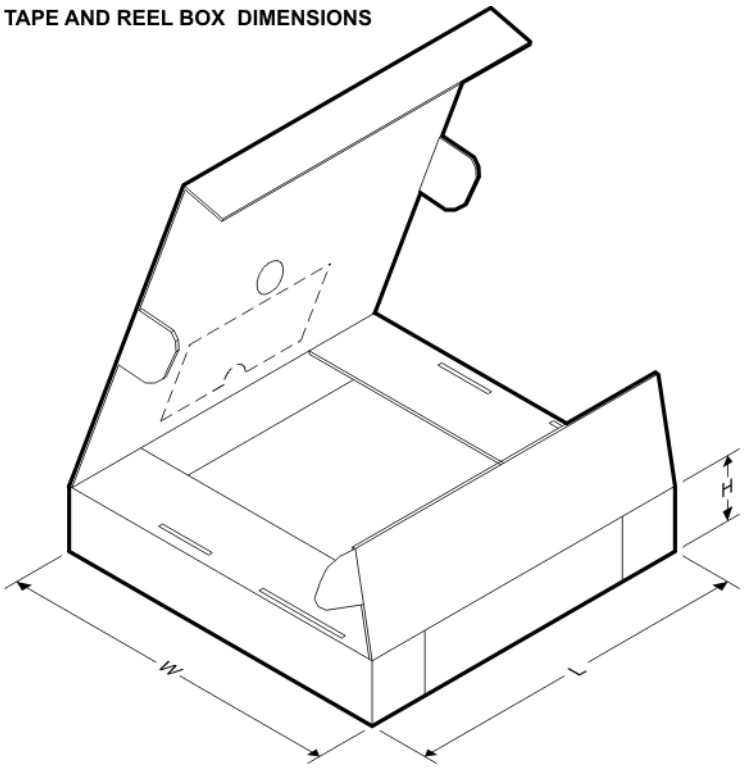
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA354AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA354AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4354AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4354AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

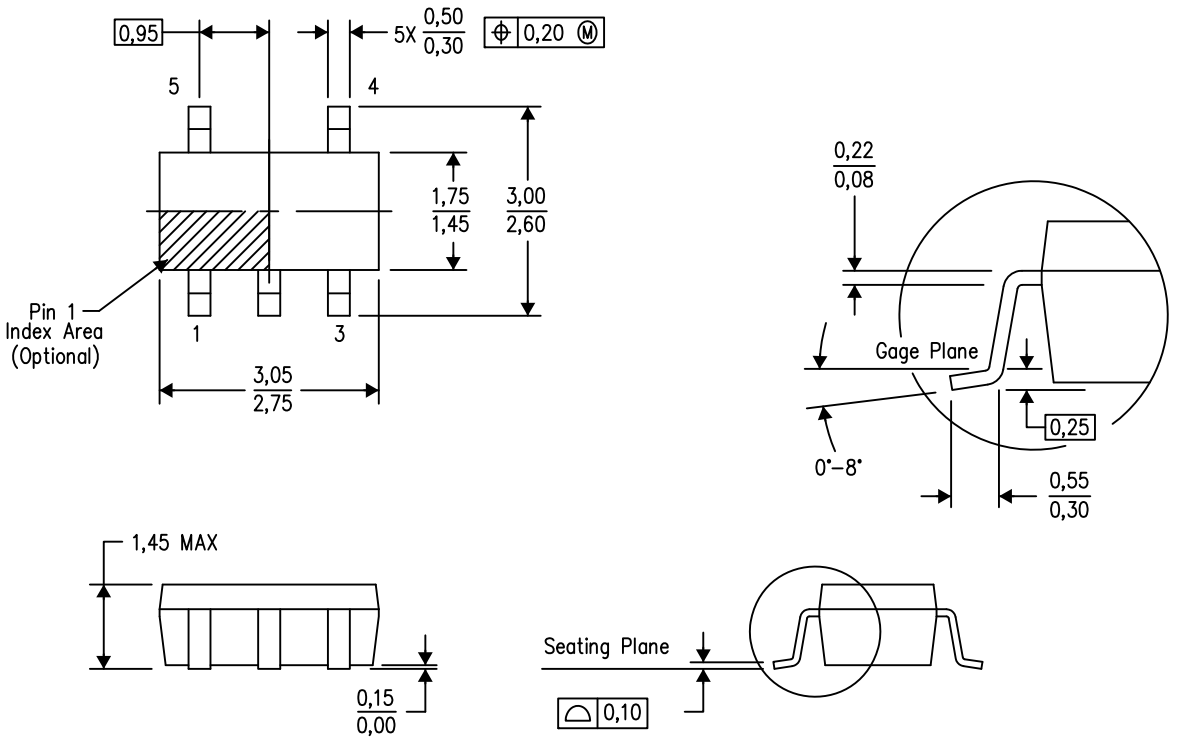
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA354AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA354AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA4354AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4354AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4354AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

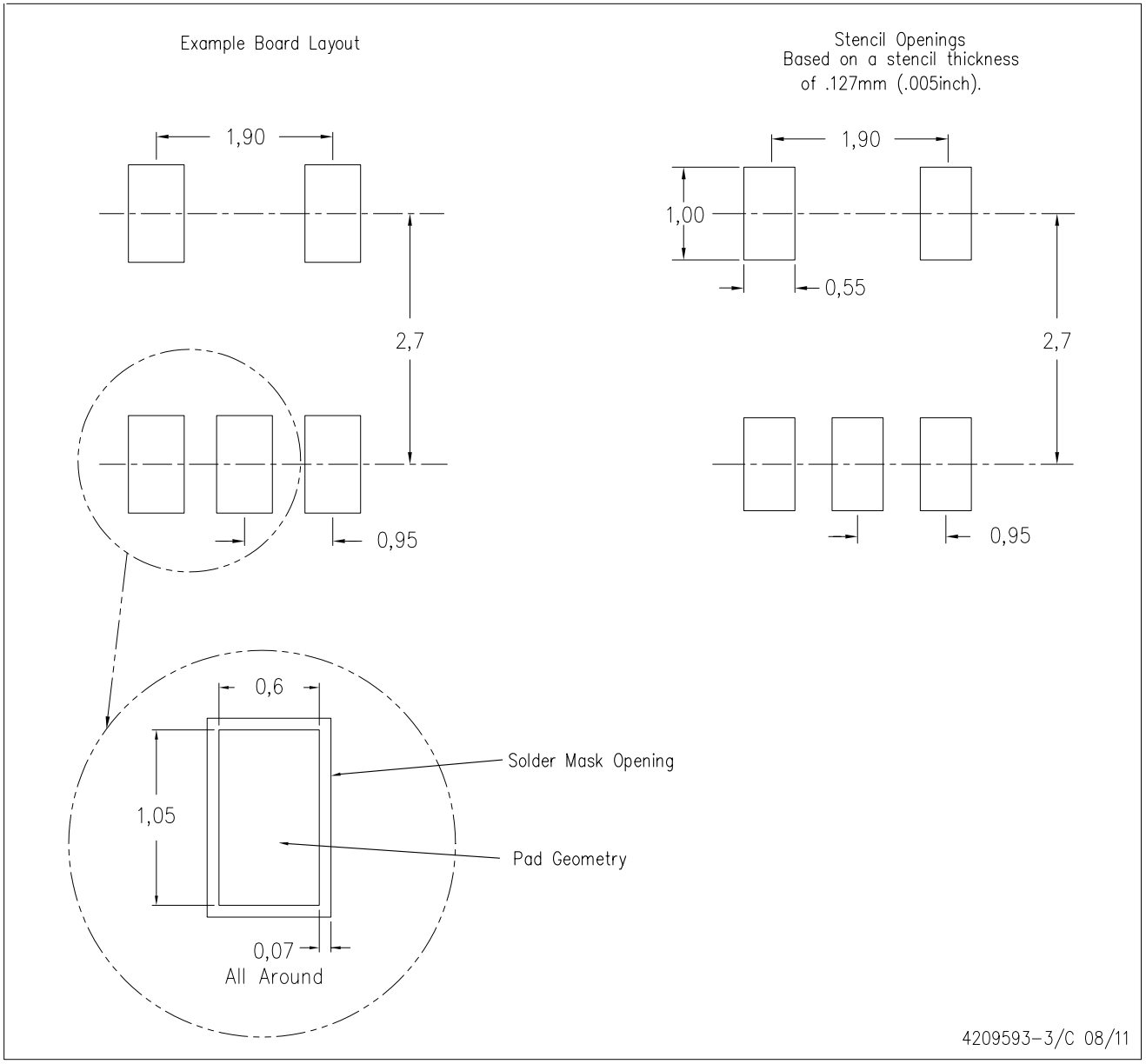
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

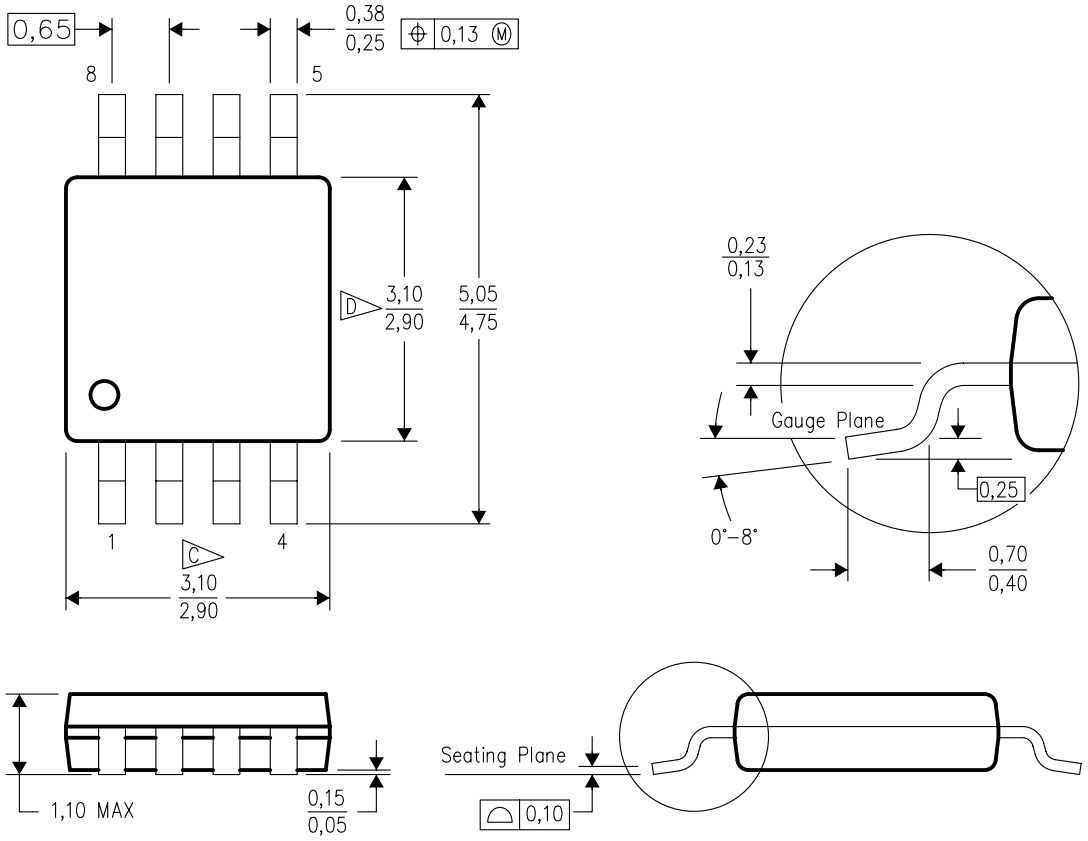
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

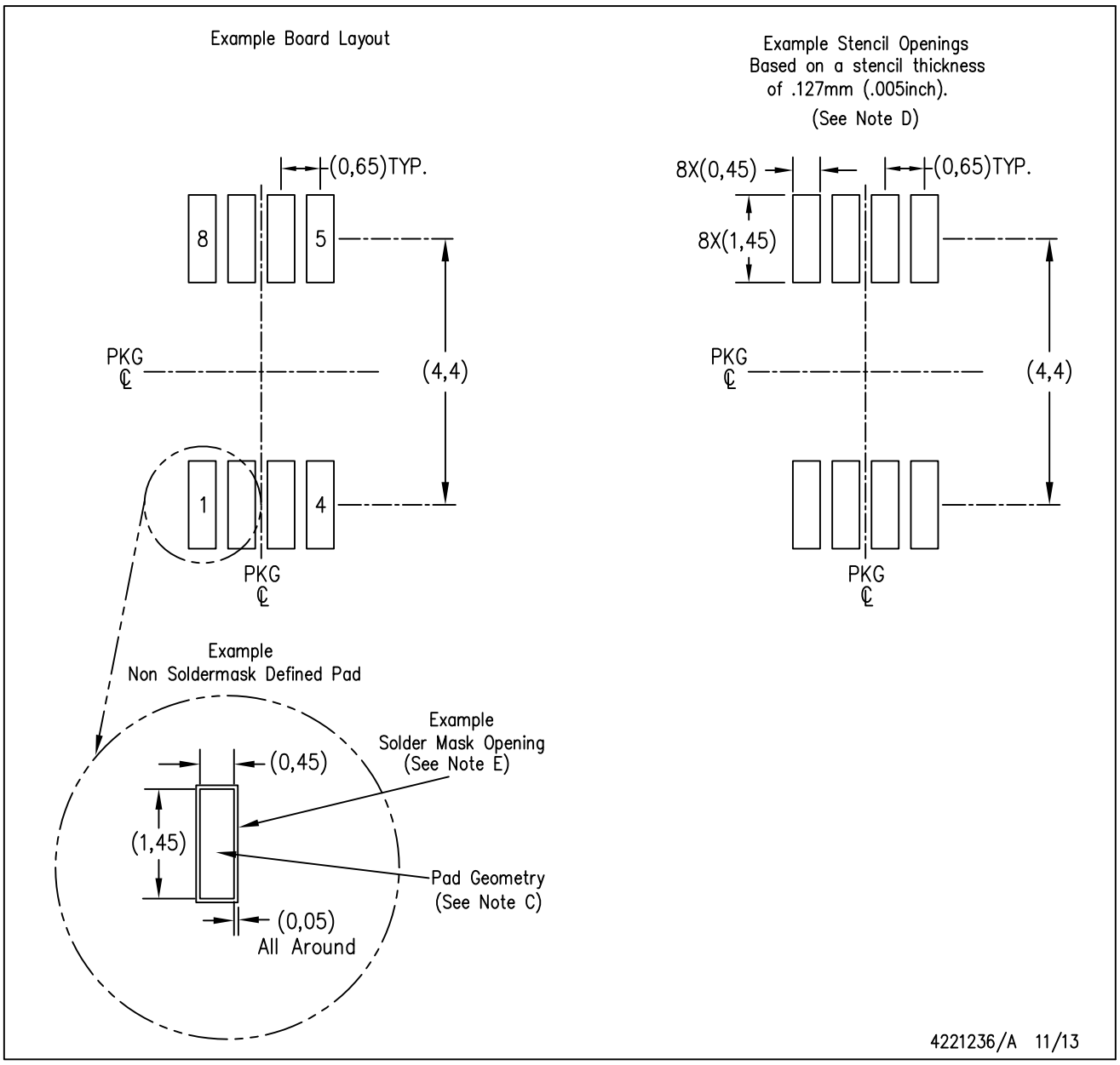
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

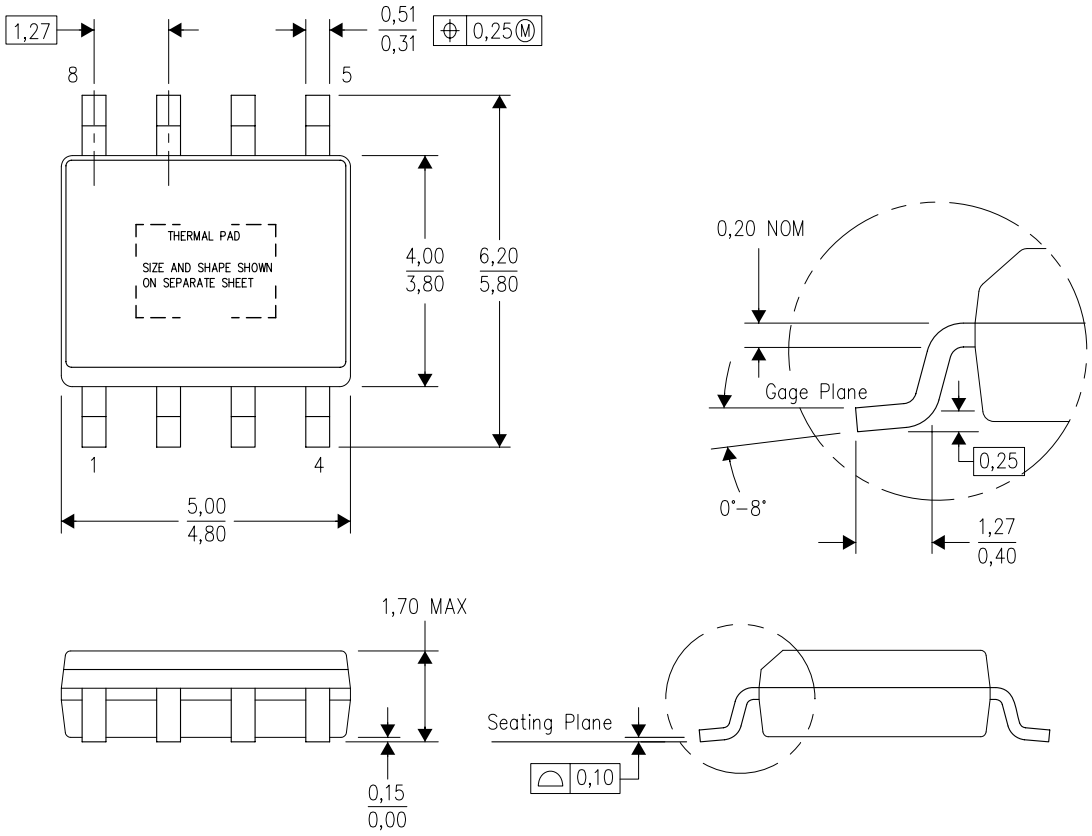
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

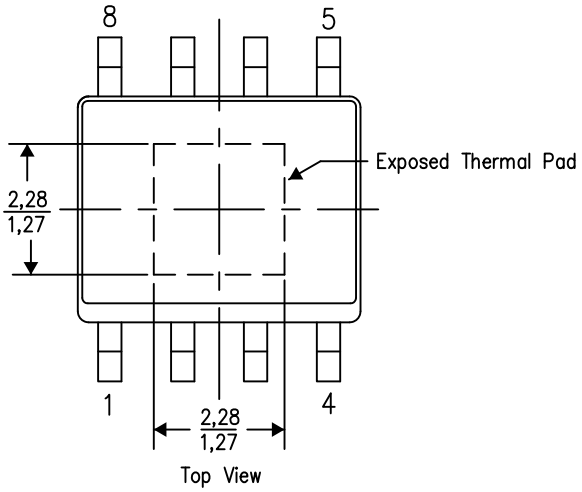
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



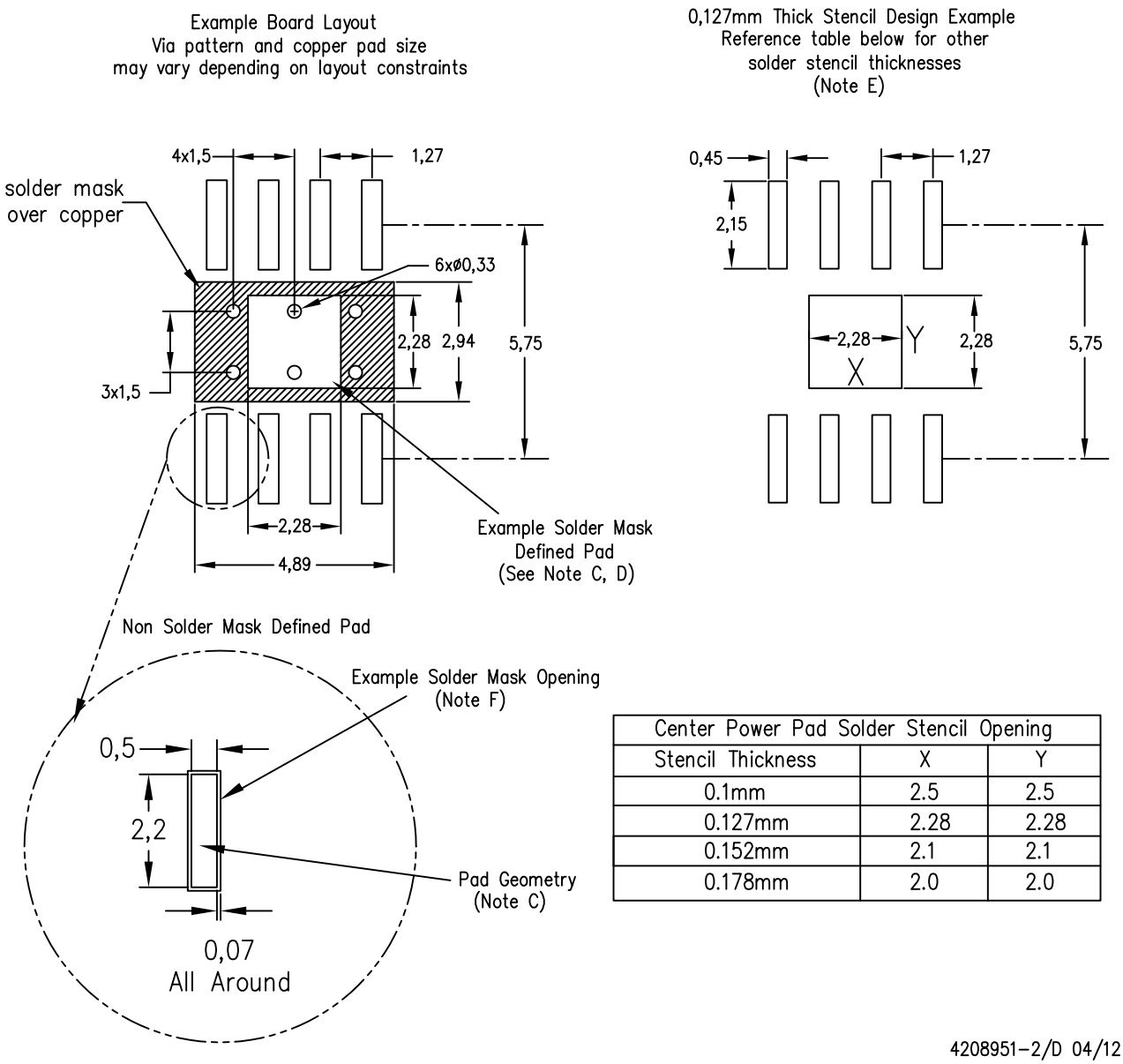
Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

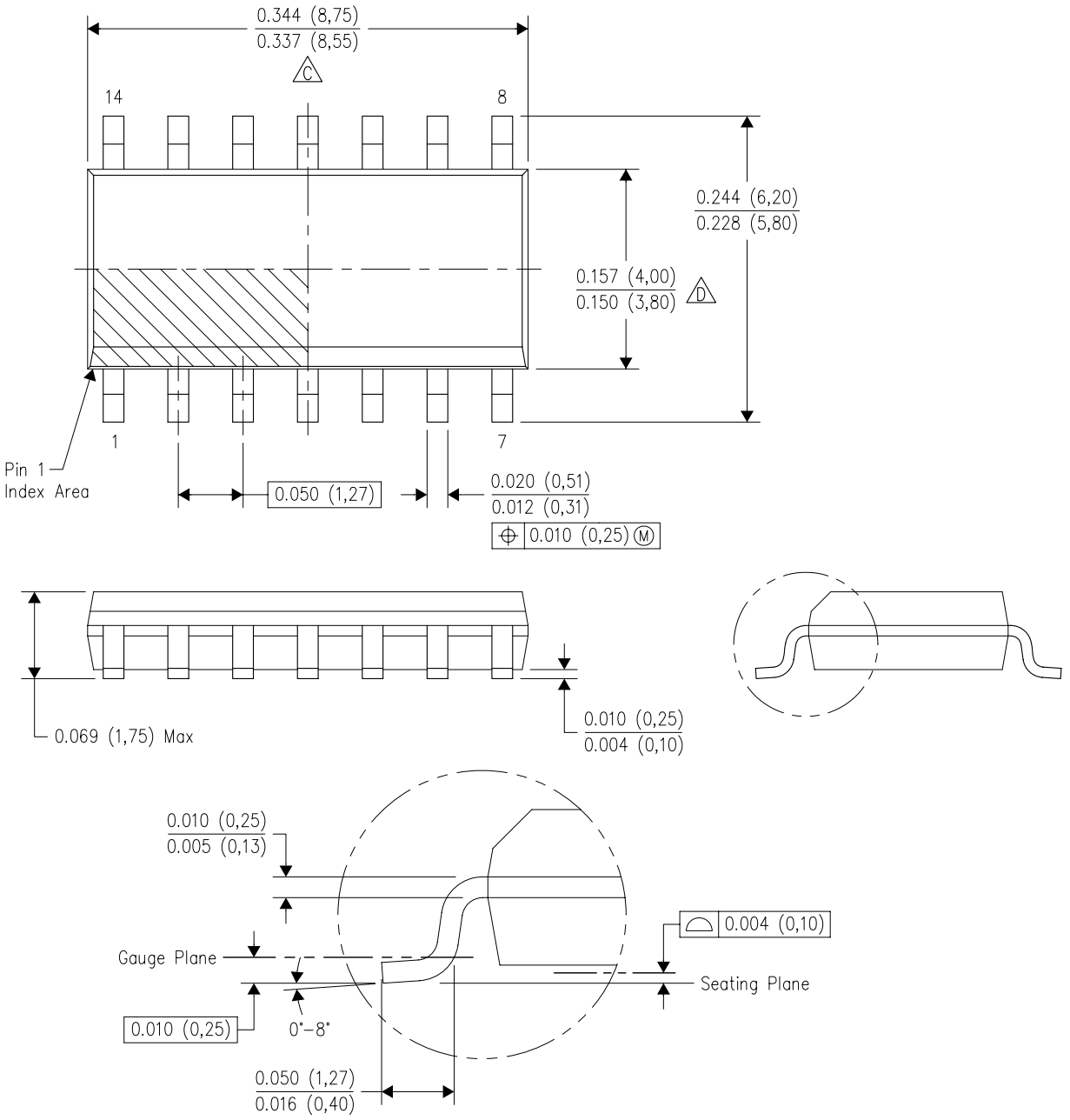


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

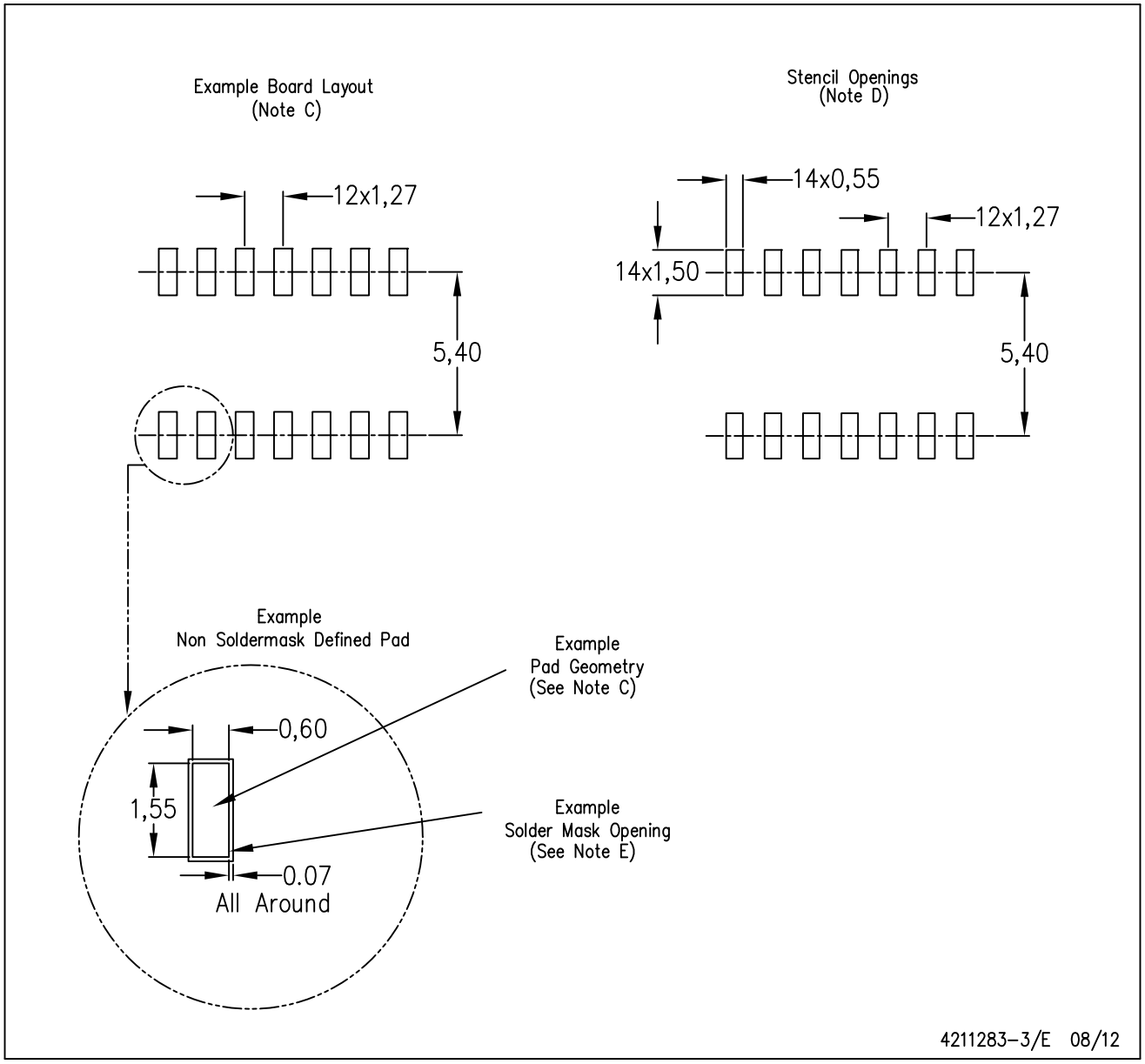
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

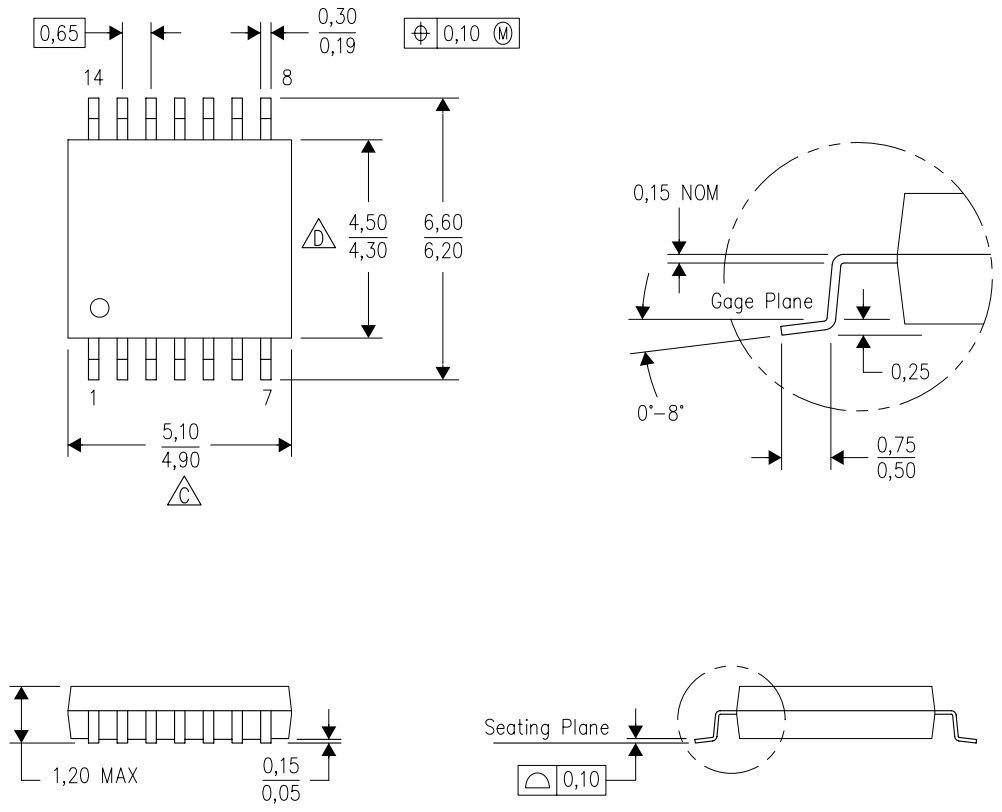
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

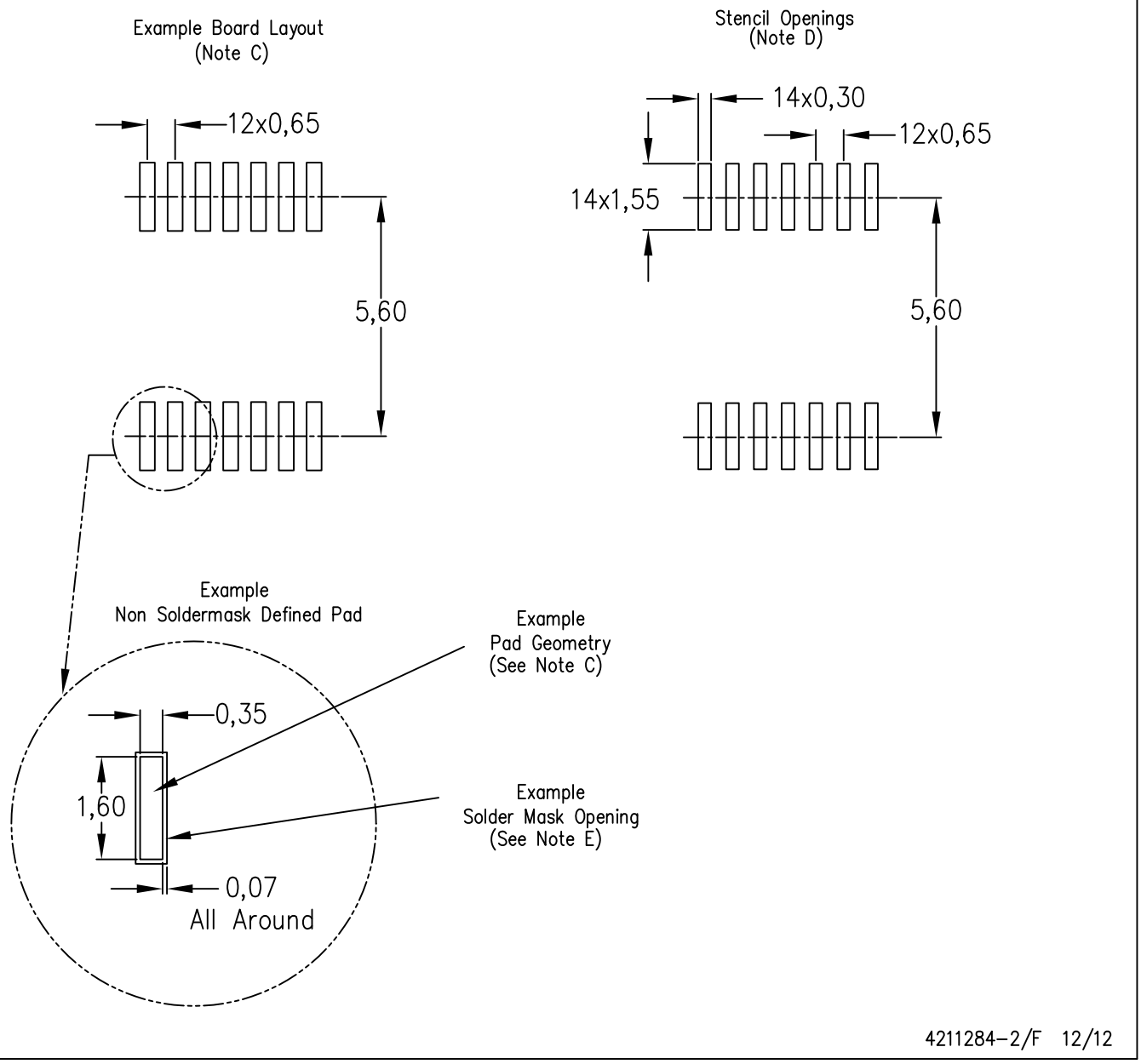
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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