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# HD74LV166A

## Parallel-Load 8-bit Shift Register

# HITACHI

ADE-205-268 (Z)  
1st Edition  
March 1999

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### Description

The HD74LV166A is 8-bit shift register with an output from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Shift/Load input is low, the data is loaded asynchronously in parallel. When the Shift/Load input is high, the data is loaded serially on the rising edge of either clock inhibit or Clock. Clear is asynchronous and active-low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.3\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  (@ $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@ $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )

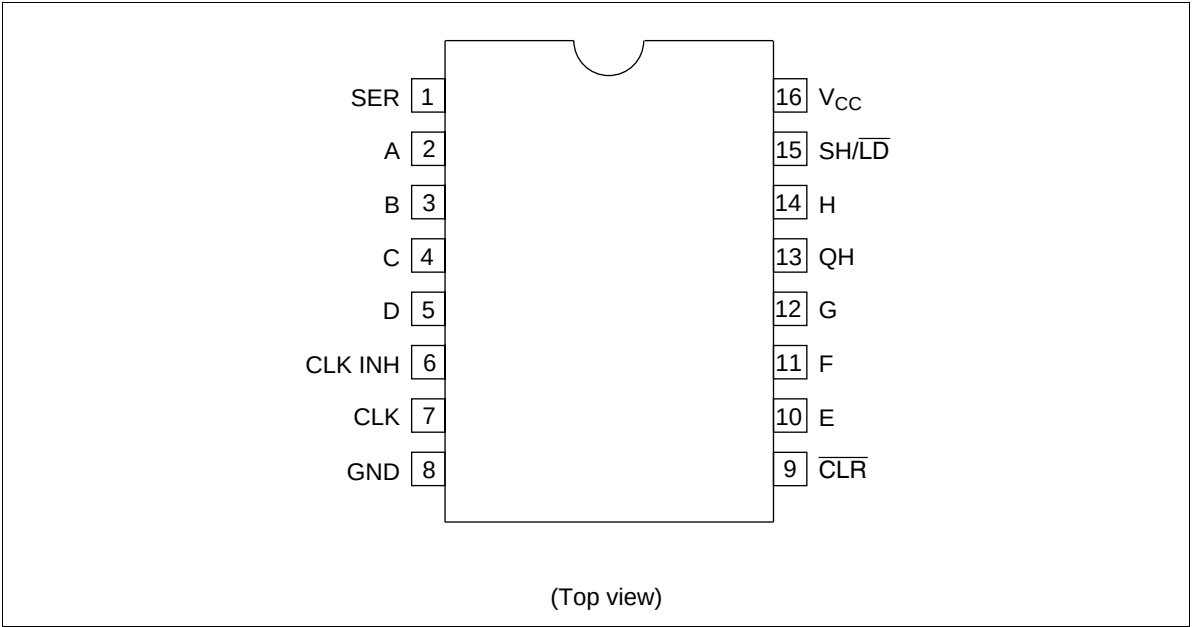
# HD74LV166A

## Function Table

| Inputs |       |         |     |     |         | Internal outputs |                 | Output          |
|--------|-------|---------|-----|-----|---------|------------------|-----------------|-----------------|
| CLR    | SH/LD | CLK INH | CLK | SER | A ... H | QA               | QB              | QH              |
| L      | X     | X       | X   | X   | X       | L                | L               | L               |
| H      | X     | L       | L   | X   | X       | Q <sub>A0</sub>  | Q <sub>B0</sub> | Q <sub>H0</sub> |
| H      | L     | L       | ↑   | X   | a ... h | a                | b               | h               |
| H      | H     | L       | ↑   | H   | X       | H                | Q <sub>An</sub> | Q <sub>Gn</sub> |
| H      | H     | L       | ↑   | L   | X       | L                | Q <sub>An</sub> | Q <sub>Gn</sub> |
| H      | X     | H       | ↑   | X   | X       | Q <sub>A0</sub>  | Q <sub>B0</sub> | Q <sub>H0</sub> |

Note: H: High level  
L: Low level  
↑: Low to high transition  
X: Immaterial  
a ... h: Parallel data  
Q<sub>A0</sub> ... Q<sub>H0</sub>: Outputs remain unchanged.  
Q<sub>An</sub> ... Q<sub>Gn</sub>: Data shifted from the previous stage on a positive edge at the clock input.

## Pin Arrangement



Absolute Maximum Ratings

| Item                                                                                 | Symbol                | Ratings                               | Unit | Conditions                       |
|--------------------------------------------------------------------------------------|-----------------------|---------------------------------------|------|----------------------------------|
| Supply voltage range                                                                 | $V_{CC}$              | −0.5 to 7.0                           | V    |                                  |
| Input voltage range* <sup>1</sup>                                                    | $V_I$                 | −0.5 to 7.0                           | V    |                                  |
| Output voltage range* <sup>1, 2</sup>                                                | $V_O$                 | −0.5 to $V_{CC} + 0.5$<br>−0.5 to 7.0 | V    | Output: H or L<br>$V_{CC}$ : OFF |
| Input clamp current                                                                  | $I_{IK}$              | −20                                   | mA   | $V_I < 0$                        |
| Output clamp current                                                                 | $I_{OK}$              | ±50                                   | mA   | $V_O < 0$ or $V_O > V_{CC}$      |
| Continuous output current                                                            | $I_O$                 | ±25                                   | mA   | $V_O = 0$ to $V_{CC}$            |
| Continuous current through $V_{CC}$ or GND                                           | $I_{CC}$ or $I_{GND}$ | ±50                                   | mA   |                                  |
| Maximum power dissipation at $T_a = 25^{\circ}\text{C}$ (in still air)* <sup>3</sup> | $P_T$                 | 785<br>500                            | mW   | SOP<br>TSSOP                     |
| Storage temperature                                                                  | $T_{stg}$             | −65 to 150                            | °C   |                                  |

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

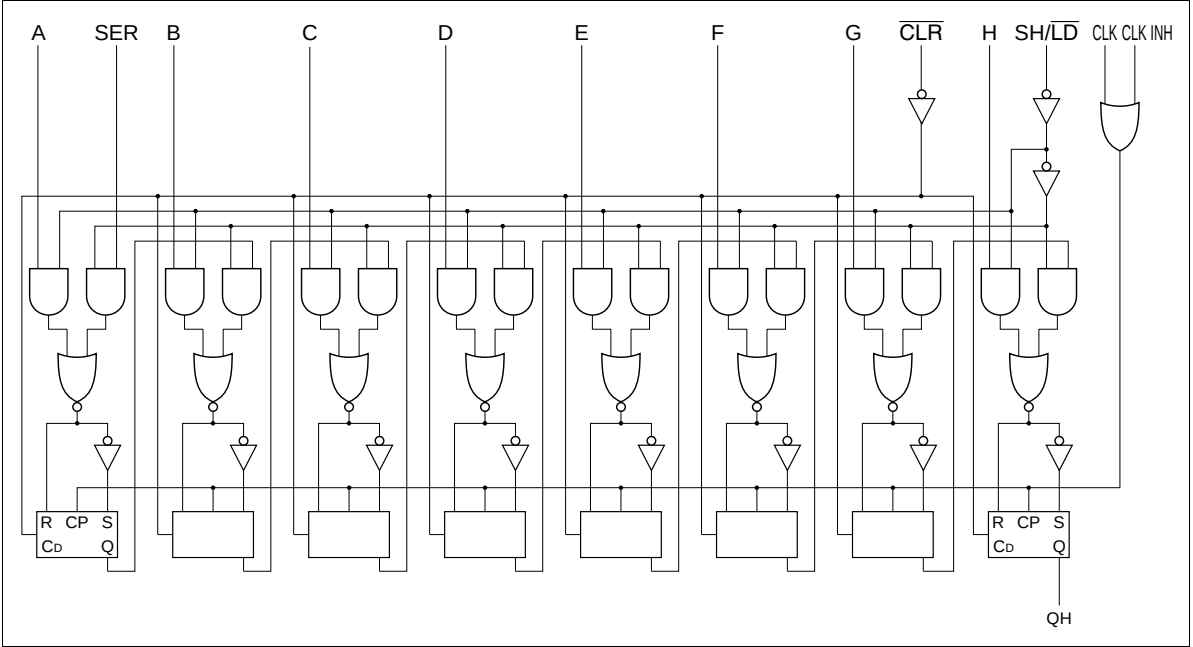
- 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. This value is limited to 5.5 V maximum.
- 3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

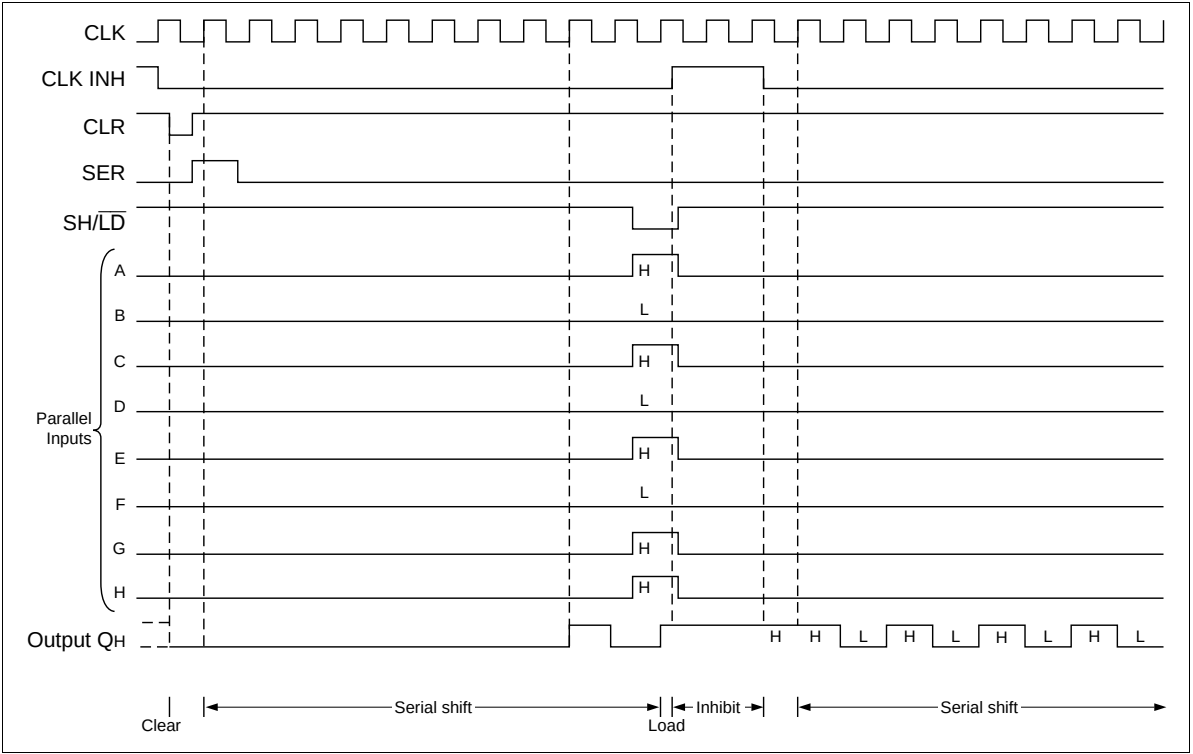
| Item                               | Symbol          | Min | Max             | Unit | Conditions                     |
|------------------------------------|-----------------|-----|-----------------|------|--------------------------------|
| Supply voltage range               | V <sub>CC</sub> | 2.0 | 5.5             | V    |                                |
| Input voltage range                | V <sub>I</sub>  | 0   | 5.5             | V    |                                |
| Output voltage range               | V <sub>O</sub>  | 0   | V <sub>CC</sub> | V    | H or L                         |
| Output current                     | I <sub>OH</sub> | —   | −50             | μA   | V <sub>CC</sub> = 2.0 V        |
|                                    |                 | —   | −2              | mA   | V <sub>CC</sub> = 2.3 to 2.7 V |
|                                    |                 | —   | −6              |      | V <sub>CC</sub> = 3.0 to 3.6 V |
|                                    |                 | —   | −12             |      | V <sub>CC</sub> = 4.5 to 5.5 V |
|                                    | I <sub>OL</sub> | —   | 50              | μA   | V <sub>CC</sub> = 2.0 V        |
|                                    |                 | —   | 2               | mA   | V <sub>CC</sub> = 2.3 to 2.7 V |
|                                    |                 | —   | 6               |      | V <sub>CC</sub> = 3.0 to 3.6 V |
|                                    |                 | —   | 12              |      | V <sub>CC</sub> = 4.5 to 5.5 V |
| Input transition rise or fall rate | Δt / Δv         | 0   | 200             | ns/V | V <sub>CC</sub> = 2.3 to 2.7 V |
|                                    |                 | 0   | 100             |      | V <sub>CC</sub> = 3.0 to 3.6 V |
|                                    |                 | 0   | 20              |      | V <sub>CC</sub> = 4.5 to 5.5 V |
| Operating free-air temperature     | Ta              | −40 | 85              | °C   |                                |

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



## DC Electrical Characteristics

- $T_a = -40$  to  $85^\circ\text{C}$

| Item                     | Symbol    | $V_{CC}$ (V)* | Min                 | Typ | Max                 | Unit          | Test Conditions                                 |
|--------------------------|-----------|---------------|---------------------|-----|---------------------|---------------|-------------------------------------------------|
| Input voltage            | $V_{IH}$  | 2.0           | 1.5                 | —   | —                   | V             |                                                 |
|                          |           | 2.3 to 2.7    | $V_{CC} \times 0.7$ | —   | —                   |               |                                                 |
|                          |           | 3.0 to 3.6    | $V_{CC} \times 0.7$ | —   | —                   |               |                                                 |
|                          |           | 4.5 to 5.5    | $V_{CC} \times 0.7$ | —   | —                   |               |                                                 |
|                          | $V_{IL}$  | 2.0           | —                   | —   | 0.5                 |               |                                                 |
|                          |           | 2.3 to 2.7    | —                   | —   | $V_{CC} \times 0.3$ |               |                                                 |
|                          |           | 3.0 to 3.6    | —                   | —   | $V_{CC} \times 0.3$ |               |                                                 |
|                          |           | 4.5 to 5.5    | —                   | —   | $V_{CC} \times 0.3$ |               |                                                 |
| Output voltage           | $V_{OH}$  | Min to Max    | $V_{CC} - 0.1$      | —   | —                   | V             | $I_{OL} = -50\ \mu\text{A}$                     |
|                          |           | 2.3           | 2.0                 | —   | —                   |               | $I_{OL} = -2\ \text{mA}$                        |
|                          |           | 3.0           | 2.48                | —   | —                   |               | $I_{OL} = -6\ \text{mA}$                        |
|                          |           | 4.5           | 3.8                 | —   | —                   |               | $I_{OL} = -12\ \text{mA}$                       |
|                          | $V_{OL}$  | Min to Max    | —                   | —   | 0.1                 |               | $I_{OL} = 50\ \mu\text{A}$                      |
|                          |           | 2.3           | —                   | —   | 0.4                 |               | $I_{OL} = 2\ \text{mA}$                         |
|                          |           | 3.0           | —                   | —   | 0.44                |               | $I_{OL} = 6\ \text{mA}$                         |
|                          |           | 4.5           | —                   | —   | 0.55                |               | $I_{OL} = 12\ \text{mA}$                        |
| Input current            | $I_{IN}$  | 0 to 5.5      | —                   | —   | $\pm 1$             | $\mu\text{A}$ | $V_I = 5.5\ \text{V}$ or GND                    |
| Quiescent supply current | $I_{CC}$  | 5.5           | —                   | —   | 20                  | $\mu\text{A}$ | $V_I = V_{CC}$ or GND, $I_O = 0$                |
| Output leakage current   | $I_{OFF}$ | 0             | —                   | —   | 5                   | $\mu\text{A}$ | $V_I$ or $V_O = 0\ \text{V}$ to $5.5\ \text{V}$ |
| Input capacitance        | $C_{IN}$  | 3.3           | —                   | 1.7 | —                   | pF            | $V_I = V_{CC}$ or GND                           |

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

|                                |                                    | Ta = 25°C |      |      | Ta = −40 to 85°C |      |      |                        |                                              |                |
|--------------------------------|------------------------------------|-----------|------|------|------------------|------|------|------------------------|----------------------------------------------|----------------|
| Item                           | Symbol                             | Min       | Typ  | Max  | Min              | Max  | Unit | Test Conditions        | FROM (Input)                                 | TO (Output)    |
| Maximum clock frequency        | fmax                               | 50        | 80   | —    | 45               | —    | MHz  | C <sub>L</sub> = 15 pF |                                              |                |
|                                |                                    | 40        | 65   | —    | 35               | —    |      | C <sub>L</sub> = 50 pF |                                              |                |
| Propa-<br>gation<br>delay time | t <sub>PLH</sub> /t <sub>PHL</sub> | —         | 12.2 | 19.8 | 1.0              | 22.0 | ns   | C <sub>L</sub> = 15 pF | CLK                                          | Q <sub>H</sub> |
|                                |                                    | —         | 15.3 | 23.3 | 1.0              | 26.0 |      | C <sub>L</sub> = 50 pF |                                              |                |
|                                | t <sub>PHL</sub>                   | —         | 10.8 | 16.0 | 1.0              | 18.0 |      | C <sub>L</sub> = 15 pF | CLR                                          |                |
|                                |                                    | —         | 14.2 | 19.5 | 1.0              | 22.0 |      | C <sub>L</sub> = 50 pF |                                              |                |
| Setup time                     | t <sub>su</sub>                    | 7.0       | —    | —    | 7.0              | —    | ns   |                        | CLK INH before CLK ↑                         |                |
|                                |                                    | 6.5       | —    | —    | 8.5              | —    |      |                        | Data before CLK ↑                            |                |
|                                |                                    | 7.0       | —    | —    | 8.5              | —    | ns   |                        | SH/ $\overline{\text{LD}}$ high before CLK ↑ |                |
|                                |                                    | 8.5       | —    | —    | 9.5              | —    |      |                        | SER before CLK ↑                             |                |
| Hold time                      | t <sub>h</sub>                     | −0.5      | —    | —    | 0.0              | —    | ns   |                        | PAR data after SH/ $\overline{\text{LD}}$ ↑  |                |
|                                |                                    | −0.5      | —    | —    | 0.0              | —    |      |                        | SER data after CLK ↑                         |                |
|                                |                                    | −0.5      | —    | —    | 0.0              | —    |      |                        | SH/LD high after CLK ↑                       |                |
| Pulse width                    | t <sub>w</sub>                     | 8.0       | —    | —    | 9.0              | —    | ns   |                        | CLR low                                      |                |
|                                |                                    | 8.5       | —    | —    | 9.0              | —    |      |                        | CLK H or L                                   |                |



Switching Characteristics (cont)

- $V_{CC} = 3.3 \pm 0.3 \text{ V}$

|                                |                                    | Ta = 25°C |      |      | Ta = −40 to 85°C |      |      |                        |                                              |                |
|--------------------------------|------------------------------------|-----------|------|------|------------------|------|------|------------------------|----------------------------------------------|----------------|
| Item                           | Symbol                             | Min       | Typ  | Max  | Min              | Max  | Unit | Test Conditions        | FROM (Input)                                 | TO (Output)    |
| Maximum clock frequency        | fmax                               | 65        | 115  | —    | 55               | —    | MHz  | C <sub>L</sub> = 15 pF |                                              |                |
|                                |                                    | 60        | 90   | —    | 50               | —    |      | C <sub>L</sub> = 50 pF |                                              |                |
| Propa-<br>gation<br>delay time | t <sub>PLH</sub> /t <sub>PHL</sub> | —         | 8.6  | 15.4 | 1.0              | 18.0 | ns   | C <sub>L</sub> = 15 pF | CLK                                          | Q <sub>H</sub> |
|                                |                                    | —         | 10.9 | 18.9 | 1.0              | 21.5 |      | C <sub>L</sub> = 50 pF |                                              |                |
|                                | t <sub>PHL</sub>                   | —         | 7.9  | 12.5 | 1.0              | 15.0 |      | C <sub>L</sub> = 15 pF | CLR                                          |                |
|                                |                                    | —         | 10.4 | 16.3 | 1.0              | 18.5 |      | C <sub>L</sub> = 50 pF |                                              |                |
| Setup time                     | t <sub>su</sub>                    | 5.0       | —    | —    | 5.0              | —    | ns   |                        | CLK INH before CLK ↑                         |                |
|                                |                                    | 5.0       | —    | —    | 6.0              | —    |      |                        | Data before CLK ↑                            |                |
|                                |                                    | 5.0       | —    | —    | 6.0              | —    | ns   |                        | SH/ $\overline{\text{LD}}$ high before CLK ↑ |                |
|                                |                                    | 5.0       | —    | —    | 6.0              | —    |      |                        | SER before CLK ↑                             |                |
| Hold time                      | t <sub>h</sub>                     | 0.0       | —    | —    | 0.0              | —    | ns   |                        | PAR data after SH/ $\overline{\text{LD}}$ ↑  |                |
|                                |                                    | 0.0       | —    | —    | 0.0              | —    |      |                        | SER data after CLK ↑                         |                |
|                                |                                    | 0.0       | —    | —    | 0.0              | —    |      |                        | SH/LD high after CLK ↑                       |                |
| Pulse width                    | t <sub>w</sub>                     | 6.0       | —    | —    | 7.0              | —    | ns   |                        | CLR low                                      |                |
|                                |                                    | 6.0       | —    | —    | 7.0              | —    |      |                        | CLK H or L                                   |                |

Switching Characteristics (cont)

- $V_{CC} = 5.0 \pm 0.5\text{ V}$

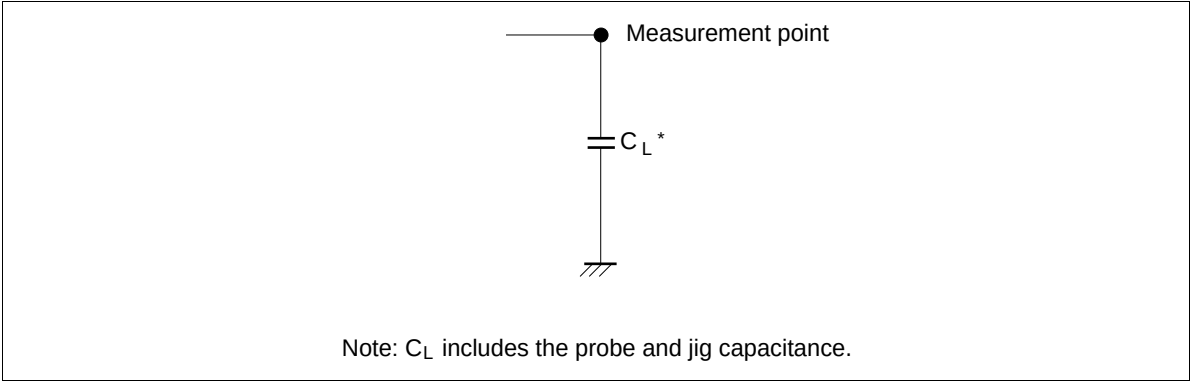
| Item                           | Symbol                             | Ta = 25°C |     |      | Ta = −40 to 85°C |      | Unit | Test Conditions        | FROM (Input)                                 | TO (Output)    |
|--------------------------------|------------------------------------|-----------|-----|------|------------------|------|------|------------------------|----------------------------------------------|----------------|
|                                |                                    | Min       | Typ | Max  | Min              | Max  |      |                        |                                              |                |
| Maximum clock frequency        | fmax                               | 110       | 165 | —    | 90               | —    | MHz  | C <sub>L</sub> = 15 pF |                                              |                |
|                                |                                    | 95        | 125 | —    | 85               | —    |      | C <sub>L</sub> = 50 pF |                                              |                |
| Propa-<br>gation<br>delay time | t <sub>PLH</sub> /t <sub>PHL</sub> | —         | 6.0 | 9.9  | 1.0              | 11.5 | ns   | C <sub>L</sub> = 15 pF | CLK                                          | Q <sub>H</sub> |
|                                |                                    | —         | 7.7 | 11.9 | 1.0              | 13.5 |      | C <sub>L</sub> = 50 pF |                                              |                |
|                                | t <sub>PHL</sub>                   | —         | 5.4 | 8.6  | 1.0              | 10.0 |      | C <sub>L</sub> = 15 pF | CLR                                          |                |
|                                |                                    | —         | 6.9 | 10.6 | 1.0              | 12.0 |      | C <sub>L</sub> = 50 pF |                                              |                |
| Setup time                     | t <sub>su</sub>                    | 3.5       | —   | —    | 3.5              | —    | ns   |                        | CLK INH before CLK ↑                         |                |
|                                |                                    | 4.5       | —   | —    | 4.5              | —    |      |                        | Data before CLK ↑                            |                |
|                                |                                    | 4.0       | —   | —    | 4.0              | —    | ns   |                        | SH/ $\overline{\text{LD}}$ high before CLK ↑ |                |
|                                |                                    | 4.0       | —   | —    | 4.0              | —    |      |                        | SER before CLK ↑                             |                |
| Hold time                      | t <sub>h</sub>                     | 1.0       | —   | —    | 1.0              | —    | ns   |                        | PAR data after SH/ $\overline{\text{LD}}$ ↑  |                |
|                                |                                    | 1.0       | —   | —    | 1.0              | —    |      |                        | SER data after CLK ↑                         |                |
|                                |                                    | 1.0       | —   | —    | 1.0              | —    |      |                        | SH/LD high after CLK ↑                       |                |
| Pulse width                    | t <sub>w</sub>                     | 5.0       | —   | —    | 5.0              | —    | ns   |                        | CLR low                                      |                |
|                                |                                    | 4.0       | —   | —    | 4.0              | —    |      |                        | CLK H or L                                   |                |

Operating Characteristics

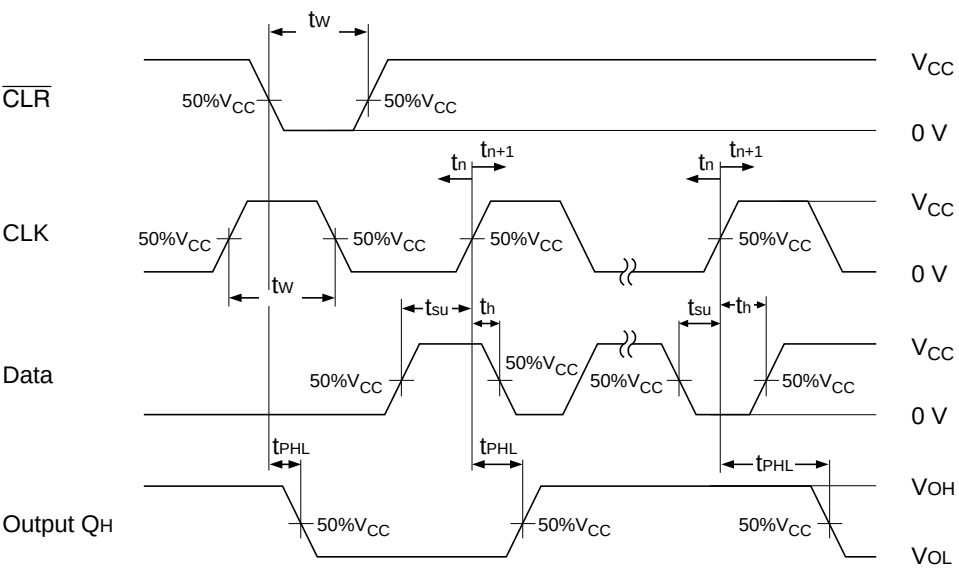
- $C_L = 50\text{ pF}$

| Item                          | Symbol   | $V_{CC}$ (V) | $T_a = 25^{\circ}\text{C}$ |      |     | Unit | Test Conditions     |
|-------------------------------|----------|--------------|----------------------------|------|-----|------|---------------------|
|                               |          |              | Min                        | Typ  | Max |      |                     |
| Power dissipation capacitance | $C_{PD}$ | 3.3          | —                          | 36.1 | —   | pF   | $f = 10\text{ MHz}$ |
|                               |          | 5.0          | —                          | 37.5 | —   |      |                     |

Test Circuit

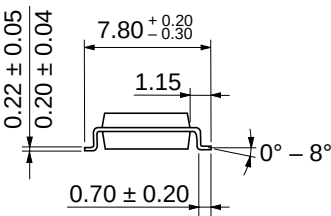
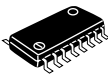
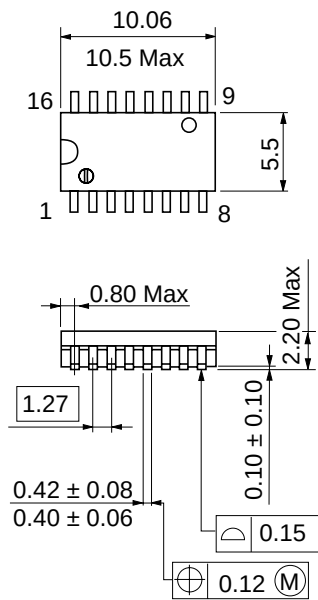


Waveform



Notes: 1. Input waveform:  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$   
2. The output are measured one at a time with one transition per measurement.

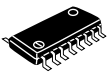
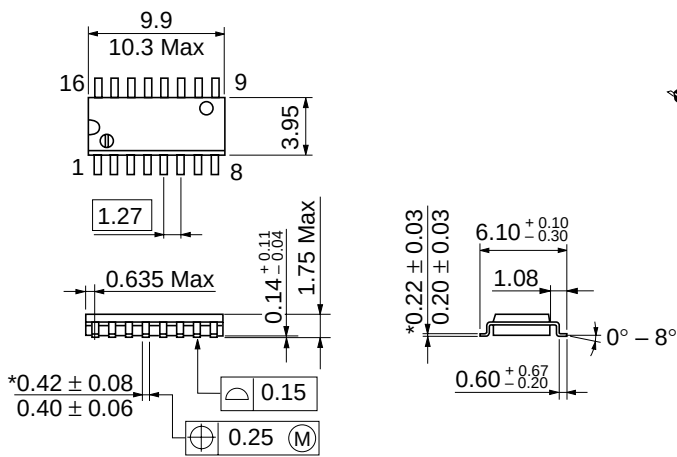
Package Dimensions



Dimension including the plating thickness  
Base material dimension

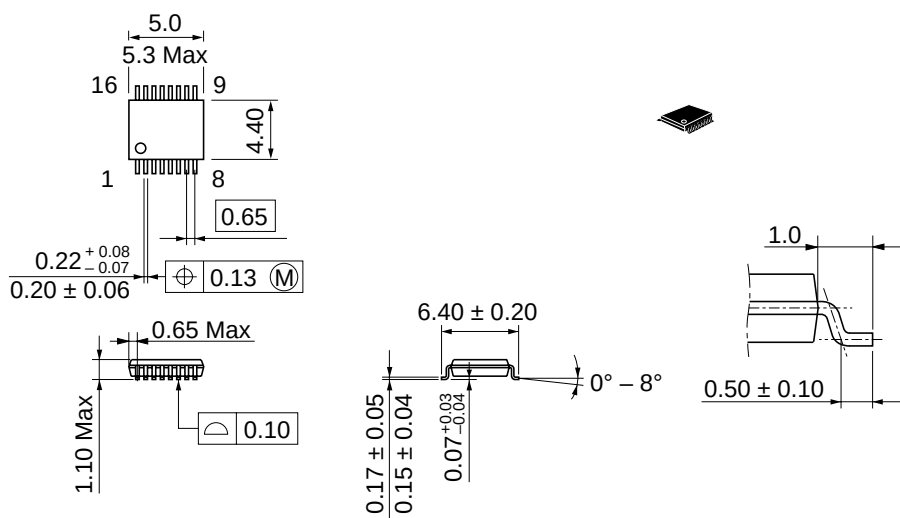
|                          |          |
|--------------------------|----------|
| Hitachi Code             | FP-16DA  |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.24 g   |

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

|                          |          |
|--------------------------|----------|
| Hitachi Code             | FP-16DN  |
| JEDEC                    | Conforms |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.15 g   |



Dimension including the plating thickness  
Base material dimension

|                          |          |
|--------------------------|----------|
| Hitachi Code             | TTP-16DA |
| JEDEC                    | —        |
| EIAJ                     | —        |
| Weight (reference value) | 0.05 g   |

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## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
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| Hitachi Semiconductor (America) Inc.<br>179 East Tasman Drive,<br>San Jose, CA 95134<br>Tel: <1> (408) 433-1990<br>Fax: <1> (408) 433-0223 | Hitachi Europe GmbH<br>Electronic components Group<br>Dornacher Straße 3<br>D-85622 Feldkirchen, Munich<br>Germany<br>Tel: <49> (89) 9 9180-0<br>Fax: <49> (89) 9 29 30 00<br><br>Hitachi Europe Ltd.<br>Electronic Components Group.<br>Whitebrook Park<br>Lower Cookham Road<br>Maidenhead<br>Berkshire SL6 8YA, United Kingdom<br>Tel: <44> (1628) 585000<br>Fax: <44> (1628) 778322 |
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|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Hitachi Asia Pte. Ltd.<br>16 Collyer Quay #20-00<br>Hitachi Tower<br>Singapore 049318<br>Tel: 535-2100<br>Fax: 535-1533<br><br>Hitachi Asia Ltd.<br>Taipei Branch Office<br>3F, Hung Kuo Building. No.167,<br>Tun-Hwa North Road, Taipei (105)<br>Tel: <886> (2) 2718-3666<br>Fax: <886> (2) 2718-8180 |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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