ELPIDA

**PRELIMINARY DATA SHEET**

# 4GB Fully Buffered DIMM

## EBE41FE4ABHD

### Specifications

- Density: 4GB
- Organization
— 512M words × 72 bits, 2 ranks
- Mounting 36 pieces of 1G bits DDR2 SDRAM with sFBGA
- Package
— 240-pin fully buffered, socket type dual in line memory module (FB-DIMM)
PCB height: 30.35mm
Lead pitch: 1.00mm
— Advanced Memory Buffer (AMB): 655-ball FCBGA
— Lead-free (RoHS compliant)
- Power supply
— DDR2 SDRAM: VDD = 1.8V ± 0.1V
— AMB: VCC = 1.5V + 0.075V/–0.045
- Data rate: 667Mbps/533Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_18
- Burst lengths (BL): 4, 8
- /CAS Latency (CL): 3, 4, 5
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
— Average refresh period
7.8µs at 0°C ≤ TC ≤ +85°C
3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
— TC = 0°C to +95°C

### Features

- JEDEC standard Raw Card D Design
- Industry Standard Advanced Memory Buffer (AMB)
- High-speed differential point-to-point link interface at 1.5V (JEDEC draft spec)
— 14 north-bound (NB) high speed serial lanes
— 10 south-bound (SB) high speed serial lanes
- Various features/modes:
— MemBIST and IBIST test functions
— Transparent mode and direct access mode for DRAM testing
— Interface for a thermal sensor and status indicator
- Channel error detection and reporting
- Automatic DDR2 SDRAM bus and channel calibration
- SPD (serial presence detect) with 1piece of 256 byte serial EEPROM

**Note: Warranty void if removed DIMM heat spreader.**

### Performance

| | FB-DIMM | | | DDR2 SDRAM | |
|---|---|---|---|---|---|
| System clock frequency | Speed grade | Peak channel throughput | FB-DIMM link data rate | Speed Grade | DDR data rate |
| 167MHz | PC2-5300F | 8.0GByte/s | 4.0Gbps | DDR2-667 (5-5-5) | 667Mbps |
| 133MHz | PC2-4200F | 6.4GByte/s | 3.2Gbps | DDR2-533 (4-4-4) | 533Mbps |

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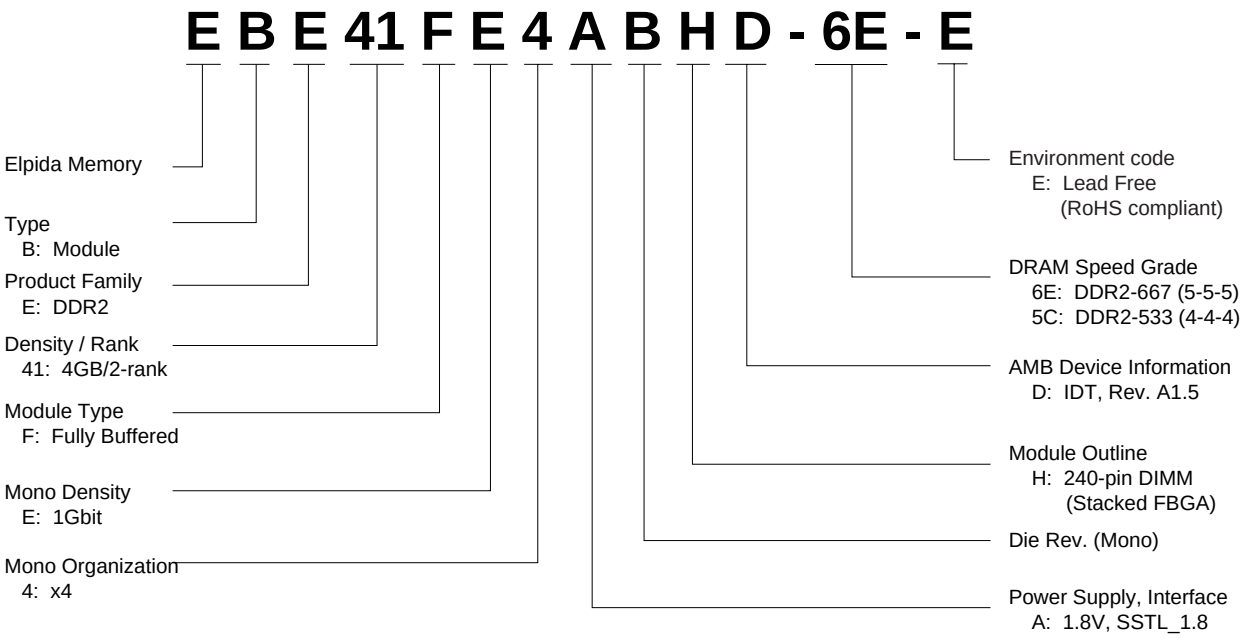
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## Ordering Information

| Part number | DIMM speed grade | Component JEDEC speed bin (CL-tRCD-tRP) | Mounted devices*[1] | Mounted AMB*[2] |
|---|---|---|---|---|
| EBE41FE4ABHD-6E-E | PC2-5300F | DDR2-667 (5-5-5) | 1G bits DDR2 SDRAM | IDT Rev. A1.5 |
| EBE41FE4ABHD-5C-E | PC2-4200F | DDR2-533 (4-4-4) | | |

Notes: 1. Please refer to 1Gb DDR2 datasheet (E0852E) for detailed operation part and timing waveforms.
2. Please refer to the following documents for detailed operation part and timing waveforms.
Advanced Memory Buffer (AMB) specification
FB-DIMM Architecture and Protocol specification

## Part Number



## Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the FB-DIMM Architecture and Protocol Specification. It supports DDR2 SDRAM main memory. The AMB allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The AMB interface is responsible for handling FB-DIMM channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FB-DIMM channel.

The FB-DIMM provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. FB-DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density.

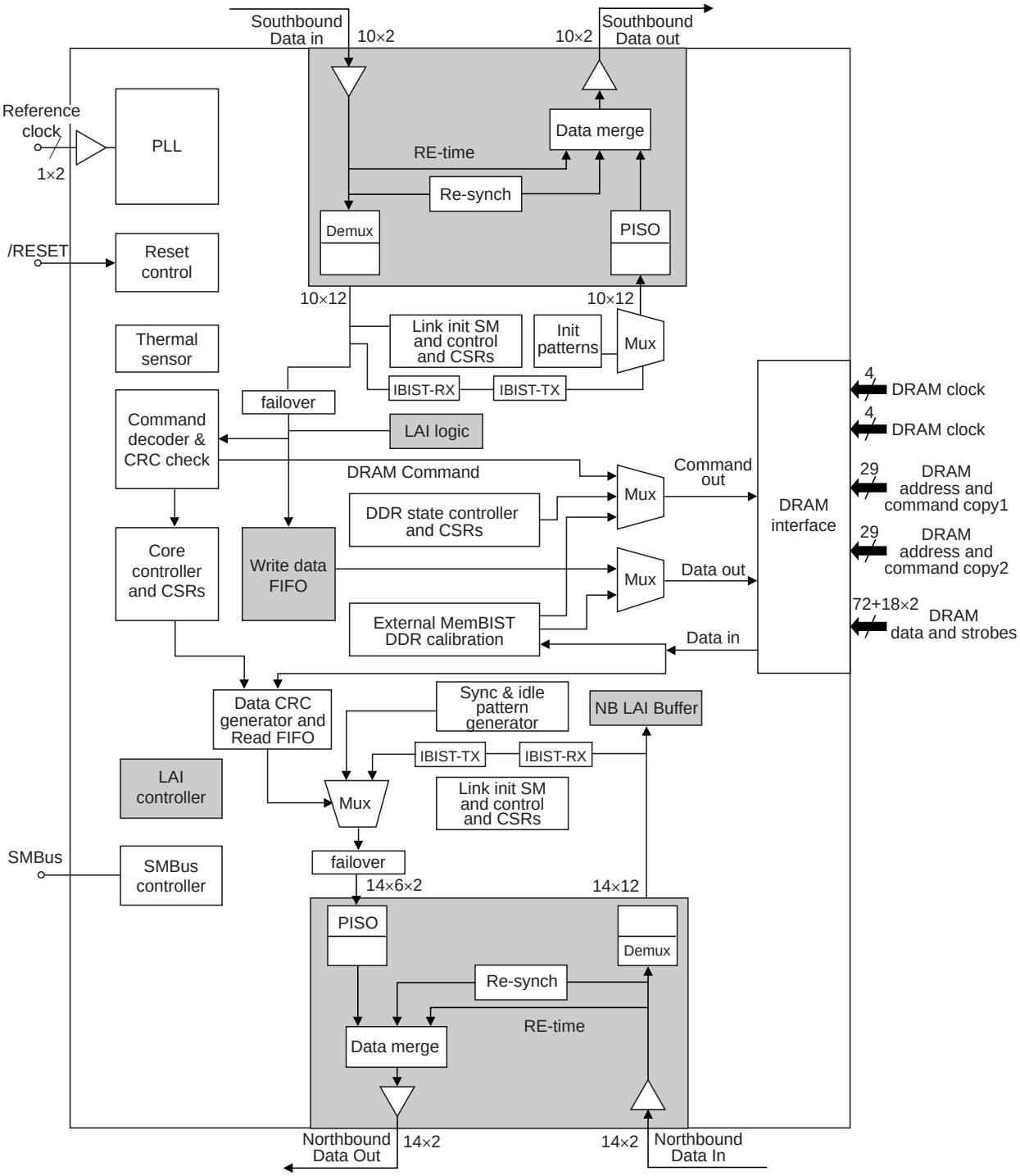
The AMB is the buffer that isolates the DRAMs from the channel.

### Advanced Memory Buffer Functionality

The AMB will perform the following FB-DIMM channel functions.

- Supports channel initialization procedures as defined in the initialization chapter of the FB-DIMM Architecture and Protocol Specification to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FB-DIMM configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MemBIST and IBIST design for test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FB-DIMM links.

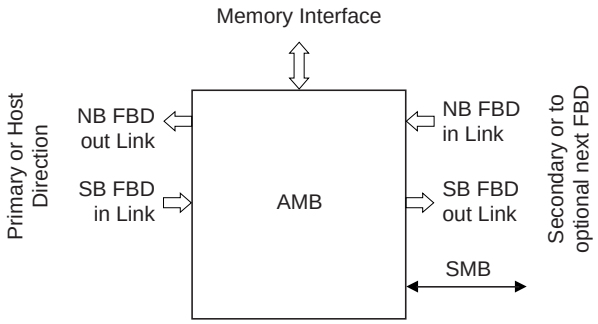
**Advanced Memory Buffer Block Diagram**




Note: This figure is a conceptual block diagram of the AMB's data flow and clock domains.

### Interfaces

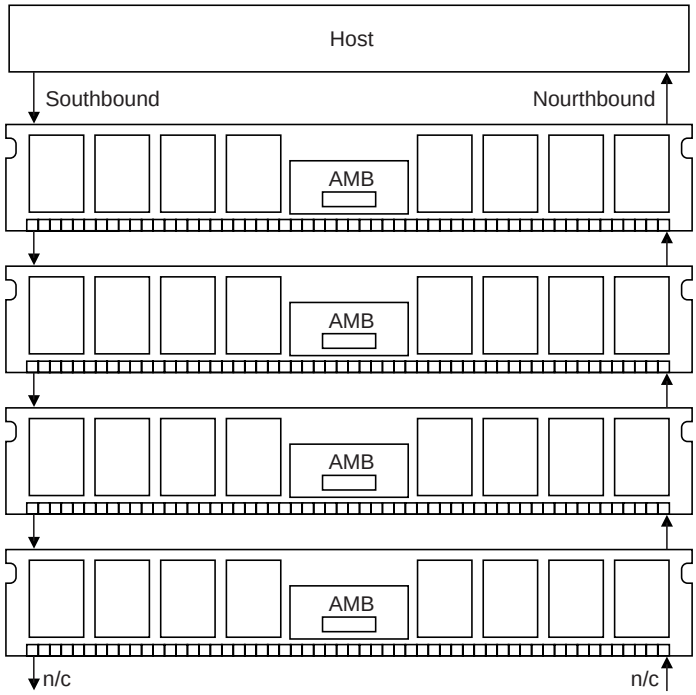
Figure Block Diagram AMB Interfaces shows the AMB and all of its interfaces. They consist of two FB-DIMM links, one DDR2 channel and an SMBus interface. Each FB-DIMM link connects the AMB to a host memory controller or an adjacent FB-DIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a FB-DIMM.




**Block Diagram AMB Interfaces**

### Interface Topology

The FB-DIMM channel uses a daisy-chain topology to provide expansion from a single DIMM per channel to up to 8 DIMMs per channel. The host sends data on the southbound link to the first DIMM where it is received and redriven to the second DIMM. On the southbound data path each DIMM receives the data and again re-drives the data to the next DIMM until the last DIMM receives the data. The last DIMM in the chain initiates the transmission of data in the direction on the host (a.k.a. northbound). On the northbound data path each DIMM receives the data and re-drives the data to the next DIMM until the host is reached.




**Block Diagram FB-DIMM Channel Southbound and Northbound Paths**

**High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces**

The AMB supports one FB-DIMM channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FB-DIMM. The northbound input link is 14 lanes wide and carries read return data or status information from the next FB-DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally. Data and commands sent to the DRAMs travel southbound on 10 primary differential signal line pairs. Data received from the DRAMs and status information travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent DIMM upstream are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the adjacent DIMM upstream travel further northbound on 14 secondary differential pairs.

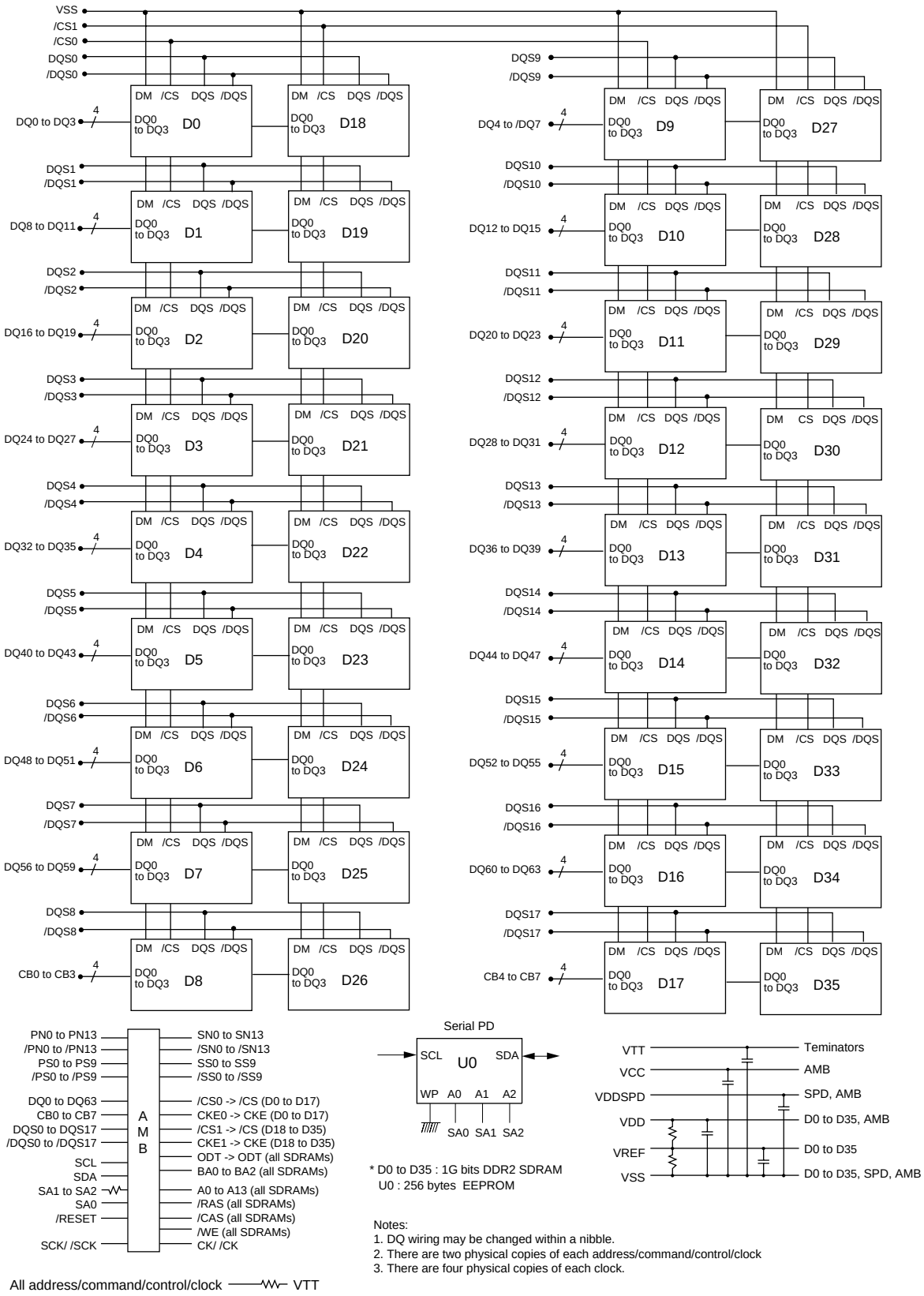
**DDR2 Channel**

The DDR2 channel on the AMB supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800MHz. Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error. Hardware aligns the read data and check-bits to a single core clock. The AMB provides four copies of the command clock phase references (CLK [3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

**SMBus Slave interface**

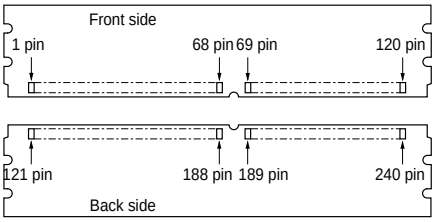
The AMB supports an SMBus interface to allow system access to configuration register independent of the FB-DIMM link. The AMB will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100kHz. SMBus access to the AMB may be a requirement to boot and to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the unique ID.

## Block Diagram




Notes:
1. DQ wiring may be changed within a nibble.
2. There are two physical copies of each address/command/control/clock
3. There are four physical copies of each clock.

## Pin Configurations




Front side

| No. | Name | No. | Name | No. | Name | No. | Name |
|---|---|---|---|---|---|---|---|
| 1 | VDD | 36 | VSS | 71 | /PS0 | 106 | NC |
| 2 | VDD | 37 | PN5 | 72 | VSS | 107 | VSS |
| 3 | VDD | 38 | /PN5 | 73 | PS1 | 108 | VDD |
| 4 | VSS | 39 | VSS | 74 | /PS1 | 109 | VDD |
| 5 | VDD | 40 | PN13 | 75 | VSS | 110 | VSS |
| 6 | VDD | 41 | /PN13 | 76 | PS2 | 111 | VDD |
| 7 | VDD | 42 | VSS | 77 | /PS2 | 112 | VDD |
| 8 | VSS | 43 | VSS | 78 | VSS | 113 | VDD |
| 9 | VCC | 44 | NC | 79 | PS3 | 114 | VSS |
| 10 | VCC | 45 | NC | 80 | /PS3 | 115 | VDD |
| 11 | VSS | 46 | VSS | 81 | VSS | 116 | VDD |
| 12 | VCC | 47 | VSS | 82 | PS4 | 117 | VTT |
| 13 | VCC | 48 | PN12 | 83 | /PS4 | 118 | SA2 |
| 14 | VSS | 49 | /PN12 | 84 | VSS | 119 | SDA |
| 15 | VTT | 50 | VSS | 85 | VSS | 120 | SCL |
| 16 | VID1 | 51 | PN6 | 86 | NC | | |
| 17 | /RESET | 52 | /PN6 | 87 | NC | | |
| 18 | VSS | 53 | VSS | 88 | VSS | | |
| 19 | NC | 54 | PN7 | 89 | VSS | | |
| 20 | NC | 55 | /PN7 | 90 | PS9 | | |
| 21 | VSS | 56 | VSS | 91 | /PS9 | | |
| 22 | PN0 | 57 | PN8 | 92 | VSS | | |
| 23 | /PN0 | 58 | /PN8 | 93 | PS5 | | |
| 24 | VSS | 59 | VSS | 94 | /PS5 | | |
| 25 | PN1 | 60 | PN9 | 95 | VSS | | |
| 26 | /PN1 | 61 | /PN9 | 96 | PS6 | | |
| 27 | VSS | 62 | VSS | 97 | /PS6 | | |
| 28 | PN2 | 63 | PN10 | 98 | VSS | | |
| 29 | /PN2 | 64 | /PN10 | 99 | PS7 | | |
| 30 | VSS | 65 | VSS | 100 | /PS7 | | |
| 31 | PN3 | 66 | PN11 | 101 | VSS | | |
| 32 | /PN3 | 67 | /PN11 | 102 | PS8 | | |
| 33 | VSS | 68 | VSS | 103 | /PS8 | | |
| 34 | PN4 | 69 | VSS | 104 | VSS | | |
| 35 | /PN4 | 70 | PS0 | 105 | NC | | |

Back side

| No. | Name | No. | Name | No. | Name | No. | Name |
|---|---|---|---|---|---|---|---|
| 121 | VDD | 156 | VSS | 191 | /SS0 | 226 | NC |
| 122 | VDD | 157 | SN5 | 192 | VSS | 227 | VSS |
| 123 | VDD | 158 | /SN5 | 193 | SS1 | 228 | SCK |
| 124 | VSS | 159 | VSS | 194 | /SS1 | 229 | /SCK |
| 125 | VDD | 160 | SN13 | 195 | VSS | 230 | VSS |
| 126 | VDD | 161 | /SN13 | 196 | SS2 | 231 | VDD |
| 127 | VDD | 162 | VSS | 197 | /SS2 | 232 | VDD |
| 128 | VSS | 163 | VSS | 198 | VSS | 233 | VDD |
| 129 | VCC | 164 | NC | 199 | SS3 | 234 | VSS |
| 130 | VCC | 165 | NC | 200 | /SS3 | 235 | VDD |
| 131 | VSS | 166 | VSS | 201 | VSS | 236 | VDD |
| 132 | VCC | 167 | VSS | 202 | SS4 | 237 | VTT |
| 133 | VCC | 168 | SN12 | 203 | /SS4 | 238 | VDDSPD |
| 134 | VSS | 169 | /SN12 | 204 | VSS | 239 | SA0 |
| 135 | VTT | 170 | VSS | 205 | VSS | 240 | SA1 |
| 136 | VID0 | 171 | SN6 | 206 | NC | | |
| 137 | M_TEST | 172 | /SN6 | 207 | NC | | |
| 138 | VSS | 173 | VSS | 208 | VSS | | |
| 139 | NC | 174 | SN7 | 209 | VSS | | |
| 140 | NC | 175 | /SN7 | 210 | SS9 | | |
| 141 | VSS | 176 | VSS | 211 | /SS9 | | |
| 142 | SN0 | 177 | SN8 | 212 | VSS | | |
| 143 | /SN0 | 178 | /SN8 | 213 | SS5 | | |
| 144 | VSS | 179 | VSS | 214 | /SS5 | | |
| 145 | SN1 | 180 | SN9 | 215 | VSS | | |
| 146 | /SN1 | 181 | /SN9 | 216 | SS6 | | |
| 147 | VSS | 182 | VSS | 217 | /SS6 | | |
| 148 | SN2 | 183 | SN10 | 218 | VSS | | |
| 149 | /SN2 | 184 | /SN10 | 219 | SS7 | | |
| 150 | VSS | 185 | VSS | 220 | /SS7 | | |
| 151 | SN3 | 186 | SN11 | 221 | VSS | | |
| 152 | /SN3 | 187 | /SN11 | 222 | SS8 | | |
| 153 | VSS | 188 | VSS | 223 | /SS8 | | |
| 154 | SN4 | 189 | VSS | 224 | VSS | | |
| 155 | /SN4 | 190 | SS0 | 225 | NC | | |

## Pin Description

| Pin name | Pin Type | Function |
|---|---|---|
| SCK, /SCK | Input | System clock input |
| PN0 to PN13, /PN0 to /PN13 | Output | Primary northbound data |
| PS0 to PS9, /PS0 to /PS9 | Input | Primary southbound data |
| SN0 to SN13, /SN0 to /SN13 | Input | Secondary northbound data |
| SS0 to SS9, /SS0 to /SS9 | Output | Secondary southbound data |
| SCL | Input | Serial presence detect (SPD) clock input |
| SDA | Input / Output | SPD data and AMB SMBus address/data |
| SA0 to SA2*[1] | Input | SPD address inputs |
| VID0 to VID1*[2] | Input | Voltage ID |
| /RESET | Input | AMB reset signal |
| M_TEST*[3] | Input | VREF margin test input |
| NC | — | No connection |
| VCC | Power supply | AMB core power and AMB channel interface power (1.5V) |
| VDD | Power supply | DRAM power and AMB DRAM I/O power (1.8V) |
| VTT | Power supply | DRAM address, Command and clock termination voltage (VDD/2) |
| VDDSPD | Power supply | SPD power (3.3V) |
| VSS | — | Ground |

Notes: 1. They are also used to select the DIMM number in the AMB.
2. These pins must be unconnected.
3. Don't connect in a system.

## Electrical Specifications

- All voltages are referenced to VSS (GND).

### Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Voltage on any pin relative to VSS | VIN/VOUT | –0.3 to +1.75 | V | |
| AMB core power voltage relative to VSS | VCC | –0.3 to +1.75 | V | |
| DRAM interface power voltage relative to VSS | VDD | –0.5 to +2.30 | V | |
| Termination voltage relative to VSS | VTT | –0.5 to +2.30 | V | |
| Storage temperature | Tstg | –55 to +100 | °C | |

### Caution

**Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Operating Temperature Conditions

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| SDRAM component case temperature | TC_DRAM | 0 to +95 | °C | 1 |
| AMB component case temperature | TC_AMB | 110 | °C | |

Note: 1. Supporting 0°C to +85°C and being able to extend to +95°C with doubling auto-refresh commands in frequency to a 32ms period (tREFI = 3.9µs) and higher temperature self-refresh entry via the control of EMRS (2) bit A7 is required.

### DC Operating Conditions

| Parameter | Symbol | min. | typ. | max. | Unit | Note |
|---|---|---|---|---|---|---|
| AMB supply voltage | VCC | 1.455 | 1.50 | 1.575 | V | |
| DDR2 SDRAM supply voltage | VDD | 1.7 | 1.8 | 1.9 | V | |
| Input termination voltage | VTT | 0.48 × VDD | 0.50 × VDD | 0.52 × VDD | V | |
| EEPROM supply voltage | VDDSPD | 3.0 | 3.3 | 3.6 | V | |
| SPD input high voltage | VIH (DC) | 2.1 | — | VDDSPD | V | 1 |
| SPD input low voltage | VIL (DC) | — | — | 0.8 | V | 1 |
| RESET input high voltage | VIH (DC) | 1.0 | — | — | V | 2 |
| RESET input low voltage | VIL (DC) | — | — | 0.5 | V | 2 |
| Leakage current (RESET) | IL | –90 | — | 90 | µA | 2 |
| Leakage current (link) | IL | –5 | — | 5 | µA | 3 |

Notes: 1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal /RESET.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.

### AMB Component Timing

For purposes of IDD testing, the following parameters are to be utilized.

| Parameter | Symbol | min. | typ. | max. | Units | Note |
|---|---|---|---|---|---|---|
| EI Assertion pass-thru timing | tEI propagate | — | — | 4 | clks | |
| EI deassertion pass-thru timing | tEID | — | — | bit lock | clks | |
| EI assertion duration | tEI | 100 | — | — | clks | |
| Resample pass-thru time | | — | TBD | — | ns | |
| Resynch pass-thru Time | | — | TBD | — | ns | |
| Bit lock Interval | tBitLock | — | — | 119 | frames | |
| Frame lock Interval | tFrameLock | — | — | 154 | frames | |

Note: 1. The EI stands for ″Electrical Idle″.

### Power Specification Parameter and Test Conditions

| | | | -6E | -5C | | | |
|---|---|---|---|---|---|---|---|
| Frequency (Mbps) | | | 667 | 533 | | | |
| Parameter | Symbol | Power Supply | max. | max. | Unit | Conditions | Note |
| Idle Current, single or last DIMM | Idd_Idle_0 | @1.5V | 2.60 | 2.20 | A | L0 state, idle (0 BW)<br>Primary channel enabled,<br>Secondary channel disabled<br>CKE high. Command and address lines stable.<br>DRAM clock active. | |
| | | @1.8V | 3.10 | 2.83 | A | | |
| | | Total | 9.14 | 7.99 | W | | |
| Idle Current, first DIMM | Idd_Idle_1 | @1.5V | 3.40 | 3.00 | A | L0 state, idle (0 BW)<br>Primary and secondary channels enabled<br>CKE high. Command and address lines stable.<br>DRAM clock active. | |
| | | @1.8V | 3.10 | 2.83 | A | | |
| | | Total | 10.39 | 9.25 | W | | |
| Active Power | Idd_Active_1 | @1.5V | 3.90 | 3.40 | A | L0 state<br>50% DRAM BW, 67% read, 33% write.<br>Primary and secondary channels enabled.<br>DRAM clock active, CKE high. | |
| | | @1.8V | 5.95 | 5.89 | A | | |
| | | Total | 16.60 | 15.68 | W | | |
| Active Power, data pass through | Idd_Active_2 | @1.5V | 3.70 | 3.20 | A | L0 state<br>50% DRAM BW to downstream DIMM, 67% read, 33% write.<br>Primary and secondary channels enabled.<br>CKE high. Command and address lines stable.<br>DRAM clock active. | |
| | | @1.8V | 2.59 | 2.36 | A | | |
| | | Total | 9.89 | 8.66 | W | | |
| Training | Idd_Training (for AMB spec. Not in SPD) | @1.5V | 4.00 | 3.50 | A | Primary and secondary channels enabled.<br>100% toggle on all channel lanes<br>DRAMs idle. 0 BW.<br>CKE high, Command and address lines stable.<br>DRAM clock active. | |
| | | @1.8V | 2.81 | 2.49 | A | | |
| | | Total | 10.79 | 9.40 | W | | |

**Reference Clock Input Specifications*[1]**

| Parameter | Symbol | min. | max. | Units | Notes |
|---|---|---|---|---|---|
| Reference clock frequency@ 3.2Gb/s (nominal 133.33MHz) | fRefclk-3.2 | 126.67 | 133.40 | MHz | 2, 3, 4 |
| Reference clock frequency@ 4.0 Gb/s (nominal 166.67MHz) | fRefclk-4.0 | 158.33 | 166.75 | MHz | 2, 3, 4 |
| Single-ended maximum voltage | Vmax | — | 1.15 | V | 5, 7 |
| Single-ended minimum voltage | Vmin | –0.3 | — | V | 5, 8 |
| Differential voltage high | VRefclk-diff-ih | 150 | — | mV | 6 |
| Differential voltage low | VRefclk-diff-il | — | –150 | mV | 6 |
| Absolute crossing point | VCross | 250 | 550 | mV | 5, 9, 10 |
| VCross variation | VCross-delta | — | 140 | mV | 5, 9, 11 |
| AC common mode | VSCK-cm-acp-p | — | 225 | mV | 12 |
| Rising and falling edge rates | ERRefclk-diff-Rise, ERRefclk-diff-Fall | 0.6 | 4.0 | V/ns | 6, 13 |
| % Mismatch between rise and fall edge rates | ERRefclk-Match | — | 20 | % | 6, 14 |
| Duty cycle of reference clock | TRefclk-Dutycycle | 40 | 60 | % | 6 |
| Ringback voltage threshold | VRB-diff | –100 | 100 | mV | 6, 15 |
| Allowed time before ringback | TStable | 500 | — | ps | 6, 15 |
| Clock leakage current | II_CK | –10 | 10 | µA | 16, 17 |
| Clock input capacitance | CI_CK | 0.5 | 2.0 | pF | 17 |
| Clock input capacitance delta | CI_CK (Δ) | –0.25 | 0.25 | pF | Difference between RefClk and RefClk# input capacitance |
| Transport delay | TD | — | 5 | ns | 18, 19 |
| | NSAMPLE | $10^{12}$ | — | periods | 20 |
| Reference clock jitter (rms), filtered | TREF-JITTER-RMS | — | 3.0 | ps | 21, 22 |
| Reference clock jitter (peak-to-peak) due to spectrum clocking effects | TREF-SSCp-p | — | 30 | ps | |
| Reference clock jitter difference between adjacent AMB | TREF-JITTER-DELTA | — | TBD | ps | |

Notes: 1. For details, refer to the JEDEC specification “FB-DIMM High Speed Differential PTP Link at 1.5V”.

2. The nominal reference clock frequency is determined by the data frequency of the link divided by 2 times the fixed PLL multiplication factor for the FB-DIMM channel (6:1). fdata = 2000MHz for a 4.0Gbps FB-DIMM channel and so on.
3. Measured with SSC disabled. Enabling SSC will reduce the reference clock frequency.
4. Not all FB-DIMM agents will support all frequencies; compliance to the frequency specifications is only required for those data rates that are supported by the device under test.
5. Measurement taken from single-ended waveform.
6. Measurement taken from differential waveform.
7. Defined as the maximum instantaneous voltage including overshoot.
8. Defined as the minimum instantaneous voltage including undershoot.
9. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
10. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
11. Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in for any particular system.
12. The majority of the reference clock AC common mode occurs at high frequency (i.e., the reference clock frequency).

13. Measured from –150mV to + 150mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential 0V crossing.
14. Edge rate matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ± 75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations. The rising edge rate of REFCLK+ should be compared to the falling edge rate of REFCLK-. The maximum allowed difference should not exceed 20% of the slowest edge
15. Tstable is the time the differential clock must maintain a minimum ±150mV differential voltage after rising /falling edges before it is allowed to droop back into the ±100mV differential range.
16. Measured with a single-ended input voltage of 1V.
17. Applies to RefClk and RefClk#.
18. This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter TREF-JITTER.
19. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
20. Direct measurement of phase jitter records over NSAMPLE periods may be impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at NSAMPLE samples extrapolated from an estimate of the sigma of the random jitter components.
21. Measured with SSC enabled on reference clock generator.
22. As “measured” after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRX-Total-MIN parameters.

**Differential Transmitter Output Specifications*[1]**

| Parameter | Symbol | min. | max. | Unit | Comments |
|---|---|---|---|---|---|
| Differential peak-to-peak output voltage for large voltage swing | VTX-DIFFp-p_L | 900 | 1300 | mV | VTX-DIFFp-p = 2 × \| VTX-D+ – VTX-D- \| Measured as note 2 |
| Differential peak-to-peak output voltage for regular voltage swing | VTX-DIFFp-p_R | 800 | — | mV | VTX-DIFFp-p = 2 × \| VTX-D+ – VTX-D- \| Measured as note 2 |
| Differential peak-to-peak output voltage for small voltage swing | VTX-DIFFp-p_S | 520 | — | mV | VTX-DIFFp-p = 2 × \| VTX-D+ – VTX-D- \| Measured as note 2 |
| DC common code output voltage for large voltage swing | VTX-CM_L | — | 375 | mV | Defined as: VTX-CM = DC (avg) of \|VTX-D+ + VTX-D-\|/2 Measured as note 2 |
| DC common code output voltage for small voltage swing | VTX-CM_S | 135 | 280 | mV | Defined as: VTX-CM = DC (avg) of \|VTX-D+ + VTX-D-\|/2 Measured as note 2. See also note 3 |
| De-emphasized differential output voltage ratio for -3.5dB de-emphasis | VTX-DE-3.5-Ratio | –3.0 | –4.0 | dB | 2, 4, 5 |
| De-emphasized differential output voltage ratio for -6dB de-emphasis | VTX-DE-6.0-Ratio | –5.0 | –7.0 | dB | 2, 4, 5 |
| AC peak-to-peak common mode output voltage for large swing | VTX-CM-ACp-p L | — | 90 | mV | VTX-CM-AC = Max \|VTX-D+ + VTX-D-\|/2 – Min \|VTX-D+ + VTX-D-\|/2 Measured as note 2. See also note 6 |
| AC peak-to-peak common mode output voltage for regular swing | VTX-CM-ACp-p R | — | 80 | mV | VTX-CM-AC = Max \|VTX-D+ + VTX-D-\|/2 – Min \|VTX-D+ + VTX-D-\|/2 Measured as note 2. See also note 6 |
| AC peak-to-peak common mode output voltage for small swing | VTX-CM-ACp-p S | — | 70 | mV | VTX-CM-AC = Max \|VTX-D+ + VTX-D-\|/2 – Min \|VTX-D+ + VTX-D-\|/2 Measured as note 2. See also note 6 |
| Maximum single-ended voltage in EI condition, DC + AC | VTX-IDLE-SE | — | 50 | mV | 7, 8 |
| Maximum single-ended voltage in EI condition, DC only | VTX-IDLE-SE-DC | — | 20 | mV | 7, 8, 9 |
| Maximum peak-to-peak differential voltage in EI condition | VTX-IDLE-DIFFp-p | — | 40 | mV | 8 |
| Single-ended voltage (w.r.t.VSS) on D+/D- | VTX-SE | –75 | 750 | mV | 2, 10 |
| Minimum TX eye width | TTX-Eye-MIN | 0.7 | — | UI | 2, 11, 12 |
| Maximum TX deterministic jitter | TTX-DJ-DD | — | 0.2 | UI | 2, 11, 12, 13 |
| Instantaneous pulse width | TTX-PULSE | 0.85 | — | UI | 14 |
| Differential TX output rise/fall time | TTX-RISE, TTX-FALL | 30 | 90 | ps | Given by 20%-80% voltage levels. Measured as note 2 |
| Mismatch between rise and fall times | TTX-RF-MISMATCH | — | 20 | ps | |
| Differential return loss | RLTX-DIFF | 8 | — | dB | Measured over 0.1GHz to 2.4GHz. See also note 15 |
| Common mode return loss | RLTX-CM | 6 | — | dB | Measured over 0.1GHz to 2.4GHz. See also note 15 |

| Parameter | Symbol | min. | max. | Unit | Comments |
|---|---|---|---|---|---|
| Transmitter termination resistance | RTX | 41 | 55 | Ω | 16 |
| D+/D- TX resistance difference | RTX-Match-DC | — | 4 | % | RTX-Match-DC = 2×\|RTX-D+ – RTX-D-\| / (RTX-D+ + RTX-D-) Bounds are applied separately to high and low output voltage states |
| Lane-to-lane skew at TX | LTX-SKEW 1 | — | 100 + 3UI | ps | 17, 19 |
| Lane-to-lane skew at TX | LTX-SKEW 2 | — | 100 + 2UI | ps | 18, 19 |
| Maximum TX Drift (resync mode) | TTX-DRIFT-RESYNC | — | 240 | ps | 20 |
| Maximum TX Drift (resample mode only) | TTX-DRIFT-RESAMPLE | — | 120 | ps | 20 |
| Bit Error Ratio | BER | — | $10^{-12}$ | | 21 |

Notes: 1. For details, refer to the JEDEC specification “FB-DIMM High Speed Differential PTP Link at 1.5V”.

2. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.
3. The transmitter designer should not artificially elevate the common mode in order to meet this specification.
4. This is the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
5. De-emphasis shall be disabled in the calibration state.
6. Includes all sources of AC common mode noise.
7. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
8. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.
9. This specification, considered with VRX-IDLE-SE-DC, implies a maximum 15mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26mV when worst case termination resistance matching is considered.
10. The maximum value is specified to be at least (VTX-DIFFp-p L / 4) + VTX-CM L + (VTX-CM-ACp-p / 2)
11. This number does not include the effects of SSC or reference clock jitter.
12. These timing specifications apply to resync mode only.
13. Defined as the dual-dirac deterministic jitter.
14. Pulse width measured at 0 V differential.
15. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
16. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed ± 5Ω. with regard to the average of the values measured at 100mV and at 400mV for that pin.
17. Lane to Lane skew at the Transmitter pins for an end component.
18. Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
19. This is a static skew. An FB-DIMM component is not allowed to change its lane to lane phase relationship after initialization.
20. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
21. BER per differential lane.

**Differential Receiver Input Specifications*[1]**

| Parameter | Symbol | min. | max. | Unit | Comments |
|---|---|---|---|---|---|
| Differential peak-to-peak input voltage | VRX-DIFFp-p | 170 | 1300 | mV | VRX-DIFFp-p = 2×\|VRX-D+ -VRX-D-\| Measured as note 2 |
| Maximum single-ended voltage for EI condition (AC + DC) | VRX-IDLE-SE | — | 65 | mV | 3, 4, 5, 6 |
| Maximum single-ended voltage for EI condition (DC only) | VRX-IDLE-SE-DC | — | 35 | mV | 3, 4, 5, 6, 7 |
| Maximum peak-to-peak differential voltage for EI condition | VRX-IDLE-DIFFp-p | — | 65 | mV | 4, 5, 6 |
| Single-ended voltage (w.r.t. VSS) on D+/D- | VRX-SE | –300 | 900 | mV | 5 |
| Single-pulse peak differential input voltage | VRX-DIFF-PULSE | 85 | — | mV | 5, 8 |
| Amplitude ratio between adjacent symbols, 1100mV < VRX-DIFFp-p <= 1300mV | VRX-DIFF-ADJ RATIO- HI | — | 3.0 | | 5, 9 |
| Amplitude ratio between adjacent symbols, VRX-DIFFp-p <= 1100mV | VRX-DIFF-ADJ RATIO | — | 4.0 | | 5, 9 |
| Maximum RX inherent timing error | TRX-TJ-MAX | — | 0.4 | UI | 5, 10, 11 |
| Maximum RX inherent deterministic timing error | TRX-DJ-DD | — | 0.3 | UI | 5, 10, 11, 12 |
| Single-pulse width at zero-voltage crossing | TRX-PW-ZC | 0.55 | — | UI | 5, 8 |
| Single-pulse width at minimum-level crossing | TRX-PW-ML | 0.2 | — | UI | 5, 8 |
| Differential RX input rise/fall time | TRX-RISE, TRX-FALL | 50 | — | ps | Given by 20%-80% voltage levels. |
| Common mode of the input voltage | VRX-CM | 120 | 400 | mV | Defined as: VRX-CM = DC (avg) of \|VRX-D+ + VRX-D-\|/2 Measured as note 2. See also note 13 |
| AC peak-to-peak common mode of input voltage | VRX-CM-ACp-p | — | 270 | mV | VRX-CM-AC = Max \|VRX-D+ + VRX-D-\|/2 – Min \|VRX-D+ + VRX-D-\|/2 Measured as note 2 |
| Ratio of VRX-CM-ACp-p to minimum VRX-DIFFp-p | VRX-CM-EH-Ratio | — | 45 | % | 14 |
| Differential return loss | RLRX-DIFF | 9 | — | dB | Measured over 0.1GHz to 2.4GHz. See also note 15 |
| Common mode return loss | RLRX-CM | 6 | — | dB | Measured over 0.1GHz to 2.4GHz. See also note 15 |
| RX termination resistance | RRX | 41 | 55 | Ω | 16 |
| D+/D- RX resistance difference | RRX-Match-DC | — | 4 | % | RRX-Match-DC = 2×\|RRX-D+ – RRX-D-\| / (RRX-D+ + RRX-D-) |
| Lane-to-lane PCB skew at Rx | LRX-PCB-SKEW | — | 6 | UI | Lane-to-lane PCB skew at the receiver that must be tolerated. See also note 17 |
| Minimum RX Drift Tolerance | TRX-DRIFT | 400 | — | ps | 18 |
| Minimum data tracking 3dB bandwidth | FTRK | 0.2 | — | MHz | 19 |
| Electrical idle entry detect time | TEI-ENTRY -DETECT | — | 60 | ns | 20 |
| Electrical idle exit detect time | TEI-EXIT -DETECT | — | 30 | ns | |
| Bit Error Ratio | BER | — | $10^{-12}$ | | 21 |

Notes: 1. For details, refer to the JEDEC specification “FB-DIMM High Speed Differential PTP Link at 1.5V”.

2. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
3. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined by comparing EI levels with common mode levels during normal operation for the case with transmitter using small voltage swing.
4. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
5. Specified at the package pins into a timing and voltage compliance test setup.
6. Receiver designers may implement either single-ended or differential EI detection. Receivers must meet the specification that corresponds to the implemented detection circuit.
7. This specification, considered with VTX-IDLE-SE-DC, implies a maximum 15mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26mV when worst case termination resistance matching is considered.
8. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eye mask.
9. The relative amplitude ratio limit between adjacent symbols prevents excessive inter-symbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
10. This number does not include the effects of SSC or reference clock jitter.
11. This number includes setup and hold of the RX sampling flop.
12. Defined as the dual-dirac deterministic timing error.
13. Allows for 15mV DC offset between transmit and receive devices.
14. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if VRX-DIFFp-p is 200mV, the maximum AC peak-to-peak common mode is the lesser of (200mV $\times$ 0.45 = 90mV) and VRX-CM-ACp-p.
15. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
16. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed ± 5Ω. with regard to the average of the values measured at 100mV and at 400mV for that pin.
17. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
18. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
19. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2MHz is 0.05UI.
20. The specified time includes the time required to forward the EI entry condition.
21. BER per differential lane.

## Serial PD Matrix for FB-DIMM

| Byte No. | Function described | Byte value | Hex value |
|---|---|---|---|
| 0 | Number of serial PD bytes written / SPD device size / CRC coverage | 116 | 92H |
| 1 | SPD revision | Revision 1.1 | 11H |
| 2 | Key byte / DRAM device type | DDR2 SDRAM FB-DIMM | 09H |
| 3 | Voltage levels of this assembly | VDD = 1.8V, VCC = 1.5V | 12H |
| 4 | SDRAM addressing | 14-row, 11-column, 8-bank | 49H |
| 5 | Module physical attributes | 8.2mm | 24H |
| 6 | Module Type / Thickness | FB-DIMM | 07H |
| 7 | Module organization | 2 ranks / 4bits | 10H |
| 8 | Fine timebase (FTB) dividend / divisor | | 00H |
| 9 | Medium timebase dividend | 1 | 01H |
| 10 | Medium timebase divisor | 4 | 04H |
| 11 | SDRAM minimum cycle time (tCK (min.))<br>-6E | 3.00ns | 0CH |
| | -5C | 3.75ns | 0FH |
| 12 | SDRAM maximum cycle time (tCK (max.)) | 8ns | 20H |
| 13 | SDRAM /CAS latencies supported<br>-6E | CL = 3, 4, 5 | 33H |
| | -5C | CL = 3, 4 | 23H |
| 14 | SDRAM minimum /CAS latencies time (tCAS) | 15ns | 3CH |
| 15 | SDRAM write recovery times supported<br>-6E | WR = 2 to 5 | 42H |
| | -5C | WR = 2 to 4 | 32H |
| 16 | SDRAM write recovery time (tWR) | 15ns | 3CH |
| 17 | SDRAM write latencies supported | WL = 2 to 5 | 42H |
| 18 | SDRAM additive latencies supported | AL = 0 to 3 | 40H |
| 19 | SDRAM minimum /RAS to /CAS delay (tRCD) | 15ns | 3CH |
| 20 | SDRAM minimum row active to row active delay (tRRD) | 7.5ns | 1EH |
| 21 | SDRAM minimum row precharge time (tRP) | 15ns | 3CH |
| 22 | SDRAM upper nibbles for tRAS and tRC | | 00H |
| 23 | SDRAM minimum active to precharge time (tRAS) | 45ns | B4H |
| 24 | SDRAM minimum auto-refresh to active /auto-refresh time (tRC) | 60ns | F0H |
| 25 | SDRAM minimum refresh recovery time delay (tRFC), LSB | 127.5ns | FEH |
| 26 | SDRAM minimum refresh recovery time delay (tRFC), MSB | 127.5ns | 01H |
| 27 | SDRAM Internal write to read command delay (tWTR) | 7.5ns | 1EH |
| 28 | SDRAM Internal read to precharge command delay (tRTP) | 7.5ns | 1EH |
| 29 | SDRAM burst lengths supported | BL = 4, 8 | 03H |
| 30 | SDRAM terminations supported | ODT = 50, 75, 150Ω | 07H |
| 31 | SDRAM drivers supported | Supported | 01H |
| 32 | SDRAM average refresh interval (tREFI) / double refresh mode bit / high temperature self-refresh rate support indication | 7.8µs Double/HT refresh | C2H |
| 33 | Tcasemax (TC (max.)) delta / DT4R4W delta | 95°C/ 0.00°C | 51H |
| 34 | Psi T-A SDRAM at still air | *3 | ×× |
| 35 | SDRAM DT0 | *3 | ×× |
| 36 | SDRAM DT2Q | *3 | ×× |

| Byte No. | Function described | Byte value | Hex value |
|---|---|---|---|
| 37 | SDRAM DT2P | *3 | ×× |
| 38 | SDRAM DT3N | *3 | ×× |
| 39 | SDRAM DT4R / mode bit | *3 | ×× |
| 40 | SDRAM DT5B | *3 | ×× |
| 41 | SDRAM DT7 | *3 | ×× |
| 42 to 78 | Reserved | | 00H |
| 79 | FB-DIMM ODT values | 150/75Ω | 12H |
| 80 | Reserved | | 00H |
| 81 to 93 | AMB personality bytes | | ×× |
| 94 to 97 | Reserved | | 00H |
| 98 | AMB junction temperature maximum (TJ (max.)) | | ×× |
| 99 | Category byte | Stack/FDHS | 1AH |
| 100 | Reserved | | 00H |
| 101 to 116 | AMB personality bytes | | ×× |
| 117 | Module ID: manufacturer's JEDEC ID code | Elpida Memory | 02H |
| 118 | Module ID: manufacturer's JEDEC ID code | Elpida Memory | FEH |
| 119 | Module ID: manufacturing location | | ×× |
| 120 | Module ID: manufacturing date | Year code (BCD) | ×× |
| 121 | Module ID: manufacturing date | Date code (BCD) | ×× |
| 122 to 125 | Module ID: module serial number | | ×× |
| 126 to 127 | Cyclical redundancy code | | ×× |
| 128 to 145 | Module part number | EBE41FE4ABHD | ×× |
| 146 | Module revision code | Initial | 30H |
| 147 | Module revision code | (Space) | 20H |
| 148 | SDRAM manufacturer's JEDEC ID code | Elpida Memory | 02H |
| 149 | SDRAM manufacturer's JEDEC ID code | Elpida Memory | FEH |
| 150 | Informal AMB content revision tag (MSB) | | ×× |
| 151 | Informal AMB content revision tag (LSB) | | ×× |
| 152 to 175 | Manufacturer's specific data | | 00H |
| 176 to 255 | Open for customer use | | 00H |

Remark IDD: DRAM current, ICC: AMB current

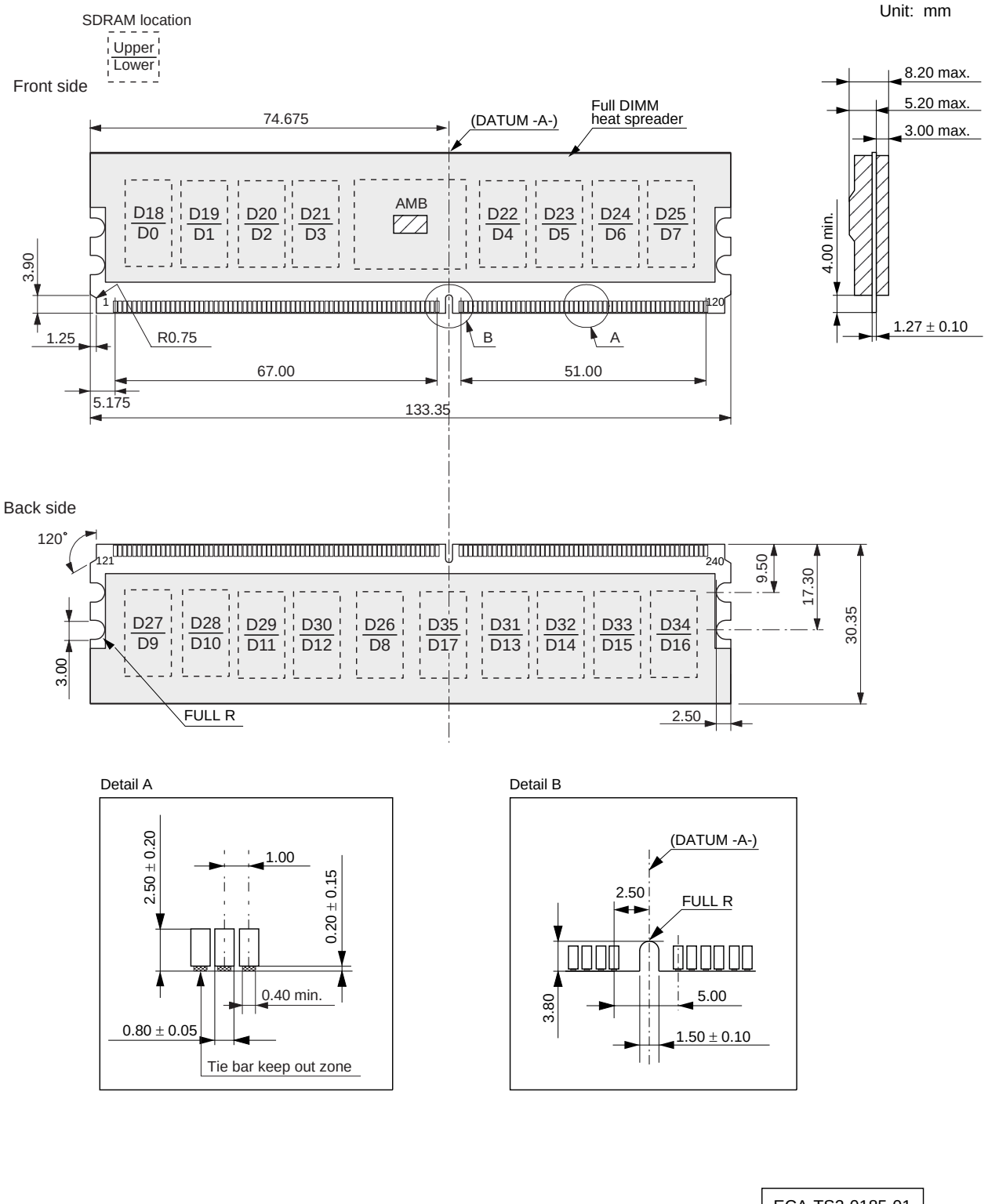
Notes: 1. Based on DDR2 SDRAM component specification.

2. Refer to JESD51-3 "Low effective thermal conductivity Test board for leaded surface mount packages" under JESD51-2 standard.

3. DT parameter is derived as following: DTx = IDDx × VDD × Psi T-A, where IDDx definition is based on JEDEC DDR2 SDRAM component specification and at VDD=1.9V, it is the datasheet (worst case) value, and Psi T-A is the programmed value of Psi T-A (value in SPD Byte 33).

## Physical Outline

Unit: mm




ECA-TS2-0185-01

## CAUTION FOR HANDLING MEMORY MODULES

**When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.**
**In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.**

**When re-packing memory modules, be sure the modules are not touching each other.**
**Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.**

MDE0202

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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