

HD14027B

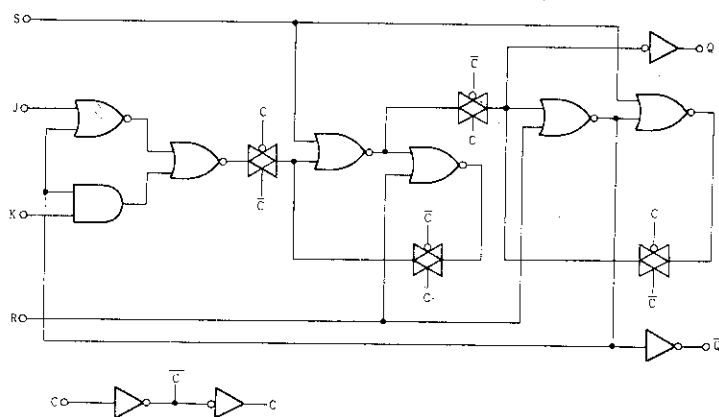
Dual J-K Flip Flop

The HD14027B dual J-K flip-flop has independent J, K, Clock (C), Set(S) and Reset(R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

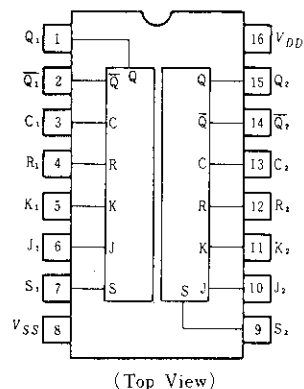
FEATURES

- Quiescent Current = 2nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Toggle Rate = 3MHz typ. @5V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B and MC14027B

LOGIC DIAGRAM (1/2)



PIN ARRANGEMENT



TRUTH TABLE

Inputs						Outputs**	
C †	J	K	S	R	Qn*	Qn+1	Qn+1
0	1	x	0	0	0	1	0
0	x	0	0	0	1	1	0
0	0	x	0	0	0	0	1
0	x	1	0	0	1	0	1
0	x	x	0	0	x	Qn	Qn
x	x	x	1	0	x	1	0
x	x	x	0	1	x	0	1
x	x	x	1	1	x	1	1

x=Don't Care
 † Level Change
 **Next State
 *Present State

■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	5.0		—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0		4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or $4.5V$	3.7	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	$V_{OH}=4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	$V_{OH}=9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	$V_{OH}=13.5V$	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	± 0.3	—	± 0.0001	± 0.3	—	± 1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	4.0	—	0.002	4.0	—	30	μA
		10		—	8.0	—	0.004	8.0	—	60	
		15		—	16	—	0.006	16	—	120	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD} ,	—	—	—	0.8	—	—	—	μA
		10	per Gate	—	—	—	1.6	—	—	—	
		15	$C_L=50pF$, $f=1kHz$	—	—	—	2.4	—	—	—	

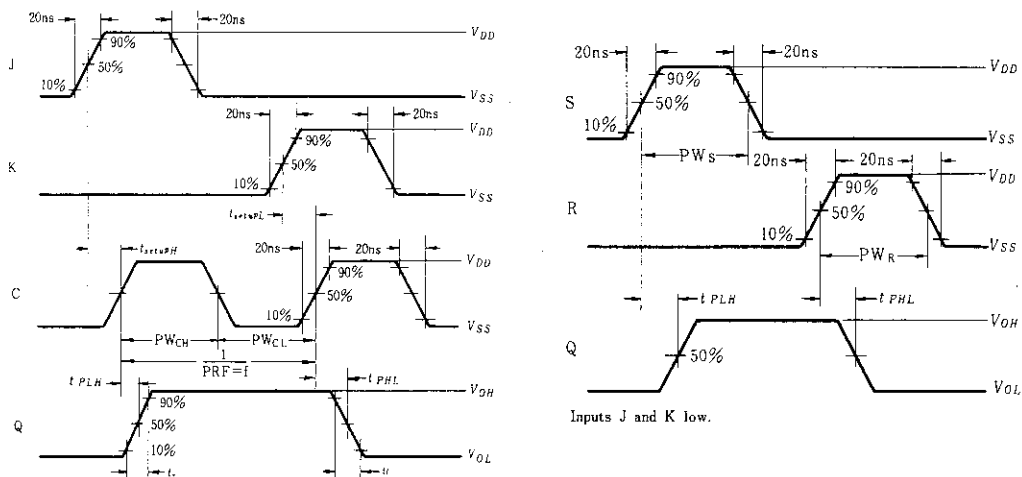
* To calculate total supply current at frequency other than 1kHz.

@ $V_{DD}=5.0V$ $I_T=(0.80\mu A/kHz)f+I_{DD}$ @ $V_{DD}=10V$ $I_T=(1.60\mu A/kHz)f+I_{DD}$ @ $V_{DD}=15V$ $I_T=(2.40\mu A/kHz)f+I_{DD}$

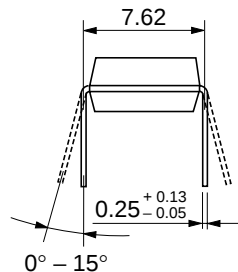
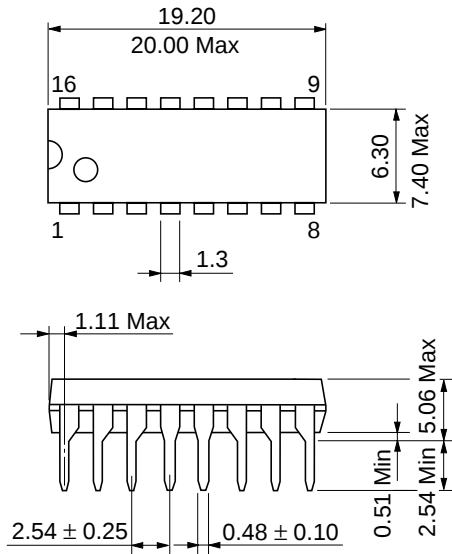
■ SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic		Symbol	$V_{DD}(V)$	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	360	ns
			10	—	90	180	
			15	—	65	130	
Output Fall Time		t_f	5.0	—	135	260	ns
			10	—	65	130	
			15	—	50	100	
Propagation Delay Time	Clock	$t_{PLH},$ t_{PHL}	5.0	—	280	400	ns
			10	—	120	200	
			15	—	95	150	
	Set		5.0	—	230	350	
			10	—	100	150	
			15	—	80	130	
	Reset		5.0	—	350	450	
			10	—	100	200	
			15	—	75	150	
Setup Time		$t_{setup\ H}$ $t_{setup\ L}$	5.0	140	70	—	ns
			10	50	25	—	
			15	35	17	—	
Clock Pulse Width		PW_{CH} PW_{CL}	5.0	330	165	—	ns
			10	110	55	—	
			15	75	38	—	
Clock Frequency		PRF	5.0	—	3.0	1.5	MHz
			10	—	9.0	4.5	
			15	—	13	6.5	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	5.0	
			15	—	—	4.0	
Set and Reset Pulse Width		$PW_S,$ PW_R	5.0	250	125	—	ns
			10	100	50	—	
			15	70	35	—	

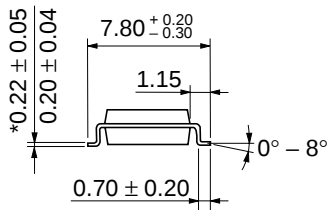
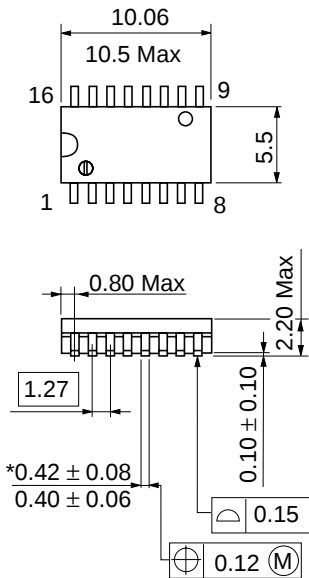
■ DYNAMIC SIGNAL WAVEFORMS



Inputs R and S low. For the measurement of PWc, PRF, and P_D the inputs, J and K are kept high.

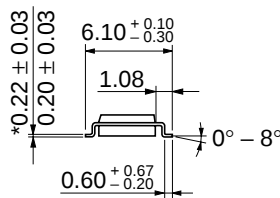
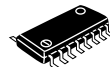


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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