Low Noise, Precision Instrumentation Amplifier

AMP01*

FEATURES

Low Offset Voltage: 50 μV Max
Very Low Offset Voltage Drift: 0.3 μV/°C Max
Low Noise: 0.12 μV p-p (0.1 Hz to 10 Hz)
Excellent Output Drive: ±10 V at ±50 mA
Capacitive Load Stability: to 1 μF
Gain Range: 0.1 to 10,000
Excellent Linearity: 16-Bit at G = 1000
High CMR: 125 dB min (G = 1000)
Low Bias Current: 4 nA Max
May Be Configured as a Precision Op Amp
Output-Stage Thermal Shutdown
Available in Die Form

GENERAL DESCRIPTION

The AMP01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high current output stage. The output remains stable with high capacitance loads (1 μF), a unique ability for an instrumentation amplifier. Consequently, the AMP01 can amplify low level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20 μV), which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.15 μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10 nA over the military temperature range. High common-mode rejection of 130 dB, 16-bit linearity at a gain of 1000, and 50 mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb dc specifications. The AMP01 slews at 4.5 V/μs into capacitive loads of up to 15 nF, settles in 50 μs to 0.01% at a gain of 1000, and boasts a healthy 26 MHz gain-bandwidth product. These features make the AMP01 ideal for high speed data acquisition systems.

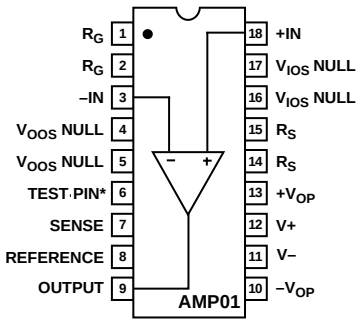
Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain temperature coefficient of 10 ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50 Ω, 500 Ω, and 2 kΩ. Loaded with 500 Ω, the output delivers ±13.0 V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP01 can also be configured as a high performance operational amplifier. In many applications, the AMP01 can be used in place of op amp/power-buffer combinations.

REV. D

PIN CONFIGURATIONS

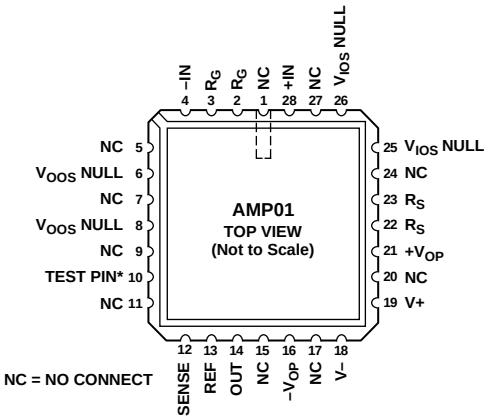
18-Lead Cerdip



TOP VIEW
(Not to Scale)

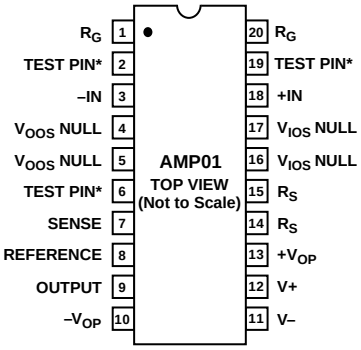
*MAKE NO ELECTRICAL CONNECTION

AMP01 BTC/883
28-Terminal LCC



*MAKE NO ELECTRICAL CONNECTION

20-Lead SOIC



*MAKE NO ELECTRICAL CONNECTION

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AMP01–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01A Min	AMP01A Typ	AMP01A Max	AMP01B Min	AMP01B Typ	AMP01B Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C		20	50		40	100	µV
		–55°C ≤ T_A ≤ +125°C		40	80		60	150	µV
Input Offset Voltage Drift	TCV_{IOS}	–55°C ≤ T_A ≤ +125°C		0.15	0.3		0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C		1	3		2	6	mV
		–55°C ≤ T_A ≤ +125°C		3	6		6	10	mV
Output Offset Voltage Drift	TCV_{OOS}	R_G = ∞							
		–55°C ≤ T_A ≤ +125°C		20	50		50	120	µV/°C
Offset Referred to Input	PSR	G = 1000	120	130		110	120		dB
vs. Positive Supply		G = 100	110	130		100	120		dB
V+ = +5 V to +15 V		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
		–55°C ≤ T_A ≤ +125°C							
		G = 1000	120	130		110	120		dB
		G = 100	110	130		100	120		dB
		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
Offset Referred to Input	PSR	G = 1000	105	125		105	115		dB
vs. Negative Supply		G = 100	90	105		90	95		dB
V– = –5 V to –15 V		G = 10	70	85		70	75		dB
		G = 1	50	65		50	60		dB
		–55°C ≤ T_A ≤ +125°C							
		G = 1000	105	125		105	115		dB
		G = 100	90	105		90	95		dB
		G = 10	70	85		70	75		dB
		G = 1	50	85		50	60		dB
Input Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V[1]		±6			±6		mV
Output Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V[1]		±100			±100		mV
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C		1	4		2	6	nA
		–55°C ≤ T_A ≤ +125°C		4	10		6	15	nA
Input Bias Current Drift	TCI_B	–55°C ≤ T_A ≤ +125°C		40			50		pA/°C
Input Offset Current	I_{OS}	T_A = +25°C		0.2	1.0		0.5	2.0	nA
		–55°C ≤ T_A ≤ +125°C		0.5	3.0		1.0	6.0	nA
Input Offset Current Drift	TCI_{OS}	–55°C ≤ T_A ≤ +125°C		3			5		pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000		1			1		GΩ
		Differential, G ≤ 100		10			10		GΩ
		Common Mode, G = 1000		20			20		GΩ
Input Voltage Range	IVR	T_A = +25°C[2]	±10.5			±10.5			V
		–55°C ≤ T_A ≤ +125°C	±10.0			±10.0			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V, 1 kΩ Source Imbalance							
		G = 1000	125	130		115	125		dB
		G = 100	120	130		110	125		dB
		G = 10	100	120		95	110		dB
		G = 1	85	100		75	90		dB
		–55°C ≤ T_A ≤ +125°C							
		G = 1000	120	125		110	120		dB
		G = 100	115	125		105	120		dB
		G = 10	95	115		90	105		dB
		G = 1	80	95		75	90		dB

NOTES

[1]V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS} respectively.

[2]Refer to section on common-mode rejection.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, –25°C ≤ T_A ≤ +85°C for E, F grades, 0°C ≤ T_A ≤ +70°C for G grade, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01E Min	AMP01E Typ	AMP01E Max	AMP01F/G Min	AMP01F/G Typ	AMP01F/G Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C		20	50		40	100	µV
		$T_{MIN} \le T_A \le T_{MAX}$		40	80		60	150	µV
Input Offset Voltage Drift	TCV_{IOS}	$T_{MIN} \le T_A \le T_{MAX}$[1]		0.15	0.3		0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C		1	3		2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$		3	6		6	10	mV
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$[1]							
		$T_{MIN} \le T_A \le T_{MAX}$		20	100		50	120	µV/°C
Offset Referred to Input vs. Positive Supply V+ = +5 V to +15 V	PSR	G = 1000	120	130		110	120		dB
		G = 100	110	130		100	120		dB
		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	130		110	120		dB
		G = 100	110	130		100	120		dB
		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
Offset Referred to Input vs. Negative Supply V– = –5 V to –15 V	PSR	G = 1000	110	125		105	115		dB
		G = 100	95	105		90	95		dB
		G = 10	75	85		70	75		dB
		G = 1	55	65		50	60		dB
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	110	125		105	115		dB
		G = 100	95	105		90	95		dB
		G = 10	75	85		70	75		dB
		G = 1	55	85		50	60		dB
Input Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V[2]		±6			±6		mV
Output Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V[2]		±100			±100		mV
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C		1	4		2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$		4	10		6	15	mV
Input Bias Current Drift	TCI_B	$T_{MIN} \le T_A \le T_{MAX}$		40			50		pA/°C
Input Offset Current	I_{OS}	T_A = +25°C		0.2	1.0		0.5	2.0	mV
		$T_{MIN} \le T_A \le T_{MAX}$		0.5	3.0		1.0	6.0	mV
Input Offset Current Drift	TCI_{OS}	$T_{MIN} \le T_A \le T_{MAX}$		3			5		pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000		1			1		GΩ
		Differential, G ≤ 100		10			10		GΩ
		Common Mode, G = 1000		20			20		GΩ
Input Voltage Range	IVR	T_A = +25°C[3]	±10.5			±10.5			V
		$T_{MIN} \le T_A \le T_{MAX}$	±10.0			±10.0			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V, 1 kΩ Source Imbalance							
		G = 1000	125	130		115	125		dB
		G = 100	120	130		110	125		dB
		G = 10	100	120		95	110		dB
		G = 1	85	100		75	90		dB
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	125		110	120		dB
		G = 100	115	125		105	120		dB
		G = 10	95	115		90	105		dB
		G = 1	80	95		75	90		dB

NOTES

[1]Sample tested.

[2]V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.

[3]Refer to section on common-mode rejection.

Specifications subject to change without notice.

AMP01
ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01A/E Min	AMP01A/E Typ	AMP01A/E Max	AMP01B/F/G Min	AMP01B/F/G Typ	AMP01B/F/G Max	Units
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from G = 1 to 1000		0.3	0.6		0.5	0.8	%
Gain Range	G		0.1		10k	0.1		10k	V/V
Nonlinearity		G = 1000[1]		0.0007	0.005		0.0007	0.005	%
		G = 100[1]			0.005			0.005	%
		G = 10[1]			0.005			0.007	%
		G = 1[1]			0.010			0.015	%
Temperature Coefficient	G_{TC}	1 ≤ G ≤ 1000[1, 2]		5	10		5	15	ppm°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	R_L = 2 kΩ	±13.0	±13.8		±13.0	±13.8		V
		R_L = 500 Ω	±13.0	±13.5		±13.0	±13.5		V
		R_L = 50 Ω	±2.5	±4.0		±2.5	±4.0		V
		R_L = 2 kΩ Over Temp.	±12.0	±13.8		±12.0	±13.8		V
		R_L = 500 Ω[3]	±12.0	±13.5		±12.0	±13.5		V
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		1 ≤ G ≤ 1000 No Oscillations[1]	0.1	1		0.1	1		µF
Thermal Shutdown Temperature		Junction Temperature		165			165		°C
NOISE									
Voltage Density, RTI	e_n	f_O = 1 kHz							
	e_n	G = 1000		5			5		nV/√Hz
	e_n	G = 100		10			10		nV/√Hz
	e_n	G = 10		59			59		nV/√Hz
	e_n	G = 1		540			540		nV/√Hz
Noise Current Density, RTI	i_n	f_O = 1 kHz, G = 1000		0.15			0.15		pA/√Hz
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz							
	e_n p-p	G = 1000		0.12			0.12		µV p-p
	e_n p-p	G = 100		0.16			0.16		µV p-p
	e_n p-p	G = 10		1.4			1.4		µV p-p
	e_n p-p	G = 1		13			13		µV p-p
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz, G = 1000		2			2		pA p-p
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3 dB)	BW	G = 1		570			570		kHz
		G = 10		100			100		kHz
		G = 100		82			82		kHz
		G = 1000		26			26		kHz
Slew Rate	SR	G = 10	3.5	4.5		3.0	4.5		V/µs
Settling Time	t_S	To 0.01%, 20 V step							
		G = 1		12			12		µs
		G = 10		13			13		µs
		G = 100		15			15		µs
		G = 1000		50			50		µs

NOTES
[1]Guaranteed by design.
[2]Gain tempco does not include the effects of gain and scale resistor tempco match.
[3]–55°C ≤ T_A ≤ +125°C for A/B grades, –25°C ≤ T_A ≤ +85°C for E/F grades, 0°C ≤ T_A ≤ 70°C for G grades.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01A/E Min	AMP01A/E Typ	AMP01A/E Max	AMP01B/F/G Min	AMP01B/F/G Typ	AMP01B/F/G Max	Units
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–		280			280		µA
Voltage Range		(Note 1)	–10.5		+15	–10.5		+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–		280			280		µA
Voltage Range		(Note 1)	–10.5		+15	–10.5		+15	V
Gain to Output				1			1		V/V
POWER SUPPLY –25°C ≤ T_A ≤ +85°C for E/F Grades, –55°C ≤ T_A ≤ +125°C for A/B Grades									
Supply Voltage Range	V_S	+V linked to $+V_{OP}$	±4.5		±18	±4.5		±18	V
	V_S	–V linked to $–V_{OP}$	±4.5		±18	±4.5		±18	V
Quiescent Current	I_Q	+V linked to $+V_{OP}$		3.0	4.8		3.0	4.8	mA
	I_Q	–V linked to $–V_{OP}$		3.4	4.8		3.4	4.8	mA

NOTE
[1]Guaranteed by design.
Specifications subject to change without notice.

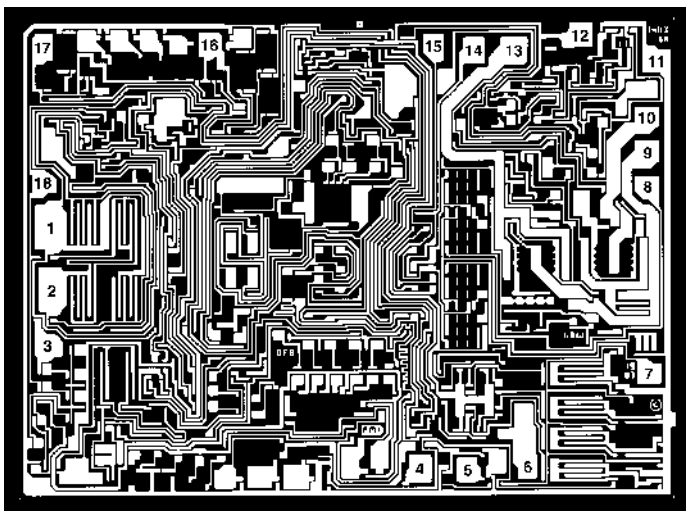
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AMP01AX	–55°C to +125°C	18-Lead Cerdip	Q-18
AMP01AX/883C	–55°C to +125°C	18-Lead Cerdip	Q-18
AMP01BTC/883C	–55°C to +125°C	28-Terminal LCC	E-28A
AMP01BX	–55°C to +125°C	18-Lead Cerdip	Q-18
AMP01BX/883C	–55°C to +125°C	18-Lead Cerdip	Q-18
AMP01EX	–25°C to +85°C	18-Lead Cerdip	Q-18
AMP01FX	–25°C to +85°C	18-Lead Cerdip	Q-18
AMP01GBC		Die	
AMP01GS	0°C to +70°C	20-Lead SOIC	R-20
AMP01GS-REEL	0°C to +70°C	13" Tape and Reel	R-20
AMP01NBC		Die	
5962-8863001VA*	–55°C to +125°C	18-Lead Cerdip	Q-18
5962-88630023A*	–55°C to +125°C	28-Terminal LCC	E-28A
5962-8863002VA*	–55°C to +125°C	18-Lead Cerdip	Q-18

*Standard military drawing available.

DICE CHARACTERISTICS

Die Size 0.111 × 0.149 inch, 16,539 sq. mils
(2.82 × 3.78 mm, 10.67 sq. mm)



1. R_G
2. R_G
3. –INPUT
4. V_{OOS} NULL
5. V_{OOS} NULL
6. TEST PIN*
7. SENSE
8. REFERENCE
9. OUTPUT
10. V– (OUTPUT)
11. V–
12. V+
13. V+ (OUTPUT)
14. R_S
15. R_S
16. V_{IOS} NULL
17. V_{IOS} NULL
18. +INPUT

*MAKE NO ELECTRICAL CONNECTION

AMP01

WAFER TEST LIMITS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01NBC Limit	AMP01GBC Limit	Units
Input Offset Voltage	V_{IOS}		60	120	µV max
Output Offset Voltage	V_{OOS}		4	8	mV max
Offset Referred to Input	PSR	V+ = +5 V to +15 V			dB min
vs. Positive Supply		G = 1000	120	110	dB min
		G = 100	110	100	dB min
		G = 10	95	90	dB min
		G = 1	75	70	dB min
Offset Referred to Input	PSR	V– = –5 V to –15 V			dB min
vs. Negative Supply		G = 1000	105	105	dB min
		G = 100	90	90	dB min
		G = 10	70	70	dB min
		G = 1	50	50	dB min
Input Bias Current	I_B		4	8	nA max
Input Offset Current	I_{OS}		1	3	nA max
Input Voltage Range	IVR	Guaranteed by CMR Tests	±10	±10	V min
Common Mode Rejection	CMR	V_{CM} = ±10 V			dB min
		G = 1000	125	115	dB min
		G = 100	120	110	dB min
		G = 10	100	95	dB min
		G = 1	85	75	dB min
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$	0.6	0.8	% max
Output Voltage Swing	V_{OUT}	R_L = 2 kΩ	±13	±13	V min
	V_{OUT}	R_L = 500 Ω	±13	±13	V min
	V_{OUT}	R_L = 50 Ω	±2.5	±2.5	V min
Output Current Limit		Output to Ground Short	±60	±60	mA min
Output Current Limit		Output to Ground Short	±120	±120	mA max
Quiescent Current	I_Q	+V Linked to $+V_{OP}$	4.8	4.8	mA max
		–V Linked to $–V_{OP}$	4.8	4.8	mA max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

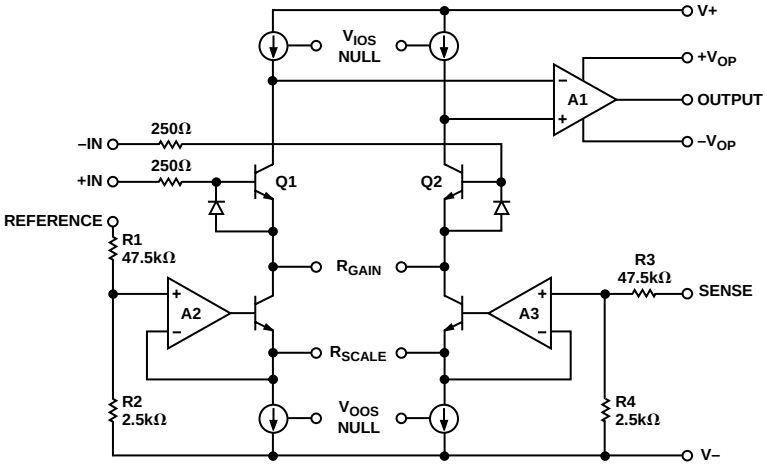


Figure 1. Simplified Schematic

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AMP01 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	AMP01NBC Typical	AMP01GBC Typical	Units
Input Offset Voltage Drift	TCV_{IOS}		0.15	0.30	µV/°C
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	20	50	µV/°C
Input Bias Current Drift	TCI_B		40	50	pA/°C
Input Offset Current Drift	TCI_{OS}		3	5	pA/°C
Nonlinearity		G = 1000	0.0007	0.0007	%
Voltage Noise Density	e_n	G = 1000			
		f_O = 1 kHz	5	5	nV/$\sqrt{Hz}$
Current Noise Density	i_n	G = 1000			
		f_O = 1 kHz	0.15	0.15	pA/$\sqrt{Hz}$
Voltage Noise	e_n p-p	G = 1000			
		0.1 Hz to 10 Hz	0.12	0.12	µV p-p
Current Noise	i_n p-p	G = 1000	2	2	pA p-p
		0.1 Hz to 10 Hz			
Small-Signal Bandwidth (–3 dB)	BW	G = 1000	26	26	kHz
Slew Rate	SR	G = 10	4.5	4.5	V/µs
Settling Time	t_S	To 0.01%, 20 V Step			
		G = 1000	50	50	µs

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

AMP01–Typical Performance Characteristics

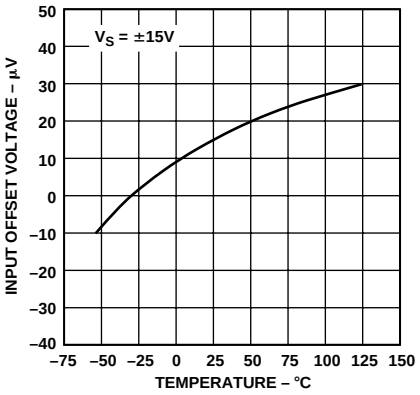


Figure 2. Input Offset Voltage vs. Temperature

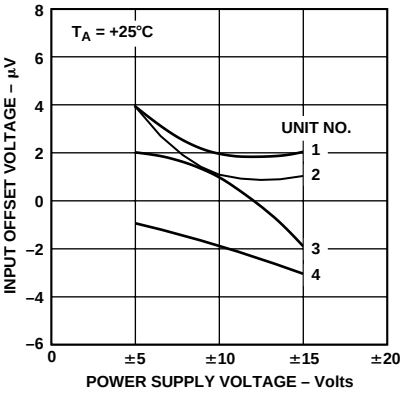


Figure 3. Input Offset Voltage vs. Supply Voltage

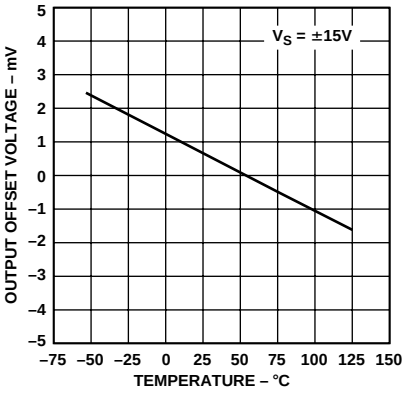


Figure 4. Output Offset Voltage vs. Temperature

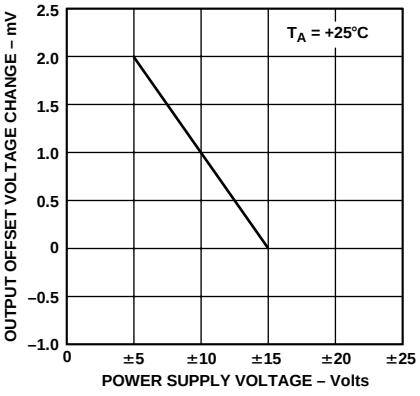


Figure 5. Output Offset Voltage Change vs. Supply Voltage

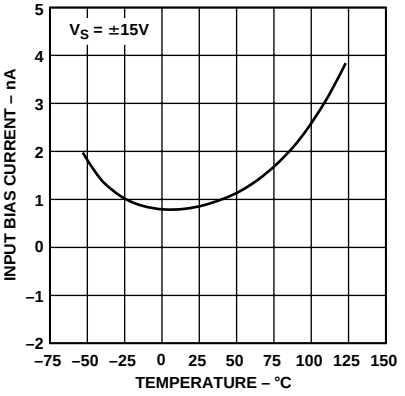


Figure 6. Input Bias Current vs. Temperature

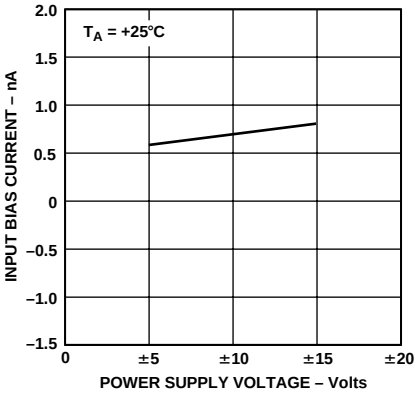


Figure 7. Input Bias Current vs. Supply Voltage

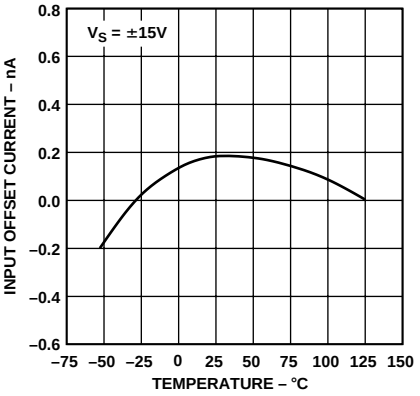


Figure 8. Input Offset Current vs. Temperature

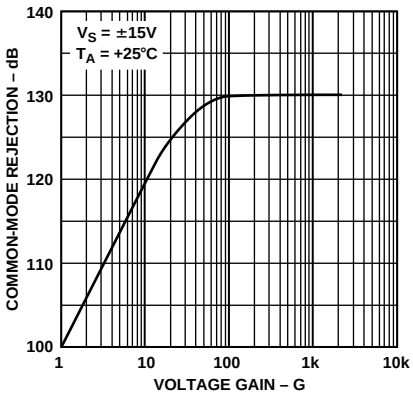


Figure 9. Common-Mode Rejection vs. Voltage Gain

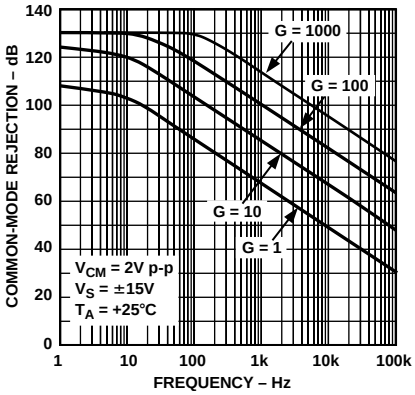


Figure 10. Common-Mode Rejection vs. Frequency

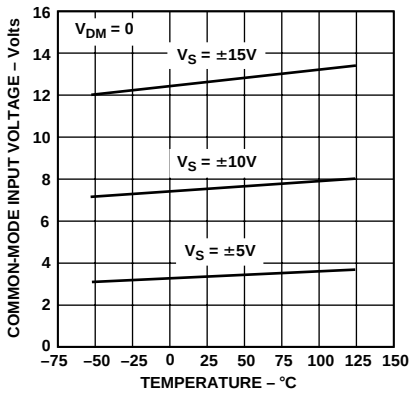


Figure 11. Common-Mode Voltage Range vs. Temperature

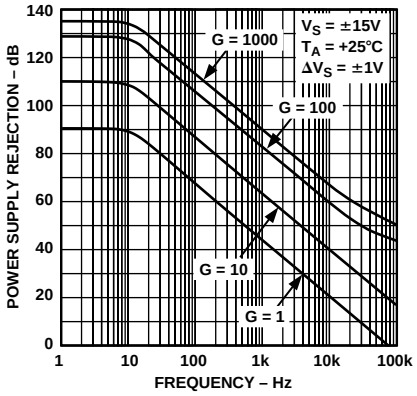


Figure 12. Positive PSR vs. Frequency

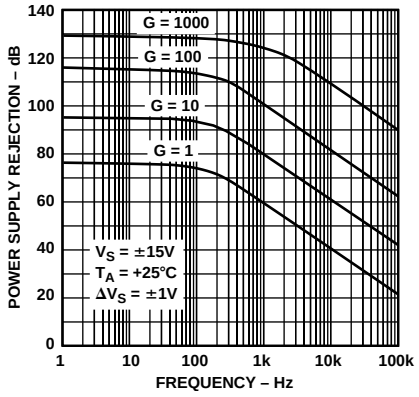


Figure 13. Negative PSR vs. Frequency

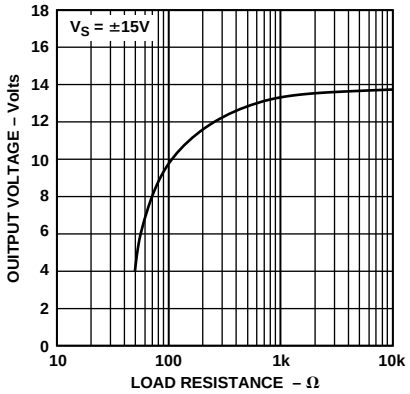


Figure 14. Maximum Output Voltage vs. Load Resistance

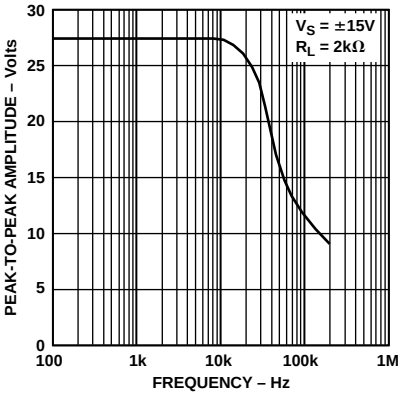


Figure 15. Maximum Output Swing vs. Frequency

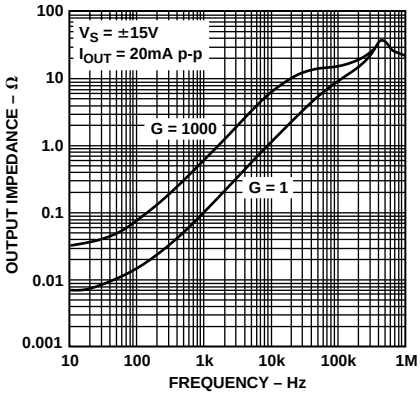


Figure 16. Closed-Loop Output Impedance vs. Frequency

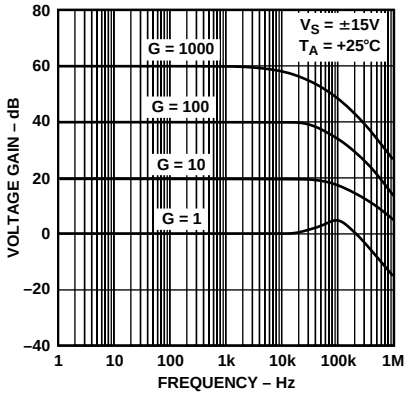


Figure 17. Closed-Loop Voltage Gain vs. Frequency

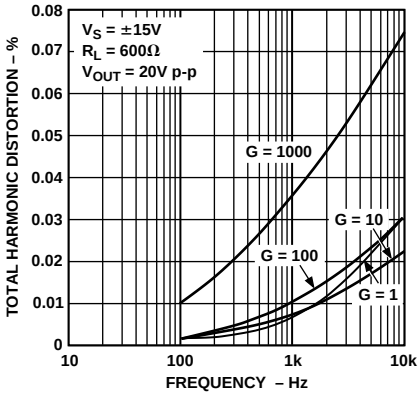


Figure 18. Total Harmonic Distortion vs. Frequency

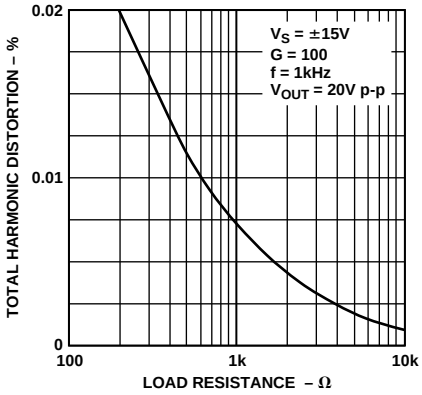


Figure 19. Total Harmonic Distortion vs. Load Resistance

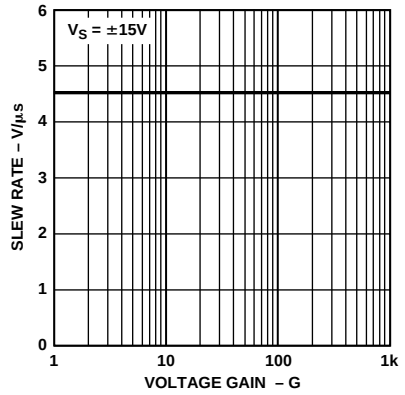


Figure 20. Slew Rate vs. Voltage Gain

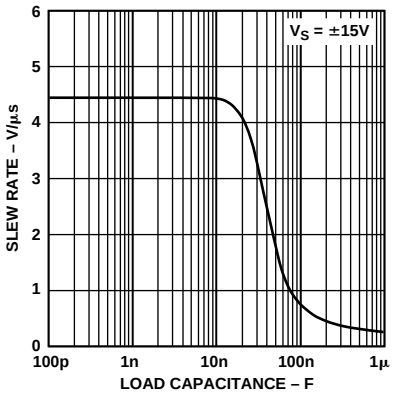


Figure 21. Slew Rate vs. Load Capacitance

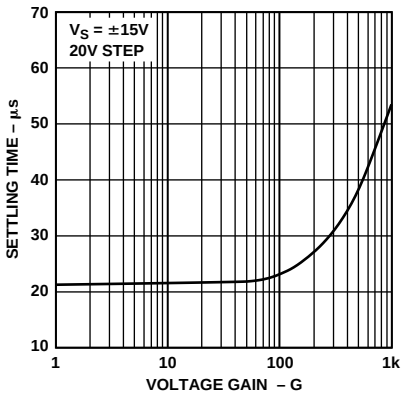


Figure 22. Settling Time to 0.01% vs. Voltage Gain

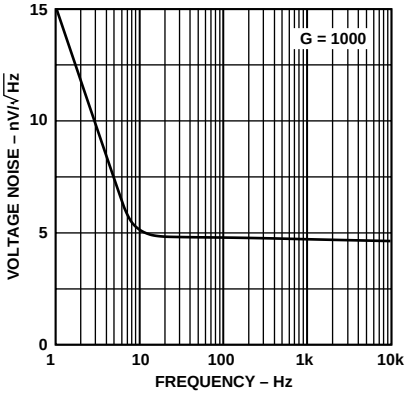


Figure 23. Voltage Noise Density vs. Frequency

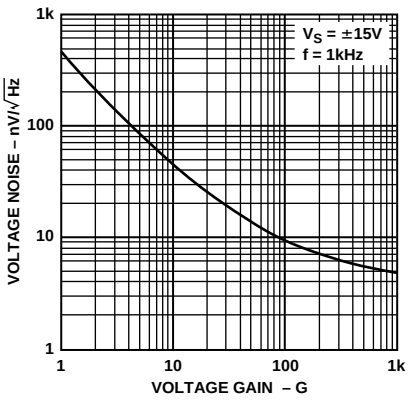


Figure 24. RTI Voltage Noise Density vs. Gain

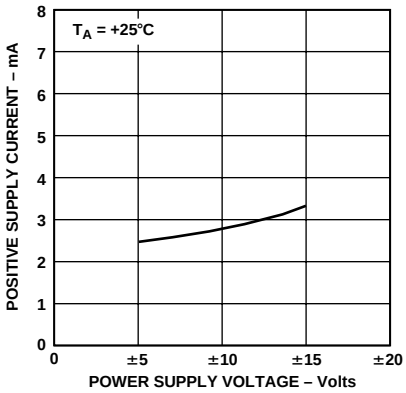


Figure 25. Positive Supply Current vs. Supply Voltage

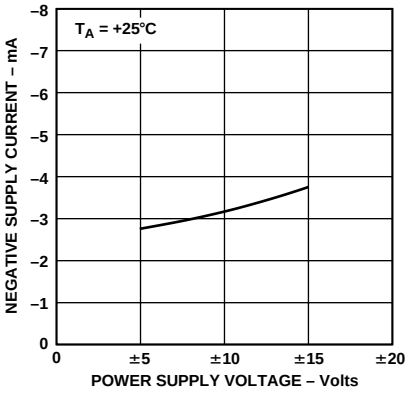


Figure 26. Negative Supply Current vs. Supply Voltage

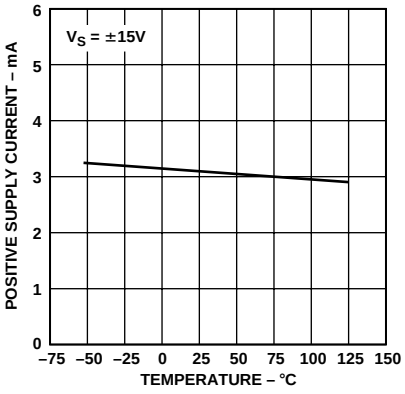


Figure 27. Positive Supply Current vs. Temperature

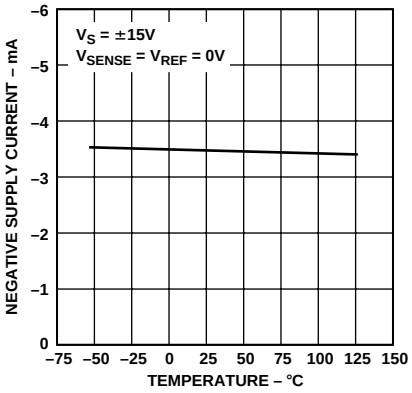


Figure 28. Negative Supply Current vs. Temperature

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both offsets can be nulled, which has minimal effect on TCV_{IOS} and TCV_{OOS}

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset errors dominate, while at high gain, input-offset errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows;

$$V_{OS}\ (RTO) = (V_{IOS} \times G) + V_{OOS} \qquad (1)$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain. Input offset nulling alone is recommended with amplifiers having fixed gain above 50. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the input offset is nulled first by short-circuiting R_G, then the output offset is nulled with the short removed.

The overall offset voltage drift TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift;

$$TCV_{OS}\ (RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \qquad (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage specification. Frequently, the amplifier drift is referred back to the input (RTI), which is then equivalent to an input signal change;

$$TCV_{OS}\ (RTI) = TCV_{IOS}\ \frac{TCV_{OOS}}{G} \qquad (3)$$

For example, the maximum input-referred drift of an AMP01 EX set to G = 1000 becomes;

$$TCV_{OS}\ (RTI) = 0.3\ \mu V/°C + \frac{100\,\mu V/°C}{1000} = 0.4\ \mu V/°C\ max$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources that can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a nontrimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain (refer to Figure 29).

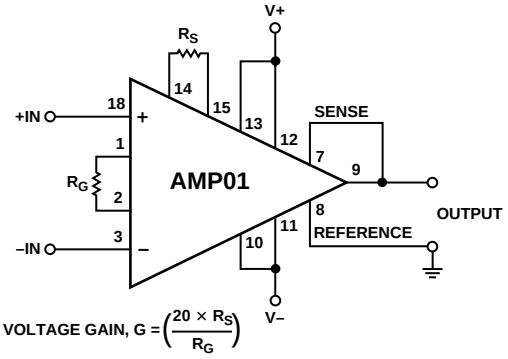


Figure 29. Basic AMP01 Connections for Gains 0.1 to 10,000

The magnitude of R_S affects linearity and output referred errors. Circuit performance is characterized using R_S = 10 kΩ when operating on ±15 volt supplies and driving a ±10 volt output. R_S may be reduced to 5 kΩ in many applications particularly when operating on ±5 volt supplies or if the output voltage swing is limited to ±5 volts. Bandwidth is improved with R_S = 5 kΩ and this also increases common-mode rejection by approximately 6 dB at low gain. Lowering the value below 5 kΩ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G. For R_S = 10 kΩ and A_V = 2000 we get R_G = 100 Ω; this value is the practical lower limit for R_G. Below 100 Ω, mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100 Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to 50 kΩ.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TCs are not too important, only the ratiometric parameters.

AC amplifiers require good gain stability with temperature and time, but dc performance is unimportant. Therefore, low cost metal-film types with TCs of 50 ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a 15 ppm/°C gain tempco at all gains requires R_S and R_G temperature coefficient matching to 5 ppm/°C or better.

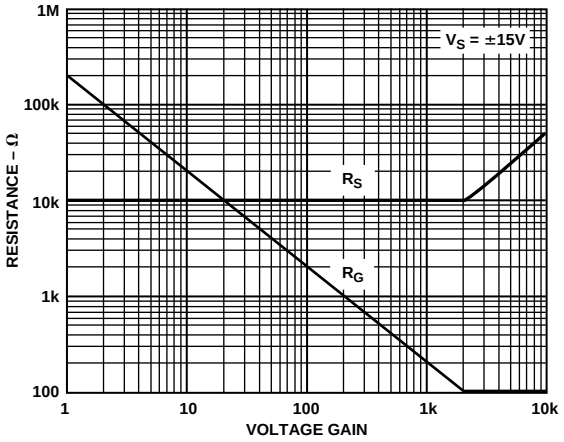


Figure 30. R_G and R_S Selection

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP01 (0.6% max for A/E grades).

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP01 which is typically 0.15 µV/°C. Resistors themselves can generate thermoelectric EMF's when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TCs of 20 ppm–50 ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP01 inherently yields high common-mode rejection. Unlike resistive feedback designs, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \quad (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; G is the chosen voltage gain. For example, at +25°C, IVR is specified as ±10.5 volt minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(10.5 - \frac{5}{G} \right) \quad (5)$$

For all gains greater than or equal to 10, CMVR is ±10 volt minimum; at gains below 10, CMVR is reduced.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving." This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2}; the center tap provides the required signal to drive the buffer amplifier (Figure 31).

GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 32).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

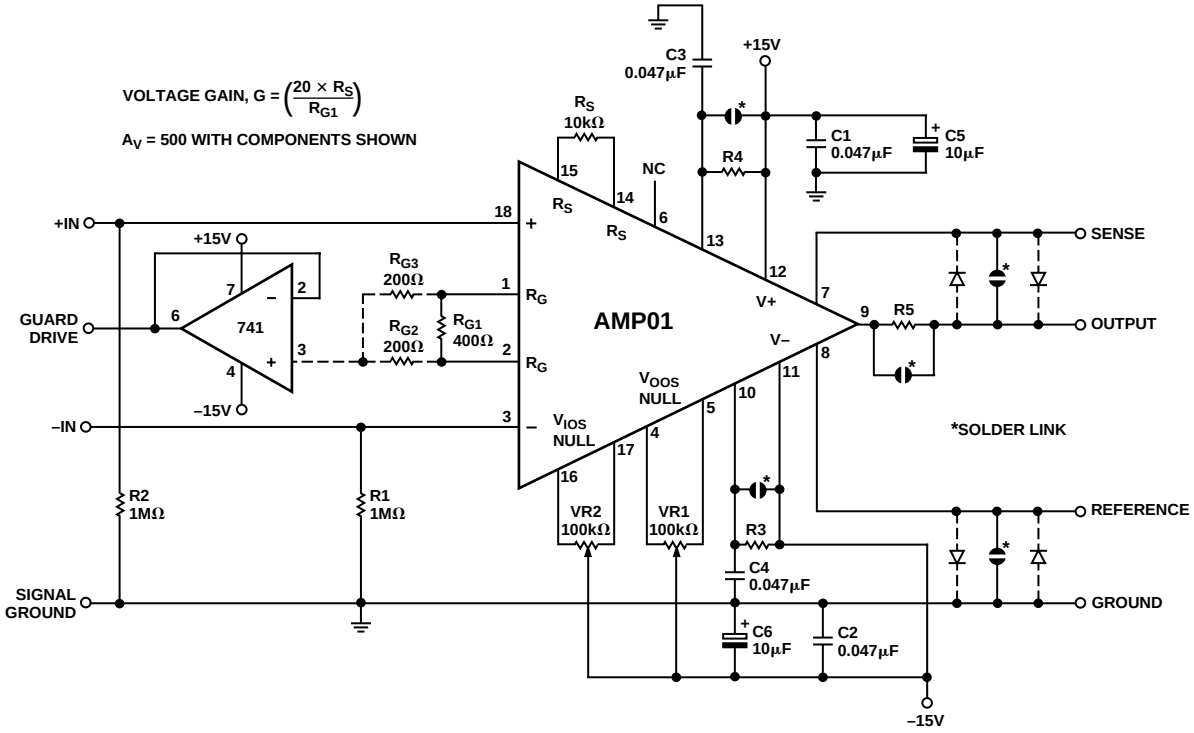


Figure 31. AMP01 Evaluation Circuit Showing Guard-Drive Connection

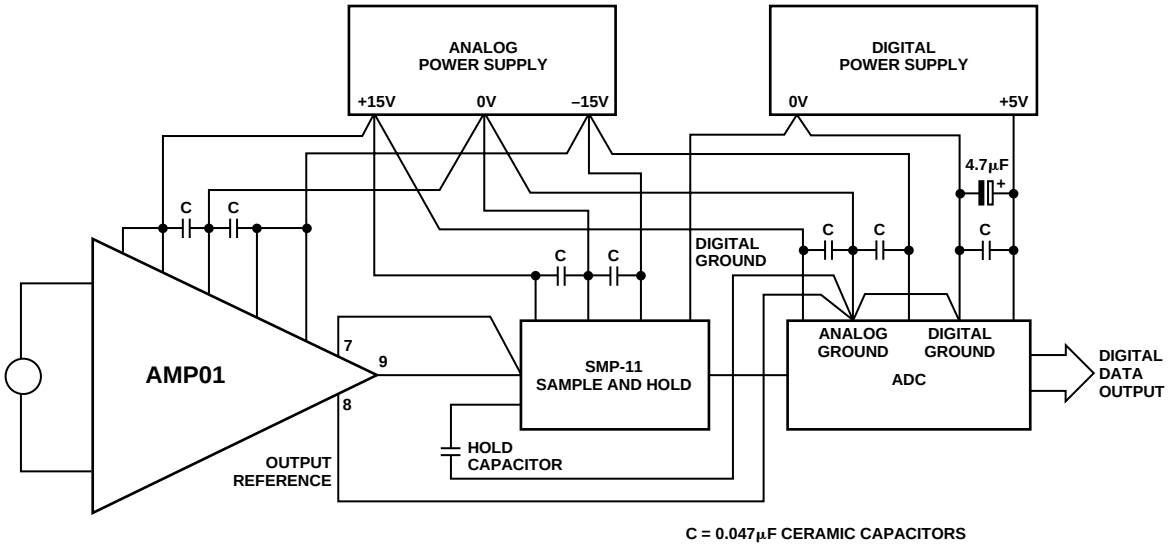


Figure 32. Basic Grounding Practice

If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50 Ω loads. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 33. This method of connection puts the I×R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3 Ω will change the output offset by only 1 mV.

DRIVING 50 Ω LOADS

Output currents of 50 mA are guaranteed into loads of up to 50 Ω and 26 mA into 500 Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be conditioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50 Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 34 shows a complete circuit for driving 50 Ω loads.

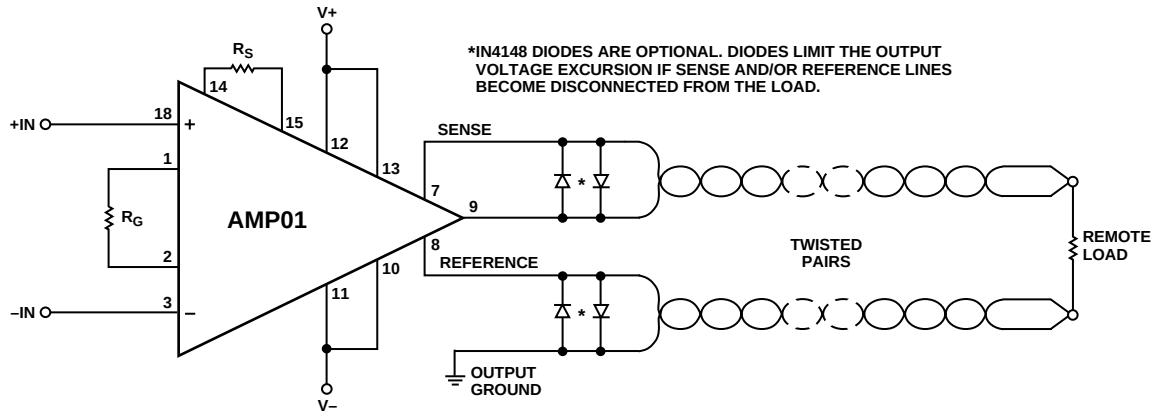


Figure 33. Remote Load Sensing

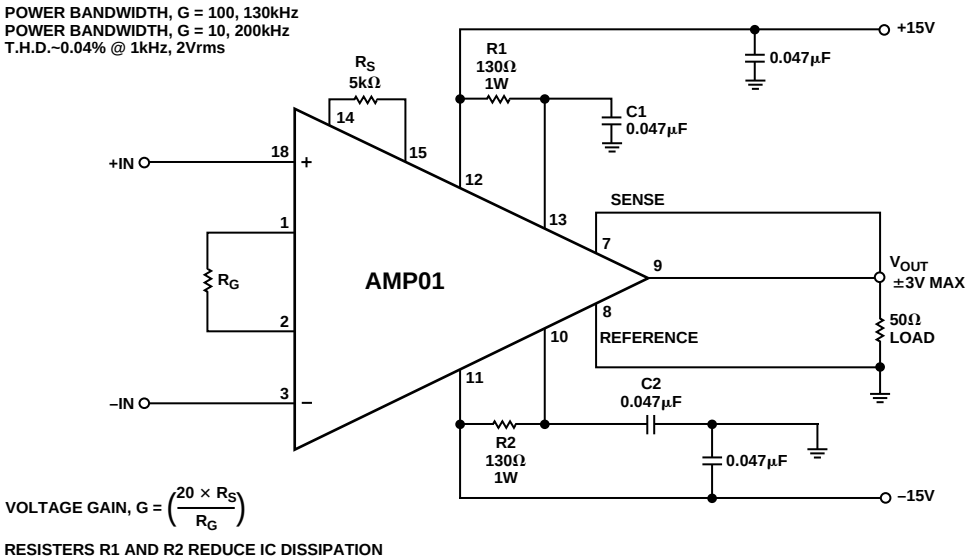


Figure 34. Driving 50 Ω Loads

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90 mW—some circuits will raise that to several hundred milliwatts (for example, the 4-20 mA current transmitter application, Figure 37). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended in power applications to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80°C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_J - T_A}{\theta_{JA}}$$

where T_J and T_A are the junction and ambient temperatures respectively, θ_{JA} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection is used so that noise performance would not be significantly degraded.

AMP01 noise level approaches the theoretical noise floor of the input stage which would be 4 nV/$\sqrt{\text{Hz}}$ at 1 kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200 Ω at a gain of 1000) and the input protection resistors (250 Ω). Active loads for the input transistors contribute less than 1 nV/$\sqrt{\text{Hz}}$ of noise. The measured noise level is typically 5 nV/$\sqrt{\text{Hz}}$.

Diodes across the input transistor's base-emitter junctions, combined with 250 Ω input resistors and R_G, protect against differential inputs of up to ±20 V for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to ±10 V.

External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1 V Zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50 mA, producing power levels that are easily handled by low-power Zeners.

Simultaneous connection of the differential inputs to a low impedance signal above 10 V during normal circuit operation is unlikely. However, additional protection involves adding 100 Ω current-limiting resistors in each signal path prior to the voltage clamp, the resistors increase the input noise level to just 5.4 nV/$\sqrt{\text{Hz}}$ (refer to Figure 35).

Input components, whether multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions that would degrade the input signal.

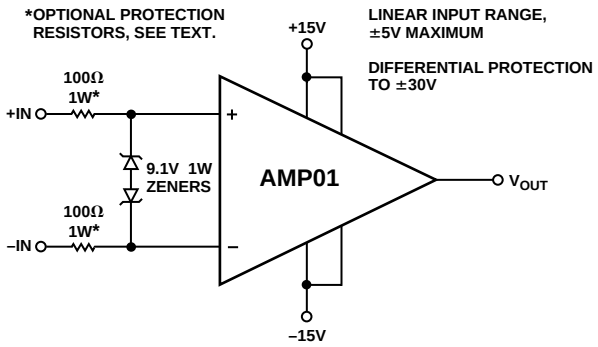


Figure 35. Input Overvoltage Protection for Gains 2 to 10,000

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80 dB means that a change of 100 mV on the supply, not an uncommon value, will produce a 10 μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

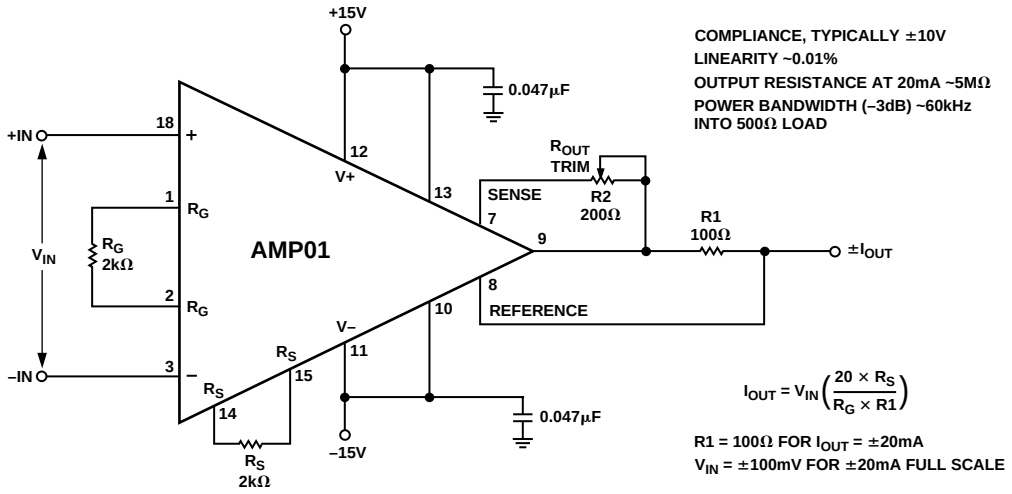


Figure 36. High Compliance Bipolar Current Source with 13-Bit Linearity

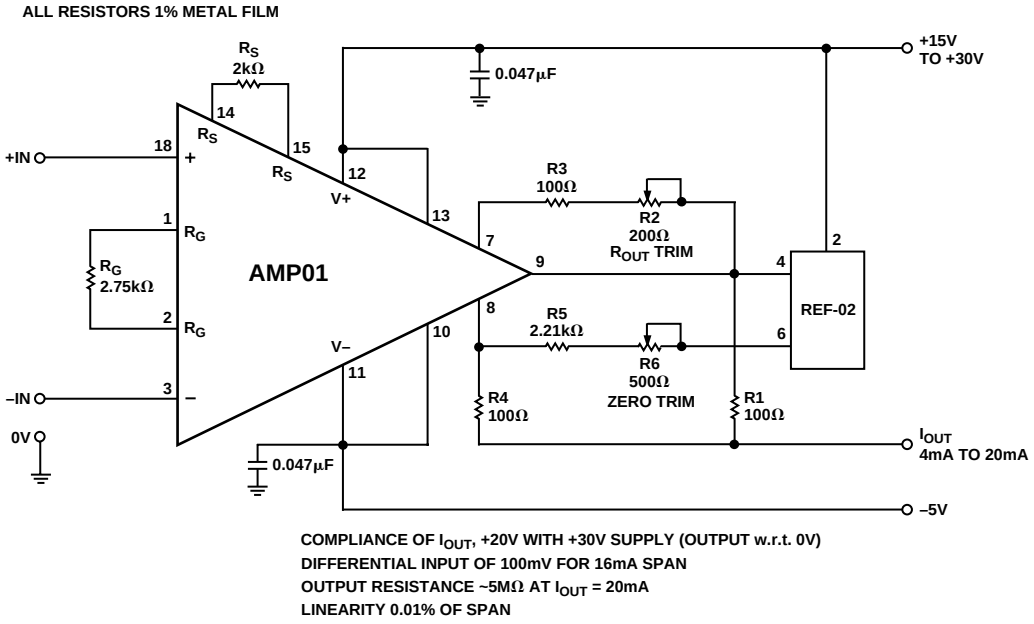


Figure 37. 13-Bit Linear 4–20 mA Transmitter Constructed by Adding a Voltage Reference. Thermocouple Signals Can Be Accepted Without Preamplification.

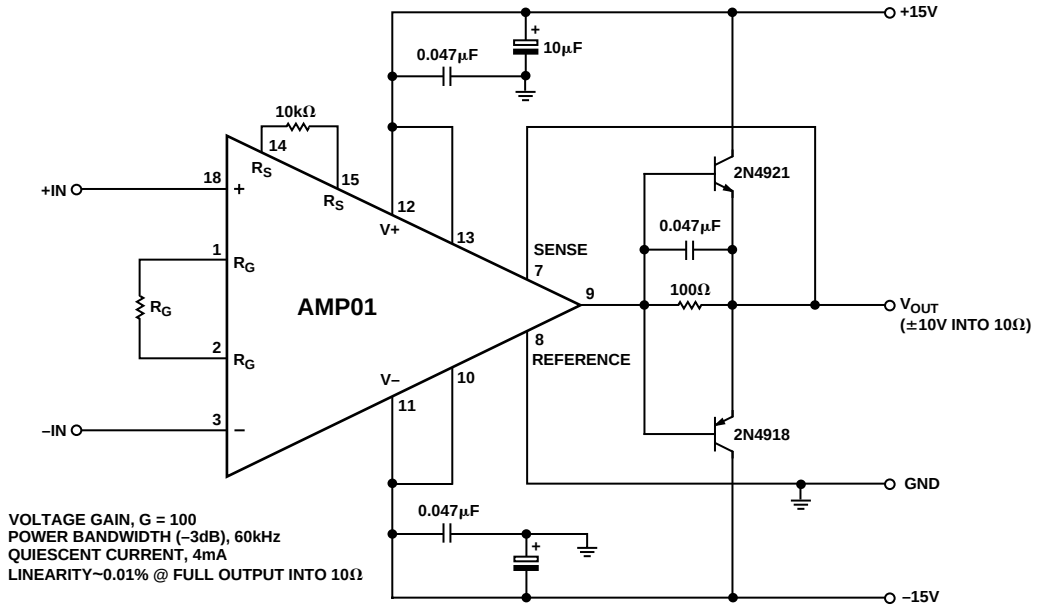


Figure 38. Adding Two Transistors Increases Output Current to ±1 A Without Affecting the Quiescent Current of 4 mA. Power Bandwidth is 60 kHz.

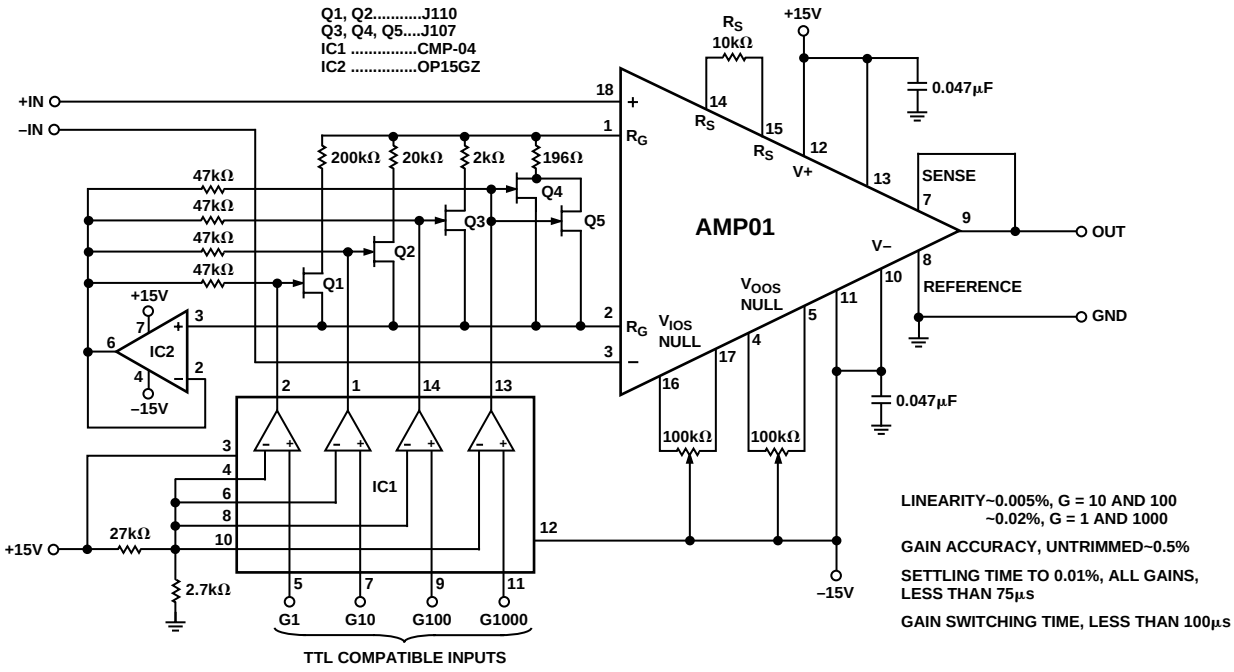


Figure 39. The AMP01 Makes an Excellent Programmable-Gain Instrumentation Amplifier. Combined Gain-Switching and Settling Time to 13 Bits Falls Below 100 µs. Linearity Is Better than 12 Bits over a Gain Range 1 to 1000.

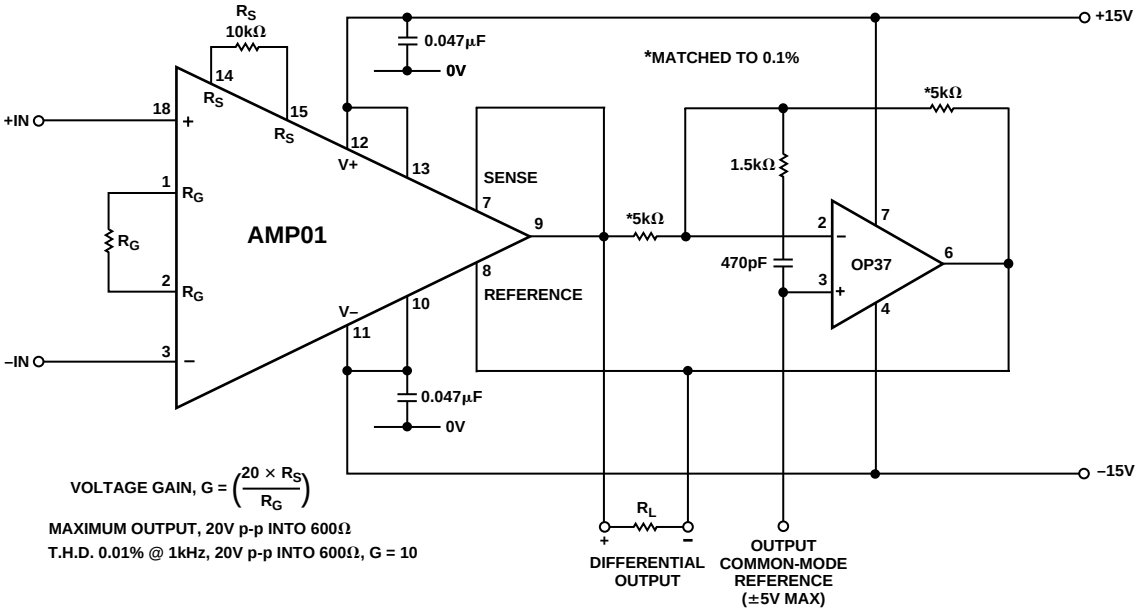


Figure 40. A Differential Input Instrumentation Amplifier with Differential Output Replaces a Transformer in Many Applications. The Output will Drive a 600 Ω Load at Low Distortion, (0.01%).

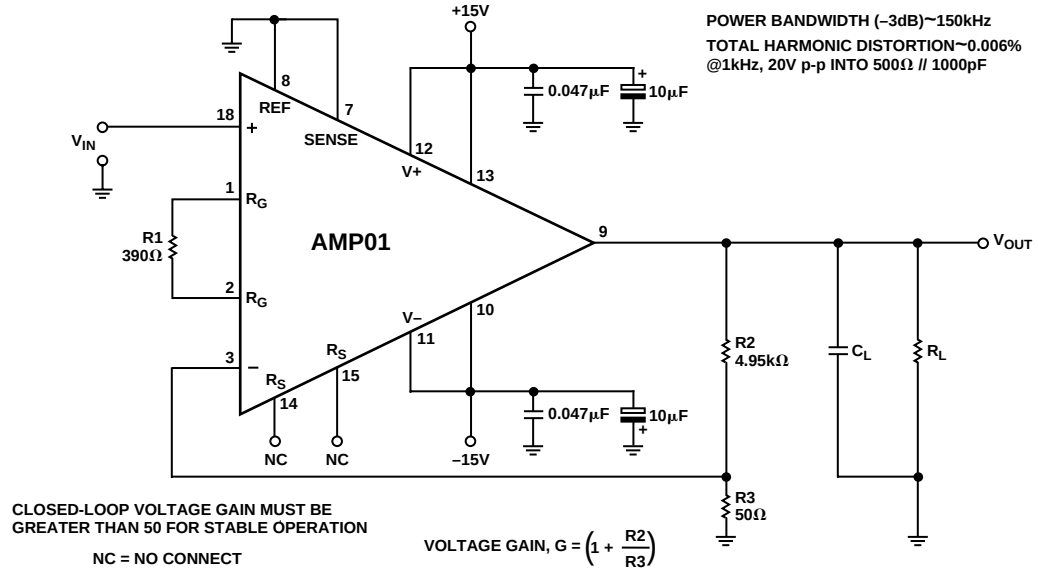


Figure 41. Configuring the AMP01 as a Noninverting Operational Amplifier Provides Exceptional Performance. The Output Handles Low Load Impedances at Very Low Distortion, 0.006%.

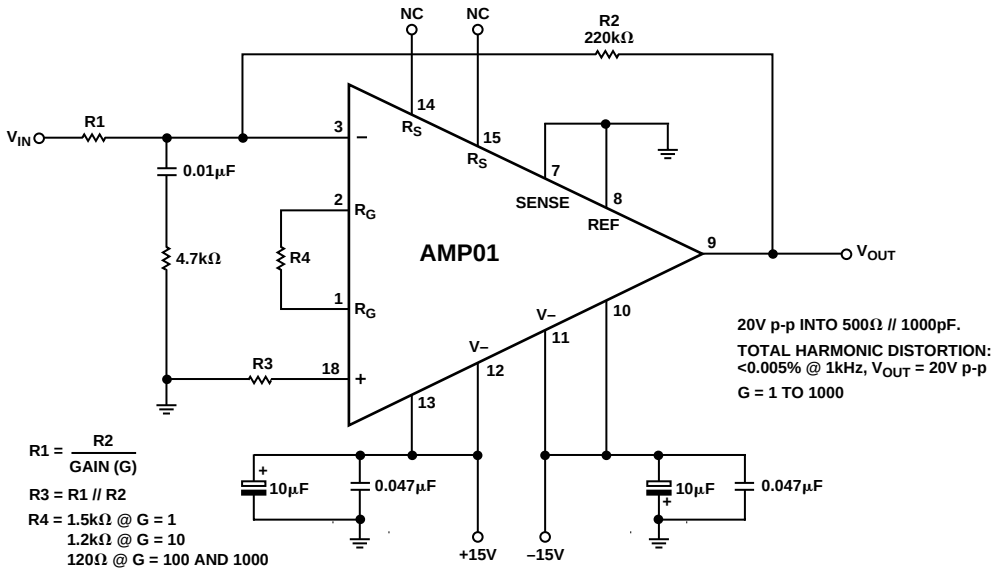


Figure 42. The Inverting Operational Amplifier Configuration has Excellent Linearity over the Gain Range 1 to 1000, Typically 0.005%. Offset Voltage Drift at Unity Gain Is Improved over the Drift in the Instrumentation Amplifier Configuration.

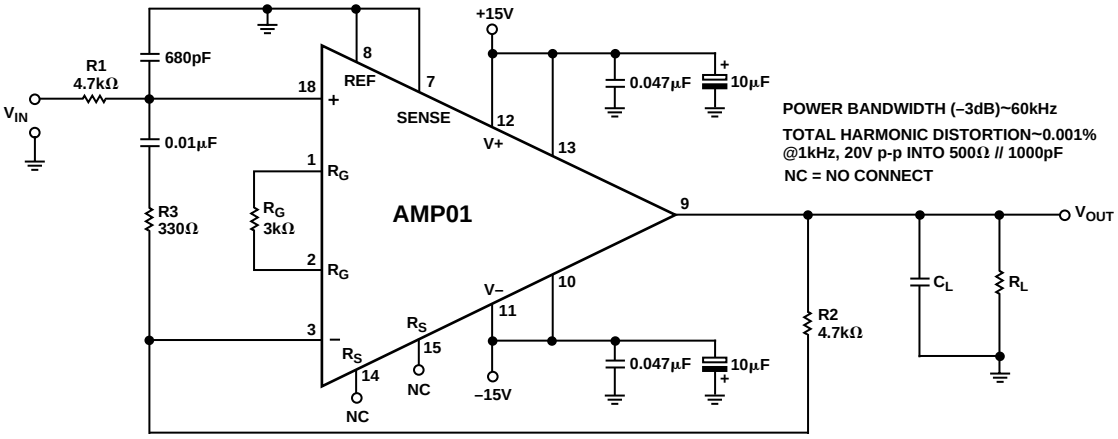


Figure 43. Stability with Large Capacitive Loads Combined with High Output Current Capability make the AMP01 Ideal for Line Driving Applications. Offset Voltage Drift Approaches the TCV_{IOS} Limit, (0.3 μV/°C).

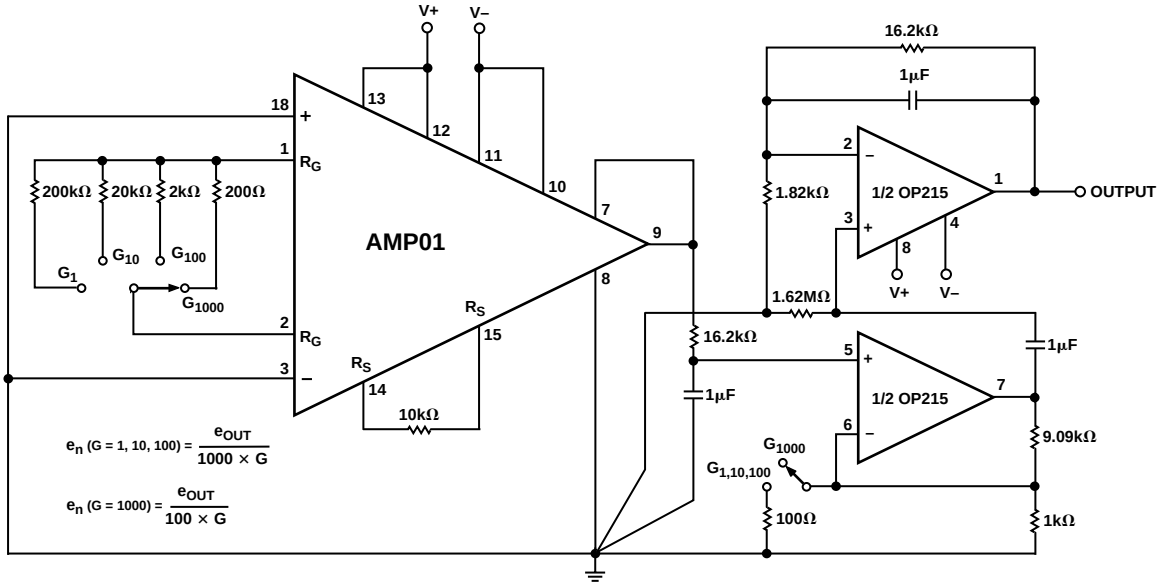


Figure 44. Noise Test Circuit (0.1 Hz to 10 Hz)

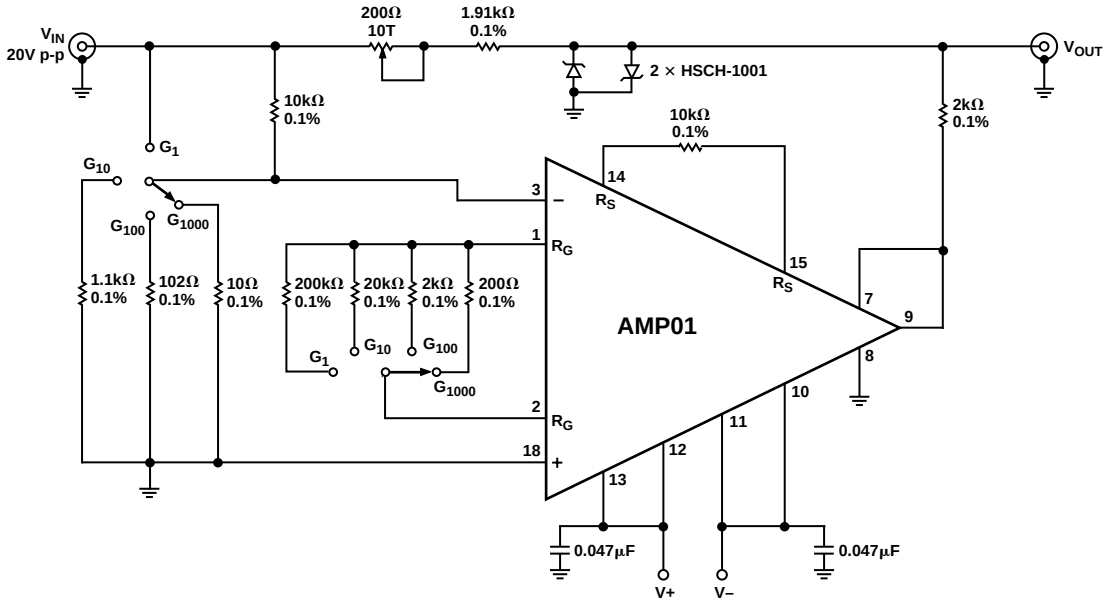


Figure 45. Settling-Time Test Circuit

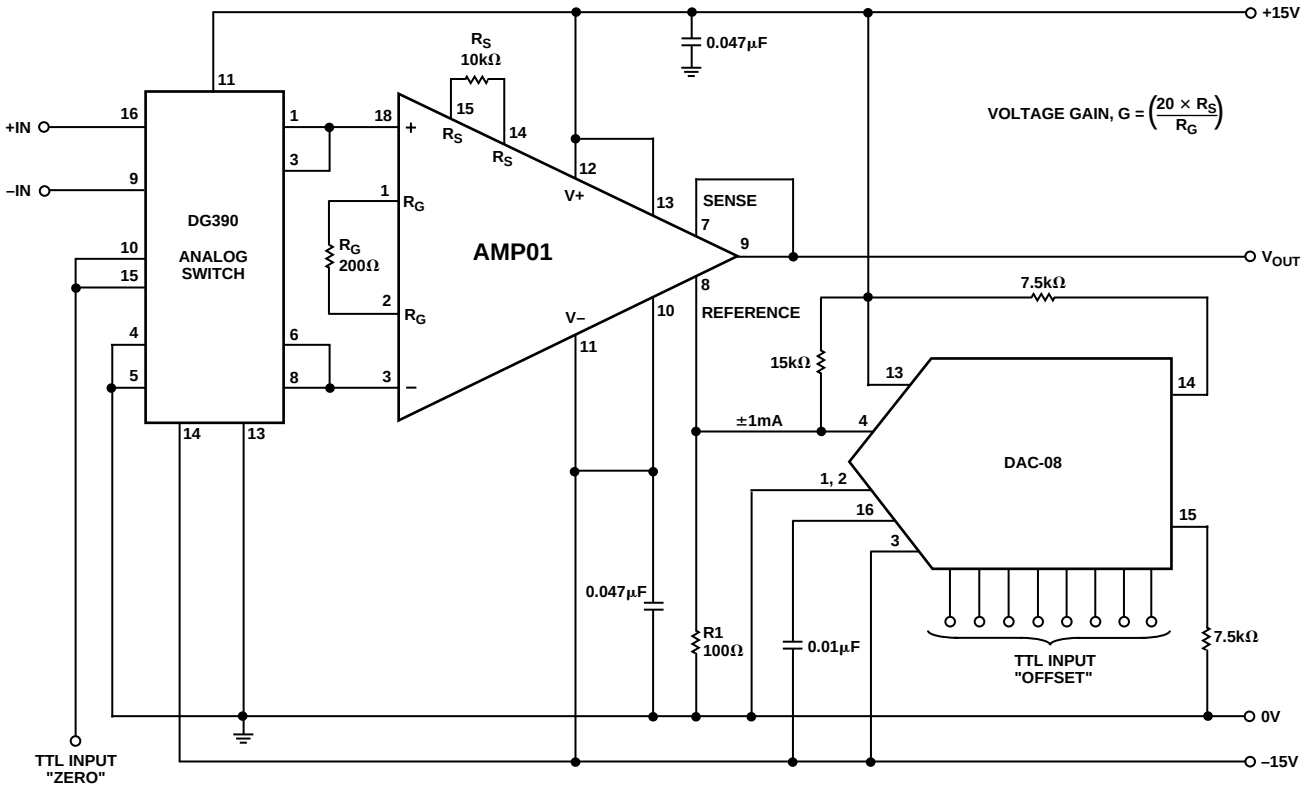


Figure 46. Instrumentation Amplifier with Autozero

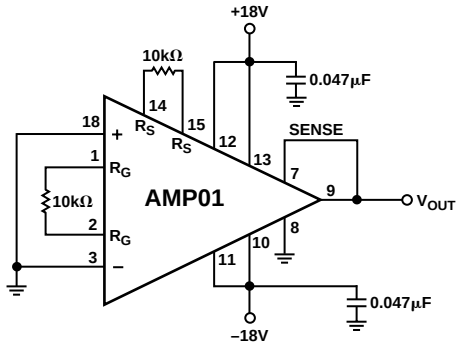
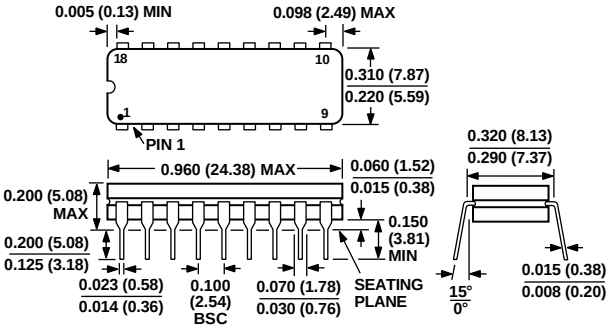


Figure 47. Burn-In Circuit

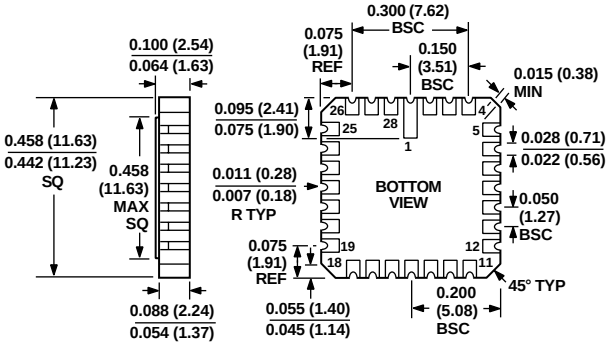
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

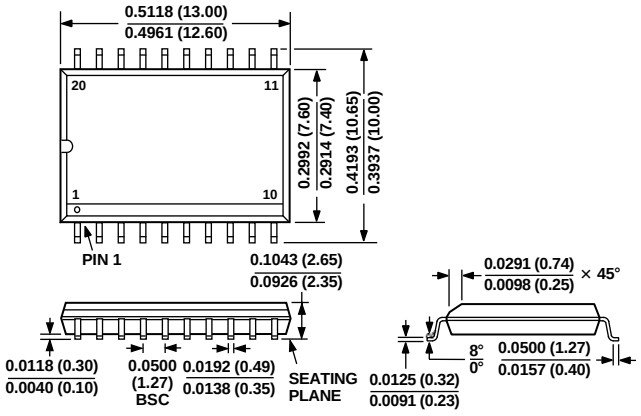
18-Lead Cerdip
(Q-18)



28-Terminal Ceramic Leadless Chip Carrier
(E-28A)



20-Lead SOIC
(R-20)



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