Application Note AN-9052

Design Guide for Selection of Bootstrap Components

1. Bootstrap Circuit

1.1 Bootstrap Floating Supply

Using a N channel MOSFET as a high side switch requires a voltage supply referenced at the source of the MOSFET. One of the most widely used method in supplying power to the high-side circuitry is the use of the bootstrap floating supply due to its inherent simplicity and inexpensive features. This kind of floating supply is suitable for providing a gate drive circuitry to directly drive high side switches that operate up to rail voltages. The basic circuit of the bootstrap supply, shown in Figure 1, is formed by a diode (Dbs) and a capacitor (Cbs). But, this type of floating supply has limitations on refreshment of Cbs when duty cycle is very high or turn-on time is very long. In the case where the gate voltage is not enough to fully turn-on the MOSFET (Q1), the output of gate drive IC (HO) should be turned-off to prevent the Q1 from operating in high dissipation mode. The optional gate resistor (Rg) is used for the purpose of controlling the turn-on/turn-off time of the Q1, and the bootstrap resistor (Rbs) is used to limit the current and prevent the bootstrap capacitor (Cbs) from overcharging.

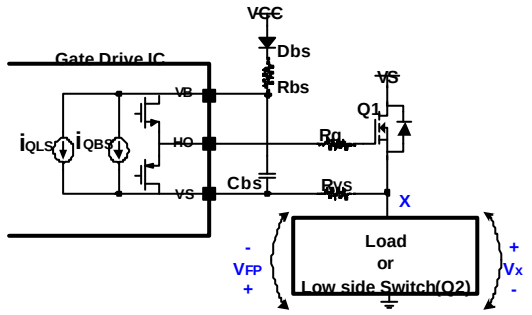

figure 1. Bootstrap Circuit

1.2 Operation of Bootstrap Circuit

The charged capacitor (Cbs) supplies the voltage to the transistors of the gate drive IC, which is used to turn ON and OFF the external high side switch (Q1). The bootstrap capacitor(Cbs) gets charged from the voltage supply (VCC), through the bootstrap diode (Dbs), when the voltage at node X (V_X) is pulled down to ground or even below ground level. The bootstrap capacitor needs to be sized properly to account for the case when Vx is pulled down to ground, which Vbs is at its lowest level, and cause under voltage lockout (UVLO) malfunction. Most gate drive ICs have undervoltage detection circuit that prevents from driving an external switch when Vbs drops below a certain level (specified in datasheets as VBSUV level). The V_{BSUV} level depends on the external switch that it is driving. The undervoltage level for IGBTs are in the 9V~10V range, and for MOSFETs in the 4V~5V range. In the case where the node X goes below the ground level, Cbs will be overcharged by the level in which it goes negative. There are negative transients at node X caused by the parasitic inductances and peak forward voltage drop (Vfp) of the body diode at the low side switch that needs to be considered also. All of the overcharging affect mentioned above needs to be taken into account in determining the size of Cbs. Adding resistors Rbs, Rvs, and using a diode with a low Vfp value are other possible solutions to limit the overcharge effect on Cbs. Let us now look at the case that causes the Cbs to discharge. Cbs discharges when Q1 turns-on or node X is floating. The associated discharging factors are gate drive power, leakage current in each component, and current consumption in the gate drive IC. From an application point of view, specific conditions such as the duty cycle of PWM that causes ripple voltages on Cbs, operation frequency, and the type of modulation at which Q1 operates needs to be examined to make sure that Cbs can handle.

1.3 Initial Charging and Refreshment of Bootstrap Capacitor

Another key parameter in selecting bootstrap components is initial start-up time. The initial charging time(***tch***) can be calculated from the following equation:

$$t_{ch} \geq C_{bs} \times R_T \times \frac{1}{D} \times \ln\left(\frac{V_{cc}}{V_{cc} - V_{bs,Min} - V_f - V_x}\right) \qquad (1)$$

Where,

RT = Rbs + Rvs (with low side switch and no load)

RT = Rbs + Rvs + RL (with loads including equivalent impedance at node X)

D = duty cycle

In the case where PWM is not used, the load not connected, and the low side switch turned on the charging time at the

start-up phase can be defined by the time constants Rbs, Rvs, and Cbs. When the load is connected and forms the charge path in the bootstrap circuit, the initial charging time is defined by Cbs and the relationship between Rbs, Rvs, and the load impedance RL. Most designs, the value of Cbs is picked with some margins, which leads to longer star-up time. If node X is left floating for a long time, Vbs will decrease due to leakage current, and consequently the gate drive IC will go into UVLO condition. Controlling the low side switch properly, the bootstrap capacitor can be recharged and maintain the voltage level needed by the gate drive IC. The gate drive IC FAN7085 (block diagram shown in Fig.2) has a built-in recharge switch that will charge the bootstrap capacitor regardless of the application. If Q1 is turned off and FAN7085 is used as a gate drive IC in the bootstrap circuit shown in Figure 1, the internal recharge switch of the FAN7085 will activate to provide the path to charge the bootstrap capacitor (Cbs) fully. Let's look at a specific application of the FAN7085, which is shown in Figure 3. In the event that both of the switch (S1 and S2) are turned off, the internal recharge switch of the FAN7085 will provide the path to charge the bootstrap capacitor. If the current level passing through the recharge switch is higher than the leakage current, bootstrap capacitor will charge through the recharge path. The voltage level on the VS pin of the FAN7085 at a given current level when the recharge switch is turned on is defined on the datasheet.

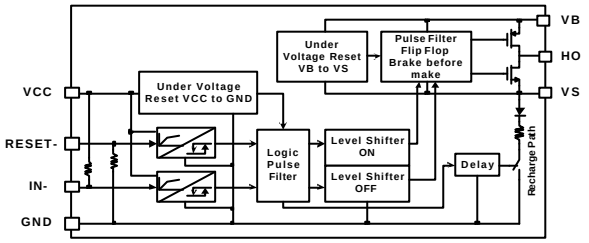

Figure 2. Internal block diagram of FAN7085

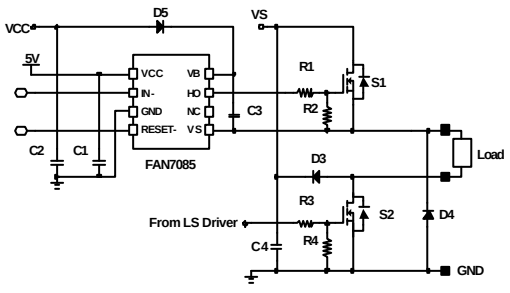

Figure 3. Application example of FAN7085

2. Selection of Bootstrap Components

2.1 Selection of Bootstrap Capacitor

The maximum allowable voltage drop across the bootstrap capacitor to ensure enough gate-source voltage is highly dependent to the internal undervoltage shutdown level of the gate drive IC, and the voltage level at the source connection of Q1 (node X)

$$V_{BS,Drop} = V_{CC} - V_f - V_{OP} - V_X \qquad (2)$$

Where:

VCC= gate drive IC supply voltage

If = static forward voltage drop of Dbs

Vop= minimum gate-source voltage level required that will prevent Q1 to go into a high dissipation mode

X = MOSFET source connection

If the minimum operating voltage (V_{OP}) requires to be greater than UVLO voltage level, then equation 2 can be denoted as follows

$$V_{BS,Drop} = V_{CC} - V_f - V_{BSUV,Max} - V_X \qquad (3)$$

Where, $V_{BSUV,Max}$ is the maximum UVLO voltage level of gate drive IC.

The total charge (Qbs) required by the bootstrap capacitor can be calculated by summing the Q1 gate charge, charge required for the level shifter in the gate drive IC, and leakage charges resulting from leakage current.

$$Q_{BS} = Q_g + (I_{LK} + I_{QBS}) \times T_{ON} + Q_{LS} \qquad (4)$$

Where:

QBS = total charge from Cbs

Qg.= gate charge of Q1

ILK= total leakage current

IQBS = operating current in gate drive IC

TON = Turning-on interval of Q1

QLS= level shift charge required per cycle.

The total leakage current is the summation of all of the individual component's leakage currents

$$I_{LK} = I_{LK,GS} + I_{LK,HS} + I_{LKD} + I_{LK,C} \qquad (5)$$

Where,

$I_{LK,GS}$ = gate leakage current of the MOSFET

$I_{LK,HS}$ = high side floating supply leakage current

$I_{LK,D}$ = bootstrap diode leakage current

$I_{LK,C}$ = capacitor leakage current, which can be ignored if it is not an electrolytic capacitor

The guiding criteria for calculating the minimum required bootstrap capacitance can be obtained through the following equation:

$$C_{bs,Min} \geq \frac{Q_{BS}}{V_{BS,Drop}} \qquad (6)$$

Equation 6 is a basic equation for calculating the minimum value for the bootstrap capacitor. It uses the value of $V_{bs,Drop}$, which is the minimum operating voltage required and does not account for the any margins. The margin that is needed is to compensate for the ripple voltage on Vbs by the PWM, and the overcharging due to negative transients at node X. It implies that $V_{bs,Drop}$, should be changed to a smaller value, $V_{bs,Min}$. In regards to the ripple voltage compensation, the value of V_{BSUVH} is assigned to $V_{bs,Min}$, in calculating the bootstrap capacitor.

$$C_{bs,Min} \geq \frac{Q_{BS}}{V_{BS,Min}} = \frac{Q_{BS}}{V_{BSUVH}} \qquad (7)$$

Where V_{BSUVH} is hysteresis voltage of UVLO in gate drive IC. The minimum bootstrap capacitance calculated in Equation 7 might need to account for additional margin depending on the specific application conditions. Conditions at node X, such as long floating state and negative transients with deep and long duration needs to be accounted for. Using the FAN7085, unlike other gate drive ICs, the long floating state of node X does not need to be accounted for when calculating the minimum bootstrap capacitor value ($C_{bs,Min}$). The internal recharge switch of the FAN7085 (pin VS) provides a path to charge the bootstrap capacitor when S1 and S2 are turned off.

2.2 Selection of Bootstrap Diode

The maximum voltage rating should be higher than power rail (VS) and current rating can be multiplication of total charge and switching frequency. A diode with a fast reverse recovery time is beneficial to minimize the leakage current.

3. Examples of Bootstrap Capacitor Selection

3.1 Example 1

The basic operation conditions are:

-. Gate drive IC: FAN7080
-. Switching device: FDB8442
-. Bootstrap diode: MMBD1405
-. Switching frequency: 20KHz
-. System operating voltage: Vcc(9 ~16V), VS(38V)

The known values from the datasheets are:

-. I_{QBS} = 150uA
-. Q_{LS} = 3nC (assumed in fairchild 600V Gate drive IC)
-. I_{LK_GS}= 100nA
-. I_{LK_HS}=50uA
-. I_{LK_D} = 100nA
-. V_F =1.1V
-. I_{LK_C} = 0
-. V_{OP} = 5.5V(is equal to V_{BSUV+})
-. Qg. = 235nC@80A,Vgs=10V
-. $R_{DS,ON(Max)}$ = 5mohm
-. Rbs and Rvs are not used.

The voltage drop is calculated as:

$$V_{BS,Drop} = V_{CC} - V_f - V_{OP} - V_X$$
$$= V_{CC,Min} - 1.1V - V_{BSUV,Max} - R_{DS,ONmax} \times I_{OUT}$$
$$= 9 - 1 - 5.5 - 0.4 = 2.0V$$

The leakage current is calculated as:

$$I_{LK} = I_{LK,GS} + I_{LK,HS} + I_{LK,D} + I_{LKC}$$
$$= 100nA + 50uA + 100nA + 0$$
$$= 50.2uA$$

The total charged required is calculated as:

$$Q_{BS} = Q_g + (I_{LK} + I_{QBS}) \times T_{ON} + Q_{LS}$$
$$= 235nC + (50.2uA + 150uA) \times 50uSec + 3nC$$
$$= 235nC + 10nC + 3nC = 248nC$$

The minimum capacitor value needed to prevent UVLO condition is calculated as

$$C_{BS,Min} = \frac{Q_{BS}}{V_{BS,Drop}} = \frac{248nC}{2.0V} = 124nF$$

The minimum capacitor value with a margin taken into account (explained in sec 2.1) is calculated as:

$$C_{BS} \geq \frac{Q_{BS}}{V_{BSUVH}} = \frac{248nC}{0.2V} = 1.2uF$$

Depending on the specific operating conditions additional margins needs to be accounted for in calculating the minimum required capacitor value.

3.2 Example 2

The basic operating conditions are:

-. Gate drive IC: FAN7085
-. Switching device: FDB42AN15A0
-. Bootstrap diode: MMBD1405
-. Switching frequency: 50KHz
-. System operating voltage: Vcc(7 ~16V), VS(130V)

The known values from the datasheets are:

-. I_{QBS} = 200uA
-. Q_{LS} = 3nC
-. I_{LK_GS}= 100nA
-. I_{LK_HS}=200uA
-. I_{LK_D} = 100nA
-. V_F = 1.1V
-. I_{LK_C} = 0
-. V_{OP} = 4.3V(is equal to V_{BSUV+})
-. Qg. = 39nC@12A,Vgs=10V
-. $R_{DS,ON(Max)}$ = 107mohm
-. Rbs and Rvs are not used.

The voltage drop is calculated as:

$$V_{BS,Drop} = V_{CC} - V_f - V_{OP} - V_X$$
$$= V_{CC,Min} - 1.1V - V_{BSUV,Max} - R_{DS,ONmax} \times I_{OUT}$$
$$= 7 - 1.1 - 4.3 - 1.3 = 0.3V$$

The leakage current is calculated as:

$$I_{LK} = I_{LK,GS} + I_{LK,HS} + I_{LK,D} + I_{LKC}$$
$$= 100nA + 200uA + 100nA + 0$$
$$= 200.2uA$$

The total charged required is calculated as:

$$Q_{BS} = Q_g + (I_{LK} + I_{QBS}) \times T_{ON} + Q_{LS}$$
$$= 39nC + (200.2uA + 200uA) \times 50uSec + 3nC$$
$$= 39nC + 20nC + 3nC = 62nC$$

The minimum capacitor value needed to prevent UVLO condition is calculated as:

$$C_{BS,Min} = \frac{Q_{BS}}{V_{BS,Drop}} = \frac{62nC}{0.3V} = 200nF$$

The minimum capacitor value with a margin taken into account (when allowable voltage drop is set to V_{UVBSH}, explained in sec 2.1) is calculated as:

$$C_{BS} \geq \frac{Q_{BS}}{V_{BSUVH}} = \frac{62nC}{0.02V} = 3.1uF$$

The initial charging time when S1 and S2 are turned off is calculated as:

$$t_{CH} \geq 5 \times (R_{Recharge} \times C_{BS})$$
$$= 5 \times (500ohm \times 3.1uF)$$
$$= 7.75mSec$$

Where, Rrecharge is the equivalent series resistance of the switch when the switch is turned on.