TPS3710-Q1 宽 VIN 电压检测器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 宽电源电压范围：1.8V 至 18V
- 可调节阈值：低至 400mV
- 高阈值精度：
  - 1.0% 过热
  - 0.25% 典型值
- 低静态电流：5.5µA（典型值）
- 开漏输出
- 内部迟滞：5.5mV（典型值）
- 温度范围：-40°C 至 +125°C
- 封装：
  - 1.5mm × 1.5mm WSON-6

2 应用

- 汽车系统
- 嵌入式计算模块
- DSP、微控制器或微处理器应用
- 笔记本和台式机
- 便携式和电池供电类产品
- FPGA 和 ASIC 应用

3 说明

TPS3710-Q1 宽电源电压检测器可在 1.8V 至 18V 的电压范围内运行。此器件具有一个内部基准电压为 400mV 的高精度比较器，和一个额定电压为 18V 的开漏输出，用于实现精确的电压检测。可以使用外部电阻设置监视电压。

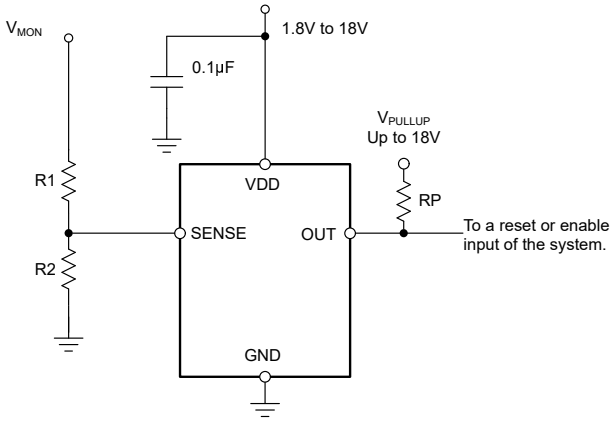
当 SENSE 引脚上的电压下降至低于 (V_{IT-}) 时，OUT 引脚被驱动至低电平，而当电压返回到对应阈值 (V_{IT+}) 之上时，OUT 引脚变为高电平。TPS3710-Q1 的比较器包括用于滤波的内部迟滞来抑制短时毛刺脉冲，从而确保器件正确运行，不会引起误触发。

TPS3710-Q1 提供 1.5mm × 1.5mm 6 引脚 WSON 封装，额定工作结温范围为 –40°C 至 +125°C。

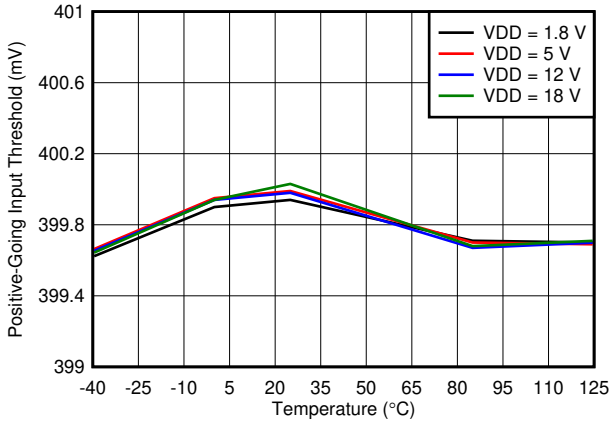
器件信息

器件型号	封装(1)	封装尺寸（标称值）(2)
TPS3710-Q1	WSON (6)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图



上升输入阈值电压 (V_{IT+}) 与温度间的关系

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 ESD Ratings 4
5.3 Recommended Operating Conditions 4
5.4 Thermal Information 4
5.5 Electrical Characteristics 5
5.6 Timing Requirements 6
5.7 Switching Characteristics 6
5.8 Typical Characteristics 7
6 Detailed Description 9
6.1 Overview 9
6.2 Functional Block Diagram 9
6.3 Feature Description 10
6.4 Device Functional Modes 10
7 Application and Implementation 11
7.1 Application Information 11
7.2 Typical Application 13
7.3 Do's and Don'ts 14
7.4 Power-Supply Recommendations 14
7.5 Layout 15
8 Device and Documentation Support 16
8.1 Device Support 16
8.2 Documentation Support 16
8.3 接收文档更新通知 16
8.4 支持资源 16
8.5 Trademarks 16
8.6 静电放电警告 16
8.7 术语表 16
9 Revision History 16
10 Mechanical, Packaging, and Orderable Information 17

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4 Pin Configuration and Functions

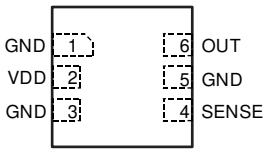


图 4-1. DSE Package
6-Pin WSON
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSE		
GND	1, 3, 5	—	Connect all three pins to ground.
OUT	6	O	SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below (V_{IT-}). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).
SENSE	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT is driven low.
VDD	2	I	Supply voltage input. Connect a 1.8V to 18V supply to VDD to power the device. Good analog design practice is to place a 0.1µF ceramic capacitor close to this pin.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VDD	–0.3	20	V
	OUT	–0.3	20	
	SENSE	–0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.8		18	V
V_I	Input voltage	SENSE	0		6.5	V
V_O	Output voltage	OUT	0		18	V

5.4 Thermal Information

THERMAL METRIC (1)		TPS3710-Q1 DSE (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	128.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	153.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, and 1.8V < V_{DD} < 18V (unless otherwise noted). Typical values are at T_J = 25°C and V_{DD} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage (1)	V_{OL}max = 0.2V, output sink current = 15µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8V	396	400	404	mV
		V_{DD} = 18V	396	400	404	
V_{IT-}	Negative-going input threshold voltage	V_{DD} = 1.8V	387	394.5	400	mV
		V_{DD} = 18V	387	394.5	400	
V_{hys}	Hysteresis voltage (hys = V_{IT+} – V_{IT-})			5.5	12	mV
$I_{(SENSE)}$	Input current (at the SENSE pin)	V_{DD} = 1.8V and 18V, V_I = 6.5V	–25	1	25	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3V, output sink current = 0.4mA			250	mV
		V_{DD} = 1.8V, output sink current = 3mA			250	
		V_{DD} = 5V, output sink current = 5mA			250	
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8V and 18V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8V, V_O = 18V			300	
I_{DD}	Supply current	V_{DD} = 1.8V, no load		5.5	11	µA
		V_{DD} = 5V		6	13	
		V_{DD} = 12V		6	13	
		V_{DD} = 18V		7	13	
UVLO	Undervoltage lockout (2)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined below $V_{(POR)}$.

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5.6 Timing Requirements

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay (1)	V_{DD} = 5V, 10mV input overdrive, R_P = 10kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400mV, see 图 5-1		18		µs
$t_{pd(LH)}$	Low-to-high propagation delay (1)	V_{DD} = 5V, 10mV input overdrive, R_P = 10kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400mV, see 图 5-1		29		µs
$t_{d(start)}$	Start-up delay (2)			150		µs

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
(2) During power on, V_{DD} must exceed 1.8V for at least 150µs before the output is in a correct state.

5.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5V, 10mV input overdrive, R_P = 10kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_f	Output fall time	V_{DD} = 5V, 10mV input overdrive, R_P = 10kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs

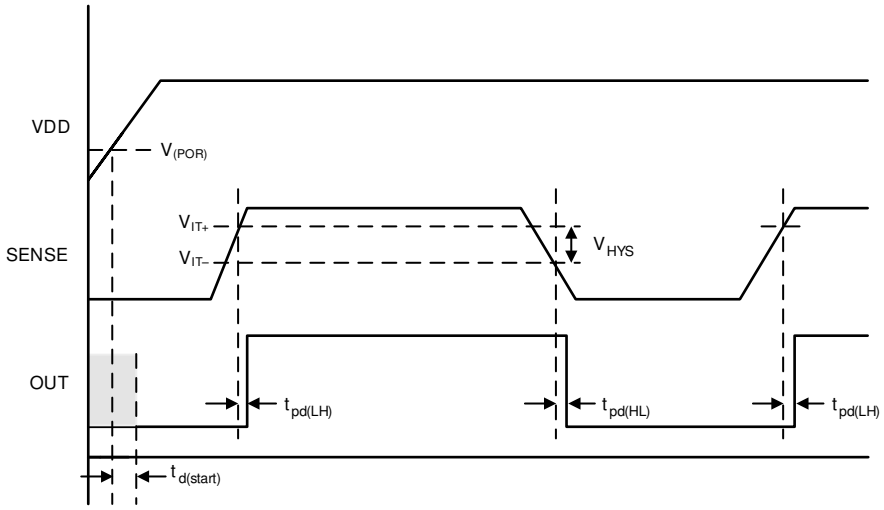


图 5-1. Timing Diagram

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5.8 Typical Characteristics

at T_J = 25°C and V_{DD} = 5V (unless otherwise noted)

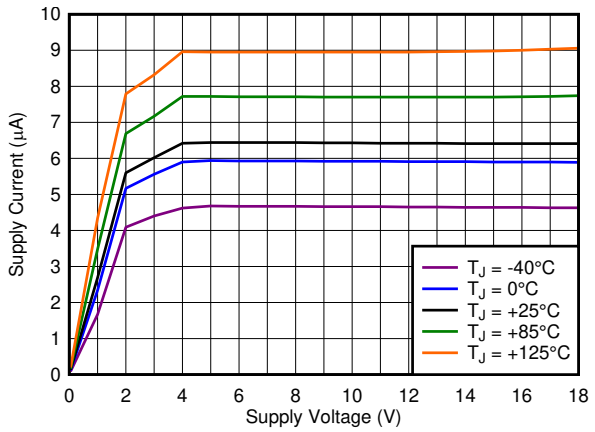


图 5-2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

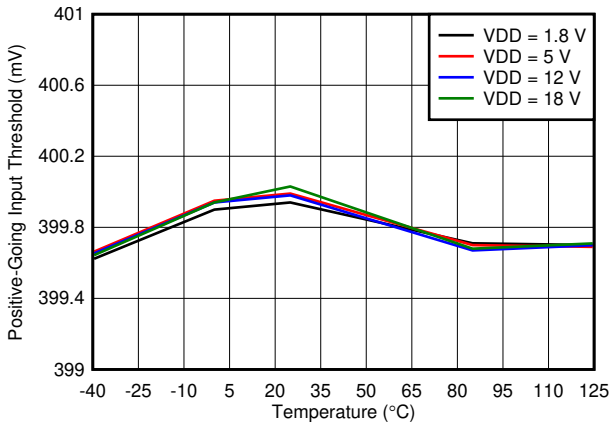


图 5-3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

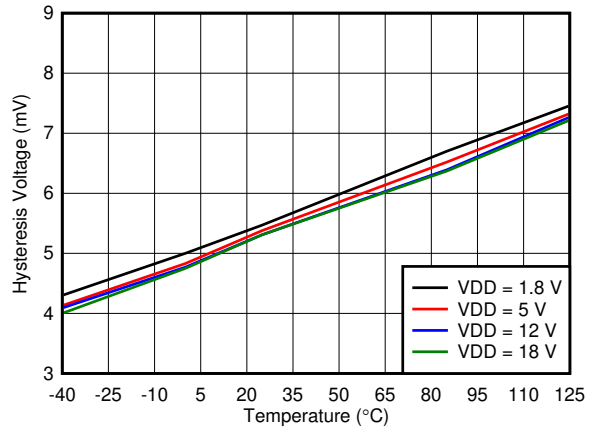


图 5-4. Hysteresis (V_{hys}) vs Temperature

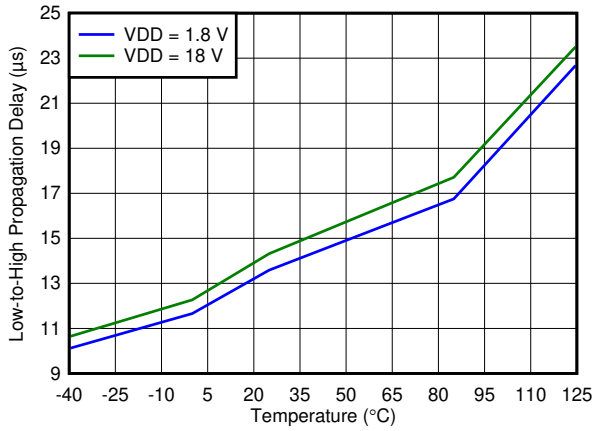


图 5-5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)

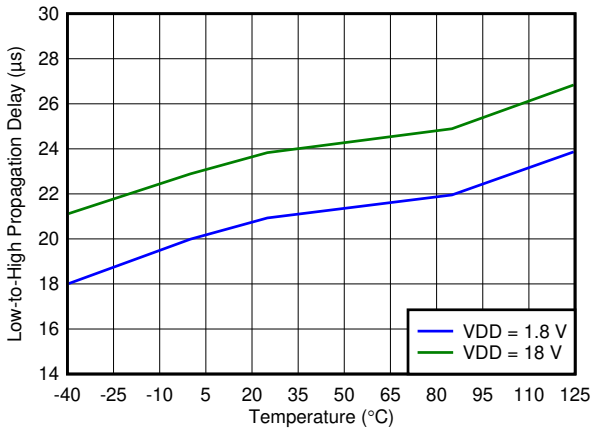
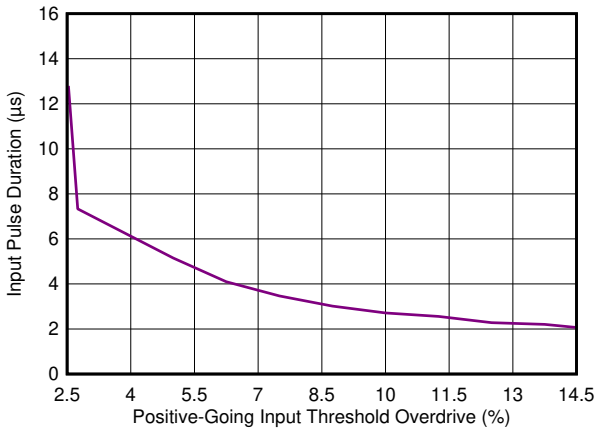


图 5-6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)



SENSE = negative spike below V_{IT-}

图 5-7. Minimum Pulse Width vs Threshold Overdrive Voltage

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5.8 Typical Characteristics (continued)

at T_J = 25°C and V_{DD} = 5V (unless otherwise noted)

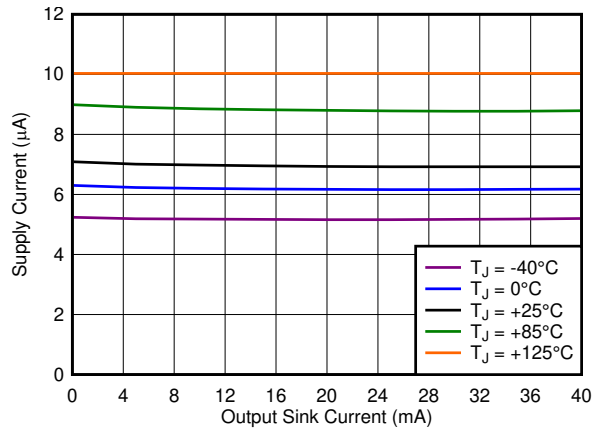


图 5-8. Supply Current (I_{DD}) vs Output Sink Current

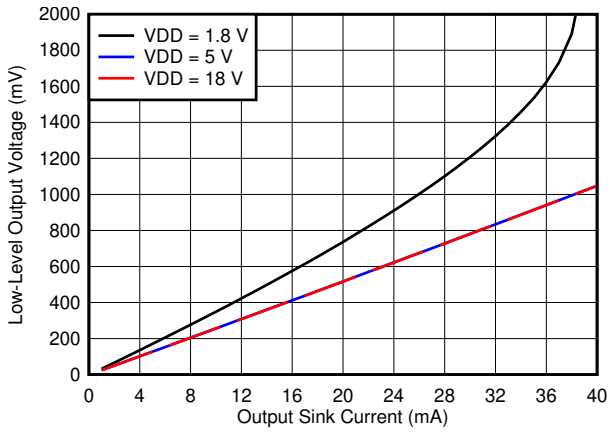


图 5-9. Output Voltage Low (V_{OL}) vs Output Sink Current (– 40°C)

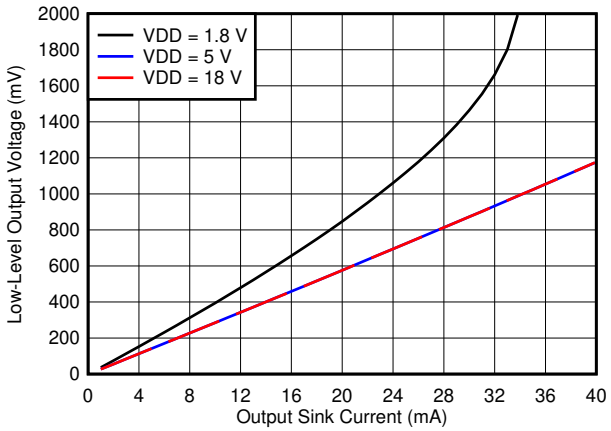


图 5-10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

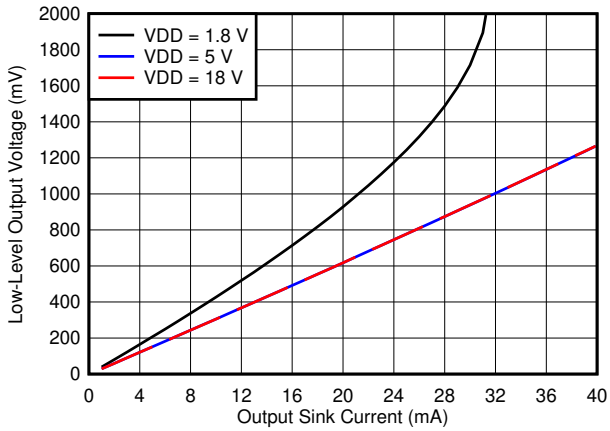


图 5-11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

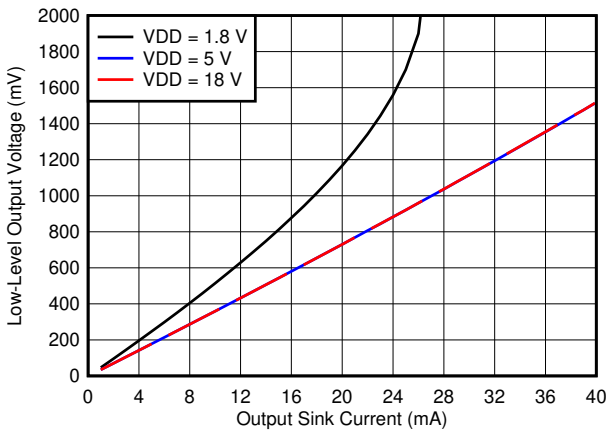


图 5-12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

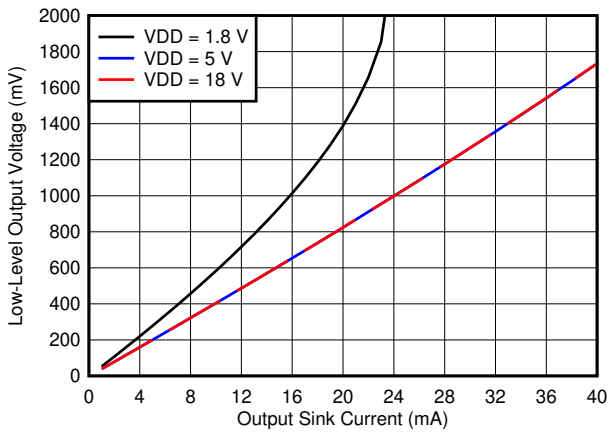


图 5-13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

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6 Detailed Description

6.1 Overview

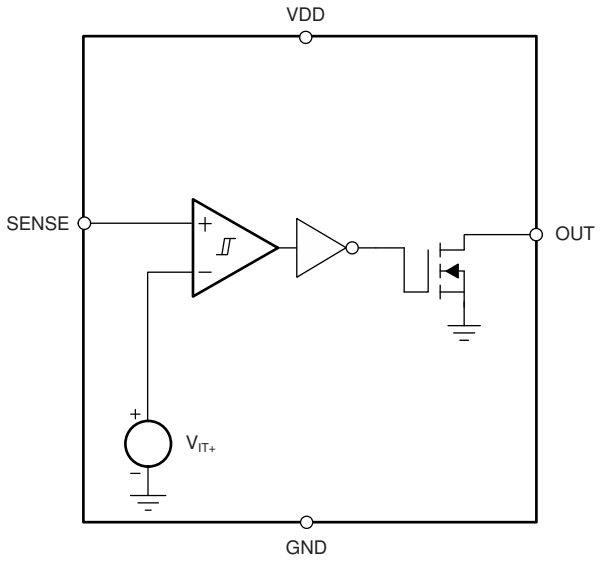
The TPS3710-Q1 provides precision voltage detection. The TPS3710-Q1 is a wide-supply voltage range (1.8V to 18V) device with a high-accuracy rising input threshold of 400mV (1% over temperature) and built-in hysteresis. The output is also rated to 18V, and can sink up to 40mA.

The TPS3710-Q1 asserts the output signal, as shown in 表 6-1. To monitor any voltage above 0.4V, set the input using an external resistor divider network. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

表 6-1. TPS3710-Q1 Truth Table

CONDITION	OUTPUT	STATUS
SENSE > V_{IT+}	OUT high	Output not asserted
SENSE < V_{IT-}	OUT low	Output asserted

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input (SENSE)

The TPS3710-Q1 comparator has two inputs: one external input, and one input connected to the internal reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1nF to 10nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below (V_{IT-}). When the voltage exceeds V_{IT+}, the output (OUT) goes to a high-impedance state; see 图 5-1.

6.3.2 Output (OUT)

In a typical TPS3710-Q1 application, the output is connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the output is connected to the enable input of a voltage regulator (such as a dc-dc converter or low-dropout regulator [LDO]).

The TPS3710-Q1device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TPS3710-Q1 output can be pulled up to 18V, independent of the device supply voltage.

表 6-1 and the *节 6.3.1* section describe how the output is asserted or deasserted. See 图 5-1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

6.3.3 Immunity to Input-Pin Voltage Transients

The TPS3710-Q1i s relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see 图 5-7, *Minimum Pulse Width vs Threshold Overdrive Voltage*.

6.4 Device Functional Modes

6.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on V_{DD} is greater than 1.8V for at least 150µs, the OUT signal correspond to the voltage on SENSE as listed in 表 6-1.

6.4.2 Undervoltage Lockout ($V_{(POR)}$ < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

6.4.3 Power-On Reset (V_{DD} < $V_{(POR)}$)

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), SENSE is in a high-impedance state and the OUT signal is undefined.

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS3710-Q1 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8V to 18V. The device has a high-accuracy comparator with an internal 400mV reference and an open-drain output rated to 18V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

7.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The output is often tied to V_{DD} through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable pins of other devices.

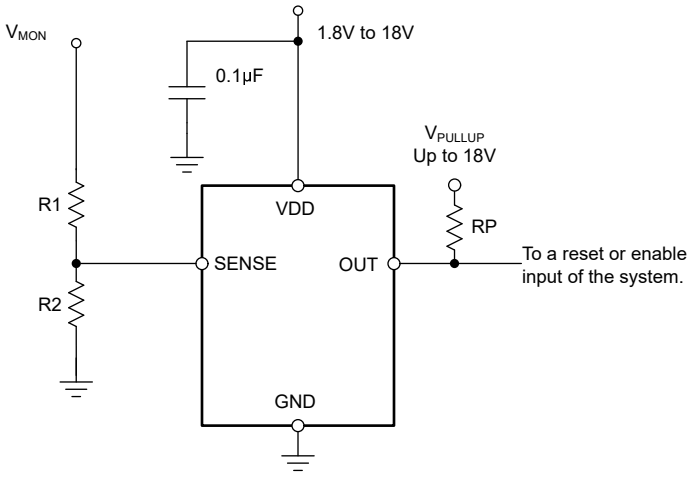


图 7-1. Interfacing to a Voltage Other Than V_{DD}

7.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

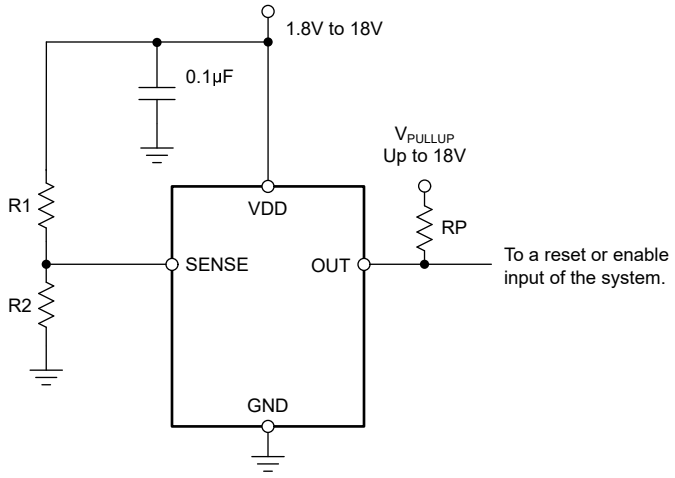
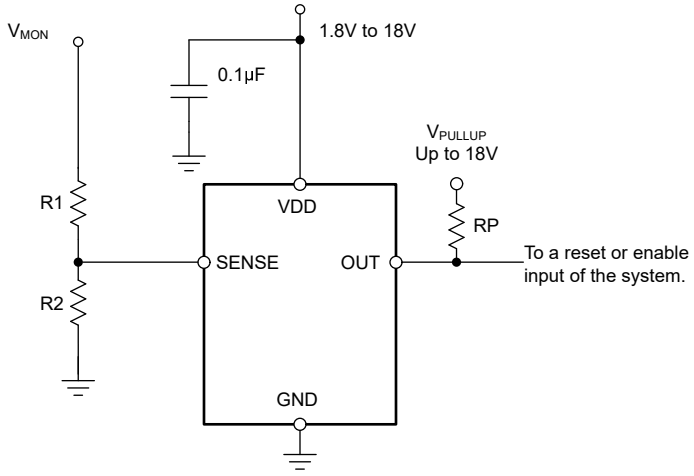


图 7-2. Monitoring the Same Voltage as V_{DD}

7.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum V_{DD} with the use of an external resistor divider network.

图 7-3. Monitoring a Voltage Other Than V_{DD}

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7.2 Typical Application

The TPS3710-Q1 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 to 18V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

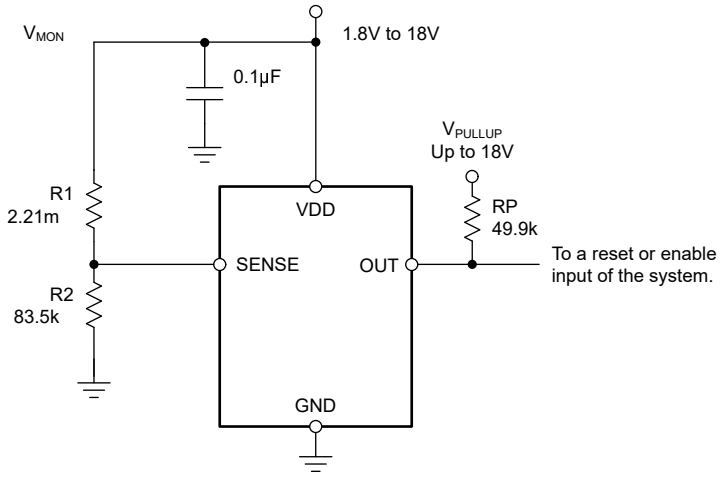


图 7-4. Wide VIN Voltage Monitor

7.2.1 Design Requirements

For this design example, use the values summarized in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)}$= 10.99V (8.33%)

7.2.2 Detailed Design Procedure

7.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using 方程式 1 to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

Choose R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

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7.2.2.2 Pullup Resistor Selection

To make ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{lkg(OD)}$) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the *节 5.5*.

Use 方程式 2 to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lkg(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (2)$$

7.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1 µF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher value capacitor can be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

7.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1nF to 10nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

7.2.3 Application Curve

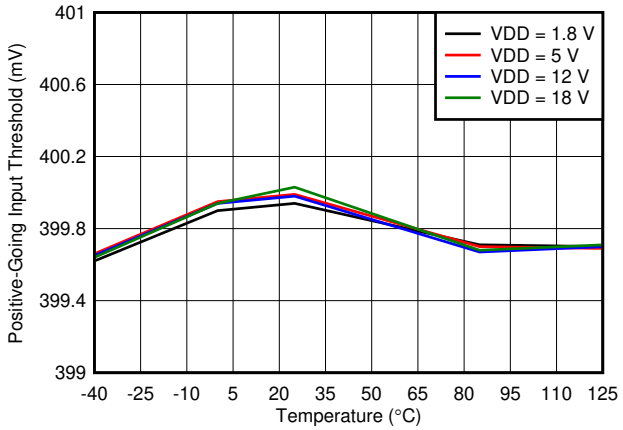


图 7-5. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

7.3 Do's and Don'ts

Do connect a 0.1µF decoupling capacitor from V_{DD} to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

7.4 Power-Supply Recommendations

This device operates from an input voltage supply range between 1.8V and 18V.

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7.5 Layout

7.5.1 Layout Guidelines

Placing a 0.1µF capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

7.5.2 Layout Example

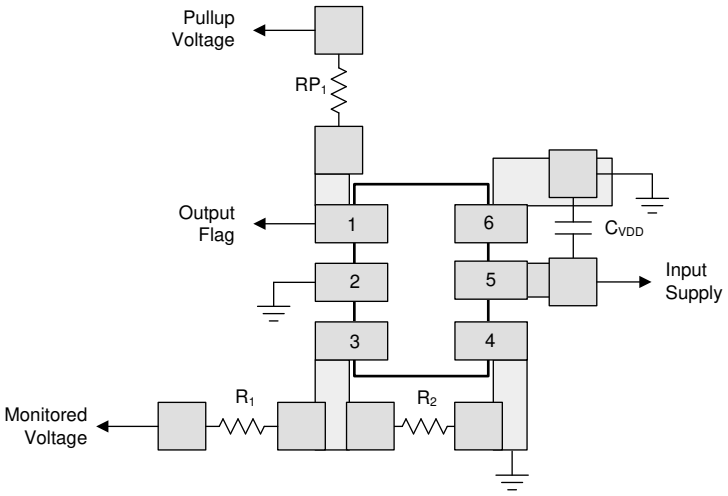


图 7-6. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT	DESCRIPTION
TPS3710**yyyz**	**yyy** is package designator **z** is package quantity

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Optimizing Resistor Dividers at a Comparator Input

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2017) to Revision A (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 通篇更新了图片，将 VDD 引脚处的电容值从 0.01uF 更改为 0.1uF	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3710QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS3710-Q1 :

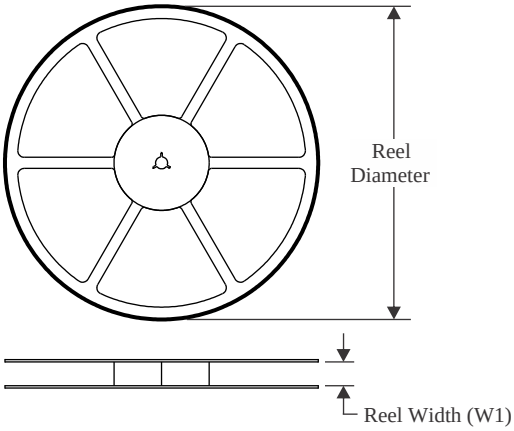
- Catalog : TPS3710

NOTE: Qualified Version Definitions:

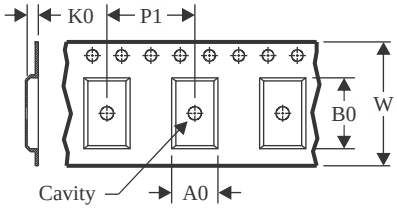
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

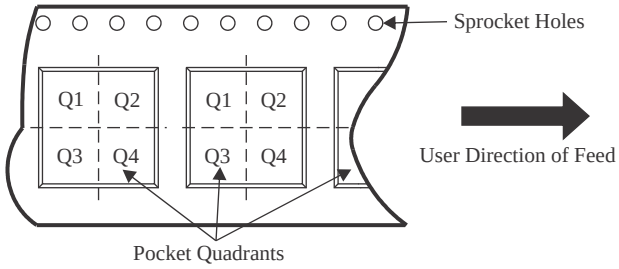


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

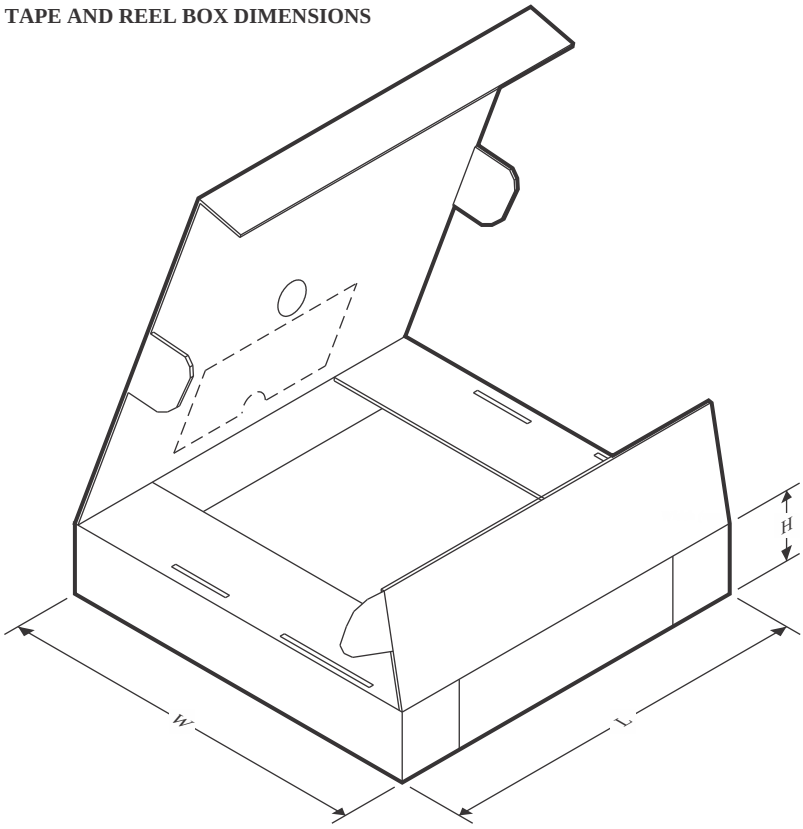
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3710QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

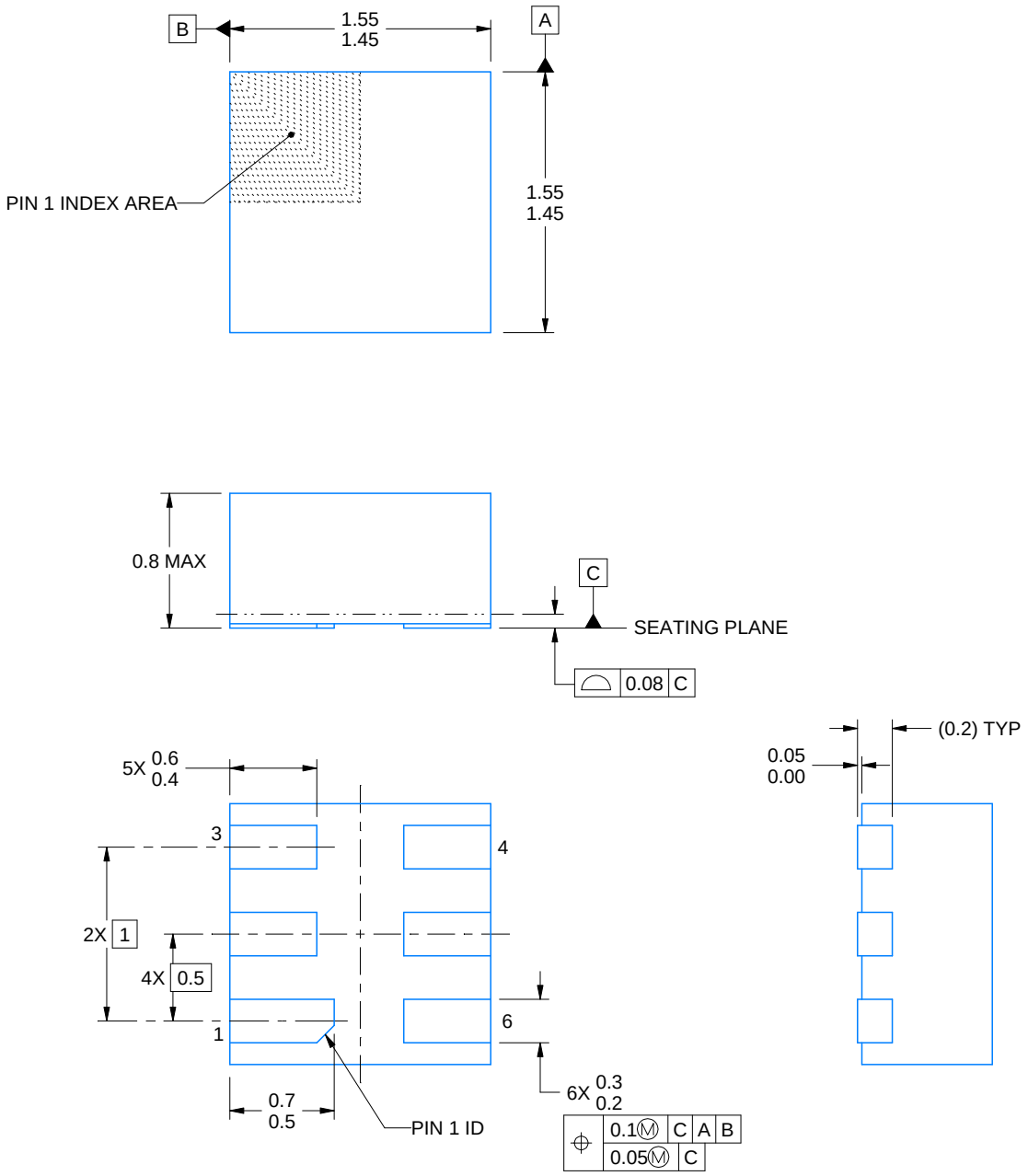
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3710QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

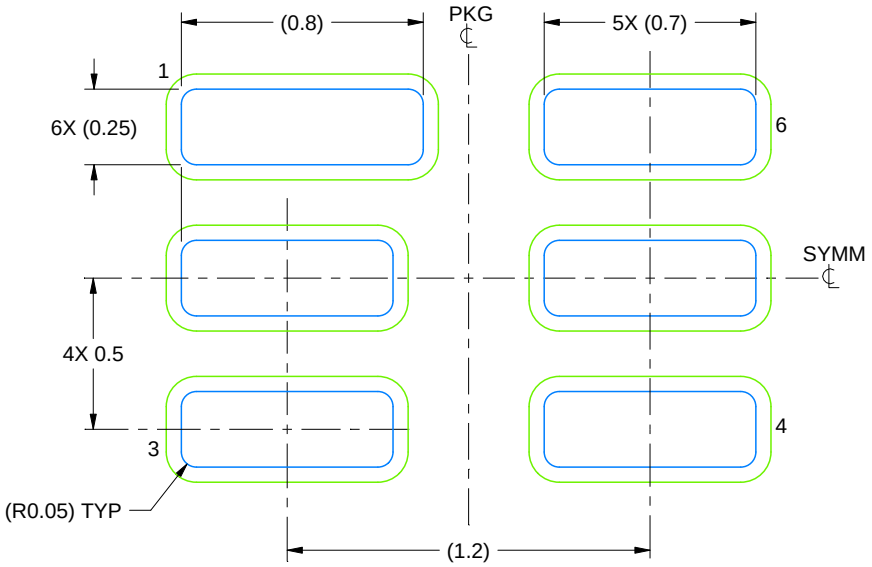
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

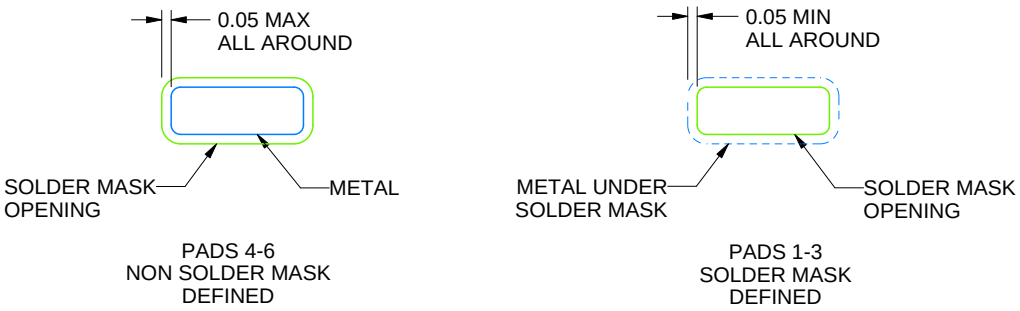
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

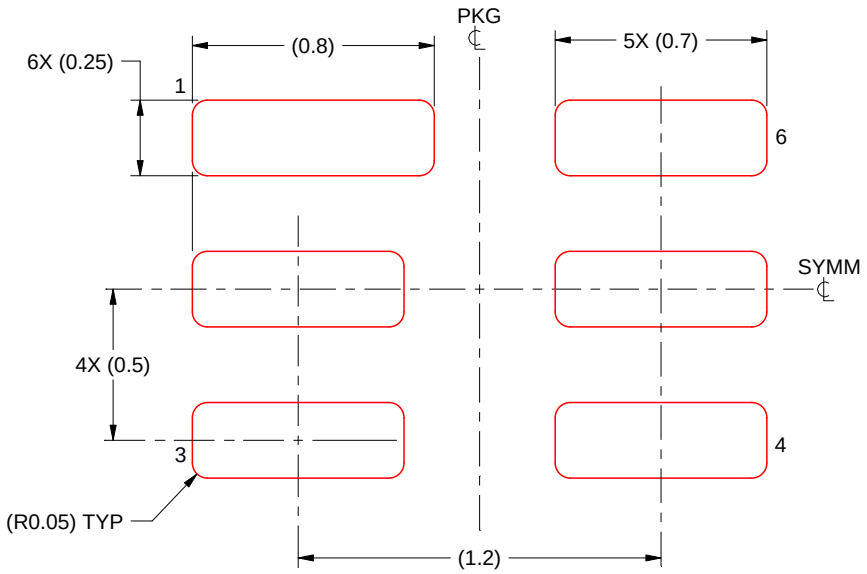
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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