Ordering number : EN4544

SANYO

No. 4544

LC89960, 89960M

NTSC 1H Delay Line

Overview

The LC89960 and LC89960M are delay lines and produce a 1H delayed signal for the NTSC format, with an external low-pass filter.

Functions

- 905-stage shift register
- Auto-bias circuit
- Sync tip clamp circuit
- Sample-and-hold circuit
- PLL 4 × frequency multiplier circuit
- VCO (4 fsc) output circuit

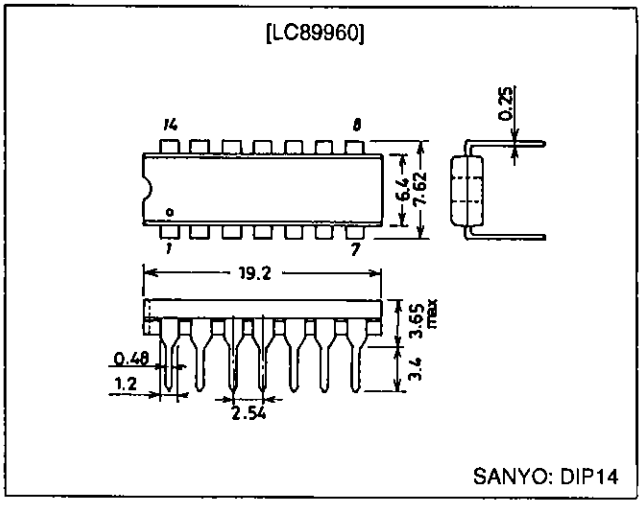
Features

- Single 5 V power supply
- The provision of a built-in 4 × frequency multiplier circuit allows the LC89960, 89960M to operate as a high bandwidth delay line from a 3.58 MHz clock input.
- Built-in peripheral circuits allow operation with minimal external circuits.
- Positive phase signal input, reverse phase signal output

Package Dimensions

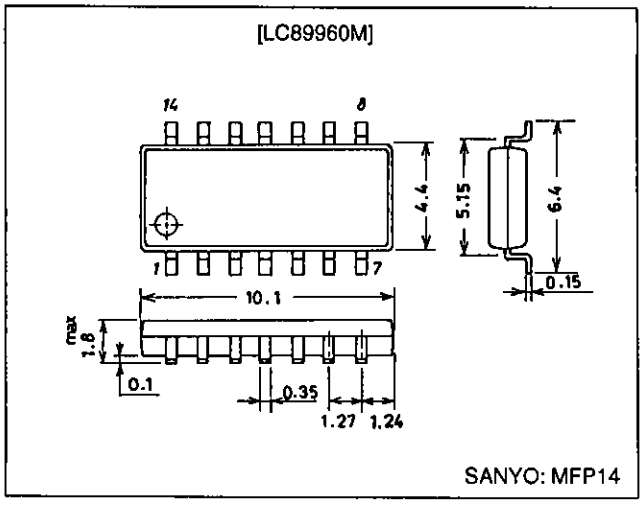
unit: mm

3003A-DIP14



unit: mm

3034A-MFP14



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89960	450	mW
		LC89960M	250	mW
Operating temperature	Topr		−10 to +60	°C
Storage temperature	Tstg		−55 to +150	°C

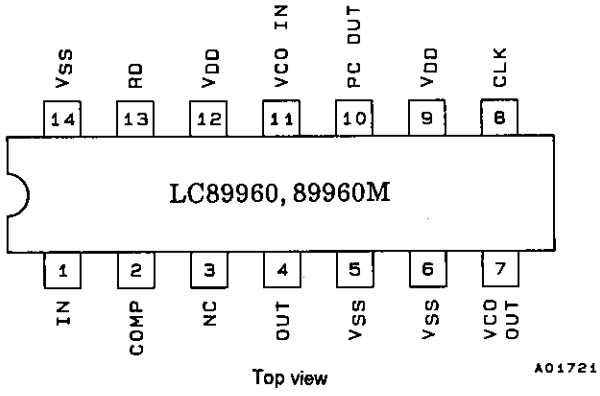
SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg.,1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}	Sine wave	300	500	1000	mVp-p
Clock frequency	F_{CLK}			3.579545		MHz
Signal input amplitude	V_{IN}	*		500	572	mVp-p

Note: * Since sync tip clamping is normally performed, the input signal must be connected in a low impedance state.

Pin Assignment

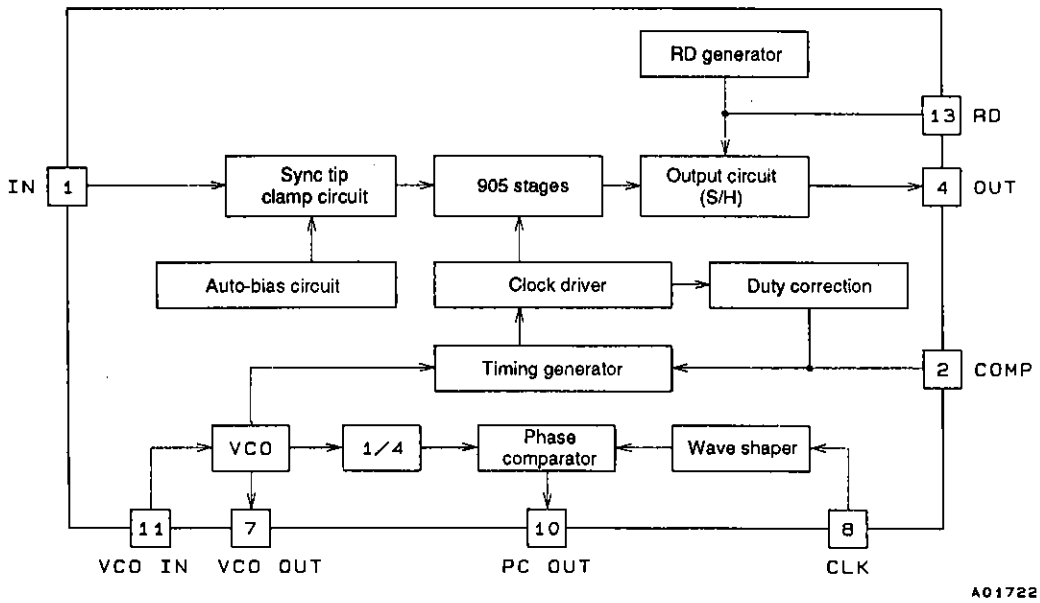


Top view

Pin Functions

Pin No.	Symbol	Function
1	IN	Signal input
2	COMP	Duty correction output
3	NC	
4	OUT	Delayed signal output
5	V_{SS}	GND
6	V_{SS}	GND
7	VCO OUT	VCO output
8	CLK	Clock input
9	V_{DD}	Power supply
10	PC OUT	Phase comparator output
11	VCO IN	VCO input
12	V_{DD}	Power supply
13	RD	High voltage generator output for Reset Drain
14	V_{SS}	GND

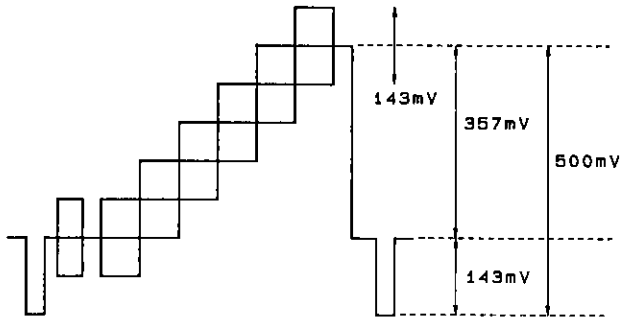
Block Diagram



Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, CLK = 3.579545 MHz; 500 mVp-p

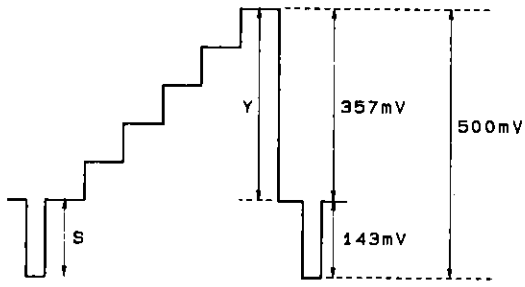
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current	I_{DD}	No signal input	15	25	35	mA
Voltage gain	G_V	With a 200 kHz 0.5 Vp-p input	–2.5	–0.5	+1.5	dB
Frequency response	G_f	3.58 MHz, 0.2 Vp-p/200 kHz, 0.2 Vp-p	–2	–1	0	dB
Differential gain	D_G	*1	0	5	7	%
Differential phase	D_P	*1	0	5	7	deg
Linearity (SYNC)	L_S	*2	37	40	43	%
Clock leakage	L_{CLK}	No signal input, the 4 fsc component		15	50	mVrms
Noise level	N_O	No signal input, 0.2 to 4.2 MHz bandwidth With the fsc trap		1.0	3.0	mVrms
Output impedance	Z_O		100	250	500	Ω
Delay time	T_D			63.28		µs

Note: 1. Input signal/output signal



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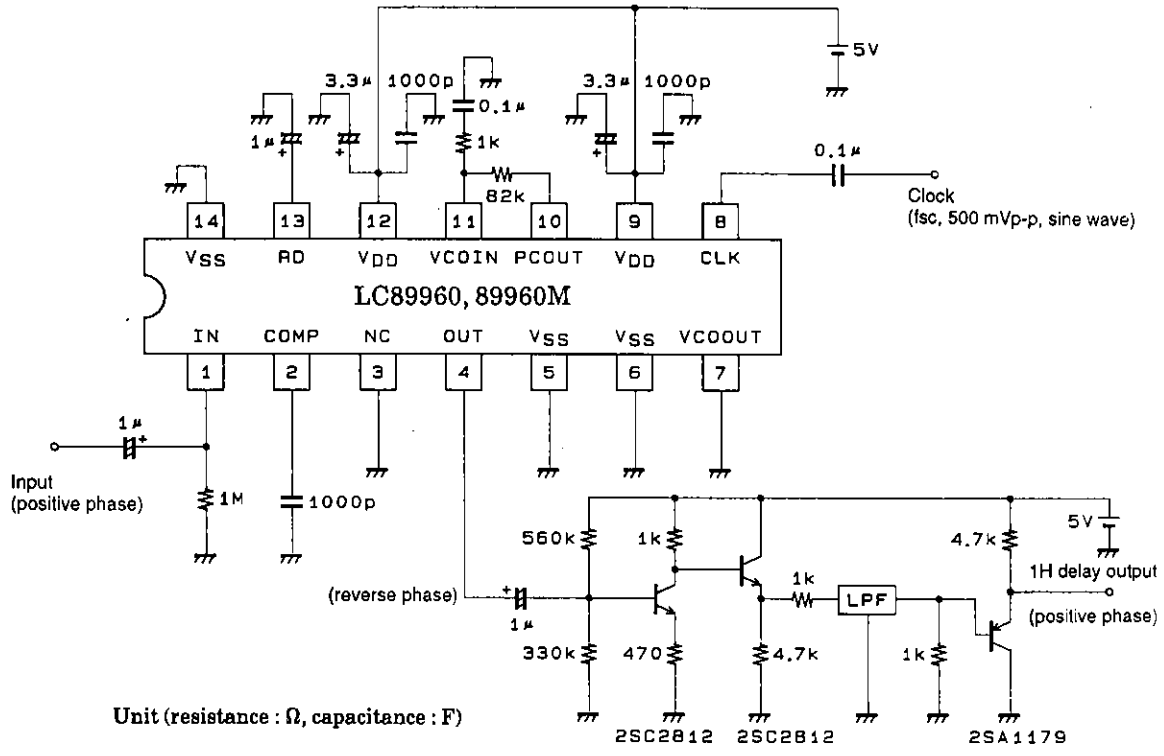
2. Input signal/output signal



$$L_S = \frac{S}{Y}$$

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Sample Application Circuit

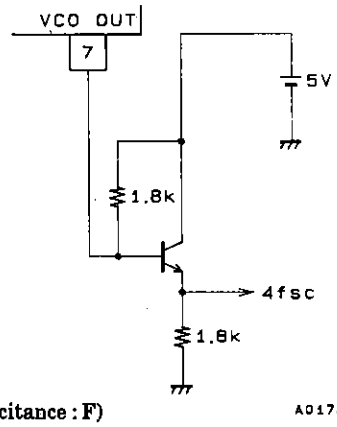


Unit (resistance : Ω, capacitance : F)

Low-pass filter delay time:
about 270 ns

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When the VCO output is used
(4fsc output)



Unit (resistance : Ω, capacitance : F)

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