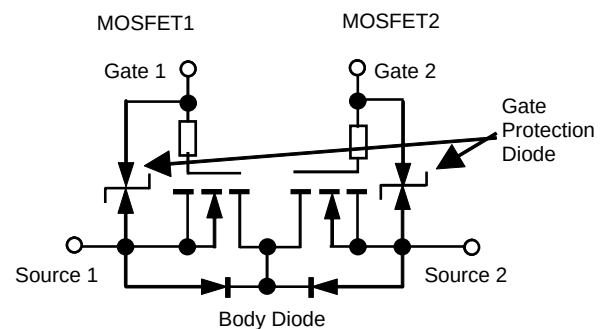
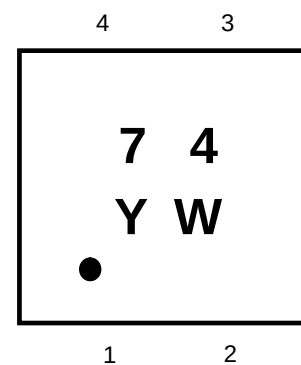


WNMD2174
Dual N-Channel, 12V, 6A, Power MOSFET
www.sh-willsemi.com

V _{SSS} (V)	Typ R _{SS(on)} (mΩ)
12	19@ V _{GS} =4.5V
	20@ V _{GS} =4.0V
	21@ V _{GS} =3.8V
	22@ V _{GS} =3.1V
	25@ V _{GS} =2.5V
ESD Rating:2000V HBM	


Descriptions

The WNMD2174 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent R_{SS(ON)} with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2174 is available in CSP 4L package. Standard Product WNMD2174 is Pb-free and Halogen-free.

CSP 4L


- 1: Source 1 74 = Device Code
- 2: Gate 1 Y = Year
- 3: Gate 2 W = Week (A~z)
- 4: Source 2

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Small package CSP 4L

Pin configuration (TOP view)&Marking
Order information

Device	Package	Shipping
WNMD2174-4/TR	CSP 4L	3000/Reel&Tape

Applications

- Lithium-Ion battery protection circuit

Electronics Characteristics (Ta=25°C, unless otherwise noted)

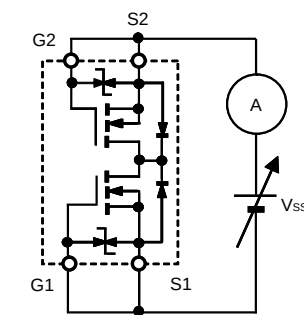
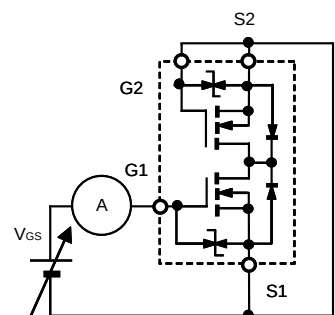
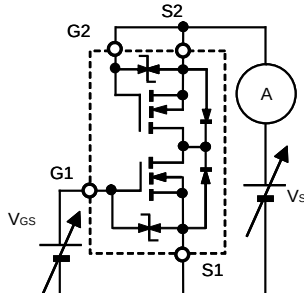
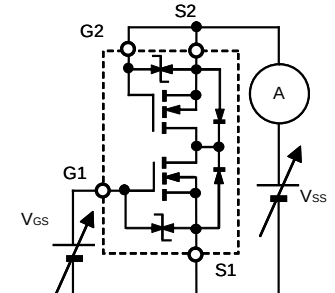
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V _{SSS}	V _{GS} = 0 V, I _S = 250uA	12			V
Zero Gate Voltage Drain Current	I _{SSS}	V _{SS} =12 V, V _{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I _{GSS}	V _{SS} = 0 V, V _{GS} = ±10V TEST CIRCUIT 2			±10	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{GS} = V _{SS} , I _S = 250uA TEST CIRCUIT 3	0.4	0.8	1.2	V
Source to Source On-state Resistance	R _{SS(on)}	V _{GS} = 4.5V, I _S = 3.0A TEST CIRCUIT 5	10	19	25	mΩ
		V _{GS} = 4.0V, I _S = 3.0A TEST CIRCUIT 5	11	20	27	
		V _{GS} = 3.8V, I _S = 3.0A TEST CIRCUIT 5	11.5	21	28	
		V _{GS} = 3.1V, I _S = 3.0A TEST CIRCUIT 5	12	22	31	
		V _{GS} = 2.5V, I _S = 3.0A TEST CIRCUIT 5	14	25	35	
Forward Transfer Admittance	y _{fs}	V _{SS} = 10 V, I _S = 1.8A TEST CIRCUIT 4		9		S
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	V _{F(S-S)}	V _{GS} = 0 V, I _F = 1.0A TEST CIRCUIT 6		0.9	1.5	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V _{GS} = 4.5 V, V _{SS} =10V, R _L =3.3 Ω , I _S =3A,R _G =6Ω TEST CIRCUIT 8		680		ns
Rise Time	tr			2960		
Turn-Off Delay Time	td(OFF)			6480		
Fall Time	tf			6760		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1kHz, V _{SS} = 10 V TEST CIRCUIT 7		1313		pF
Output Capacitance	C _{OSS}			257		
Reverse Transfer Capacitance	C _{RSS}			238		
Total Gate Charge	Q _{G(TOT)}	V _{G1S1} = 4.5 V, V _{SS} = 10V, I _S =6A TEST CIRCUIT 9		17.8		nC
Threshold Gate Charge	Q _{G(TH)}			0.79		
Gate-to-Source Charge	Q _{GS}			2.5		
Gate-to-Drain Charge	Q _{GD}			6.4		

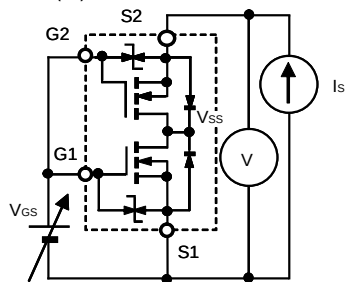
Absolute Maximum ratings

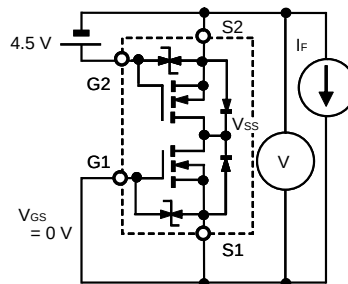
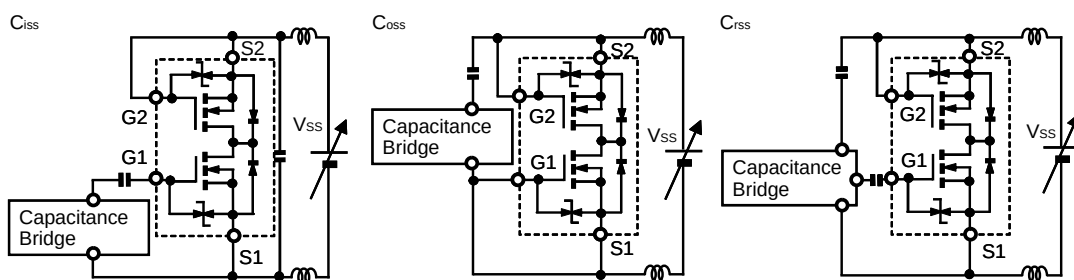
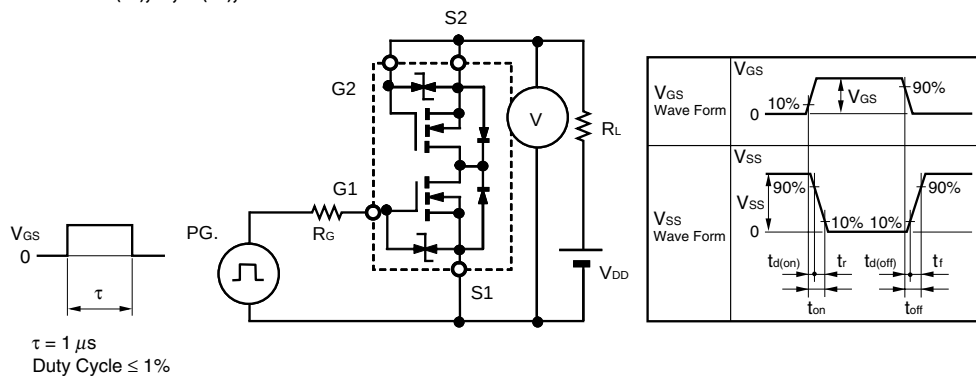
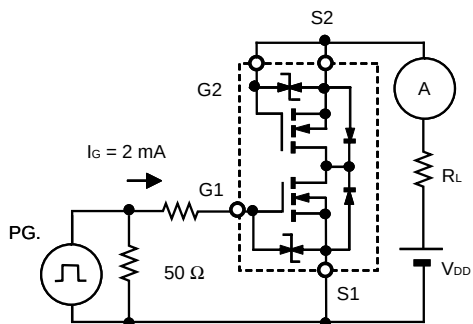
Parameter	Symbol	10 s	Steady State	Unit
Source to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{SSS}	12	V	
Gate to Source Voltage ($V_{SS} = 0\text{ V}$)	V_{GSS}	± 10		
Source Current (pulse) ^{Note.c}	$I_{S(\text{pulse})}$	60	A	
Source Current (DC)	I_S	6	A	
Channel Temperature	T_{ch}	150	°C	
Storage Temperature Range	T_{stg}	-55 to 150	°C	

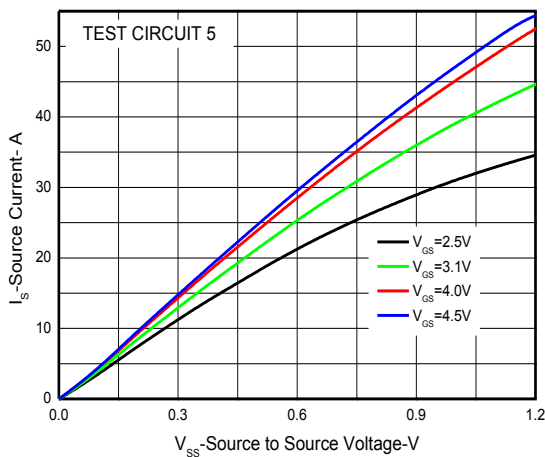
Note.c $PW \leq 10\mu s$, duty cycle $\leq 1\%$;

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

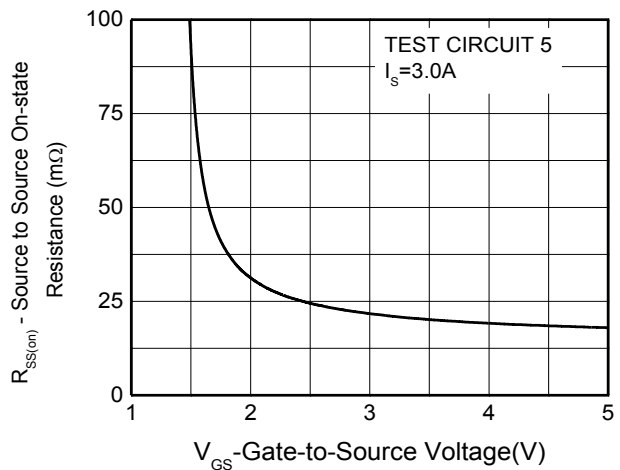
TEST CIRCUIT 1 I_{SSS} 	TEST CIRCUIT 2 I_{GSS} When FET1 is measured, between GATE and SOURCE of FET2 are shorted. 
TEST CIRCUIT 3 $V_{GS(\text{off})}$ When FET1 is measured, between GATE and SOURCE of FET2 are shorted. 	TEST CIRCUIT 4 y_{fs} $\Delta I_S / \Delta V_{GS}$ 

TEST CIRCUIT 5 $R_{SS(on)}$
 V_{SS}/I_S

TEST CIRCUIT 6 $V_{F(S-S)}$

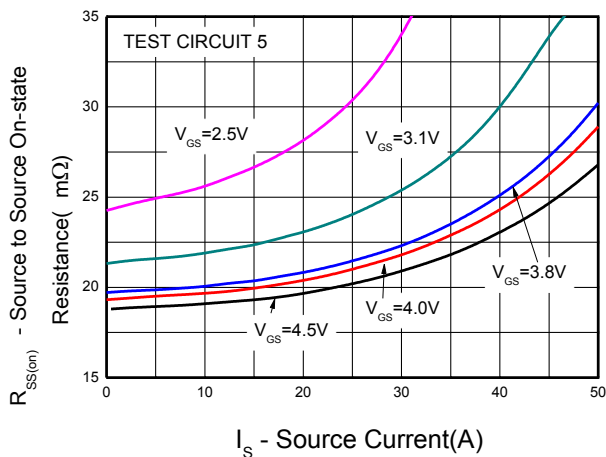
 When FET1 is measured,
FET2 is added $V_{GS} + 4.5\text{ V}$.

TEST CIRCUIT 7

TEST CIRCUIT 8 $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

TEST CIRCUIT 9 Q_G


Typical Characteristics (Ta=25°C, unless otherwise noted)


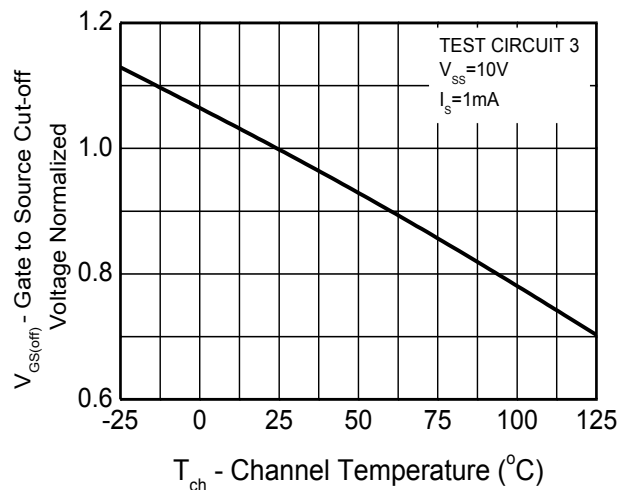
**SOURCE CURRENT vs.
SOURCE TO SOURCE VOLTAGE**



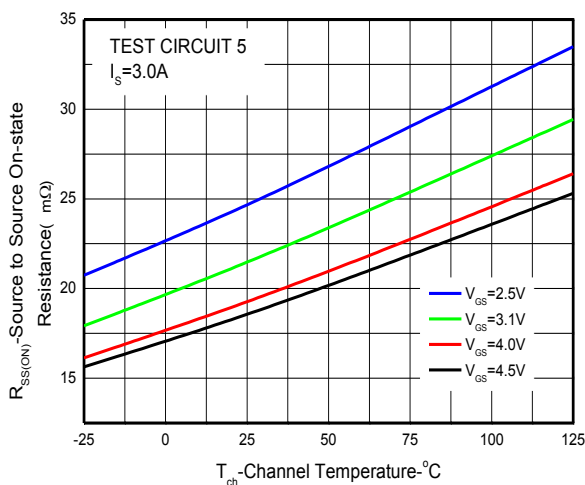
**SOURCE TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE**



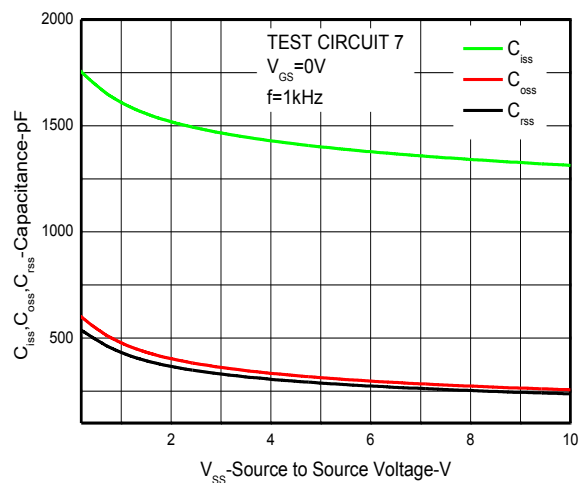
**SOURCE TO SOURCE ON-STATE RESISTANCE vs.
SOURCE CURRENT**



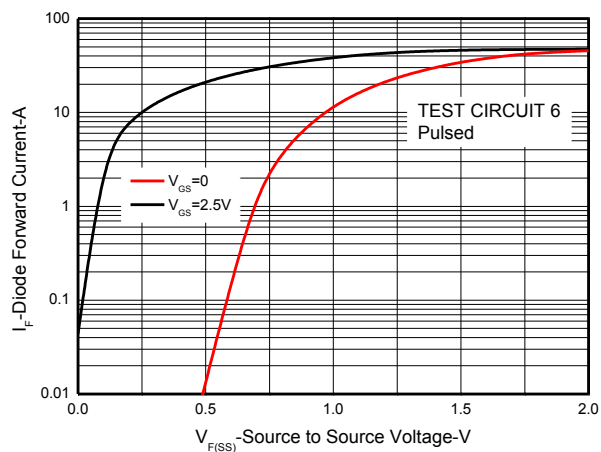
**GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE**



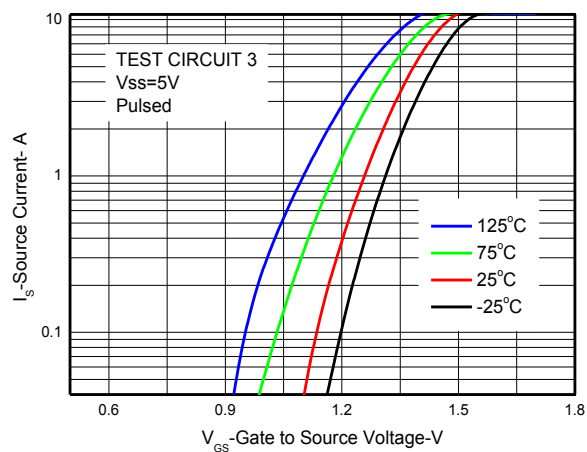
**SOURCE TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE**



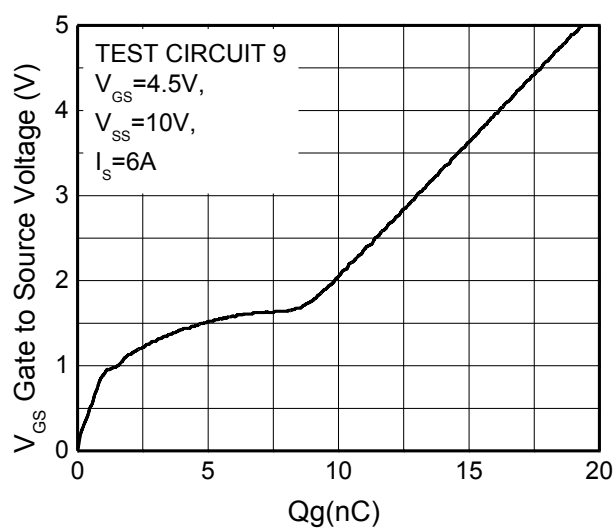
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



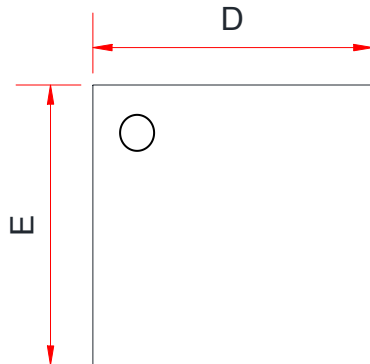
FORWARD TRANSFER CHARACTERISTICS



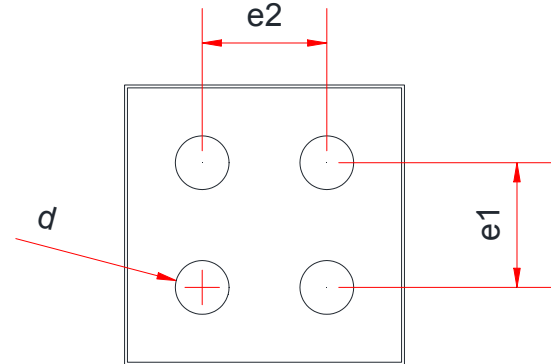
DYNAMIC INPUT CHARACTERISTICS

Package outline dimensions (Unit:um)

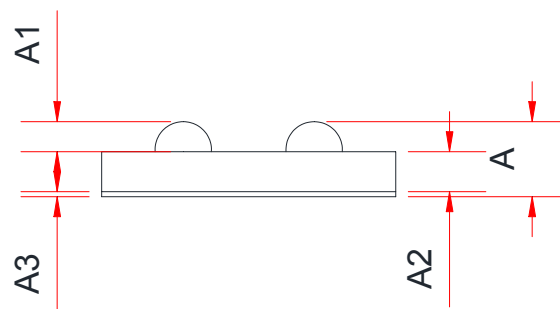
CSP-4L



TOP VIEW

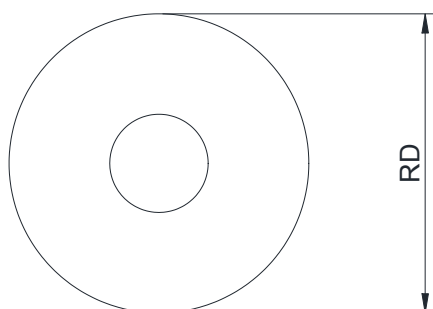
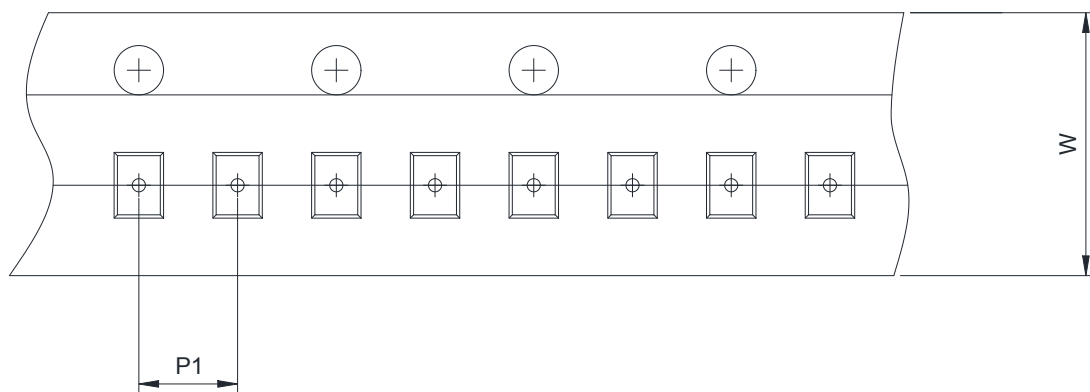
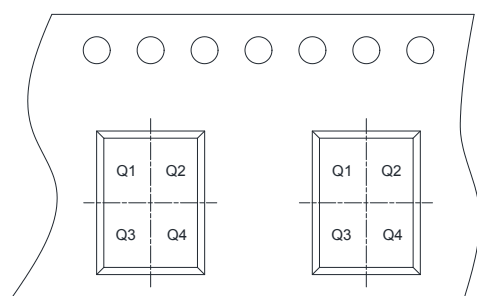


BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.33	0.37	0.42
A1	0.13	0.15	0.17
A2	0.18	0.20	0.22
A3	0.02	—	0.030
D	1.43	1.46	1.49
E	1.43	1.46	1.49
e1	0.65 Typ.		
e2	0.65 Typ.		
d	0.26	0.28	0.30

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape



 User Direction of Feed

RD	Reel Dimension	☒ 7inch	☐ 13inch
W	Overall width of the carrier tape	☒ 8mm	☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm	☒ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☒ Q1	☐ Q2 ☐ Q3 ☐ Q4