R2A25107KFP

Intelligent Power Device for MOSFET Pre-drive

R07DS0689EJ0100
Rev.1.00
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Description

The R2A25107KFP device is an intelligent power device to pre-drive the FET inverter of a 3-phase blushless motor. This device contains three sets of pre-driver that are applicable to both 12-V and 24-V battery systems. This IC also contains a step down converter, charge pump circuit for the power supply of high-side MOSFET gate driver, 5 V series regulator, watchdog timer and protection circuits for thermal shutdown (TSD) and over-current detection.

Features

- Wide operating voltage range: 7 V to 36 V (VBAT, VBAT2)
- On-chip 3-phase pre-driver circuit
  - PWM control: up to 20 kHz
  - Totem pole type MOSFET gate drive circuit
- On-chip power supplies
  - Step down converter: 6.2 V typ.
  - Charge pump circuit for power supply of high-side FET drive: >5 V
  - 5-V series regulator for MCU: <70 mA
- On-chip protection circuits
  - Thermal shutdown (TSD)
  - Over-current detection in the step down converter
  - Over-current detection of motor current
- On-chip watchdog timer circuit (WDT)
- Band gap reference circuit
- Internal oscillator: 265 kHz typ.
- 48-pin LFQFP package

Application

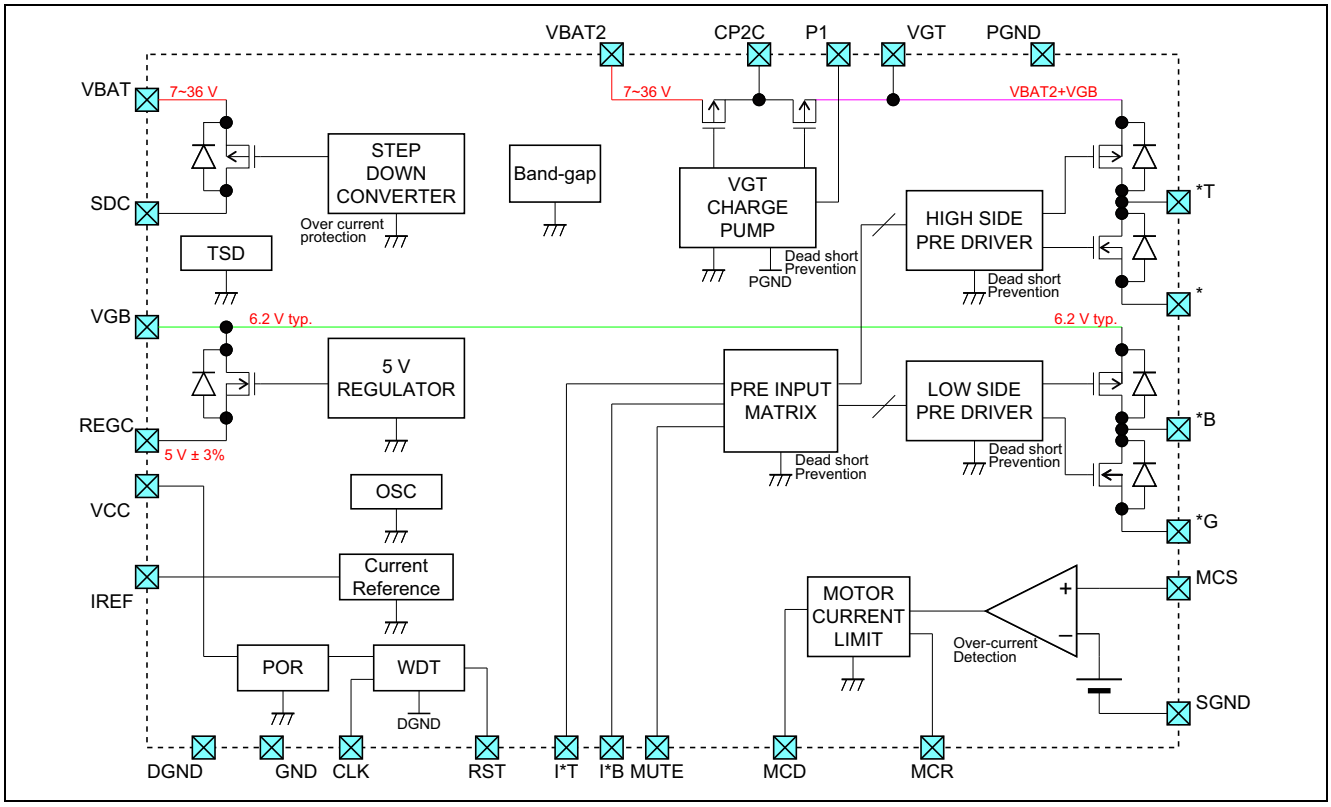
- Pre-driver for middle class 3-phase blushless motors (up to 50 A)
- Best suited for automotive

Ordering Information

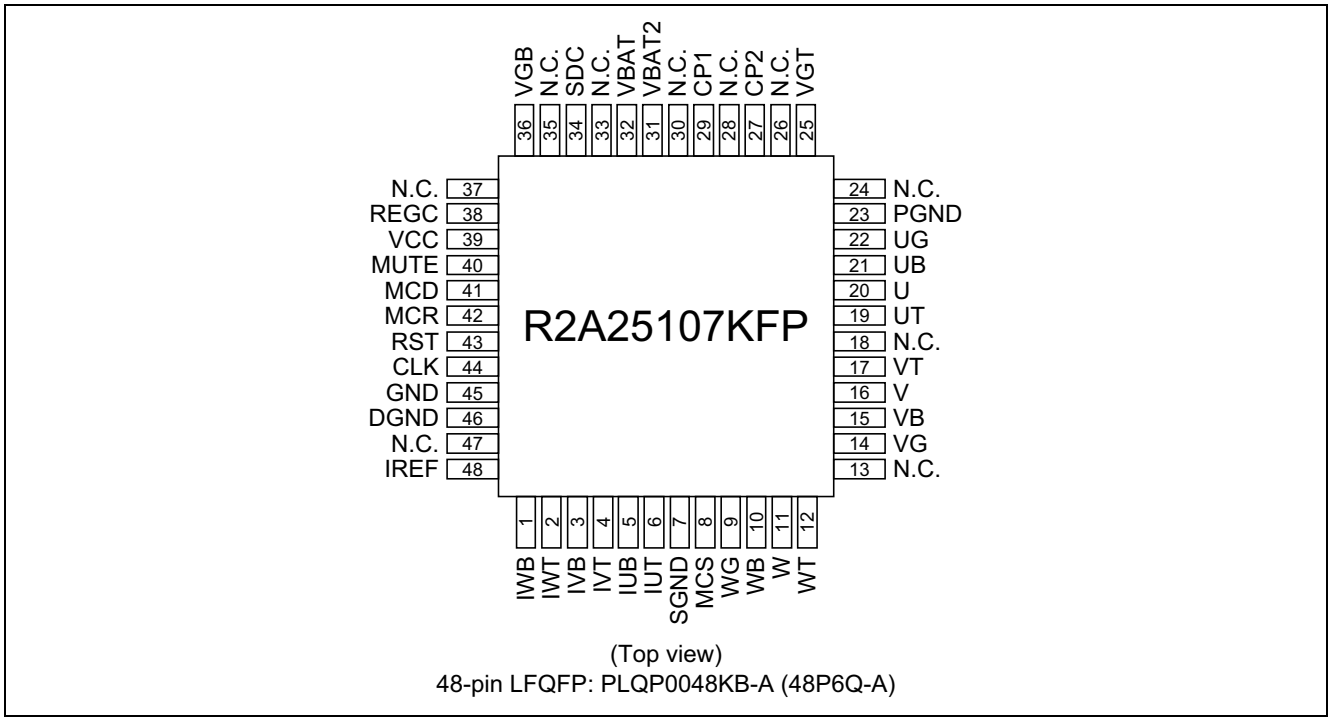
Part No.	Lead Plating	Packing	Package
R2A25107KFP#U5	Sn-Cu	Tray	PLQP0048KB-A

Note: The information contained in this document is the one that was obtained when the document was issued, and may be subject to change.

Block Diagram



Pin Arrangement



(Top view)
48-pin LFQFP: PLQP0048KB-A (48P6Q-A)

Pin Description

Pin No.	Pin Name	Function
1	IWB	Input pin for low side of W phase
2	IWT	Input pin for high side of W phase
3	IVB	Input pin for low side of V phase
4	IVT	Input pin for high side of V phase
5	IUB	Input pin for low side of U phase
6	IUT	Input pin for high side of U phase
7	SGND	GND pin for Motor current
8	MCS	Input pin for Motor current detection
9	WG	GND pin of W phase
10	WB	Output pin for low side gate drive of W phase
11	W	Output pin of W phase
12	WT	Output pin for high side gate drive of W phase
13	N.C.	No connection
14	VG	GND pin of V phase
15	VB	Output pin for low side gate drive of V phase
16	V	Output pin of V phase
17	VT	Output pin for high side gate drive of V phase
18	N.C.	No connection
19	UT	Output pin for high side gate drive of U phase
20	U	Output pin of U phase
21	UB	Output pin for low side gate drive of U phase
22	UG	GND pin of U phase
23	PGND	Power GND pin
24	N.C.	No connection
25	VGT	Power supply pin of high side gate drive
26	N.C.	No connection
27	CP2	Pin to connect external capacitor for charge pump 2
28	N.C.	No connection
29	CP1	Pin to connect external capacitor for charge pump 1
30	N.C.	No connection
31	VBAT2	Power supply pin of charge pump
32	VBAT	Power supply pin to connect battery
33	N.C.	No connection
34	SDC	Output pin for step down converter drive
35	N.C.	No connection
36	VGB	Power supply pin of low side gate drive
37	N.C.	No connection
38	REGC	Output pin of 5-V series regulator
39	VCC	5 V power supply pin
40	MUTE	Input pin of mute
41	MCD	Output pin of motor over-current detection
42	MCR	Input pin to reset motor over-current detection
43	RST	Output pin of reset
44	CLK	Input pin of watchdog timer clock
45	GND	GND pin
46	DGND	GND pin of digital circuit
47	N.C.	No connection
48	IREF	Pin for reference current

Absolute Maximum Ratings

(Ta = –40 to 125°C, All of the voltages are with respect to GND, unless otherwise specified)

Item	Symbol	Ratings			Unit	Test Conditions
		Min.	Typ.	Max.		
Battery power supply voltage	Vbat	–0.3	—	40	V	VBAT, VBAT2 pin, DC and short pulse (<500 ms) condition
Step down converter power supply voltage	Vgb	–0.3	—	40	V	VGB pin
Step down converter output voltage	Vsdc	–0.3	—	40	V	SDC pin
High side gate driver supply voltage	Vgt	VBAT2 –0.6	—	60	V	VGT pin
CP1 pin voltage	Vcp1	–0.3	—	Vgb +0.3	V	CP1 pin
CP2 pin voltage	Vcp2	VBAT2 –0.3	—	Vgt +0.3	V	CP2 pin
High side gate driver output voltage	Vto	Vo –0.3	—	Vgt +0.3	V	UT, VT, WT pin
Motor output voltage	Vo	–1.0	—	Vgt +0.6	V	U, V, W pin
Low side gate driver output voltage	Vbo	–0.3	—	Vgb +0.3	V	UB, VB, WB pin
Motor GND voltage	Vbg	–1.0	—	Vgb +0.6	V	UG, VG, WG pin
MCS voltage	Vmcs	–1.0	—	Vcc +0.3	V	MCS pin
5 V power supply voltage	V_{REGC}	–0.3	—	6.0	V	REGC, VCC pin
5 V Input/output voltage	Vin	–0.3	—	Vcc +0.3	V	at IUT, IUB, IVT, IVB, IWT, IWB, MUTE, CLK, RST, MCR, MCD, IREF
GND voltage	Vgnd	–0.3	—	+0.3	V	SGND~GND, DGND~GND, PGND~GND
Power dissipation	Pt	—	2.55	—	W	Simulation result, Ta = 25°C, See page 5
Power dissipation derating rate	Kt	—	20.4	—	mW/°C	Simulation result, See page 5
Junction temperature	Tj	—	—	150	°C	
Operating temperature	Topr	–40	—	125	°C	
Storage temperature	Tstg	–55	—	150	°C	

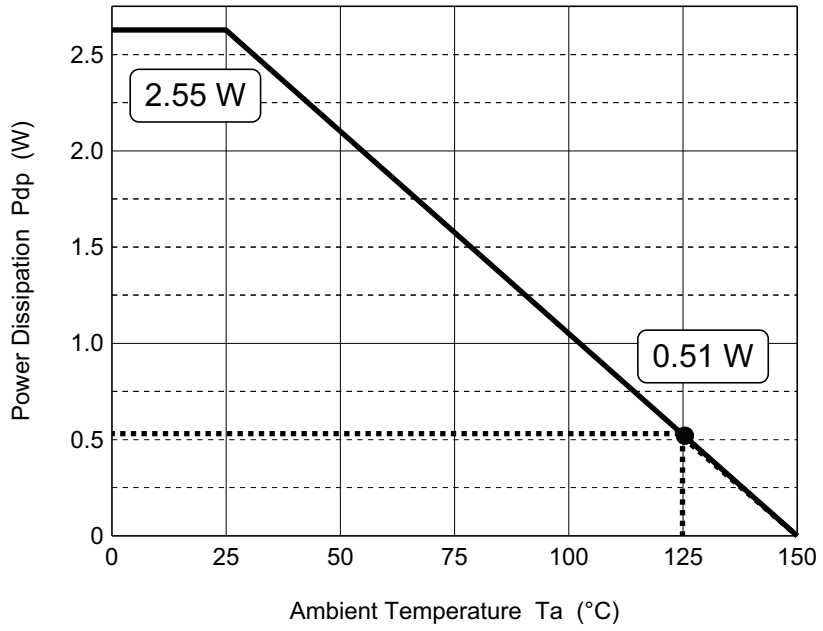
Recommended Operating Conditions

(Ta = –40 to 125°C, VBAT = VBAT2 = 7.0 to 36 V, VGB = 5.9 to 6.5 V, REGC = VCC = 4.85 to 5.15 V, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Battery power supply voltage	Vb	7.0	—	36	V	VBAT, VBAT2 pin
Logic input voltage	V_{IN}	0	—	VCC	V	IUT, IUB, IVT, IVB, IWT, IWB, MUTE, CLK, MCR pin
PWM input frequency	Fpwm	—	20	40 *Note 1	kHz	IUT, IUB, IVT, IVB, IWT, IWB pin
WDT clock input frequency	Fwdt	200	—	5 k	Hz	CLK pin

Note: *1 This value guarantees circuit operation only; the junction temperature is not considered.

Power Dissipation Derating Curve



- Simulated values
- Mounted on a Renesas standard circuit board (4 layers)

Notes: *1 This data is obtained under recommended conditions and is not intended to guarantee the absolute maximum rating.
*2 Actual power dissipation derating rate should be evaluated with this device mounted on the circuit board of the actual application.

Electrical Characteristics

(Ta = –40 to 125°C, VBAT = VBAT2 = 7.0 to 36 V, VGB = 5.9 to 6.5 V, REGC = VCC = 4.85 to 5.15 V, unless otherwise specified)

Power Supply (VBAT, VBAT2, VGB, SDC, REGC, VCC, VGT, CP1, CP2, IREF)

- DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Battery power supply current	I_{VBAT}	—	—	3	mA	VBAT, VBAT2 pin, IUT, IUB, IVT, IVB, IWT, IWB: High, MUTE: Low
Step down converter power supply current	I_{VGB}	—	—	3	mA	VGB pin, IUT, IUB, IVT, IVB, IWT, IWB: High, MUTE: Low
VCC power supply current	I_{VCC}	—	—	5	mA	VCC pin, IUT, IUB, IVT, IVB, IWT, IWB: High, MUTE: Low, IREF: High
DGND current	I_{DGND}	–10	—	—	μA	DGND pin, IUT, IUB, IVT, IVB, IWT, IWB: High, MUTE: Low, IREF: High
Step down converter threshold voltage	Vth_{VGB}	5.9	6.2	6.5	V	VGB pin, VBAT = 12 V
Step down converter output On resistance	R_{VGB}	0.92	2.3	6.0	Ω	SDC pin, VGB < 5.9 V, VBAT = 12 V, IL = –0.1 A
Step down converter output leakage current	IL_{VGB}	–10	—	0	μA	SDC pin, VGB > 6.5 V, VBAT = 12 V, SDC = 0 V
Step down converter over-current detection current	$Ilim_{VGB}$	–1.4	–1.0	–0.6	A	SDC pin, See figure 3
High side gate driver output voltage	VGT	VBAT2 +5.0	VBAT2 +5.5	VBAT2 +6.2	V	VGT pin, VGB = 6.2 V, f_{CP1} = 135 kHz, Cp = 0.1 μF, Cgb = 1.0 μF, Io = 3 mA
5 V regulator output voltage	$Vo_{(REGC)}$	4.85	5.0	5.15	V	VGB = 6.2 V, Io(external load) = 0 mA, CL = 33 μF
5 V regulator output current	$Io_{(REG)}$	–70	—	—	mA	VGB = 6.2 V
5 V regulator input voltage stability	REG_{IN}	—	5.0	30	mV	VGB = 5.9~6.5 V, Io(external load) = 0 mA
5 V regulator load current stability	REG_{OUT}	—	5.0	30	mV	Io(external load) = 0~70 mA, VGB = 6.2 V
IREF output voltage	$Vo_{(IREF)}$	1.16	1.25	1.34	V	
TSD temperature	TSDon	170	200	230	°C	Not subjected to production test, but guaranteed through designing.
TSD hysteresis temperature	TSDhys	30	40	50	°C	

- AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Step down converter OFF time at over-current detection	T_{SDC}	10	25	50	μs	SDC pin, See figure 3
Step down converter driving frequency	f_{SDC}	205	265	325	kHz	SDC pin, Rref = 47 kΩ
Charge pump driving frequency	f_{CP1}	105	135	165	kHz	CP1 pin, Rref = 47 kΩ
High side gate drive pre-charge time	T_{GT}	—	5.0	30	ms	VGT pin, f_{CP1} = 135 kHz, Cp = 0.1 μF, Cgt = 1.0 μF, See figure 5

Note: Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Electrical Characteristics (cont.)

(Ta = –40 to 125°C, VBAT = VBAT2 = 7.0 to 36 V, VGB = 5.9 to 6.5 V, REGC = VCC = 4.85 to 5.15 V, unless otherwise specified)

Watchdog Timer (CLK, RST, REGC)

- DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
WDT start voltage	Von	—	0.7× REGC	0.74× REGC	V	WDT start operation when REGC ≥ Von
REGC low voltage detection reset voltage	Vprl	0.87× REGC	0.90× REGC	0.93× REGC	V	REGC pin: High→Low
REGC low voltage detection hysteresis voltage	Vprh	60	100	140	mV	REGC pin: Low→High
CLK high level input voltage	$V_{IH(CLK)}$	0.7× VCC	—	VCC	V	CLK pin
CLK low level input voltage	$V_{IL(CLK)}$	0	—	0.3× VCC	V	CLK pin
CLK high level input current	$I_{IH(CLK)}$	20	50	250	μA	CLK = 5 V, Pull-Down = 100 kΩ
CLK low level input current	$I_{IL(CLK)}$	–10	—	0	μA	CLK = 0 V
RST high level output voltage	$V_{OH(RST)}$	0.8× VCC	—	VCC	V	RST pin, Io = –2 mA
RST low level output voltage	$V_{OL(RST)}$	0	—	0.2× VCC	V	RST pin, Io = +2 mA

- AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
REGC minimum low voltage detection time	Tprw	8	—	16	cycle	RST pin *Note 2
Power on reset time	Tpr	—	1.25×10^4	—	cycle	RST pin *Note 2
WDT reset time	Twd	—	2.5×10^3	—	cycle	RST pin *Note 2
WDT reset pulse width	Twr	—	16	—	cycle	RST pin *Note 2

Note: Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Notes: *1 See figure 7 for the electrical characteristics in this page.
*2 Is defined by the number of cycles of WDT driving frequency (265 kHz typ.: = f_{SDC}).

Electrical Characteristics (cont.)

(Ta = –40 to 125°C, VBAT = VBAT2 = 7.0 to 36 V, VGB = 5.9 to 6.5 V, REGC = VCC = 4.85 to 5.15 V, unless otherwise specified)

Over-Current Detection of Motor (MCS, SGND, MCD, MCR)

- DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Over-current detection threshold voltage	Vth_{MCS}	1.0	1.1	1.2	V	MCS pin
Over-current detection threshold hysteresis voltage	$Vhys_{MCS}$	—	40	—	mV	MCS pin, Not subjected to production test, but guaranteed through designing.
MCS input bias current	Iin_{MCS}	–1.0	—	—	µA	MCS pin, VMCS = 0 V
MCS common mode input voltage range	$V_{(MCS)}$	0	—	VCC –2.0	V	MCS pin
MCR high level input voltage	$V_{IH(MCR)}$	0.8× VCC	—	VCC	V	MCR pin
MCR low level input voltage	$V_{IL(MCR)}$	0	—	0.4× VCC	V	MCR pin
MCR high level input current	$I_{IH(MCR)}$	20	50	250	µA	MCR = 5 V, Pull-Down = 100 kΩ
MCR low level input current	$I_{IL(MCR)}$	–10	—	0	µA	MCR = 0 V
MCD high level output voltage	$V_{OH(MCD)}$	0.8× VCC	—	VCC	V	MCD pin, Io = –2 mA
MCD low level output voltage	$V_{OL(MCD)}$	0	—	0.2× VCC	V	MCD pin, Io = +2 mA

- AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Over-current detection filtering time	t_{FLT}	0	—	3.0	µs	MCS, MCD pin, I*T, I*B: Low, MUTE: High, MCR: Low, See figure 9
Over-current detection latch clear pulse width	t_{MCR}	1	—	—	µs	MCR, MCD pin, I*T, I*B: Low, MUTE: High, MCS < (Vth_{MCS} – $Vhys_{MCS}$), See figure 9
Over-current detection latch clear delay time	t_{DLY}	—	—	1	µs	MCR, MCD pin, I*T, I*B: Low, MUTE: High, MCS < (Vth_{MCS} – $Vhys_{MCS}$), See figure 9

Note: Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Electrical Characteristics (cont.)

(Ta = –40 to 125°C, VBAT = VBAT2 = 7.0 to 36 V, VGB = 5.9 to 6.5 V, REGC = VCC = 4.85 to 5.15 V, unless otherwise specified)

Gate Drive (I*T, I*B, MUTE, *T, *, *B, *G)

- DC characteristics

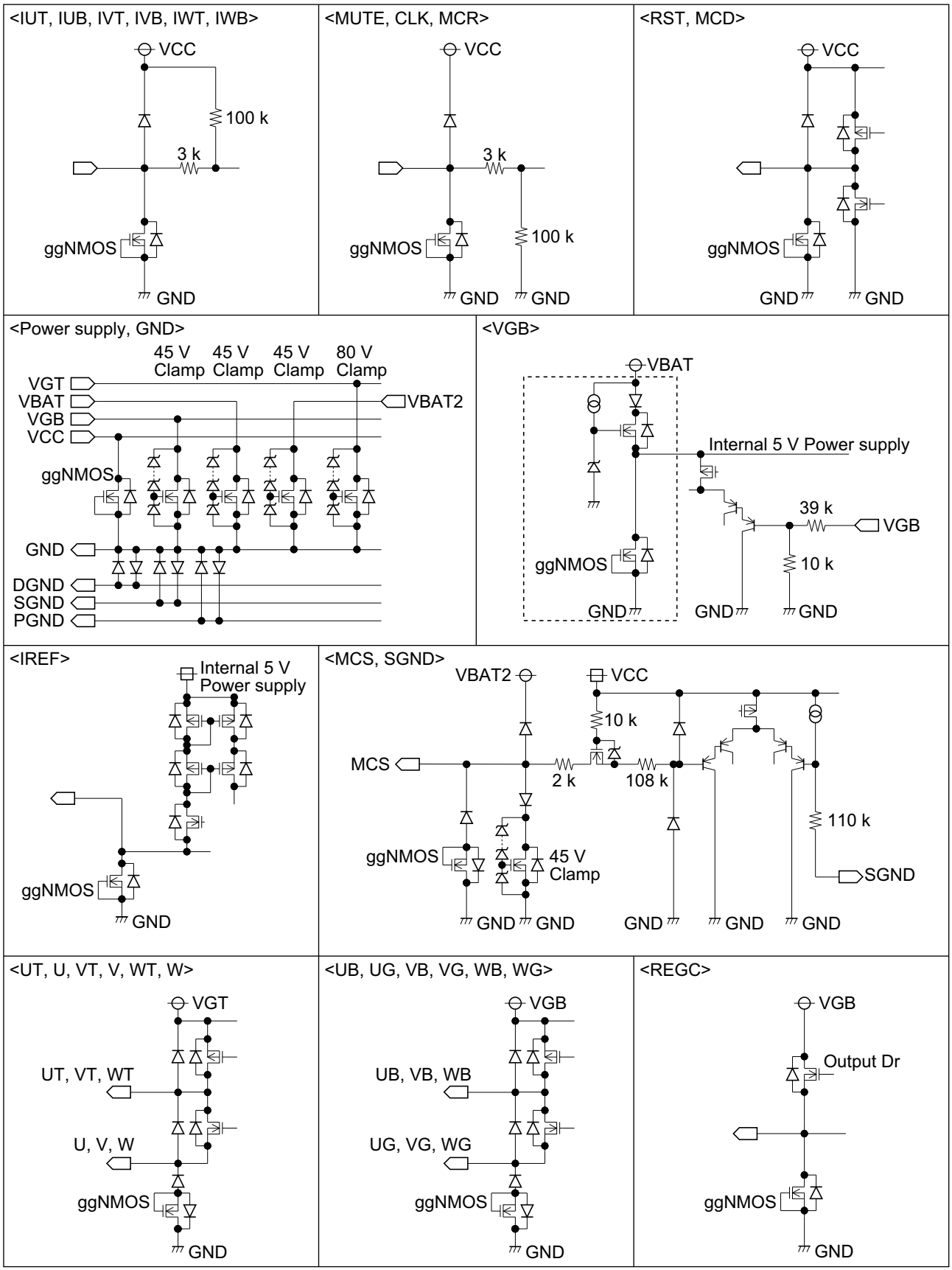
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate drive input pin high level input voltage	V_{IH}	0.6× VCC	—	VCC	V	IUT, IUB, IVT, IVB, IWT, IWB pin
Gate drive input pin low level input voltage	V_{IL}	0	—	0.2× VCC	V	IUT, IUB, IVT, IVB, IWT, IWB pin
Gate drive input pin high level input current	I_{IH}	0	—	10	µA	IUT, IUB, IVT, IVB, IWT, IWB = 5 V
Gate drive input pin low level input current	I_{IL}	–250	–50	–20	µA	IUT, IUB, IVT, IVB, IWT, IWB = 0 V, Pull-Up = 100 kΩ
MUTE high level input voltage	$V_{IH(MUTE)}$	0.8× VCC	—	VCC	V	MUTE pin
MUTE low level input voltage	$V_{IL(MUTE)}$	0	—	0.4× VCC	V	MUTE pin
MUTE high level input current	$I_{IH(MUTE)}$	20	50	250	µA	MUTE = 5 V, Pull-Down = 100 kΩ
MUTE low level input current	$I_{IL(MUTE)}$	–10	—	0	µA	MUTE = 0 V
Output pin output current	$Io_{(MTR)}$	–180	–90	–40	µA	U, V, W pin, I*T = I*B = VCC (*T = *B = "L" output), U, V, W = 0, VGT = VBAT2 + 5.5 V
High side gate drive high level output voltage	Vtoh	0.4	1.0	2.5	V	Vtoh = VGT-UT, VGT-VT, VGT-WT VBAT2 = 12 V, VGB = 6.2 V, VGT-VBAT2 = 5.5 V, IUT = IVT = IWT = 0 V, Iload = –20 mA
High side gate drive low level output voltage	Vtol	0.4	1.0	2.5	V	Vtol = UT-U, VT-V, WT-W, VBAT2 = 12 V, VGB = 6.2 V, VGT-VBAT2 = 5.5 V, IUT = IVT = IWT = 5V, Iload = 40 mA
Low side gate drive high level output voltage	Vboh	0.56	1.4	3.5	V	Vboh = VGB-UB, VGB-VB, VGB-WB VBAT2 = 12 V, VGB = 6.2 V, VGT-VBAT2 = 5.5 V, IUB = IVB = IWB = 0 V, Iload = –20 mA
Low side gate drive low level output voltage	Vbol	0.4	1.0	2.5	V	Vbol = UB-UG, VB-VG, WB-WG VBAT2 = 12 V, VGB = 6.2 V, VGT-VBAT2 = 5.5 V, IUB = IVB = IWB = 5 V, Iload = 40 mA

- AC characteristics

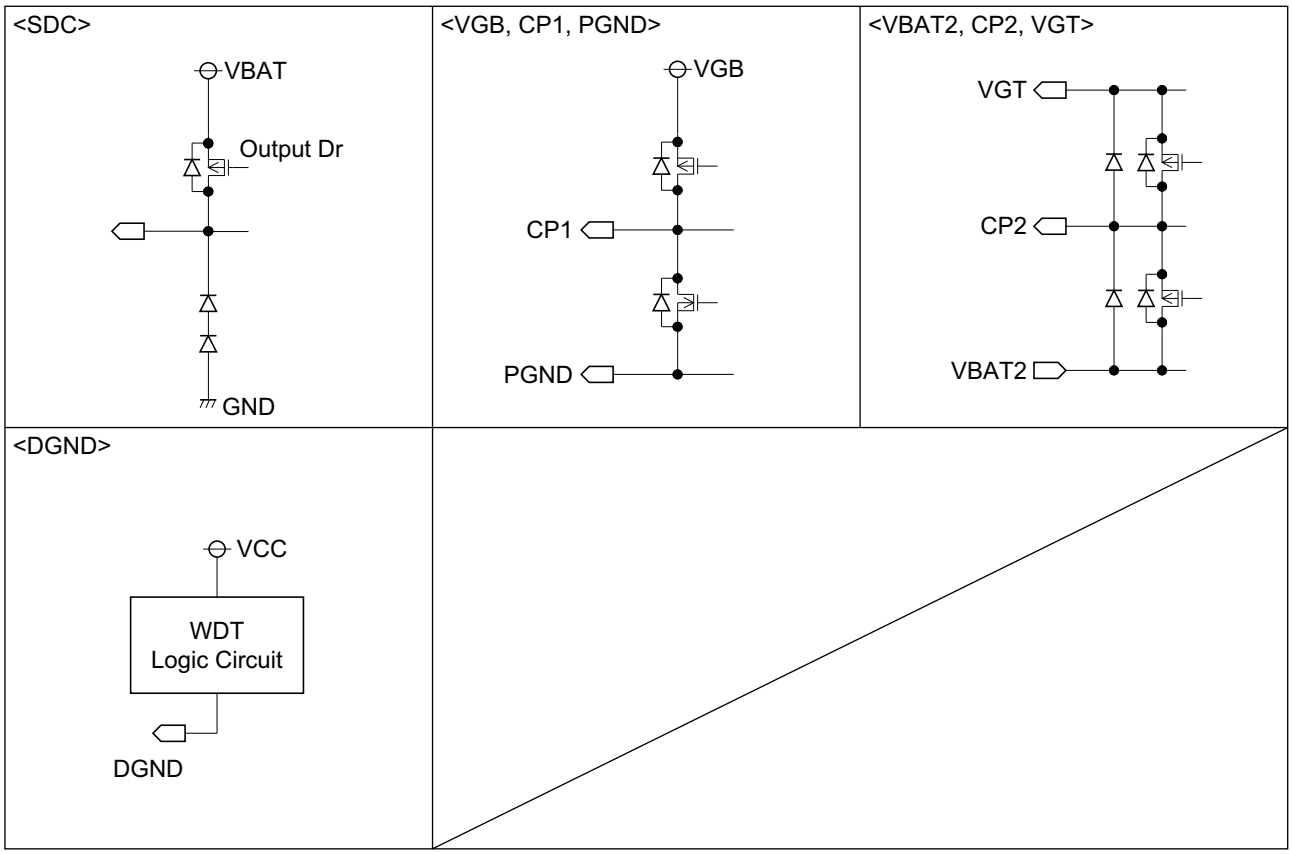
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Turn-on delay time	Ton	100	200	400	ns	IUT, IUB, IVT, IVB, IWT, IWB, MUTE pin, See figure 10
Turn-off delay time	Toff	100	200	400	ns	IUT, IUB, IVT, IVB, IWT, IWB, MUTE pin, See figure 10
High side gate drive rise time	Ttr	500	1000	2000	ns	IUT, IVT, IWT, MUTE pin, CL = 3000 pF, RL = 100 Ω, See figure 10
High side gate drive fall time	Ttf	450	900	1800	ns	
Low side gate drive rise time	Tbr	500	1000	2000	ns	IUB, IVB, IWB, MUTE pin, CL = 3000 pF, RL = 100 Ω, See figure 10
Low side gate drive fall time	Tbf	450	900	1800	ns	

Note: Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Equivalent Circuits of Input/Output Circuits



Equivalent Circuits of Input/Output Circuits (cont.)



Function Description

Step Down Converter

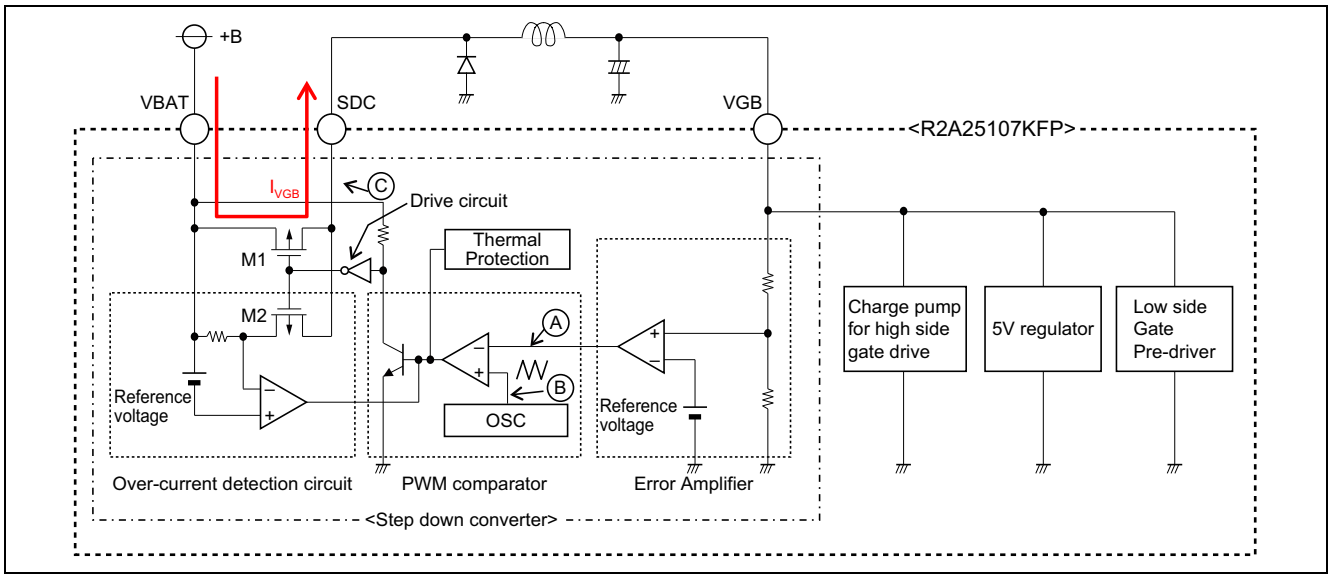


Figure 1 Block Diagram of Step Down Converter Circuit

This IC contains a step down converter circuit to generate a typical 6.2-V voltage from VBAT voltage for efficiently powering the charge pump circuit for high-side gate drive and the 5 V series regulator. The resulting 6.2-V output of the step down converter is also used for powering the low-side gate drive.

The block diagram of the step down converter circuit is shown in figure 1. This circuit contains an error amplifier, PWM comparator, drive circuit, over-current detection circuit and thermal shutdown (TSD) circuit. As shown in figure 2, this circuit controls the VGB voltage based on Vth_{VGB} of 6.2 V typical through the PWM operation.

The over-current detection circuit monitors the current flowing the drive transistor M1 (I_{VGB}). If over load is generated at power up or in the load circuits (gate drive circuit and 5 V regulator) and then I_{VGB} exceeds the over -current detection current, $Ilim_{VGB}$ (–1.0 A), the drive transistor M1 is placed to off for typical 25 µs of T_{SDC} (Step down converter off time at over-current detection). In addition, if the chip junction temperature is increased to the TSD temperature (TSDon: 200°C typ.) through intermittent operation of the over-current detection circuit, drive transistor M1 is placed to off until the TSD circuit starts to be operated and the chip temperature is decreased by TSD hysteresis temperature (TSDhys: 40°C typ.). These operations prevent the IC from being thermally destructed.

Table 1 and figure 3 show the operation of over-current detection circuit and thermal shutdown circuit.

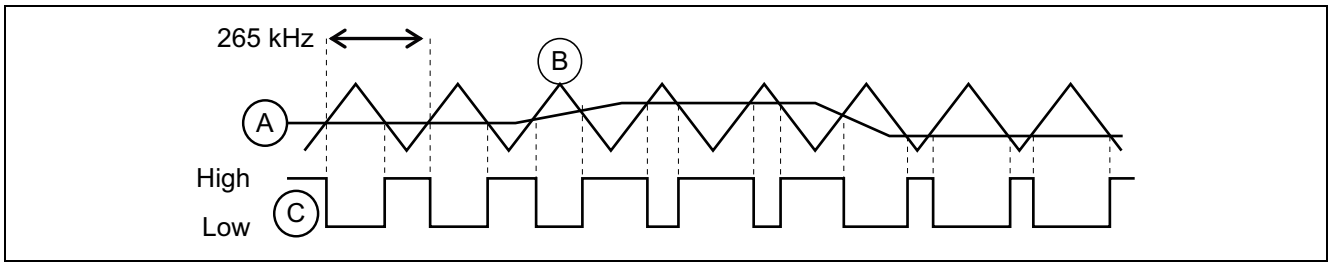


Figure 2 Step Down Converter PWM Timing Chart

Table 1 Operations under Protection

Over-Current Protection	Thermal Shutdown	Step Down Converter Output: M1
OFF	OFF	ON (Driven by PWM)
ON (detected)	OFF	OFF (Stopped by PWM)
OFF	ON (detected)	OFF (Stopped by PWM)
ON (detected)	ON (detected)	OFF (Stopped by PWM)

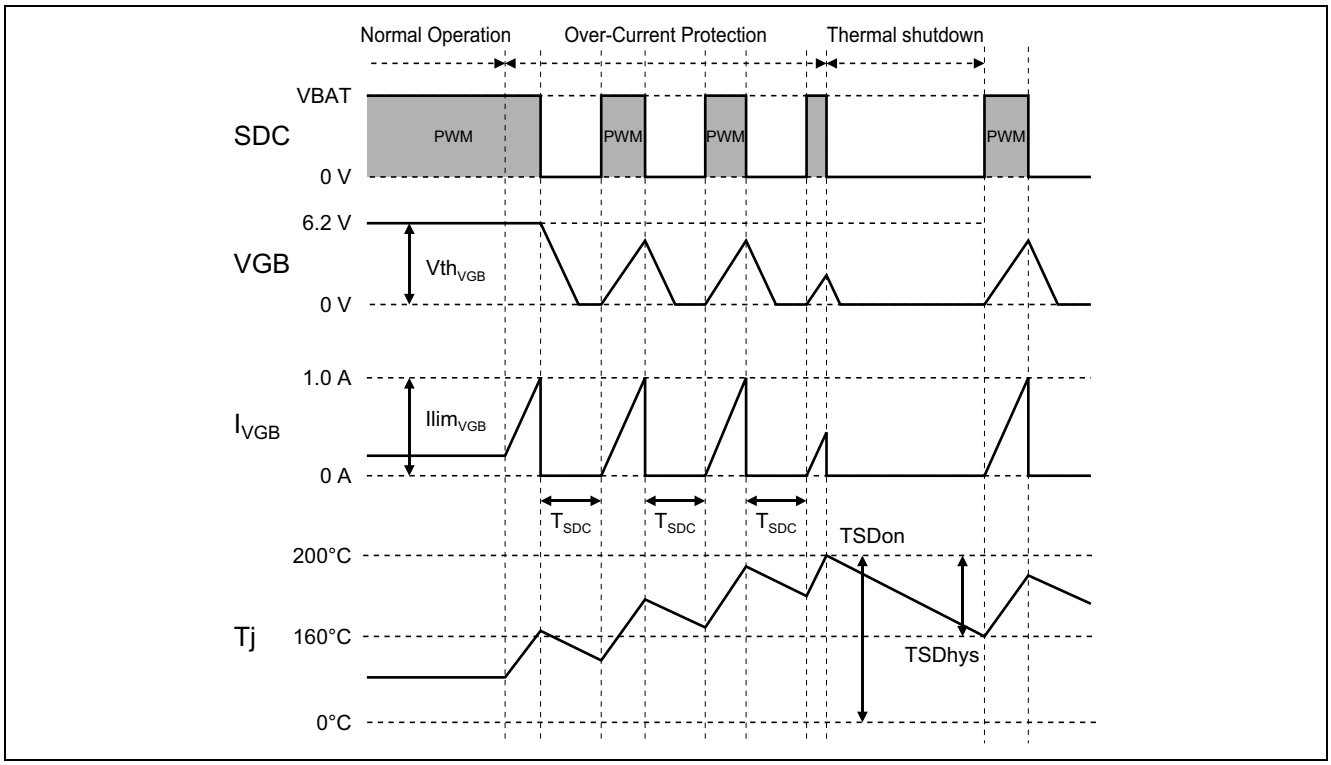


Figure 3 Step Down Converter Operation under Protection

Charge Pump

This IC contains a charge pump circuit (upper side gate drive voltage: VGT = VBAT2 + 5.5 V typ.) to drive the gate of the high-side external power MOSFET. This circuit is also configured to add the low-side gate drive voltage (step down converter output: VGB) to the VBAT2 power supply voltage.

Figure 4 shows the charge pump circuit configuration. Figure 5 shows timing chart for pre-charge.

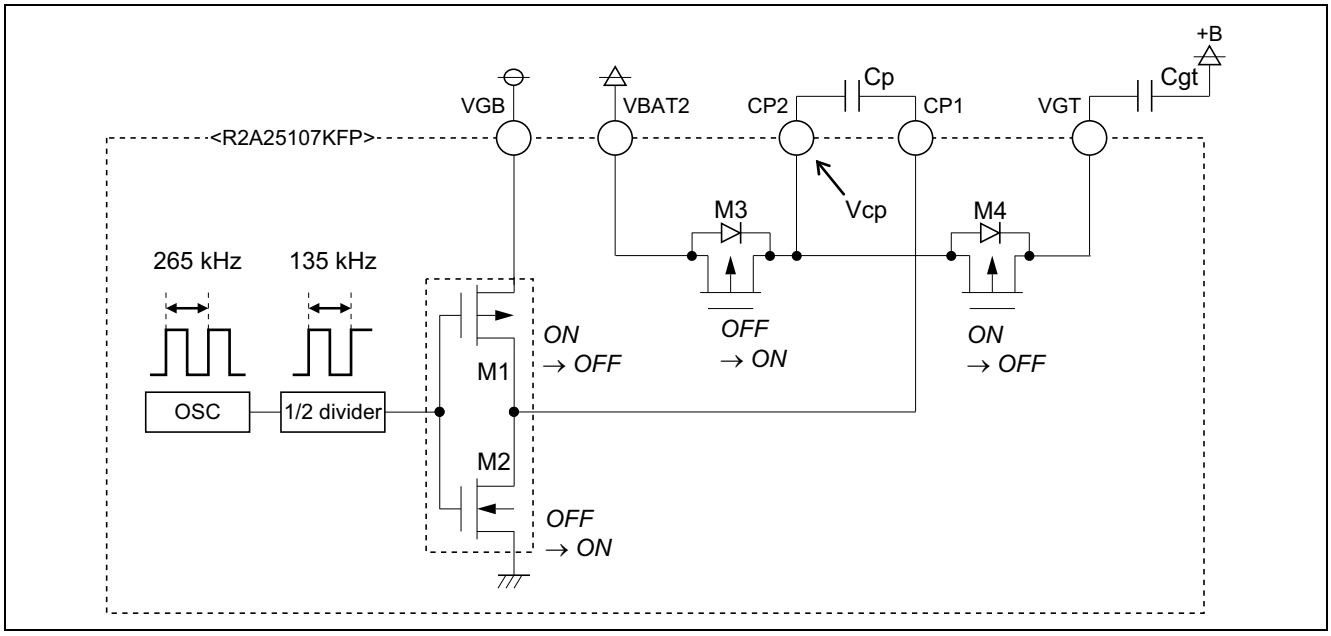


Figure 4 Charge Pump Circuit

(1) When M1 and M4 = OFF and M2 and M3 = ON

External capacitor, Cp is charged.

$$Vcp = \underline{VBAT2 - Vds3} \quad (Vds3; \text{Drain to Source voltage of M3})$$

(2) When M1 and M4 = ON and M2 and M3= OFF

The electric charge on external capacitance, Cp is moved to external capacitance, Cgt and the resulting VGT voltage is:

$$Vcp = (VBAT2 - Vds3) + VGB = VBAT2 + VGB - Vds3$$

Thus

$$VGT = Vcp - Vds4 = (VBAT2 + VGB - Vds3) - Vds4 \quad (Vds4; \text{Drain to Source voltage of M4})$$
$$= \underline{VBAT2 + VGB - 2 \times Vds} \quad (Vds = Vds3 \approx Vds4)$$

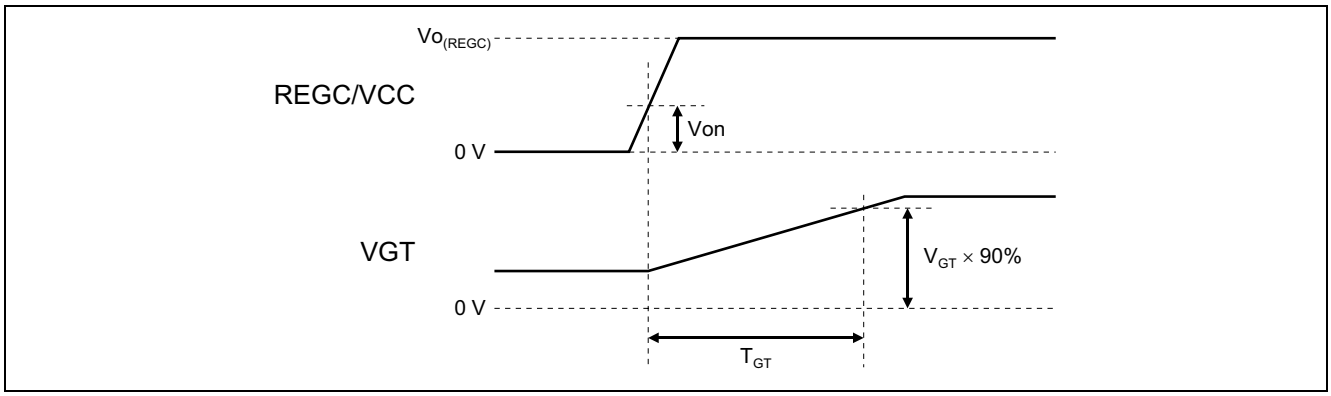


Figure 5 Pre-charge Operation Timing of Charge Pump

5 V Regulator

This IC contains the 5 V series regulator with internal Nch MOS driver for MCU power supply circuit. Figure 6 shows the 5 V regulator circuit.

The over-current detection circuit of the step down converter is activated if an over-current is caused due to the short circuit of REGC output. If the over-current condition is continued, this regulator circuit is protected by the thermal shutdown circuit in the same way as the step down converter. If the junction temperature of the chip exceeds the TSD temperature (TSDon) of 200°C typical, the TSD circuit starts to be operated to place the drive transistor M1 to off until the chip temperature is decreased by the TSD hysteresis temperature (TSDhys) of 40°C typical. This operation protects the chip from thermal destruction. Table 2 shows the operation of over-current detection circuit and thermal shutdown circuit.

This IC also contains watchdog timer (WDT), and returns the reset signal (RST) to the MCU when the low voltage of REGC is detected. Figure 7 shows the timing chart of the watchdog timer.

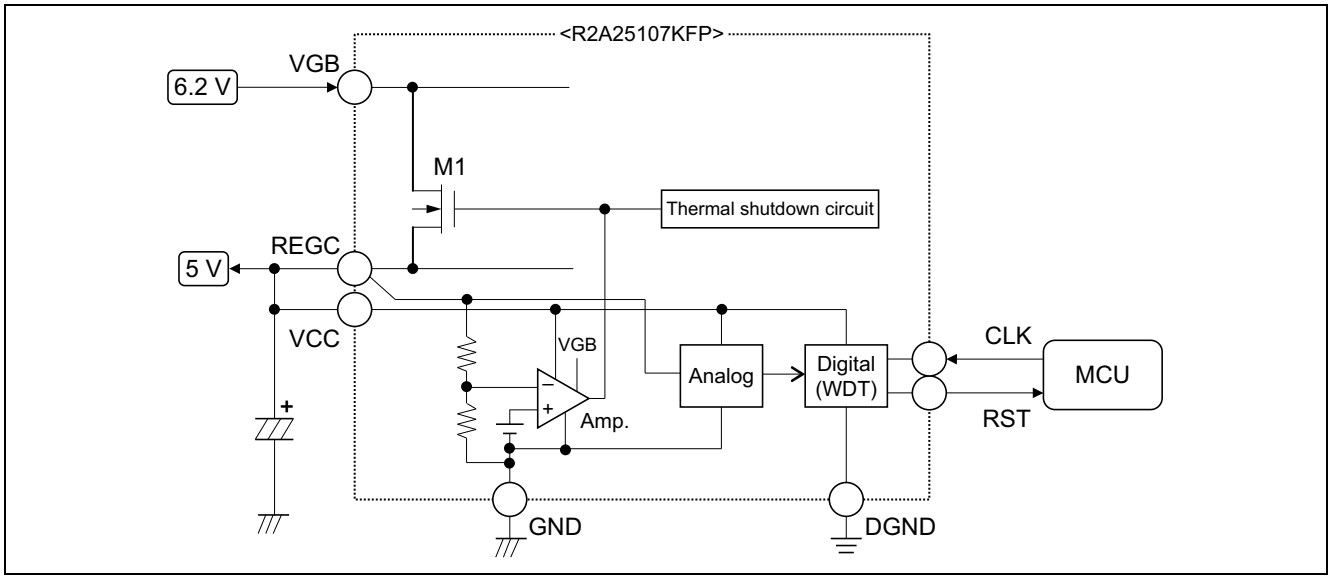


Figure 6 5 V Regulator Circuit

Table 2 Operations under Protection

Over-Current Protection	Thermal Shutdown	5 V Regulator Output	Step Down Converter Output
OFF	OFF	ON	ON (Driven by PWM)
ON (detected)	OFF	ON	OFF (Stopped by PWM)
OFF	ON (detected)	OFF	OFF (Stopped by PWM)
ON (detected)	ON (detected)	OFF	OFF (Stopped by PWM)

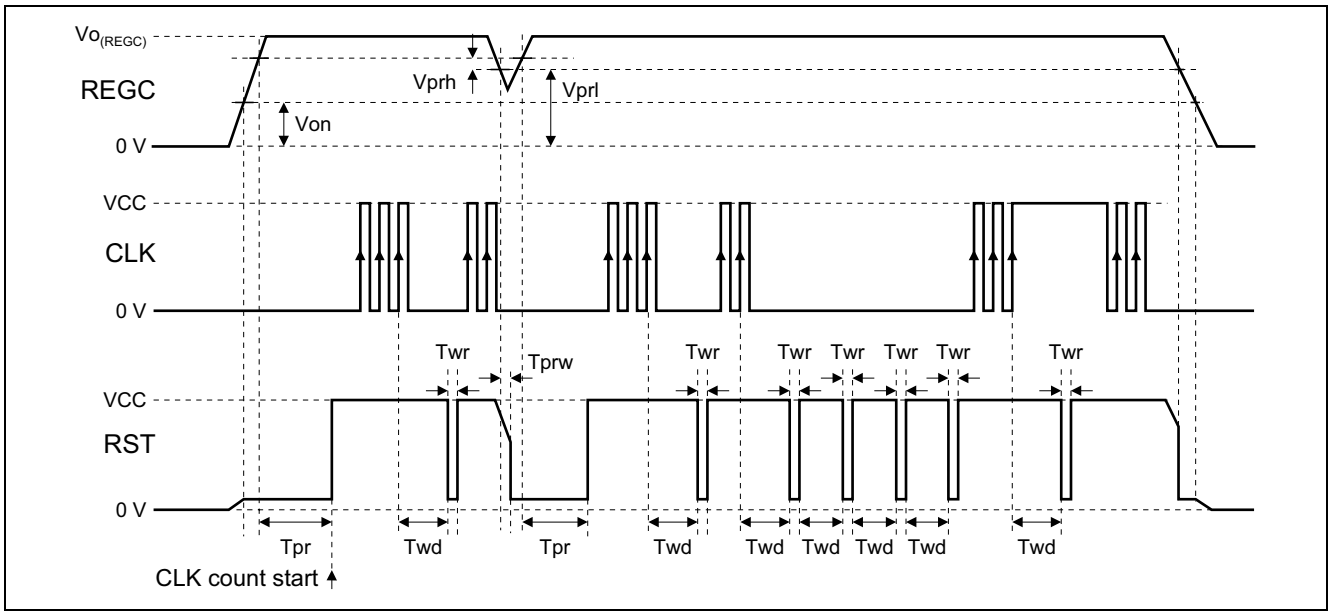


Figure 7 Timing Chart of Watchdog Timer

Motor Over-Current Detection Circuit

This IC contains a motor over-current detection circuit. Figure 8 shows the block diagram of this circuit and figure 9 shows the timing chart when over-current is detected.

This circuit monitors the MCS pin voltage. If the MCS voltage exceeds the over-current detection threshold voltage (Vth_{MCS}) of 1.1 V typical, motor over-current detection signal (ILIM) is output to the MCU by the time the motor over-current detection filtering time (t_{FLT}) of 3 µs max. has elapsed.

When motor over-current is detected, the over-current detection output remains low until a high level signal pulse (with a pulse width longer than the over-current detection latch clear pulse width, t_{MCR} of 1 µs min.) is applied to the MCR pin.

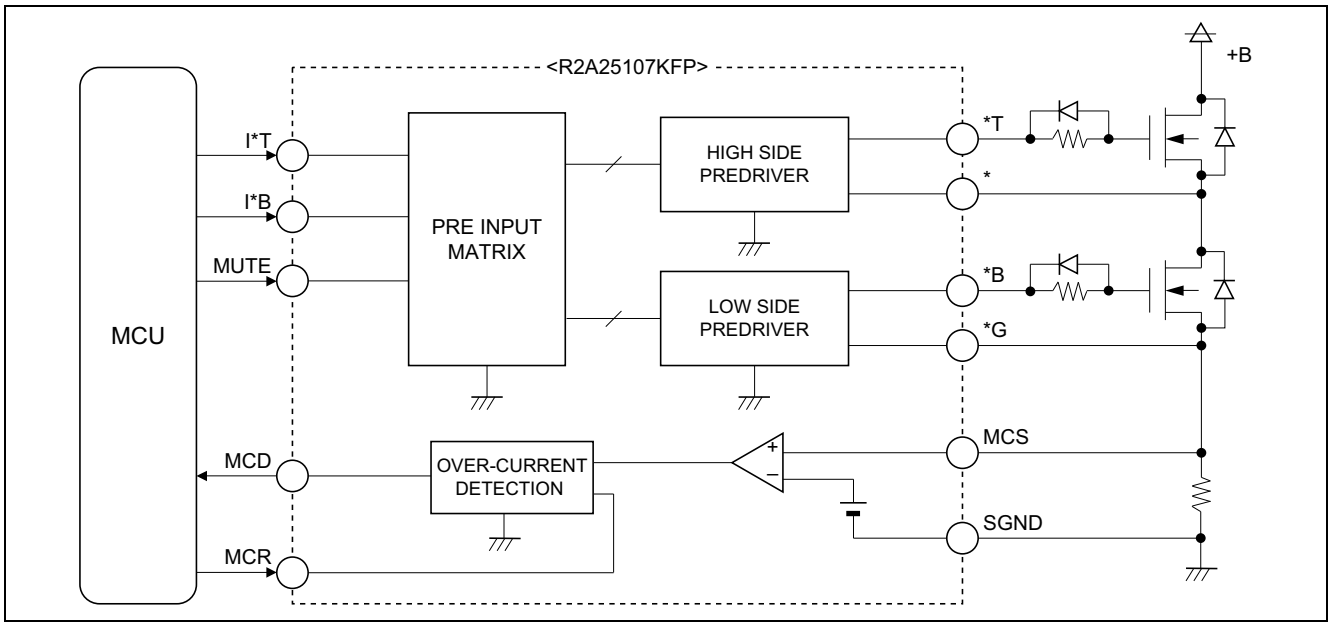


Figure 8 Block Diagram of Motor Over-Current Detection Circuit

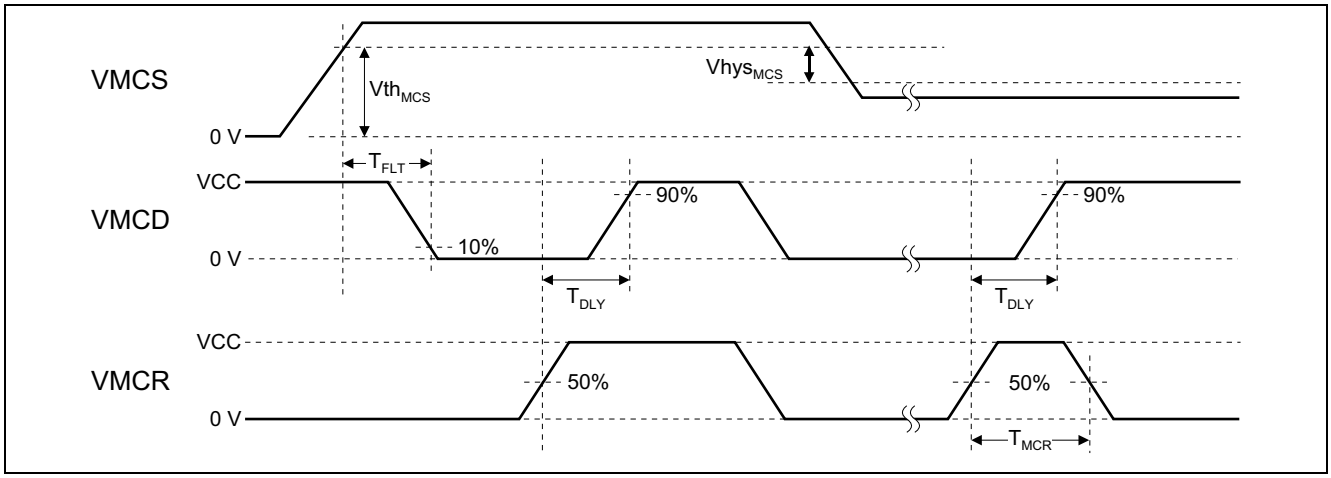
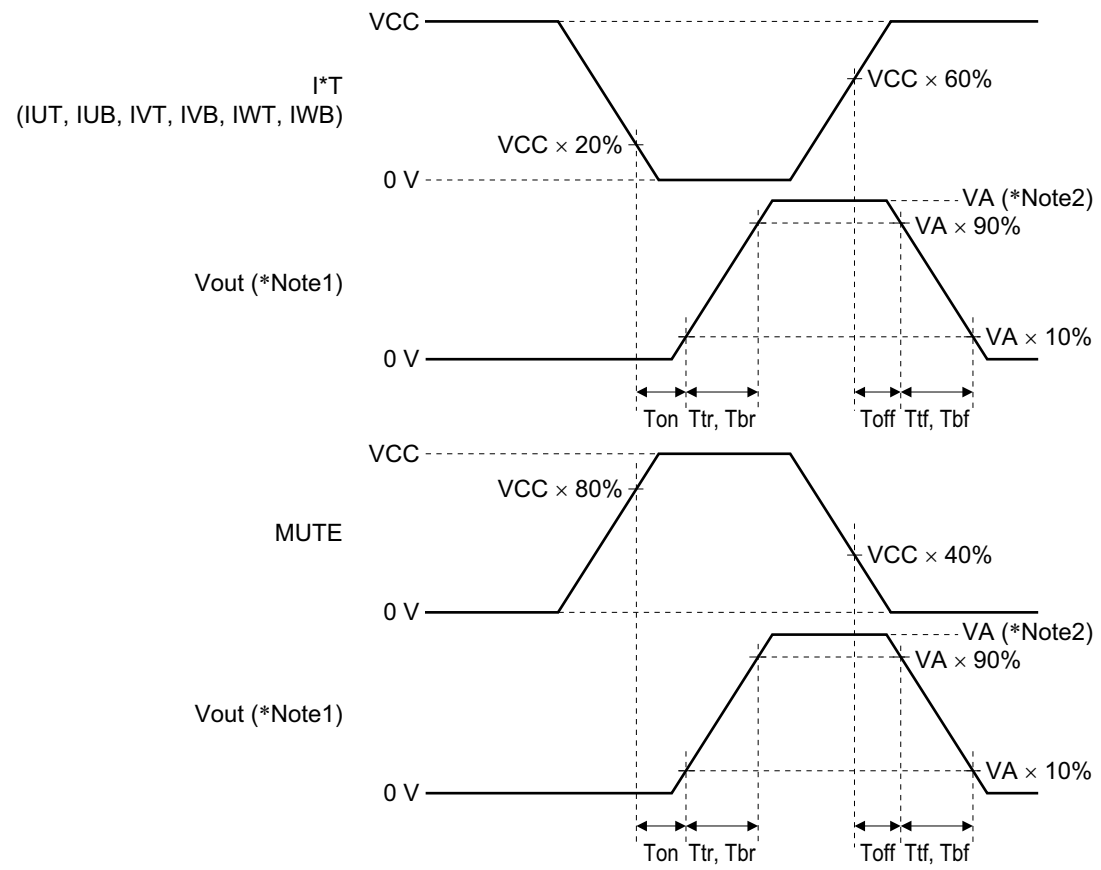


Figure 9 Timing Chart of Motor Over-Current Detection Circuit

Gate Pre-driver

This IC contains three sets of totem pole type output FET gate drive circuits. Figure 10 shows the timing chart and table 3 shows the truth table of the gate pre-driver functions.



Notes: *1 Vout is the gate to source voltage for external power MOSFET
(UT-U, VT-V, WT-W: U = V = W = VBAT2 = 12 V, capacitive load: CL = 3000 pF, gate resistance RL = 100 Ω)
(UB-UG, VB-VG, WB-WG: capacitive load CL = 3000 pF, gate resistance RL = 100 Ω)

*2 VA is the power supply voltage of gate drive output
(UT-U, VT-V, WT-W: 5.5 V (= VGT – VBAT2))
(UB-UG, VB-VG, WB-WG: 6.2 V (= VGB))

Figure 10 Timing Chart of Input/Output Signals of Gate Drive Pins

Table 3 Truth Table of Gate Pre-driver

Input			Output	
I*T	**I*B**	**MUTE**	***T**	***B**
H	H	H	L	L
H	L	H	L	H
L	H	H	H	L
L	L	H	L	L
H/L	H/L	L	L	L

Note: (I*T, I*B, *T, *B) = (IUT, IUB, UT, UB), (IVT, IVB, VT, VB), (IWT, IWB, WT, WB)

Thermal Protection Circuit

This IC contains a thermal shutdown protection circuit to prevent the IC from thermal destruction. Table 4 shows the operating temperatures of this circuit. When this circuit detects an over temperature, the step down converter and 5 V regulator are stopped. When the over temperature is reduced to a TSD hysteresis temperature, operation is resumed. (See figure 3 on page 13.)

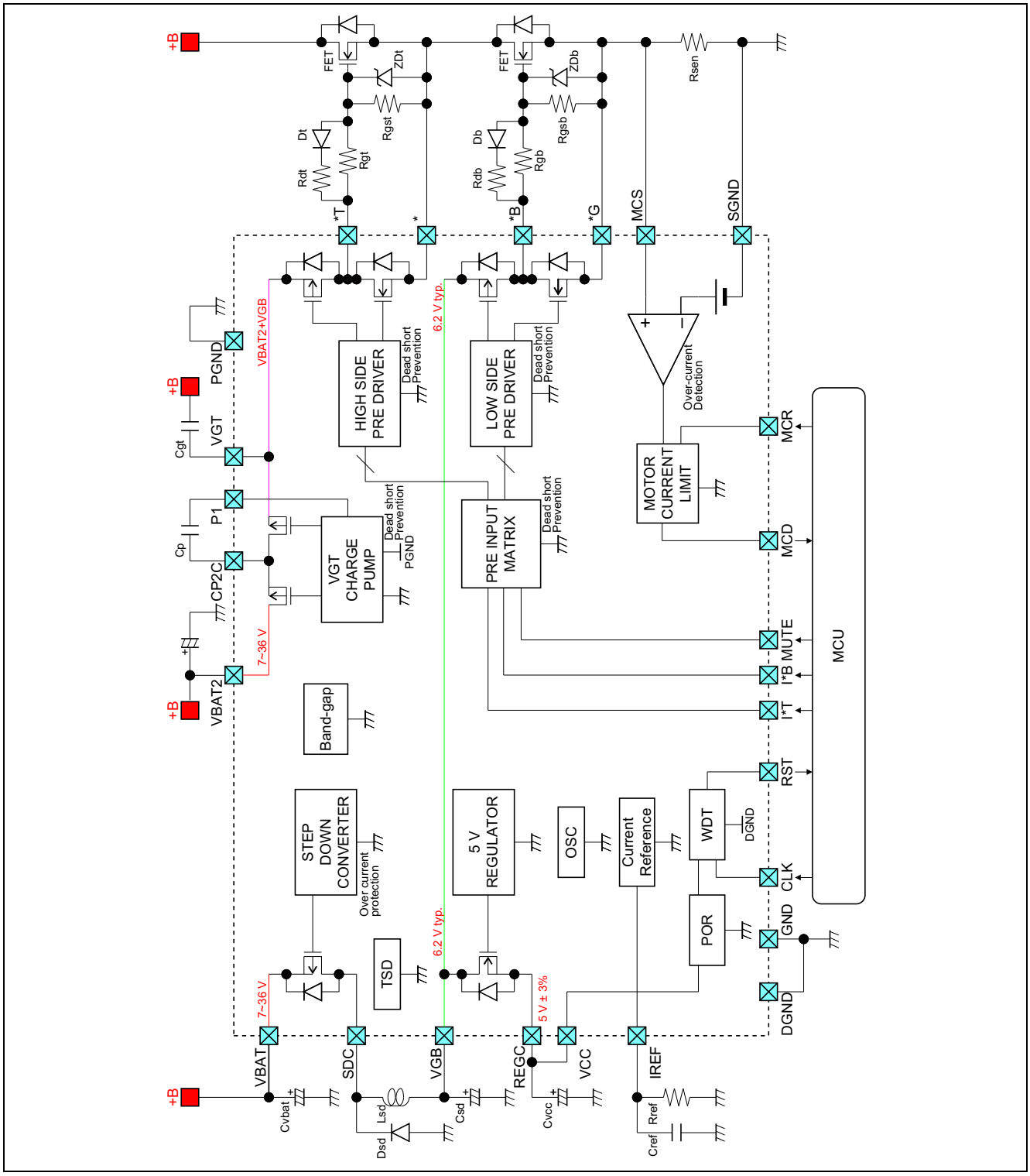
The TSD temperatures are not intended to guarantee device operation at the TSD temperatures. The guaranteed operating temperature of this IC is Tjmax defined in the absolute maximum rating, not the TSD temperatures. The TSD temperatures should be only for protection if the chip temperature rises above the TJmax.

Accordingly, this IC should be operated under Tj ≤ 150°C condition.

Table 4 Operating Temperatures of TSD

Symbol	Item	Value			Unit
		Min.	Typ.	Max.	
TSDon	TSD temperature	170	200	230	°C
TSDhys	TSD hysteresis temperature	30	40	50	°C

Application Example



Recommended Values for External Components

Component Name	Remarks	Symbol	Value			Unit
			Min.	Typ.	Max.	
Cvbat	Bypass Capacitor for VBAT *Note 1	Cvbat	—	10	—	μF
Cvbat2	Bypass Capacitor for VBAT2 *Note 1	Cvbat2	—	10	—	μF
Lsd	Step Down Converter Coil *Note 2	Lsd	—	100	—	μH
Csd	Bypass Capacitor for Step Down Converter *Note 1, 2	Csd	—	47	—	μF
Dsd	Diode for Step Down Converter	VFsd	—	0.6	—	V
Cvcc	Bypass Capacitor for REGC, VCC *Note 1	Cvcc	—	33	47	μF
Rref	External Resistance for Current Reference *Note 2	Rref	—	47	—	kΩ
Cref	Filter Capacitor for Current Reference *Note 2, 3	Cref	—	100	—	pF
Cp	Charge-pump Capacitor *Note 2	Cp	68	100	220	nF
Cgt	Bypass Capacitor for Charge-pump Voltage *Note 1, 2	Cgt	—	1.0	—	μF
FET	Nch Power MOSFET	Ciss	—	3000	5000	pF
Rgt, Rgb	Gate Resistances of FETs Rise time adjustment *Note 2	Rg	100	—	—	Ω
Rdt, Rdb	Reverse Gate Resistances of FETs Fall time adjustment *Note 2	Rd	51	—	—	Ω
Rgst, Rgsb	Gate-Source Resistances of FETs	Rgs	100	—	—	kΩ
Dt, Db	Diode	VFd	—	0.7	—	V
ZDt, ZDb	Zener Diode FET gate protection	Vak	—	16	—	V
Rsen	Resister for Motor Current sensing	Rsen	—	*Note 4	—	mΩ

Notes: *1 Capacitors connected to the power supply pins (Cvbat, Cvbat2, Csd, Cvcc, Cgt) should be mounted as closely as to this IC.

*2 Since these values determine the electrical characteristics of this IC, they should be set with the consideration of the actual application.

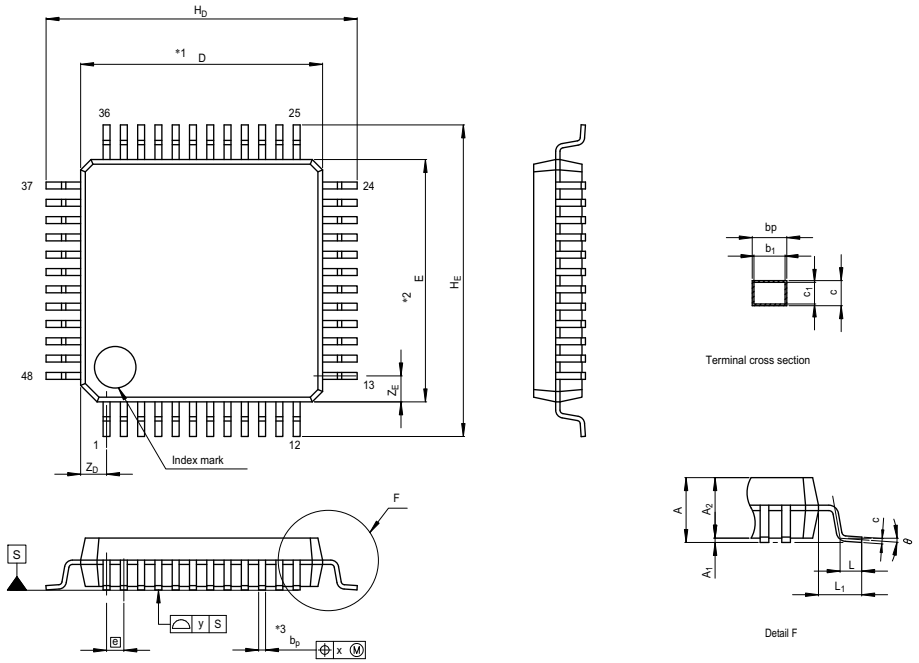
*3 Since this value determines the operation at power up, it should be set with the consideration of the actual application. If the value is changed, contact us separately.

*4 Since this value determines the constant for motor over-current detection, it should be set with the consideration of the limited current of the motor.

*5 For the components with the Min. and Max. values defined in the table above, the values of the components should be determined in the range of the Min. to Max. For the components with the Min. and Max. values not defined, those values should be determined based on the Typ. value, with the consideration of the actual application.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Revision History	R2A25107KFP Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 22, 2012	—	First Edition Issued

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