2.5A LINEAR REGULATOR

FEATURES

- Sink and Source up to 2.5Amp
- Integrated Power MOSFETs
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Built-in Soft-start Function
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in ESOP-8 (Exposed Pad) Packages
- V_{IN} and V_{CNTL} Under Voltage Protection
- RoHS Compliant and 100% Lead (Pb)-Free
- Halogen Free Product

APPLICATION

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses

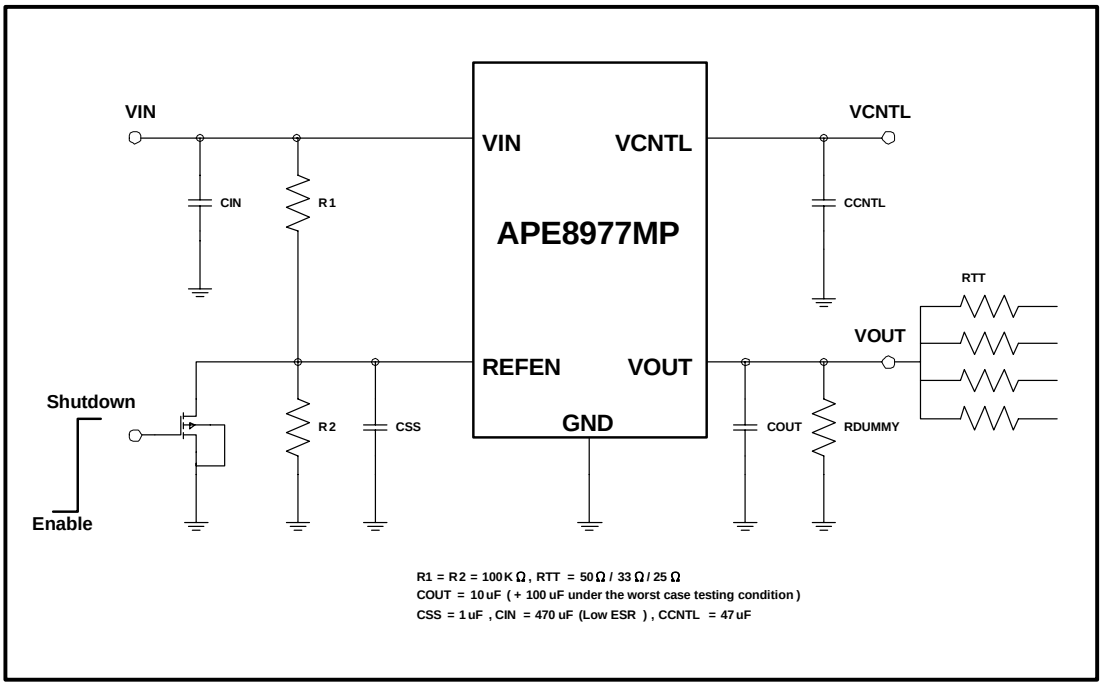
DESCRIPTIOON

The APE8977MP is a simple, cost-effective and high-speed linear regulator. The regulator is capable of actively sinking or sourcing up to 2.5A while regulating an output voltage to within 40mV. The desired output voltage can be programmed by two external voltage divider resistors of the REFEN pin.

The APE8977MP also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection. Built-in soft-start function avoids a mis-operation by inrush current.

The APE8977MP are available in the ESOP-8 (Exposed Pad) surface mount packages.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS(Note1)

Input Voltage (V_{IN})	6V
CNTL Pin Voltage (V_{CNTL})	6V
Power Dissipation (P_D)	Internally Limited
Storage Temperature Range (T_{ST})	-65 to +150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Case (R_{thjc})	28°C/W

Note1 : Exceeding the absolute maximum rating may damage the device.

OPERATING RATING(Note2)

Input Voltage (V_{IN})	2.5V to 1.5V ±3%
CNTL Pin Voltage (V_{CNTL})	5.5V or 3.3V ±5%
Junction Temperature Range (T_J)	-40 to +125°C
Ambient Temperature Range (T_A)	-40 to +85°C

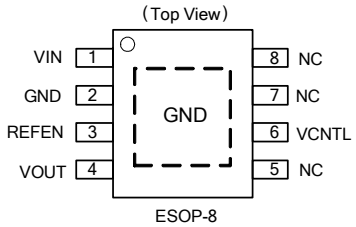
Note2 : The device is not guaranteed to function outside its operating conditions.

ORDERING / PACKAGE INFORMATION

APE8977X

Package Type

MP : ESOP-8



R_{thja} = 75°C/W

ELECTRICAL SPECIFICATIONS

(V_{IN}=1.8V, V_{CNTL}=3.3V, V_{REFEN}=0.9V, C_{OUT}=10uF(Ceramic), T_A =25°C, unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operation Current	I_{CNTL}	I_{OUT} = 0A	-	1	2.5	mA
Standby Current	I_{STBY}	$V_{REFEN=}$ 0V (Shutdown)	-	2	5	uA
VIN Shutdown Current	I_{VIN}	$V_{REFEN=}$ 0V (Shutdown)	-	-	5	uA
UVP Function						
VCNTL UVP Rising Threshold	V_{COP}	V_{CNTL} Rising	2.4	2.55	2.7	V
VCNTL UVP Hysteresis	V_{CHYS}		-	0.35	-	V
VIN UVP Rising Threshold	V_{IOP}	V_{IOP} Rising	0.8	0.95	1.1	V
VIN UVP Hysteresis	V_{IHYS}		-	0.15	-	V
Output (DDR / DDRII / DDRIII)						
Output Offset Voltage(Note3)	ΔV_{Load}	I_{OUT} = 10mA	-20	-	20	mV
		I_{OUT} = -10mA	-20	-	20	
Load Regulation(Note4)	ΔV_{Load}	I_{OUT} = 10mA ~ 2A	-20	-	20	
		I_{OUT} = -10mA ~ -2A	-20	-	20	

ELECTRICAL SPECIFICATIONS

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Protection						
Current Limit	I_{LIM}	V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.0V	2.5	-	-	A
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	-	150	-	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	-	20	-	
ENABLE and Soft-Start						
REFEN Threshold	V_{EN}		0.15	-	0.4	V
Soft-Start Interval	T_{SS}	ΔV_{OUT}=1V	-	0.8	-	ms

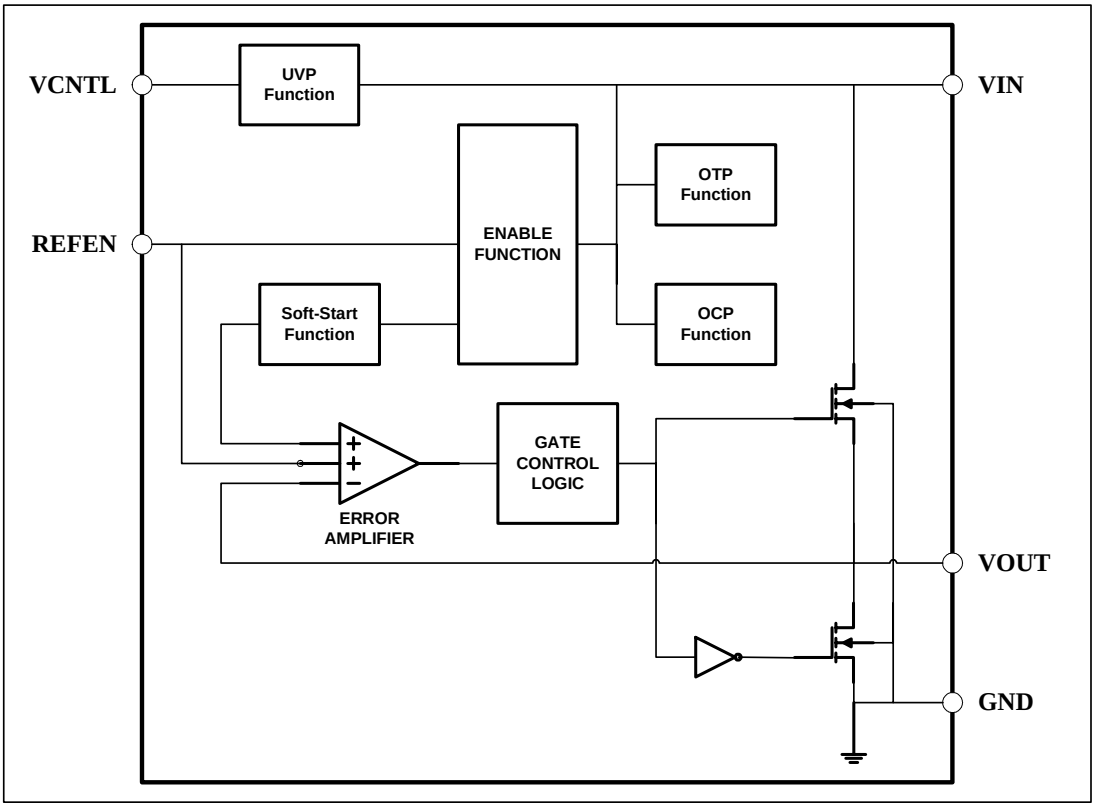
Note3. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Note4. Regulation is measured at constant junction temperature by using a 1ms(on) / 9ms(off) current pulse. Devices are tested for load regulation in the load range from 10mA to 2A for source and -10mA to -2A for sink capability.

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VIN	Power Input Voltage.
GND	Ground Pin
VOUT	Output Voltage
VCNTL	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable

BLOCK DIAGRAM



APPLICATION INFORMATION

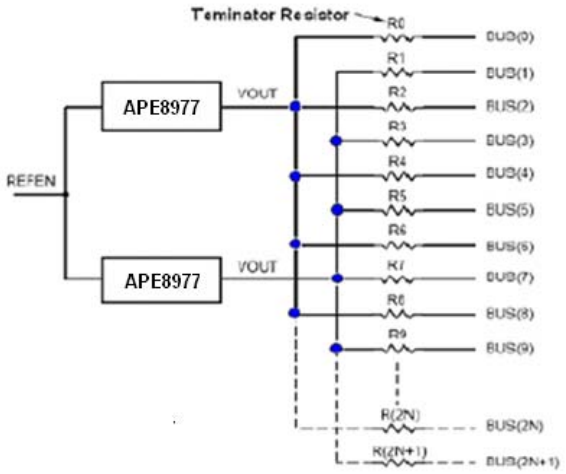
Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the APE8977MP. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between APE8977MP and the preceding powe converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.15V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Consideration

APE8977MP regulators have internal thermal limiting circuitry designed to protect the device during overload conditions.For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{thja}$$

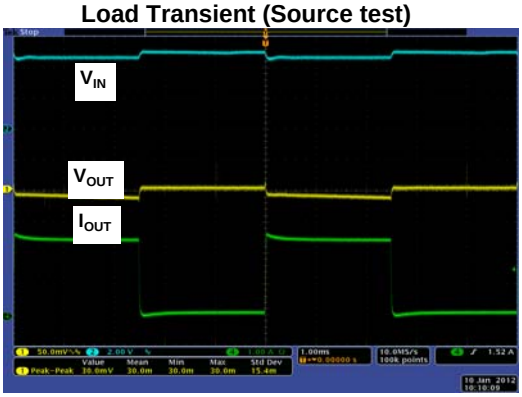
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the R_{thja} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (R_{thja} is layout dependent) for ESOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$$P_{D(MAX)} = (125°C - 25°C) / 75°C/W = 1.33W$$

The thermal resistance R_{thja} of ESOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of ESOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

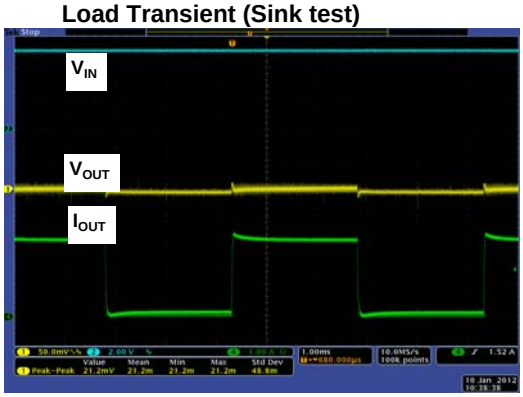
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient (Source test)



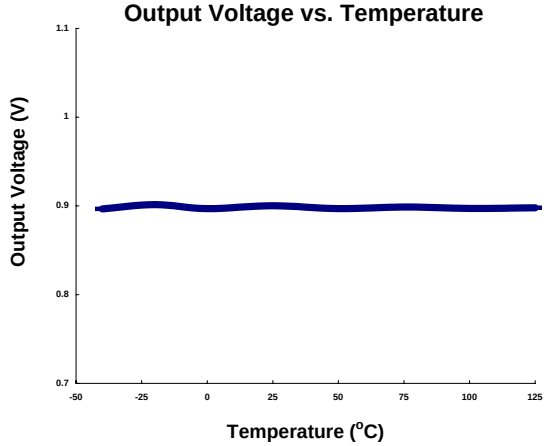
V_{IN} = 5V, V_{CNTL} = 5V
V_{REF} = 2.5V Supplied by a regulator

Load Transient (Sink test)



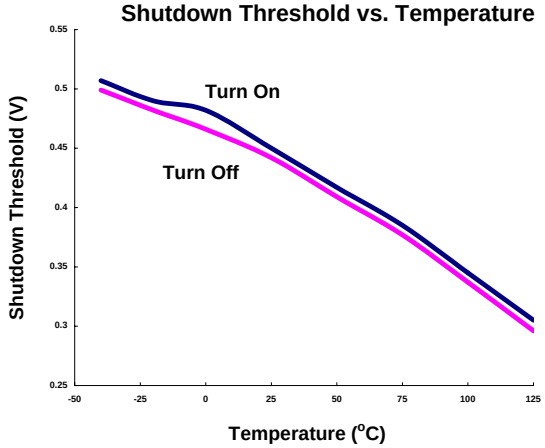
V_{IN} = 5V, V_{CNTL} = 5V
V_{REF} = 2.5V Supplied by a regulator

Output Voltage vs. Temperature



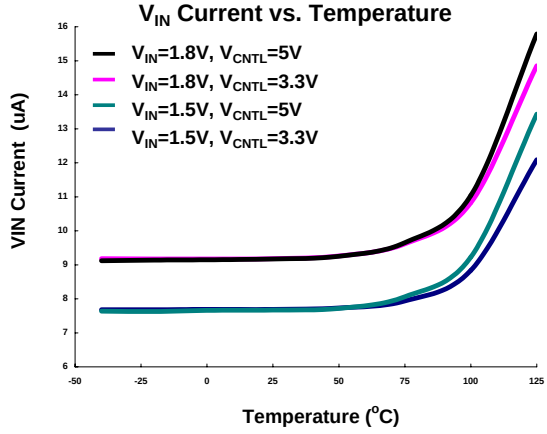
V_{IN} = 1.8V, V_{CNTL} = 3.3V, I_{OUT} = 0A, Source test

Shutdown Threshold vs. Temperature



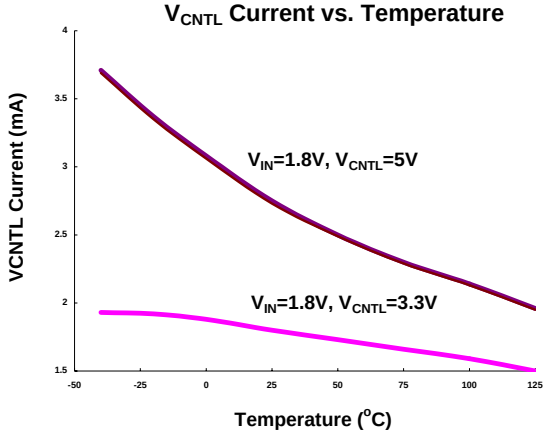
V_{IN} = 1.8V, V_{CNTL} = 3.3V, I_{OUT} = 10mA, Source test

V_{IN} Current vs. Temperature



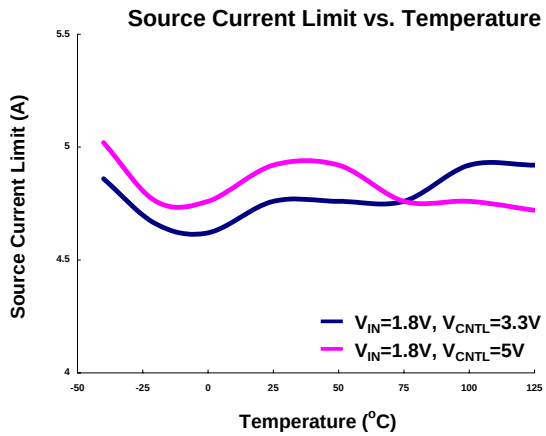
I_{OUT} = 0A, Source test

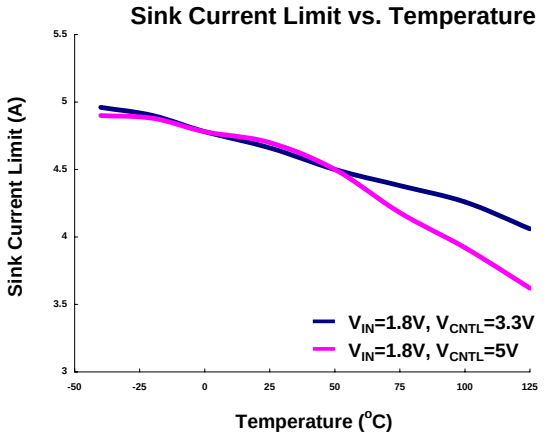
V_{CNTL} Current vs. Temperature

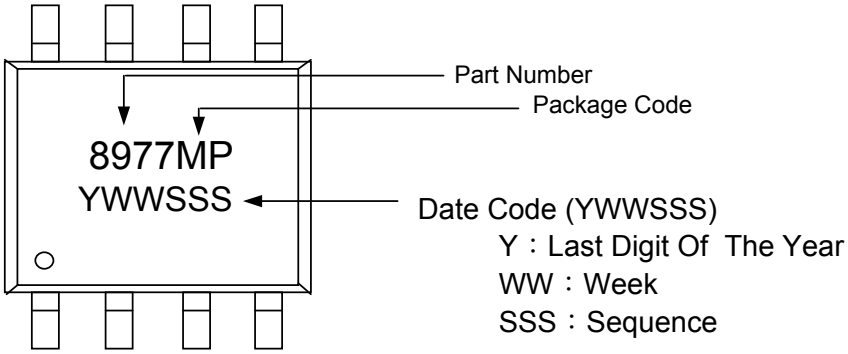


I_{OUT} = 0A, Source test

TYPICAL PERFORMANCE CHARACTERISTICS





MARKING INFORMATION

ESOP-8