TPS61177A WLED Driver for Notebooks With PWM Interface and Mixed Dimming Mode

1 Features

- 2.5-V to 24-V Input Voltage Range
- 39-V Maximum Output Voltage
- Integrated 1.8-A, 40-V MOSFET
- 450-kHz to 1.2-MHz Programmable Switching Frequency
- Adaptive Boost Output to WLED Voltages
- 100-Hz to 25-kHz Wide Input PWM Dimming Frequency Range
- 1% Minimum Dimming Duty Cycle
- Small External Components
- Integrated Loop Compensation
- Six Current Sinks of 30 mA Maximum
- 1% (Typical) Current Matching
- Input PWM Glitch Filter
- PWM Brightness Interface Control
- Three Optional Dimming Methods, including Direct PWM Dimming, Analog Dimming, and Analog and PWM Mixed Dimming
- Built-in WLED Open Protection
- Thermal Shutdown

2 Applications

- Notebook and Tablet LCD Display Backlights
- Patient Monitors
- Medical Displays
- HMI
- Test and Measurement Equipment

3 Description

The TPS61177A device provides a highly integrated white LED (WLED) driver solution for notebook LCD backlight. This device has a built-in high-efficiency boost regulator with integrated 1.8-A, 40-V power MOSFET. The six current sink regulators provide high precision current regulation and matching. In total, the device can support up to 72 WLEDs. In addition, the boost output automatically adjusts its voltage to the WLED forward voltage to optimize efficiency.

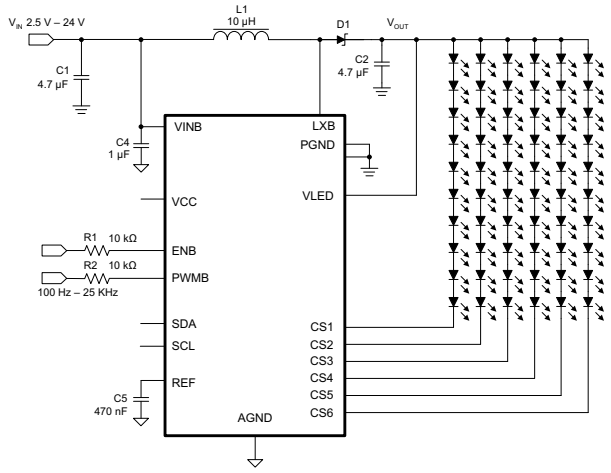
The TPS61177A supports the analog dimming, analog and PWM dimming, and direct PWM dimming method. During analog dimming mode, each CS current linearly varies depending on the duty cycle information on the PWMB pin. During analog and PWM mixed dimming mode, the input PWM duty cycle information is translated to an analog signal to control the WLED current linearly over 25% to 100% brightness area. The device also allows adding PWM dimming when the analog current is down to 25%. Below 25%, the analog signal translates to PWM duty cycle information to control the on or off of WLED current and averages the WLED current down to 1%. The frequency of adding PWM dimming is same to input PWM frequency on the PWMB pin. While the TPS61177A also supports a direct PWM dimming method, in direct PWM dimming mode the WLED current is turned on or off, synchronized with the input PWM signal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61177A	VQFN (20)	3.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application – Analog and PWM Mixed Mode



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

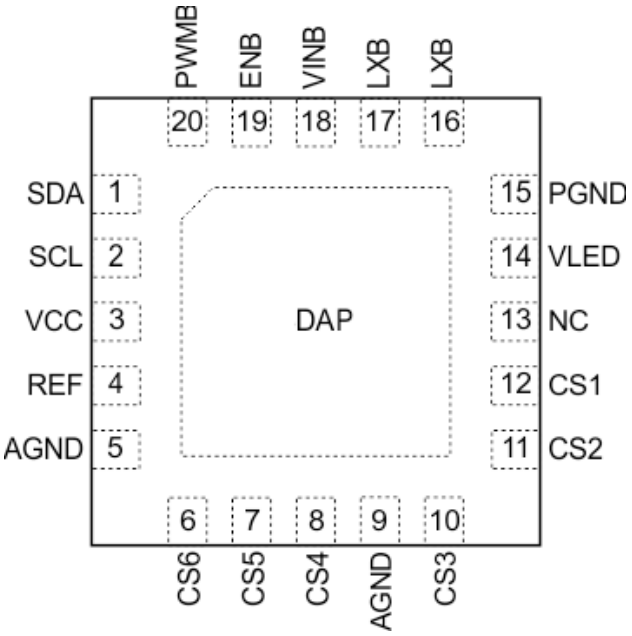
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to Revision A	Page
• Added several items to "Applications" on page 1	1

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5 Pin Configuration and Functions

RGR Package
20-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AGND	5, 9	—	Signal ground of the device.
CS1, CS2, CS3, CS4, CS5, CS6	6, 7, 8, 10, 11, 12	I	Current sink regulation inputs. They are connected to the cathode of WLEDs. The PWM loop regulates the lowest V_{CS} to 500 mV. Each channel is limited to 30-mA current. Connect any unused CS pin to AGND or leave it open.
ENB	19	I	Enable pin
LXB	16, 17	I	Drain connection of the internal PWM switch MOSFET and external Schottky diode.
REF	4	O	The reference pin for internal error amplifier. Connect a 470-nF ceramic capacitor to REF.
PGND	15	—	Power ground of the IC. Internally, it connects to the source of the PWM switch. Tie the ground of power stage components to this ground.
PWMB	20	I	Dimming control logic input. The dimming frequency range is from 100 Hz to 25 kHz.
SCL	2	I	Clock input for I^2C interface
SDA	1	I/O	Data input for I^2C interface
VCC	3	I	Internal pre-regulator and supply rail for the internal logic. Do not connect any capacitor to VCC pin.
VINB	18	I	Power supply to the IC
VLED	14	I	The voltage detect pin for V_{OUT}.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	VINB	–0.3	26.4	V
	LXB, VLED, CS1, CS2, CS3, CS4, CS5, CS6	–0.3	40	
	ENB, PWMB	–0.3	30	
	SDA, SCL, VCC	–0.3	3.6	
Continuous power dissipation		See *Thermal Information*		°C
Operating junction temperature		–40	150	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.5	24	V
V_{OUT}	Output voltage	V_{IN} + 2	39	
F_{PWM_I}	PWM input signal frequency	0.1	25	kHz
D_{MIN_I}	PWM input signal minimum duty cycle	1%		
F_{BOOST}	Boost regulator switching frequency	450	1200	kHz
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	

6.4 Thermal Information

THERMAL METRIC(1)		TPS61177A RGR (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

VINB = 12 V, PWMB/ENB = logic high, CS current = 20 mA, CS voltage = 500 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{INB}	Input voltage range		2.5		24	V
I_{q_VINB}	Operating quiescent current into V_{IN}	Device enable, no switching and no load, V_{INB} = 12 V			3.5	mA
I_{SD}	Shutdown current	V_{INB} = 12 V, EN = low			10	µA
		V_{INB} = 24 V, EN = low			15	
V_{INB_UVLO}	V_{INB} undervoltage lockout threshold, voltage ramp up	UVLO = 000	2.1	2.25	2.4	V
		UVLO = 001	2.4	2.55	2.7	
		UVLO = 010	2.8	3	3.2	
		UVLO = 011	3.3	3.5	3.7	
		Other case	3.8	4	4.2	
V_{IN_Hys}	V_{IN} undervoltage lockout hysteresis			200		mV
BOOST OUTPUT REGULATION						
V_{CS}	CS voltage regulation			500	600	mV
$R_{DS(ON)}$	Switch FET on-resistance	V_{IN} = 12 V		0.20	0.35	Ω
		V_{IN} = 3.3 V		0.30	0.40	
I_{LIM}	Switching MOSFET current limit	D = D_{max}	1.8	2.2	2.6	A
I_{LEAK_LX}	Switch FET leakage current	V_{SW} = 40 V			5	µA
F_{LX}	Switching frequency	FREQ = 00	0.36	0.45	0.54	MHz
		FREQ = 01	0.48	0.6	0.72	
		FREQ = 10	0.64	0.8	0.96	
		FREQ = 11	0.96	1.2	1.44	
D_{MAX}	Maximum duty cycle	F_{LX} = 0.8 MHz	90%	95%		
T_F	Slew rate of switching FET ON	SR = 00		4.6		V/ns
		SR = 01		3.5		
		SR = 10		2.5		
		SR = 11		1.3		
CS CURRENT REGULATION						
I_{CS}	CSn current (See Figure 23)	I_{CS} = 0000		15		mA
		I_{CS} = 0001		16		
		…		…		
		ICS = 1111		30		
I_{CSA}	CSn current accuracy (I_{CSn} – 20 mA × D_{PWM_I})/20 mA x D_{PWM_I}	I_{CS} = 20 mA, MODE = 00 and 01 D_{PWM_I} = 100%, T_A = 25°C	–3%		3%	
		I_{CS} = 20 mA, MODE = 01 D_{PWM_I} = 255/1023, T_A = 25°C	–3%		3%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 255/1023, T_A = 25°C	–3%		3%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 51/1023, T_A = 25°C	–5%		5%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 10/1023, T_A = 25°C	–8%		8%	

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Electrical Characteristics (continued)

VINB = 12 V, PWMB/ENB = logic high, CS current = 20 mA, CS voltage = 500 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CSM}	Current matching (I_{CSn} – I_{AVG})/I_{AVG}	I_{CS} = 20 mA, MODE = 00 and 01, D_{PWM_I} = 100%, T_A = 25°C	–2%		2%	
		I_{CS} = 20 mA, MODE = 01, D_{PWM_I} = 255/1023, T_A = 25°C	–2%		2%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 255/1023, T_A = 25°C	–2%		2%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 51/1023, T_A = 25°C	–5%		-5%	
		I_{CS} = 20 mA, MODE = 10, D_{PWM_I} = 10/1023, T_A = 25°C	–5%		5%	
	DC dimming resolution steps	MODE = 01 and 10, F_{PWM_I} = 0.1 to 5 kHz		1024		
		MODE = 01 and 10, F_{PWM_I} = 5 to 10 kHz		512		
		MODE = 01 and 10, F_{PWM_I} = 10 to 25 kHz		256		
	Brightness response time	D_{PWM_I} 10% to 90% MODE = mixed and DC, F_{PWM_I} = 25 kHz		400		µs
		D_{PWM_I} 10% to 90% MODE = mixed and DC, F_{PWM_I} = 100 Hz		10.4		ms
I_{CSLK}	CSn leakage current	V_{CS} = 40 V			5	µA
I_{CSIR}	CSn current inrush			10%		
t_{MP}	Minimum dimming pulse	MODE = 00	400			ns
t_{DEG}	Deglitch pulse width			125		ns
CONTROL AND PROTECTION						
V_H	ENB logic high threshold	VINB = 2.7 V and 3.3 V	1.8			V
V_L	ENB logic low threshold	VINB = 2.7 V and 3.3 V			0.5	
V_H	PWMB logic high threshold	VINB = 2.7 V and 3.3 V	1.8			
V_L	PWMB logic low threshold	VINB = 2.7 V and 3.3 V			0.5	
R_{PD}	Pulldown resistor on ENB	ENB = 3.3 V	300	600	1200	kΩ
	Pulldown resistor on PWMB	PWMB = 3.3 V	300	600	1200	
V_{OVP}	Output overvoltage threshold		39	39.5	40	V
$T_{shutdown}$	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			15		
F_{SAMPLE}	Input sampling oscillator frequency		22	25	29	MHz

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6.6 I²C Timing Requirements

			MIN	NOM	MAX	UNIT
ADDR	Configuration parameters slave address	Write		58h		
		Read		59h		
V_{IL}	Low level input voltage	Supply = 2.5 V, V_{IN} falling, standard and fast modes			0.75	V
V_{IH}	High level input voltage	Supply = 2.5 V, V_{IN} rising, standard and fast modes	1.75			V
V_{HYS}	Hysteresis	Supply = 2.5 V, applicable to fast mode only	125			mV
V_{OL}	Low level output voltage	Sinking 3 mA			500	mV
C_I	Input capacitance				10	pF
f_{SCL}	Clock frequency	Standard mode			100	kHz
		Fast mode			400	
t_{LOW}	Clock low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	Clock high period	Standard mode	4			µs
		Fast mode	0.6			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{hd:STA}$	Hold time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:STA}$	Set-up time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
$t_{hd:DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	
t_{RCL1}	Rise time of SCL after a repeated START condition and after an ACK bit	Standard mode	20+0.1CB		1000	ns
		Fast mode	20+0.1CB		1000	
t_{RCL}	Rise time of SCL	Standard mode	20+0.1CB		1000	ns
		Fast mode	20+0.1CB		300	
t_{FCL}	Fall time of SCL	Standard mode	20+0.1CB		300	ns
		Fast mode	20+0.1CB		300	
t_{RDA}	Rise time of SDA	Standard mode	20+0.1CB		1000	ns
		Fast mode	20+0.1CB		300	
t_{FDA}	Fall time of SDA	Standard mode	20+0.1CB		300	ns
		Fast mode	20+0.1CB		300	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4			µs
		Fast mode	0.6			
C_B	Capacitive load on SDA and SCL	Standard mode			400	pF
		Fast mode			400	
N_{WRITE}	Number of write cycles		1000			
t_{WRITE}	Write time				100	ms
	Data retention	Storage temperature = 150°C	100,000			hrs

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6.7 Typical Characteristics

Table 1. Table of Graphs

TITLE	DESCRIPTION	FIGURE
Efficiency vs PWM Duty in PWM Mode	V_{IN} = 12 V, V_{OUT} = 6S6P, 8S6P, 10S6P, I_{CS} = 20 mA, L = 10 µH	Figure 1
Efficiency vs PWM Duty in PWM Mode	V_{IN} = 3 V, 12 V, 21 V, V_{OUT} = 6S6P, 8S6P, 10S6P, L = 10 µH	Figure 2
Efficiency vs PWM duty in Mixed Mode	V_{IN} = 12 V, V_{OUT} = 6S6P, 8S6P, 10S6P, I_{CS} = 20 mA, L = 10 µH	Figure 3
Efficiency vs PWM duty in Mixed Mode	V_{IN} = 3 V, 12 V, 21 V, V_{OUT} = 6S6P, 8S6P, 10S6P, L = 10 µH	Figure 4
Efficiency vs PWM duty in Analog Mode	V_{IN} = 12 V, V_{OUT} = 6S6P, 8S6P, 10S6P, I_{CS} = 20 mA, L = 10 µH	Figure 5
Efficiency vs PWM duty in Analog Mode	V_{IN} = 3 V, 12 V, 21 V, V_{OUT} = 6S6P, 8S6P, 10S6P, L = 10 µH	Figure 6
Dimming Linearity in PWM Mode	V_{IN} = 12 V, V_{OUT} = 10S6P , F_{DIM} = 200 Hz and 20 kHz, L = 10 µH	Figure 7
Dimming Linearity in Mixed Mode	V_{IN} = 12 V, V_{OUT} = 10S6P , F_{DIM} = 200 Hz and 20 kHz, L = 10 µH	Figure 8
Dimming linearity in Analog Mode	V_{IN} = 12 V, V_{OUT} = 10S6P , F_{DIM} = 200 Hz and 20 kHz, L = 10 µH	Figure 9
Switch Waveform	V_{IN} = 3 V, V_{OUT} = 6S6P, Duty = 100%, L = 10 µH	Figure 10
Switch Waveform	V_{IN} = 12 V, V_{OUT} = 10S6P, Duty = 100%, L = 10 µH	Figure 11
Mixed-Mode Dimming Ripple	V_{IN} = 12 V, V_{OUT} = 10S6P, F_{DIM} = 200 Hz, Duty = 50%, L = 10 µH	Figure 12
Mixed-Mode Dimming Ripple	V_{IN} = 12 V, V_{OUT} = 10S6P, F_{DIM} = 200 Hz, Duty = 12.5%, L = 10 µH	Figure 13
Mixed-Mode Dimming Ripple	V_{IN} = 12 V, V_{OUT} = 10S6P, F_{DIM} = 20 kHz, Duty = 12.5%, L = 10 µH	Figure 14
PWM-Mode Dimming Ripple	V_{IN} = 12 V, V_{OUT} = 10S6P, F_{DIM} = 200 Hz, Duty = 50%, L = 10 µH	Figure 15
PWM-Mode Dimming Ripple	V_{IN} = 12 V, V_{OUT} = 10S6P, F_{DIM} = 20 kHz, Duty = 50%, L = 10 µH	Figure 16

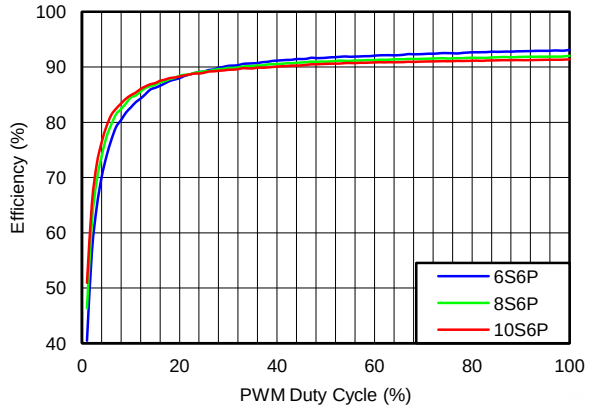


Figure 1. Efficiency vs PWM Duty in PWM Mode

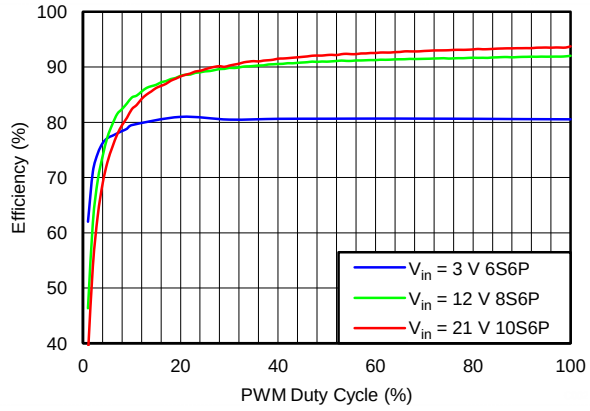


Figure 2. Efficiency vs PWM Duty in PWM Mode

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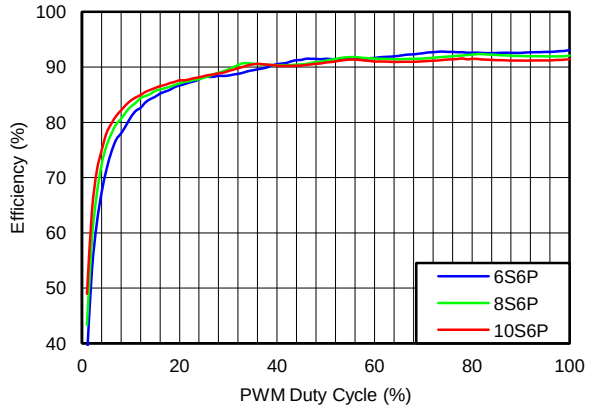


Figure 3. Efficiency vs PWM Duty in Mixed Mode

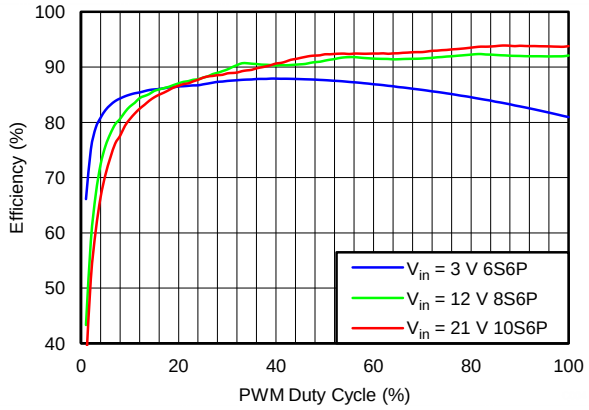


Figure 4. Efficiency vs PWM Duty in Mixed Mode

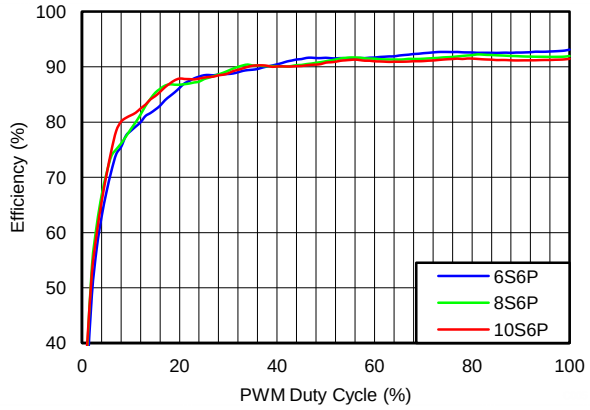


Figure 5. Efficiency vs PWM Duty in Analog Mode

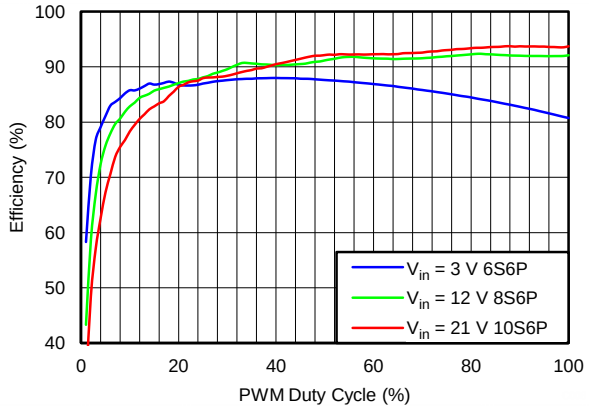


Figure 6. Efficiency vs PWM Duty in Analog Mode

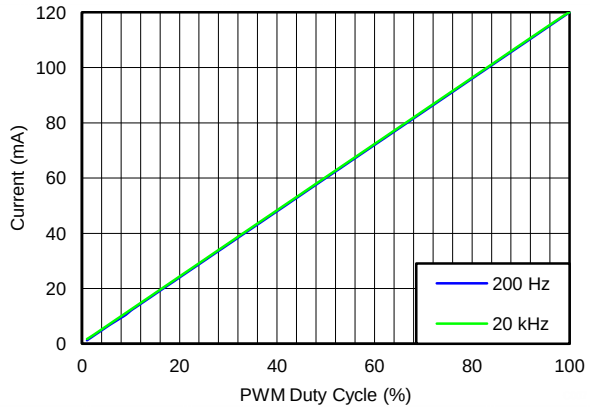


Figure 7. Dimming Linearity in PWM Mode

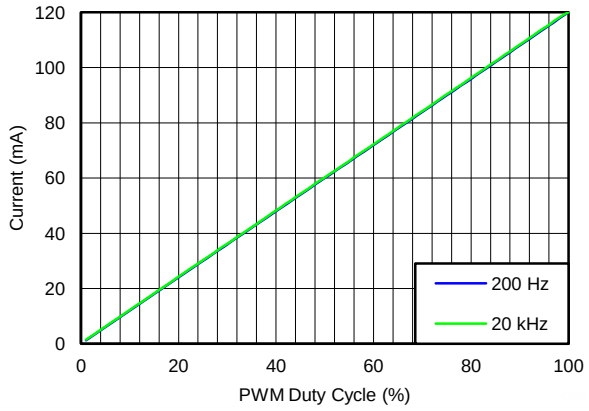


Figure 8. Dimming Linearity in Mixed Mode

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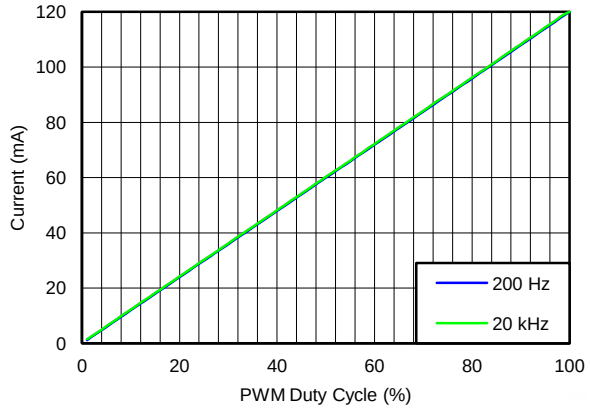


Figure 9. Dimming Linearity in Analog Mode

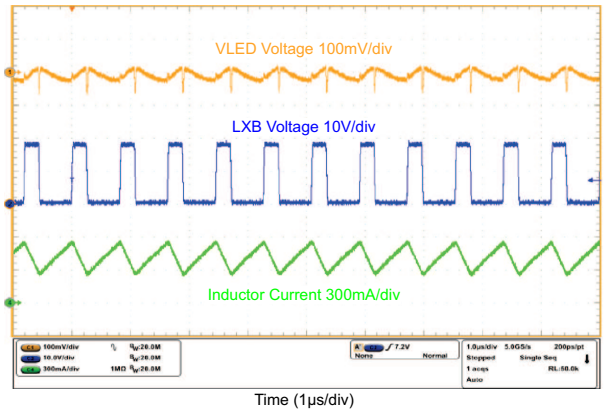


Figure 10. Switch Waveform

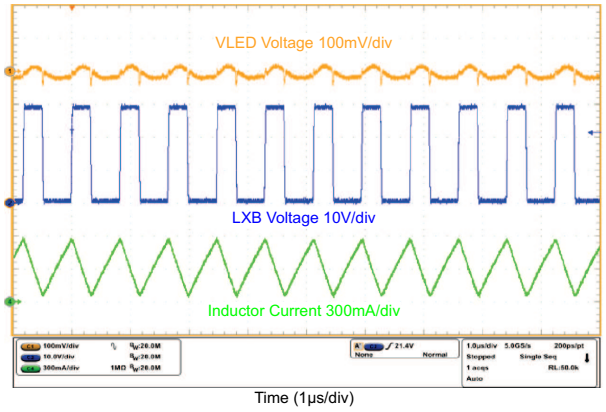
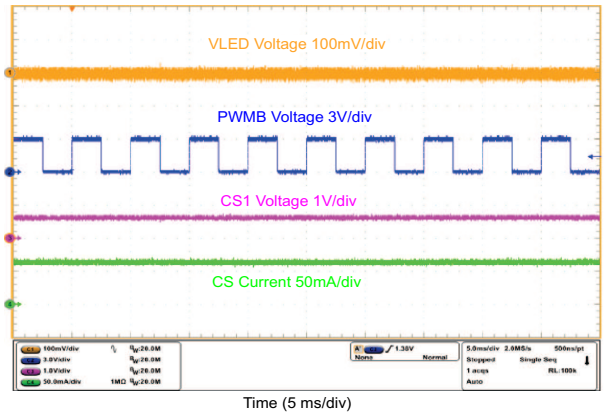
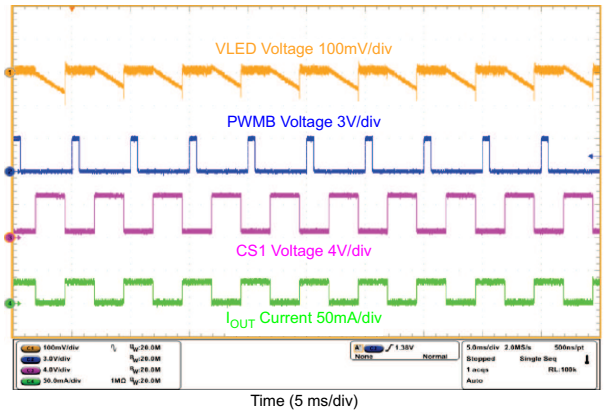


Figure 11. Switch Waveform



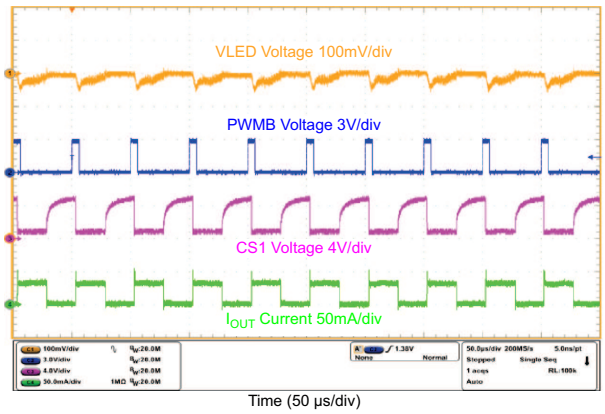
F_{DIM} = 200 Hz Duty = 50%

Figure 12. Mixed-Mode PWM Dimming



F_{DIM} = 200 Hz Duty = 12.5%

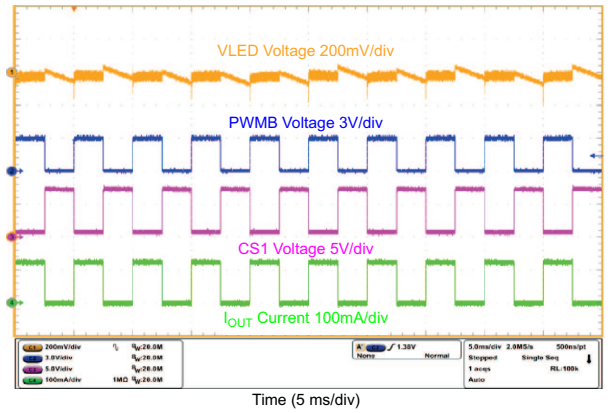
Figure 13. Mixed-Mode PWM Dimming



F_{DIM} = 20 kHz Duty = 12.5%

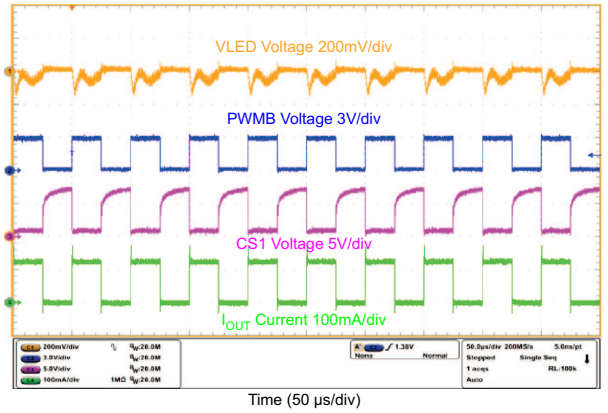
Figure 14. Mixed-Mode PWM Dimming

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F_{DIM} = 200 Hz Duty = 50%

Figure 15. PWM Mode Dimming



F_{DIM} = 20 kHz Duty = 50%

Figure 16. PWM Mode Dimming

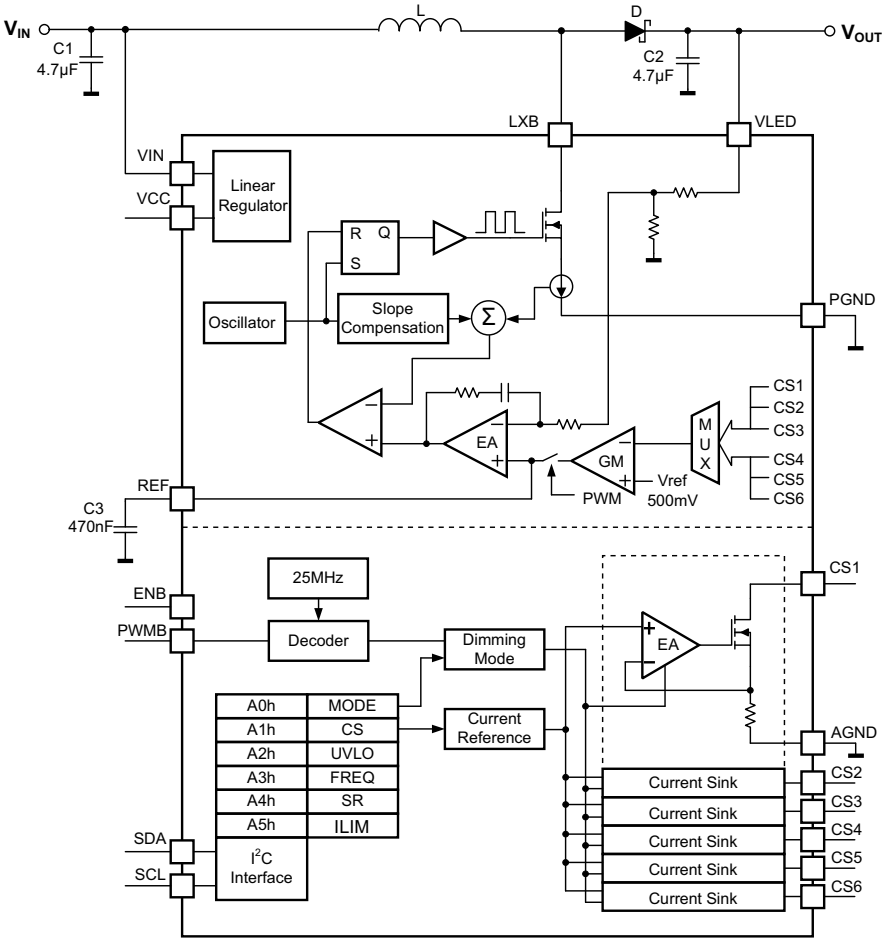
7 Detailed Description

7.1 Overview

The TPS61177A is a high-efficiency, high output voltage white-LED (WLED) driver for notebook panel backlighting applications. Due to the large number of white LEDs required to provide backlighting for medium-to-large display panels, the LEDs must be arranged in parallel strings of several LEDs in series. Therefore, the backlight driver for battery-powered systems is almost always a boost regulator with multiple current-sink regulators. Having more WLEDs in series reduces the number of parallel strings, thus improving overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there must be enough white LEDs in series to ensure the output voltage stays above the input voltage range.

The TPS61177A device has integrated all of the key function blocks to power and control up to 72 WLEDs. The device includes a 1.8-A, 40-V boost regulator, six 30-mA current sink regulators, and a protection circuit for overcurrent, overvoltage, open LED, short LED, and overtemperature failures. The TPS61177A integrates mixed mode dimming methods with the PWM interface to reduce the output ripple voltage and audible noise. Optional direct PWM and pure analog dimming modes are user selectable through the I^2C programming.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61177A device has a built-in linear regulator to supply the device analog and logic circuit. The VCC pin is recommended to be open without any capacitance load. VCC does not have high current sourcing capability for external use and typically is regulated at 3.3 V.

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Feature Description (continued)

7.3.2 Boost Regulator

The fixed-frequency PWM boost converter uses current-mode control and has integrated loop compensation. The internal compensation ensures stable output over the full input and output voltage ranges assuming the recommended inductance and output capacitance values shown in *Figure 36*. The output voltage of the boost regulator is automatically set by the device to minimize voltage drop across the CS pins. The device regulates the lowest CS pin to 500 mV at 20-mA current and consistently adjusts the boost output voltage to account for any changes in LED forward voltages. If the input voltage is higher than the sum of the WLED forward voltage drops (at low duty cycles), the boost converter is not able to regulate the output due to its minimum duty cycle limitation. In this case, increase the number of WLEDs in series or include series ballast resistors in order to provide enough headroom for the converter to boost the output voltage. Since the TPS61177A integrates a 1.8-A, 40-V power MOSFET, the boost converter can provide up to a 39-V output voltage.

7.3.3 Programmable Switch Frequency and Slew Rate

Both switching frequency and slew rate of TPS61177A can be programmable by a E^2PROM register value which is pre-set before device power up. The switching frequency has four options adjustable to 450 kHz, 600 kHz, 800 kHz, or 1200 kHz. The slew rate of switching FET from off to on also has four selections: 1.3 V/ns, 2.5 V/ns, 3.5 V/ns to 4.6 V/ns.

See *FREQ (A3h)* and *SR (A4h)* for E^2PROM address and data table of boost switching frequency programming and boost switching slew rate selection.

The adjustable switching frequency feature provides the user with the flexibility of choosing either a faster switching frequency by using an inductor with smaller inductance and footprint or a slower switching frequency to get potentially higher efficiency due to lower switching losses. In additional, the selectable slew rate for switching gives flexibility to trade off between switching loss and electronic-magnetic interference (EMI) effects to the application system.

7.3.4 LED Current Sinks

The six current sink regulators embedded in the TPS61177A can be collectively configured to provide up to a maximum of 30 mA each. These six specialized current sinks are accurate to within ±3% max for currents at 20 mA, with a string-to-string difference of ±2%.

Each CS channel current must be programmed to the highest WLED current expected; each CS channel current is programmable from 15 mA to 30 mA by an E^2PROM register through the I^2C interface. See *CS (A1h)* for the E^2PROM register table of CS current programming.

7.3.5 Enable and Start-Up Timing

The internal regulator which provides VCC wakes up as soon as ENB is applied. VCC does not come to full regulation until VINB voltage is above UVLO. Before boost convert start-up, the TPS61177A checks the status of all current feedback channels and shuts down any unused feedback channels. It is recommended to short the unused channels to ground for faster start-up.

After the device is enabled, if the PWM pin is left floating or grounded, the output voltage of the TPS61177A regulates to the minimum output voltage. Once the device detects a voltage on the PWM pin, the TPS61177A begins to regulate the CS pin current, as a pre-set per the E^2PROM register data, according to the duty cycle of the signal on the PWMB pin. The boost converter output voltage rises to the appropriate level to accommodate the sum of the white LED string with the highest forward voltage drops plus the headroom of the current sink at that current.

Pulling the ENB pin low shuts down the device, resulting in consumption of less than 10 µA in shutdown mode.

The TPS61177A also integrates power-up sequence control for start-up. There is no specified power or control signal sequence requirement for VINB, ENB, and PWMB. Figure 17 provides the detail timing diagram for TPS61177A start-up and shutdown.

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Feature Description (continued)

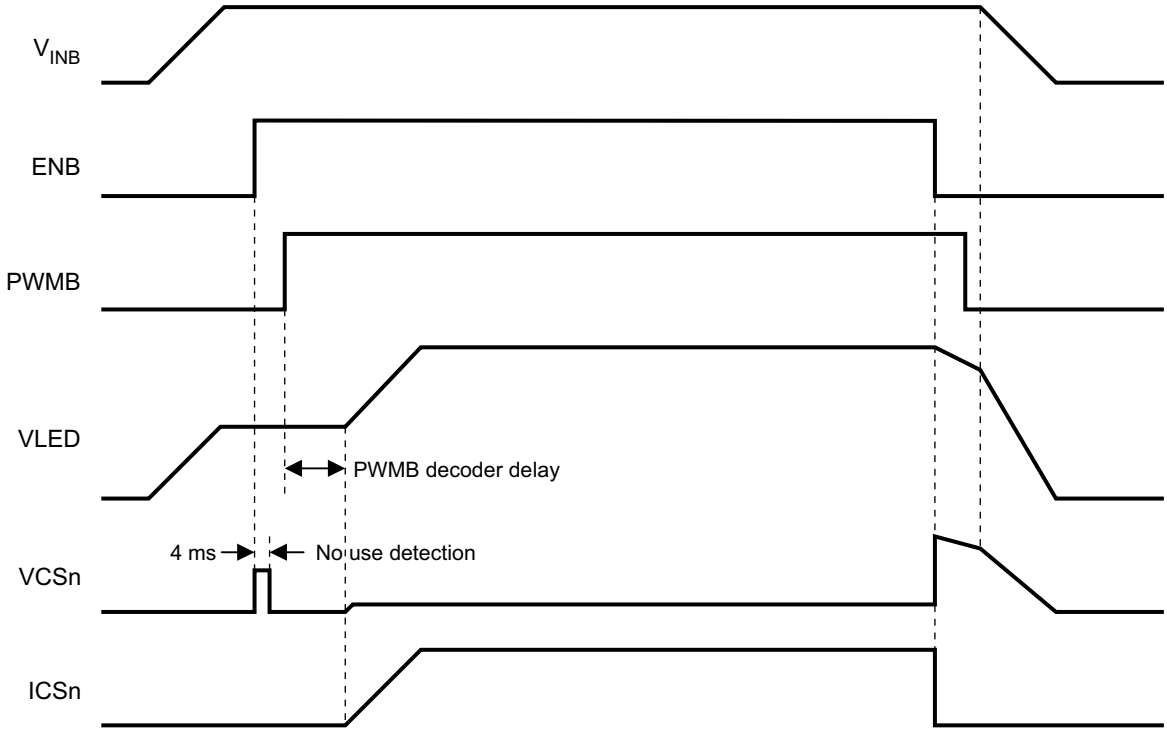


Figure 17. Start-up and Shutdown Timing Diagram

The PWMB decoder delay time period is determined by different dimming mode, input duty cycle, and frequency on the PWMB pin. In PWM mode, the decoder delay time is zero. Once the rising edge is detected on the PWMB pin, the output voltage starts ramping up immediately. While in mixed dimming mode or analogdimming mode, the decoder delay time is equal to twice input PWM signal cycle time and 400 µs minimally. If PWM signal input keeps at high level after first rising edge, the decoder delay is about 20 ms.

Figure 18 provides the detail timing diagram for TPS61177A start-up and shutdown when one of CS channel is open. The VLED voltage always ramps up to the overvoltage protection threshold which is 39.5 V typically, if one of CS pin is floating. The device then detects the zero current string, and removes it from the feedback loop.

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Feature Description (continued)

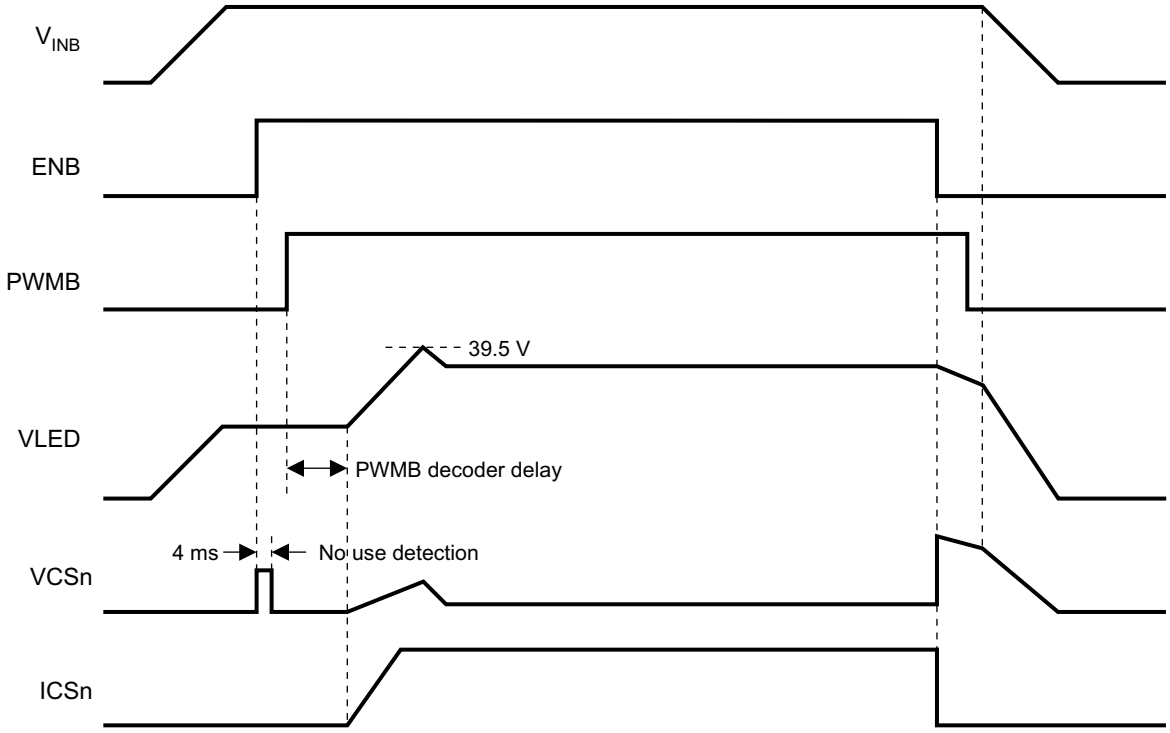


Figure 18. Start-Up and Shutdown Timing Diagram (Mixed Mode and DC Mode)

7.3.6 Input Undervoltage Protection (UVLO)

The TPS61177A will not start up until the VINB voltage is higher than the UVLO threshold which is preset by E^2PROM register data. During normal operation, if the VINB drops below UVLO with 200-mV hysteresis, the TPS61177A immediately shuts down. See *UVLO (A2h)* for E^2PROM address and data table of UVLO threshold.

7.3.7 Overvoltage Protection (OVP)

The TPS61177A integrates output OVP which is fixed at 39.5 V typically. Once the VLED pin detects the voltage higher than 39.5 V, the boost switching regulator stops switching until the voltage of VLED pin drop below 39.5 V with 500-mV hysteresis.

7.3.8 Current-Sink Open Protection

If one of the device WLED strings is open, the device automatically detects and disables that string. The open WLED string is detected by sensing no current in the corresponding CS pin. As a result, the TPS61177A deactivates the open current sink and removes it from the voltage feedback loop. Subsequently, the output voltage drops and is regulated to the minimum voltage required for the connected WLED strings. The CS currents of the connected WLED strings remain in regulation.

The device turns off if it detects that all of the WLED strings are open. If an open string is reconnected again, a power-on reset (POR) or ENB pin toggling is required to reactivate a previously deactivated string.

7.3.9 Overcurrent Protection

The TPS61177A has a pulse-by-pulse overcurrent limit of 1.8 A (minimum). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the device and external components during an overload condition. When there is a sustained overcurrent condition more than 2 ms, the device shuts down and requires a POR or EN pin toggling to restart. The overcurrent shutdown protection can be disabled by E^2PROM register through I^2C interface. See *ILIM (A5h)* for E^2PROM register table of ILIM shutdown protection programming.

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Feature Description (continued)

7.3.10 Thermal Protection

When the junction temperature of the TPS61177A is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature is back to less than 150°C with about 15°C hysteresis.

7.4 Device Functional Modes

7.4.1 Mode Selection

The mixed-mode dimming method, analog dimming method, or direct PWM dimming method can be selected through the E^2PROM register. See *MODE (A0h)* for E^2PROM register table of dimming mode programming.

7.4.2 Analog and PWM Mixed Dimming Mode

In analog and PWM mixed mode, the TPS61177A features both analog dimming and PWM digital dimming. Analog dimming can provide potentially a lower power requirement for the same WLED brightness output because of a low voltage drop across each WLED when the current is low. Digital PWM dimming provides less WLED color distortion since the WLED current is held at 25% of full scale when the WLED is on.

The brightness control signal on the PWM pin is translated to a 10-bit digital signal and sent to control the six current regulators. Each current regulator outputs is DC, and PWM (25% < D_{PWM} < 100%) modulates the amplitude of the currents from 25% to 100% of preset full-scale current. For D_{PWM} < 25%, each CS turns on/off at translated duty cycle and same frequency to the input PWM, and in the WLED on duty current is regulated at 25% of full scale. Mixed-mode dimming provides the benefits of both the analog and PWM dimming. For 25% < D_{PWM} < 100%, analog dimming benefits the low power requirement and increases the power to brightness transform efficiency. At light load conditions, D_{PWM} < 25%, the PWM dimming provides both high accuracy brightness and low color distortion. Figure 19 provides the detailed timing diagram of the analog and PWM mixed dimming mode.

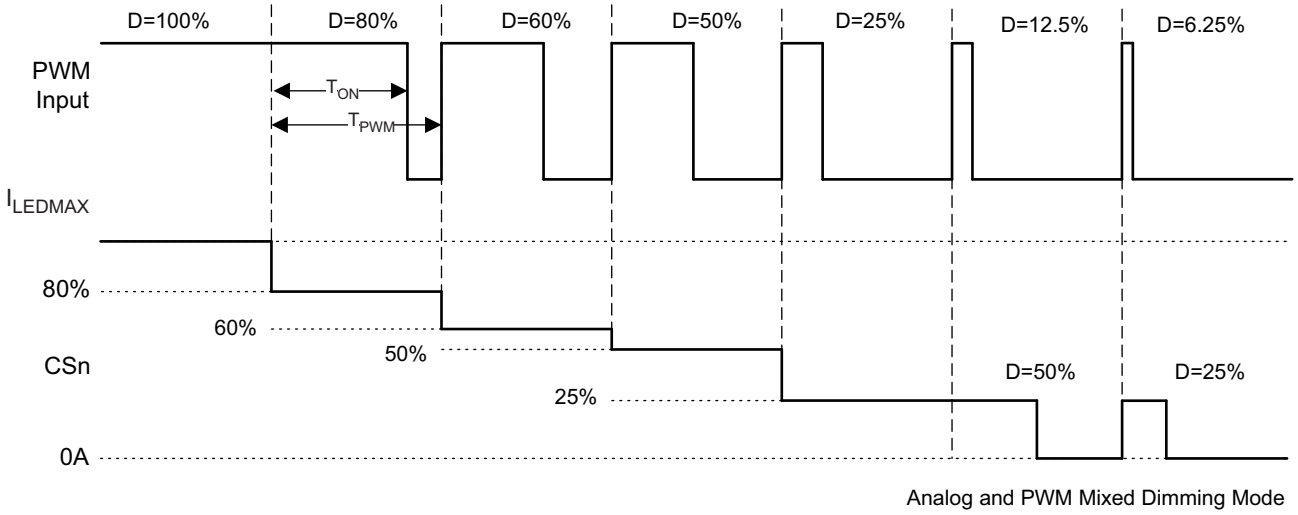


Figure 19. Analog and PWM Mixed-Mode Dimming Diagram

7.4.3 Analog Dimming Mode

In analog dimming mode, TPS61177A features pure analog dimming all over the brightness range of full-scale LED current. Analog dimming can provide potentially low power requirement for same WLED brightness output because of low voltage drop across each WLED when the current is low. In additional, the brightness control signal on the PWMB pin is translated to an up to 10-bits digital signal and sent to control the six current regulators. Each current regulator output DC modulates the amplitude of the currents from 1% to 100% of preset full-scale current. Figure 20 provides the detailed timing diagram of the analog dimming mode.

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Device Functional Modes (continued)

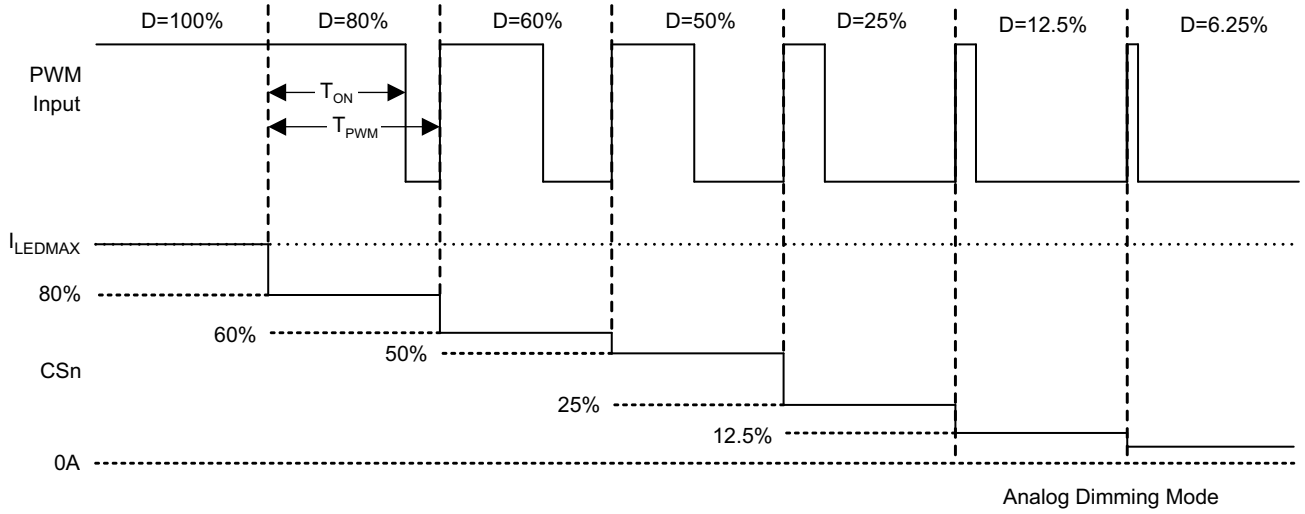


Figure 20. Analog-Mode Dimming Diagram

7.4.4 Direct PWM Dimming

In direct PWM mode, all current feedback channels are turned on and off and are synchronized with the input PWM signal. Figure 21 provides the detailed timing diagram of the direct PWM dimming mode.

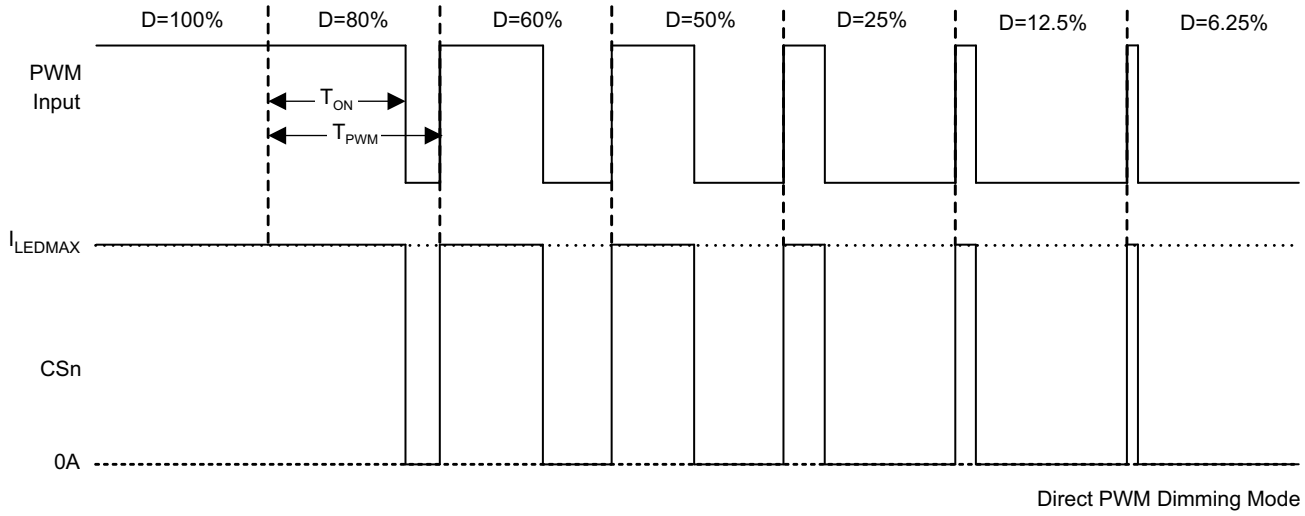


Figure 21. Direct PWM-Mode Dimming Diagram

7.5 Programming

7.5.1 Configuration Parameters

Table 2 shows the memory map of the configuration parameters.

Table 2. Configuration Memory Map

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
A0h	MODE	01h	Sets brightness dimming mode
A1h	CS	05h	Sets the current sinks full scale current
A2h	UVLO	03h	Sets the input voltage UVLO threshold
A3h	FREQ	01h	Sets the boost switching frequency
A4h	SR	00h	Sets the boost switching slew rate
A5h	ILIM	00h	Enables/disables the shutdown protection for current limit
FFh	Control	00h	Controls whether read and write operations access RAM or E^2PROM registers.

7.6 Register Maps

7.6.1 MODE (A0h)

The **MODE** register can be written to and read from.

Figure 22. MODE Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED						MODE	
R/W-0						R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. MODE Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.
1:0	MODE	R/W	1	These bits configure the current sink dimming method for brightness control. 00 = Direct PWM dimming mode 01 = Analog and PWM mixed dimming mode 10 = Analog dimming mode

7.6.2 CS (A1h)

The **CS** register can be written to and read from.

Figure 23. CS Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED					CS		
R/W-0					R/W-5		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. CS Register Bit Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.

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Table 4. CS Register Bit Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CS	R/W	5	These bits select the full scale current for all six current sinks. 0000: I_{CS} = 15 mA 0001: I_{CS} = 16 mA 0010: I_{CS} = 17 mA 0011: I_{CS} = 18 mA 0100: I_{CS} = 19 mA 0101: I_{CS} = 20 mA 0110: I_{CS} = 21 mA 0111: I_{CS} = 22 mA 1000: I_{CS} = 23 mA 1001: I_{CS} = 24 mA 1010: I_{CS} = 25 mA 1011: I_{CS} = 26 mA 1100: I_{CS} = 27 mA 1101: I_{CS} = 28 mA 1110: I_{CS} = 29 mA 1111: I_{CS} = 30 mA

7.6.3 UVLO (A2h)

The **UVLO** register can be written to and read from.

Figure 24. UVLO Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED						UVLO	
R/W-0						R/W-3	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. UVLO Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.
2:0	UVLO	R/W	3	These bits select the UVLO threshold. 000: V_{UVLO} = 2.25 V 001: V_{UVLO} = 2.55 V 010: V_{UVLO} = 3 V 011: V_{UVLO} = 3.5 V 100: V_{UVLO} = 4 V Others: V_{UVLO} = 4 V

7.6.4 FREQ (A3h)

The **FREQ** register can be written to and read from.

Figure 25. FREQ Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED						FREQ	
R/W-0						R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. FREQ Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.
1:0	FREQ	R/W	1	These bits configure the switching frequency. 00: F_{LX} = 450 kHz 01: F_{LX} = 600 kHz 10: F_{LX} = 800 kHz 11: F_{LX} = 1200 kHz

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7.6.5 SR (A4h)

The **SR** register can be written to and read from.

Figure 26. SR Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED						SR	
R/W-0						R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. SR Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.
1:0	SR	R/W	0	These bits configure the falling slew rate of switching voltage from OFF to ON. 00: SR = 4.6 V/ns 01: SR = 3.5 V/ns 10: SR = 2.5 V/ns 11: SR = 1.3 V/ns

7.6.6 ILIM (A5h)

The **ILIM** register can be written to and read from.

Figure 27. ILIM Register Bit Allocation

7	6	5	4	3	2	1	0
RESERVED							ILIM
R/W-0							R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. ILIM Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.
0	ILIM	R/W	0	This bit configures the current limit shutdown protection. 0 = Disable current limit shutdown protection 1 = Enable current limit shutdown protection

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7.6.7 Control (FFh)

Figure 28. Control Register Bit Allocation

7	6	5	4	3	2	1	0
WED	RESERVED						RED
	R/W-0						R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Control Register Bit Field Descriptions

Bit	Field	Type	Reset	Description
7	WED			Setting this bit forces the contents of all registers to be copied into E^2PROM, thereby making them the default values during power up. When the contents of all the registers have been written to E^2PROM, the TPS61177A device automatically resets this bit.
6:1	RESERVED	R/W	0	These bits are reserved for future use. During write operations, data intended for these bits are ignored, and during read operations 0 is returned.
0	RED	R/W	0	The state of this bit determines whether read operations return the contents of the registers or the contents of the E^2PROM. 0 = Read operations return the contents of the registers. 1 = Read operations return the contents of the E^2PROM.

7.6.8 Example – Writing to a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h)
3. TPS61177A acknowledges
4. Bus master sends address of RAM register (A0h)
5. TPS61177A acknowledges
6. Bus master sends data to be written
7. TPS61177A acknowledges
8. Bus master sends STOP condition

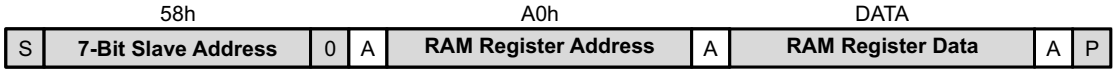


Figure 29. Writing To A Single Ram Register

7.6.9 Example – Writing to Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h).
3. TPS61177A acknowledges
4. Bus master sends address of first RAM register to be written to (A0h)
5. TPS61177A acknowledges
6. Bus master sends data to be written to first RAM register
7. TPS61177A acknowledges
8. Bus master sends data to be written to RAM register at next higher address (auto-increment)
9. TPS61177A acknowledges
10. Steps (8) and (9) repeated until data for final RAM register has been sent
11. TPS61177A acknowledges
12. Bus master sends STOP condition

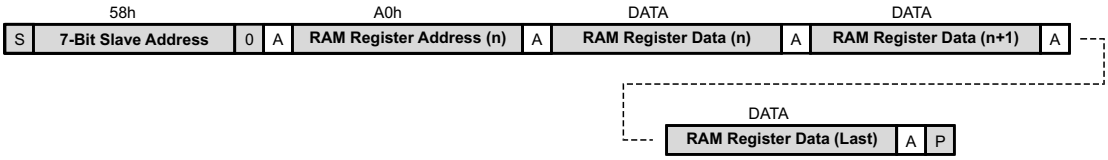


Figure 30. Writing To Multiple Ram Registers

7.6.10 Example – Saving Contents of all RAM Registers to E^{2}PROM

1. Pull high the Enable pin of TPS61177A
2. Pull the PWM pin of TPS61177A to low
3. Bus master sends START condition
4. Bus master sends 7-bit slave address plus low R/W bit (58h)
5. TPS61177A acknowledges
6. Bus master sends address of Control Register (FFh)
7. TPS61177A acknowledges
8. Bus master sends data to be written to the Control Register (80h)
9. TPS61177A acknowledges
10. Bus master sends STOP condition



Figure 31. Saving Contents Of All Ram Registers To E^{2}PROM

The TPS61177A needs a 50-ms time period after receiving STOP condition for saving all RAM registers data to E^{2}PROM. If bus master send 7-bit slave address to call TPS61177A again within 50-ms period, the TPS61177A pulls down the SCL line to LOW until the all RAM registers data saving to E^{2}PROM is completed.

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7.6.11 Example – Reading from a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h)
3. TPS61177A acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS61177A acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS61177A acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (58h)
11. TPS61177A acknowledges
12. Bus master sends address of RAM register (A0h)
13. TPS61177A acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (59h)
16. TPS61177A acknowledges
17. TPS61177A sends RAM register data
18. Bus master not acknowledges
19. Bus master sends STOP condition

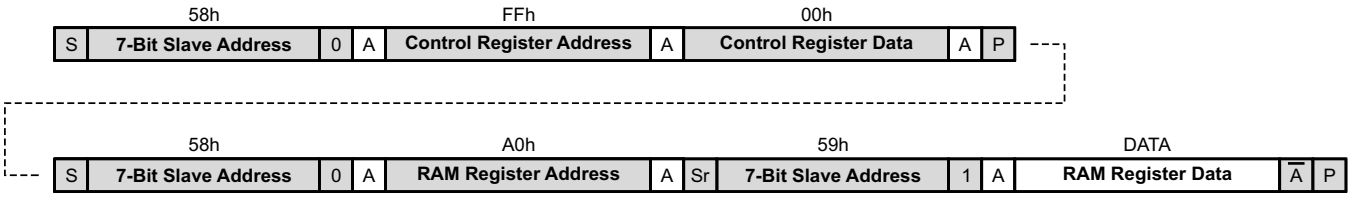


Figure 32. Reading From A Single Ram Register

7.6.12 Example – Reading from a Single E²PROM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h)
3. TPS61177A acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS61177A acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS61177A acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (58h)
11. TPS61177A acknowledges
12. Bus master sends address of RAM register (A0h)
13. TPS61177A acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (59h)
16. TPS61177A acknowledges
17. TPS61177A sends E²PROM register data
18. Bus master not acknowledges
19. Bus master sends STOP condition

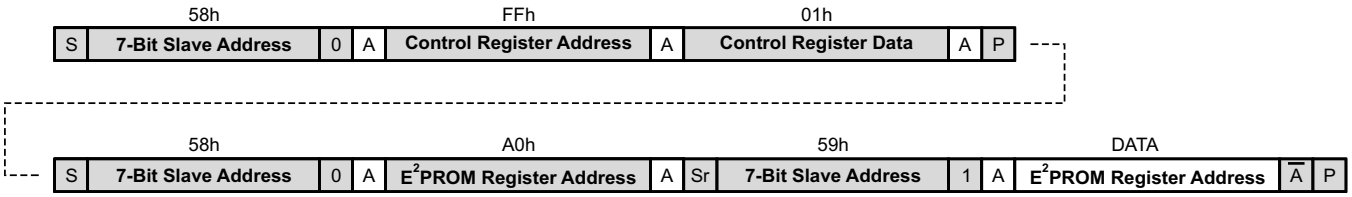


Figure 33. Reading From A Single E²PROM Register

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7.6.13 Example – Reading from Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h)
3. TPS61177A acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS61177A acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS61177A acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (58h)
11. TPS61177A acknowledges
12. Bus master sends address of RAM register (A0h)
13. TPS61177A acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (59h)
16. TPS61177A acknowledges
17. TPS61177A sends contents of first RAM register to be read
18. Bus master acknowledges
19. TPS61177A sends contents of second RAM register to be read
20. Bus master acknowledges
21. TPS61177A sends contents of third (last) RAM register to be read
22. Bus master not acknowledges
23. Bus master sends STOP condition

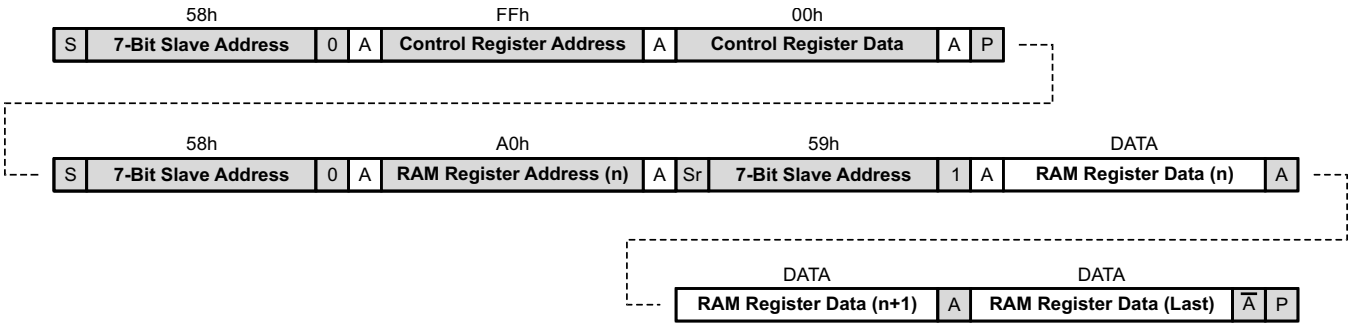


Figure 34. Reading From A Multiple Ram Register

7.6.14 Example – Reading from Multiple E²PROM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (58h)
3. TPS61177A acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS61177A acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS61177A acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (58h)
11. TPS61177A acknowledges
12. Bus master sends address of E²PROM register (00h)
13. TPS61177A acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (59h)
16. TPS61177A acknowledges
17. TPS61177A sends contents of first E²PROM register to be read
18. Bus master acknowledges
19. TPS61177A sends contents of second E²PROM register to be read
20. Bus master acknowledges
21. TPS61177A sends contents of third (last) E²PROM register to be read
22. Bus master not acknowledges
23. Bus master sends STOP condition

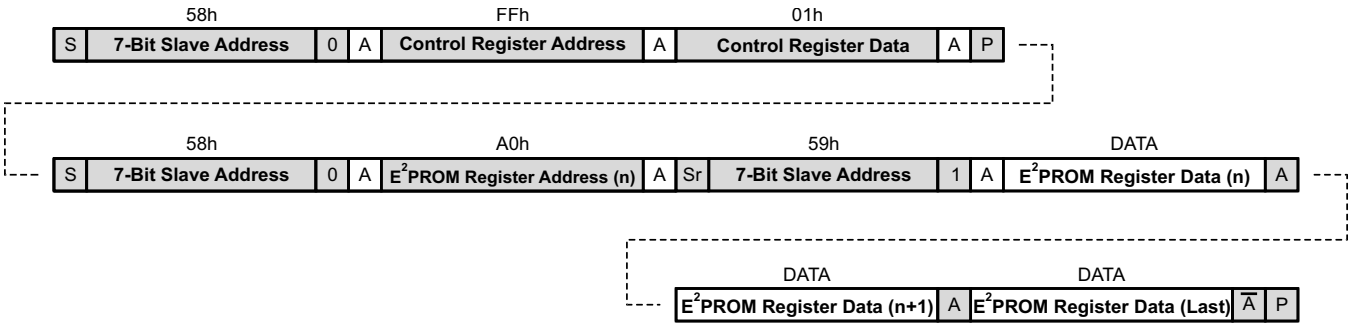


Figure 35. Reading From Multiple E²PROM Registers

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 CS Pin Unused

The TPS61177A has open/short string detection. For an unused CS string, simply short it to ground or leave it open. If the CS pin is open, the boost output voltage ramps up to overvoltage threshold during start-up. The device then detects the zero current string and removes it from the feedback loop. If the CS pin is shorted to ground, the device detects the short and immediately removes it (or them) out of feedback loop within 4 ms after device enable, and the boost output voltage does not go up to overvoltage threshold. Instead, it ramps to the regulation voltage after soft start.

Shorting unused CS pins to ground for faster start-up is recommended.

8.1.2 Brightness Dimming Control

The TPS61177A has three dimming methods. See *Mode Selection* section for dimming mode selection. With analog and PWM mixed dimming or pure analog dimming through the PWM control interface, the internal decoder block detects duty information from the input PWM signal, saves it in an up to 10-bits register and delivers to either a mixed mode dimming control circuit or pure analog dimming control circuit. In mixed dimming mode, the output dimming control circuit sets the DC current of six current sinks linearly between 25% and 100% at same scale to the value in up to a 10-bits register. When the brightness level is below 25% to full-scale value, the dimming control circuit turns on/off six output current sinks at same frequency with PWMB and duty cycle out of shift register. See *Analog and PWM Mixed Dimming Mode* section for more explanation. While in pure analog dimming mode, the output dimming control circuit sets the DC current of six current sinks linearly between 1% and 100% at same scale to the value in up to a 10-bits register. See *Analog Dimming Mode* section for more detail explanation.

The TPS61177A also has direct PWM dimming control through the PWM control interface. In direct PWM mode, each current sink turns on/off at the same frequency and duty cycle as the input PWM signal. See *Direct PWM Dimming* section for more explanation.

When in analog and PWM mixed mode, insertion of a series 10-kΩ to 20-kΩ resistor close to PWMB pin is recommended. This resistor, together with an internal capacitor, forms a low pass R-C filter with a 30-ns to 60-ns time constant. This prevents possible high frequency noise being coupled into the input PWM signal and causing interference to the internal duty cycle decoding circuit. However, it is not necessary for direct PWM mode since the duty cycle decoding circuit is disabled during direct PWM mode.

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8.2 Typical Application

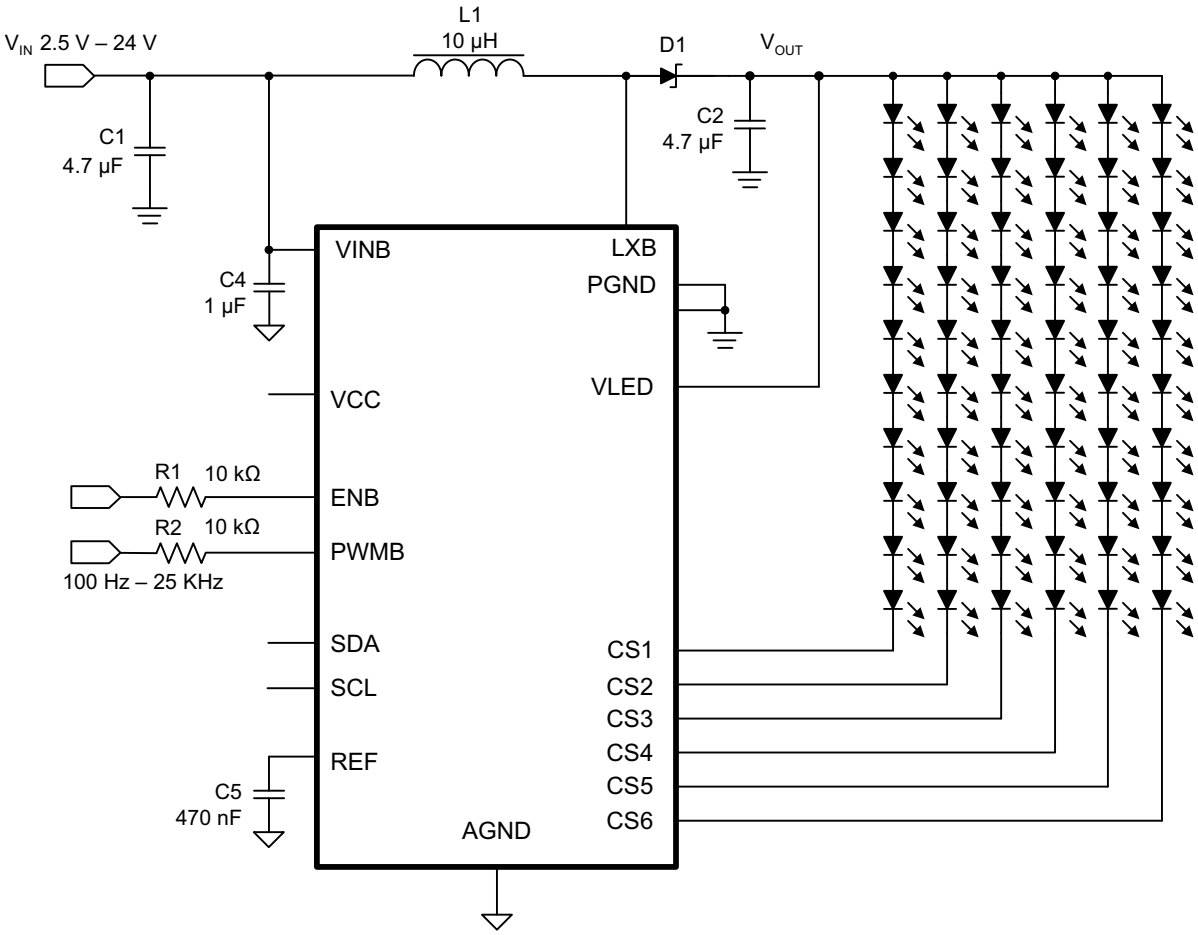


Figure 36. TPS61177A Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Inductor	10 µH
Minimum input voltage	2.5 V
Number of series LED	12
LED maximum forward voltage (Vf)	3.3 V
Schottky diode forward voltage (Vf)	0.2 V
Efficiency (η)	85%
Switching frequency	600 kHz
PWM input frequency	1 kHz
Maximum LED string current	30 mA

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The TPS61177A is designed to support up to 2.2 A (typical) SW current. Thus, SW current must be carefully calculated with factors such as inductor, target efficiency, output voltage, load current, and so forth. In most cases, the voltage ratio between input and boost output must be < 10.

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

Because selection of the inductor affects power supply steady-state operation, transient behavior, and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The TPS61177A is designed to work with inductor values between 4.7 µH and 22 µH. A 10-µH inductor is typically available in a smaller or lower profile package, while a 22-µH inductor may produce higher efficiency due to a slower switching frequency and/or lower inductor ripple. If the boost output current is limited by the overcurrent protection of the device, using a 10-µH inductor and the highest switching frequency maximizes controller output current capability.

Internal loop compensation for PWM control is optimized for the external component values, including typical tolerances, recommended in Table 10. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value depending on how the inductor vendor defines saturation. In a boost regulator, the inductor DC current can be calculated with Equation 1.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = power conversion efficiency, use 90% for TPS61177A applications (1)

The inductor current peak-to-peak ripple can be calculated with Equation 2.

$$\Delta I_{L(P-P)} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_S}$$

where

- $\Delta I_{L(P-P)}$ = inductor peak-to-peak ripple
- L = inductor value
- F_S = Switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage (2)

Therefore, the peak current seen by the inductor is calculated with Equation 3.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (3)$$

Select an inductor with a saturation current over the calculated peak current. To calculate the worst-case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the power FET switch and power diode. Although the TPS61177A device has optimized the internal switch resistances, the overall efficiency is affected by the inductor DC resistance (DCR). Lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 10 lists the recommended inductors.

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Table 10. Recommended Inductor

	L (µH)	DCR (mΩ)	I_{SAT} (A)	Size (L × W × H mm)
Cyntec				
PCMB051H-100MS	10	140	3.0	5.4 x 5.2 x 1.6
Taiyo				
NRA6012T 100ME	10	335	1.45	6 x 6 x 1.2

8.2.2.2 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 4:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (4)$$

where

- V_{ripple} = peak-to-peak output ripple.

The additional part of the ripple caused by ESR is calculated using: $V_{ripple_ESR} = I_{OUT} \times R_{ESR}$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used. The controller output voltage also ripples due to the load transient that occurs during PWM dimming. The TPS61177A adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. In a typical application, the output ripple is less than 250 mV during PWM dimming with a 4.7-µF output capacitor. However, the output ripple decreases with higher output capacitances.

8.2.3 Application Curves

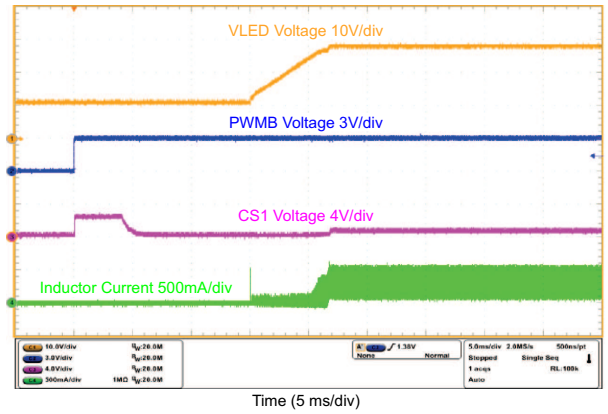


Figure 37. Start-Up Waveform

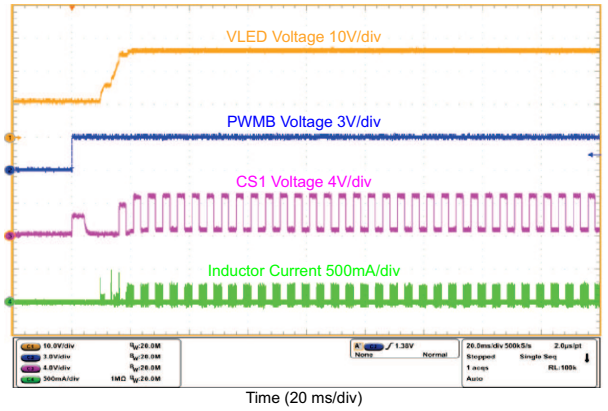


Figure 38. Start-Up Waveform

9 Power Supply Recommendations

The power supply for applications using the TPS61177A device must be big enough considering output power and efficiency at a given input voltage condition. Minimum current requirement condition is (V_{OUT} × I_{OUT})/(V_{IN} × efficiency), and TI recommends a minimum current that is approximately 20% to 30% higher than this value.

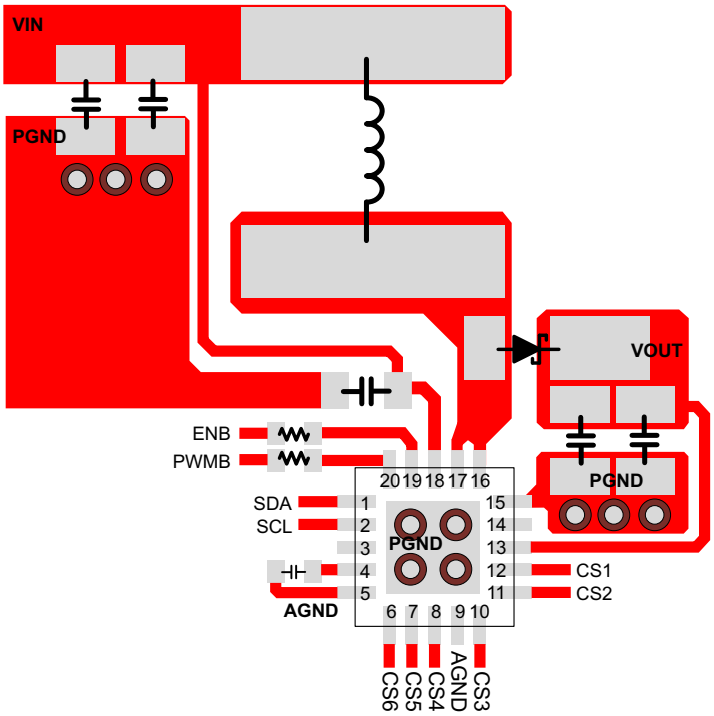
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10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in the *Typical Application* , must not only to be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the device. The input capacitor, C4 in the *Typical Application* , must also be placed close to the inductor. C5 is the reference capacitor for the internal integration circuit. It must be placed as close between the REF and AGND pins as possible to prevent any noise insertion to the digital circuits. The LX pin carries high current with fast rising and falling edges. Therefore, the connection between the pin to the inductor and Schottky diode must be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin because there is a large ground return current flowing between them. When laying out signal grounds, TI recommends using short traces separated from power ground traces, and connecting them together at a single point, for example on the DAP. The DAP must be soldered on to the PCB and connected to the GND pin of the device. An additional thermal via can significantly improve power dissipation of the device.

10.2 Layout Example



11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61177ARGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	77AS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

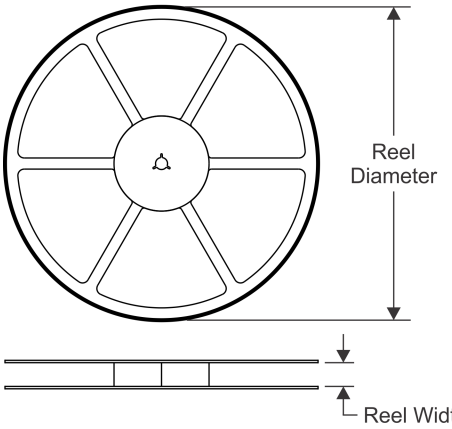
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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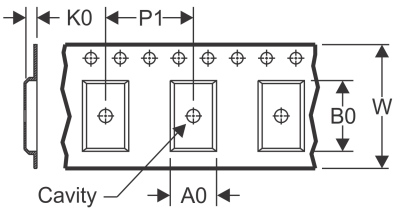
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

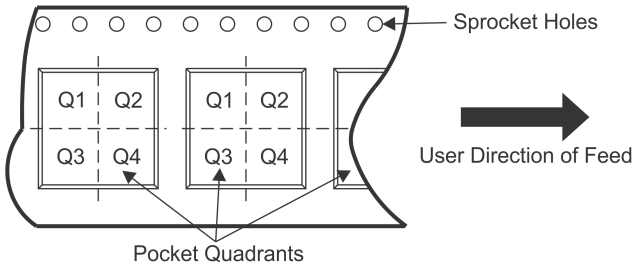


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

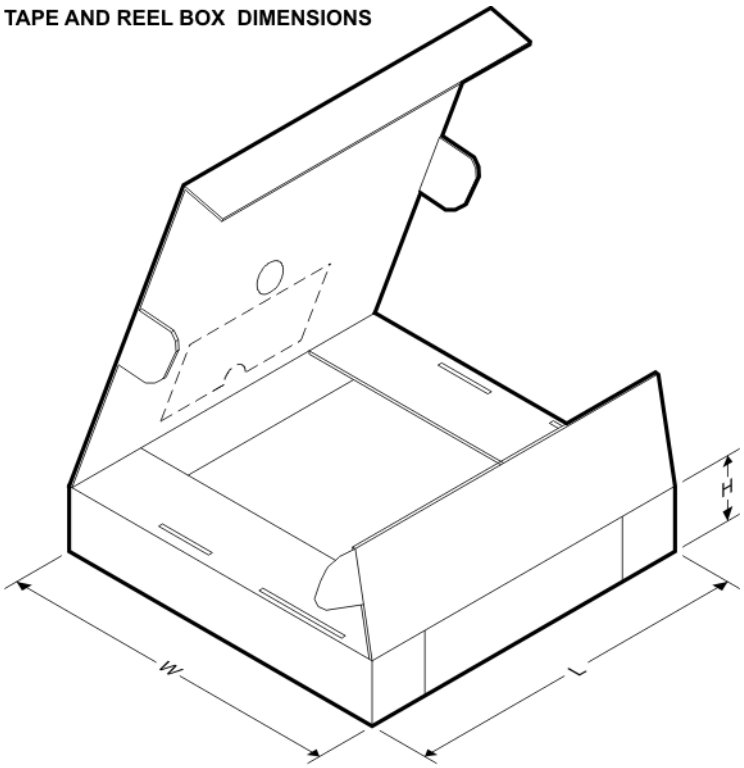
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61177ARGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

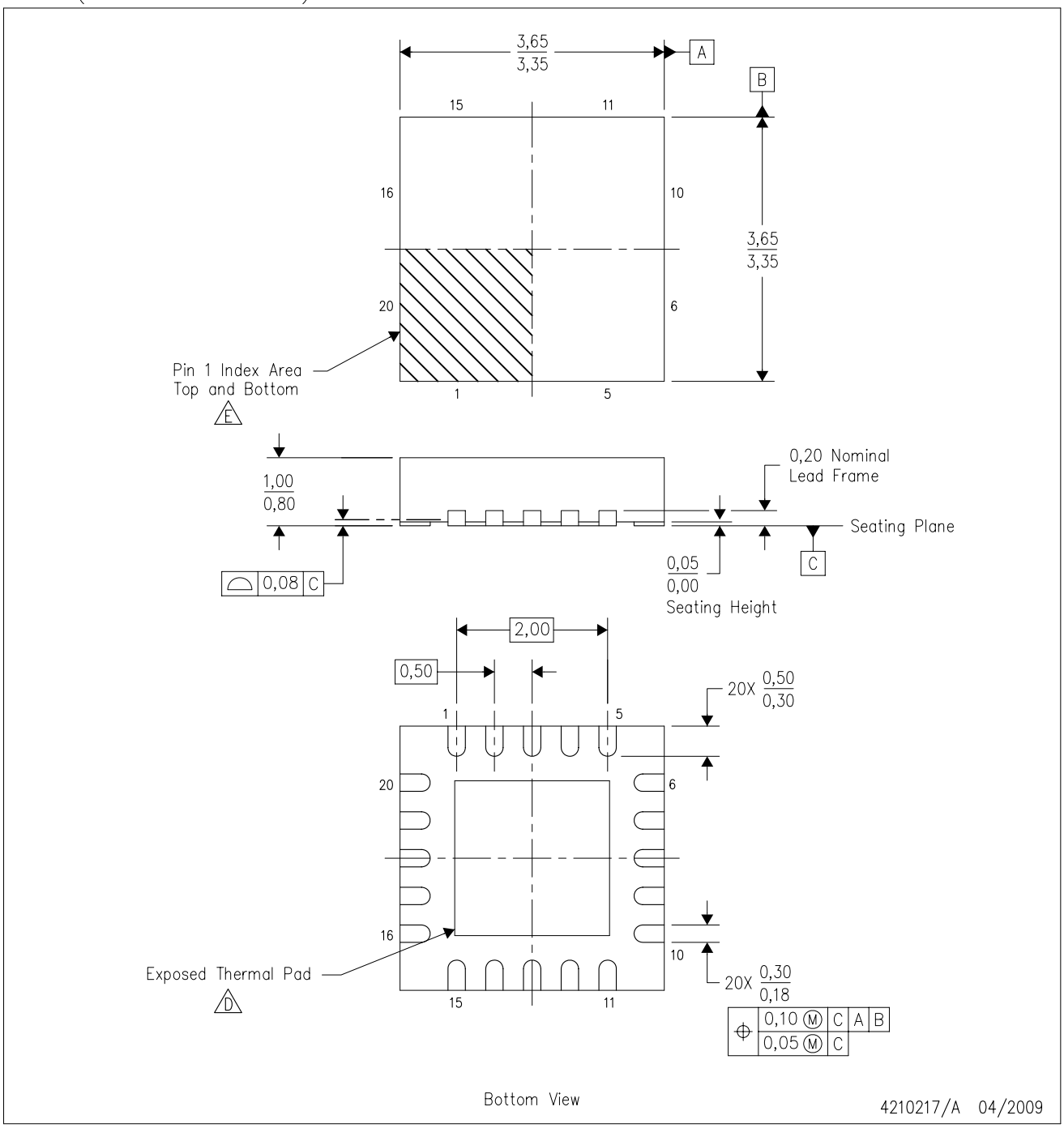
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61177ARGRR	VQFN	RGR	20	3000	367.0	367.0	35.0

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

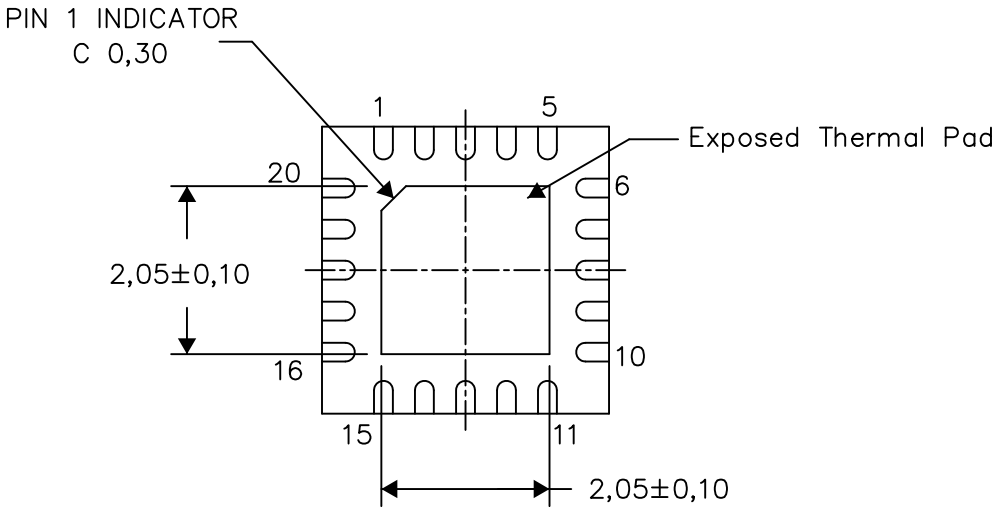
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



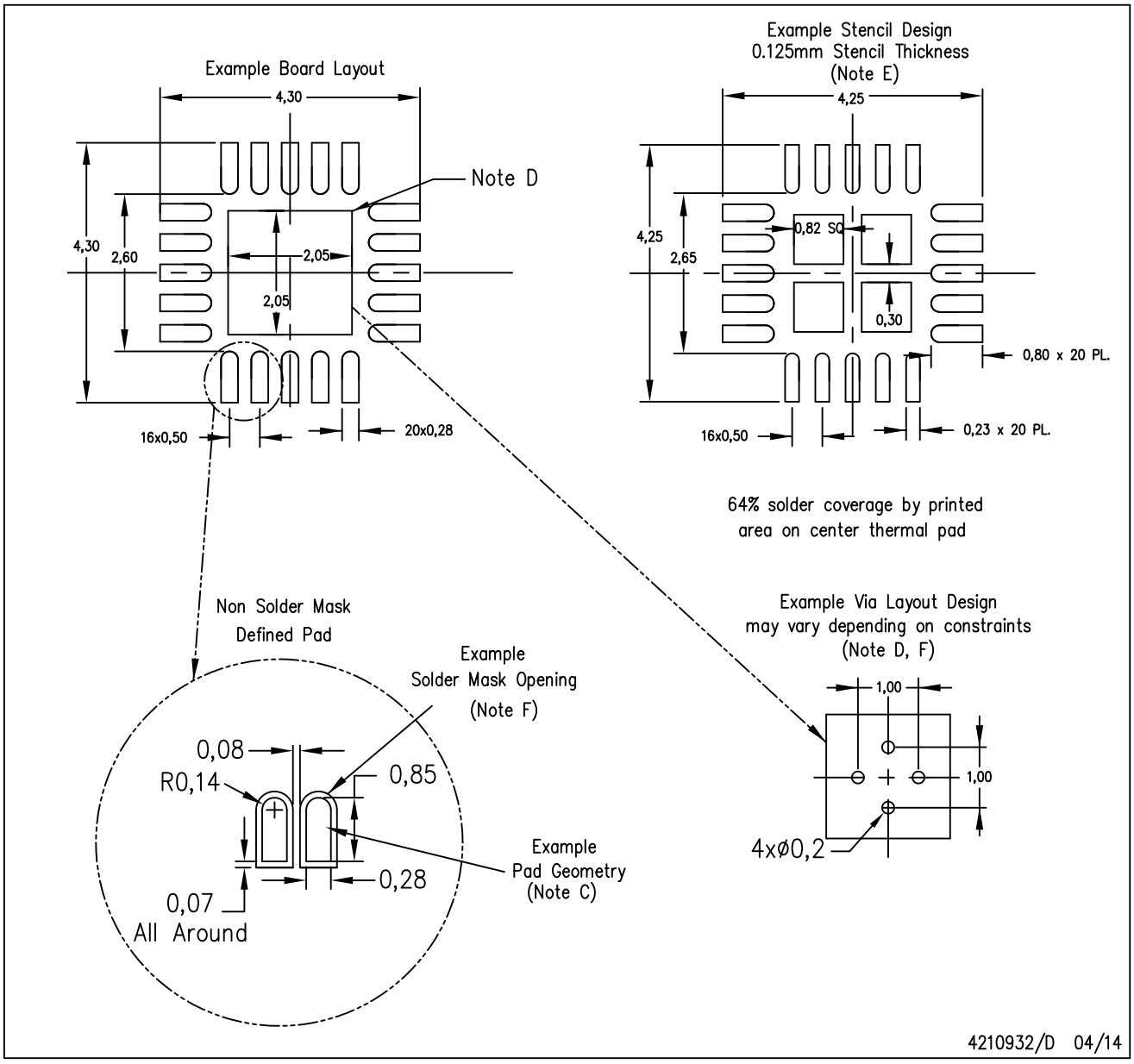
Bottom View

Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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