NXP Semiconductors
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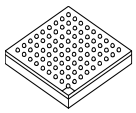
MCIMX6SxExxxxxB	**MCIMX6SxDxxxxxB**
MCIMX6SxExxxxxC	**MCIMX6SxDxxxxxC**
MCIMX6SxExxxxxD	**MCIMX6SxDxxxxxD**
MCIMX6UxExxxxxB	**MCIMX6UxDxxxxxB**
MCIMX6UxExxxxxC	**MCIMX6UxDxxxxxC**
MCIMX6UxExxxxxD	**MCIMX6UxDxxxxxD**

i.MX 6Solo/6DualLite Applications Processors for Consumer Products



Package Information
Plastic Package
BGA Case 2240 21 x 21 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 3

1 Introduction

The i.MX 6Solo/6DualLite processors represent the latest achievement in integrated multimedia-focused products offering high performance processing with lower cost, as well as optimization for low power consumption.

The processors feature advanced implementation of single/dual Arm® Cortex®-A9 core, which operates at speeds of up to 1 GHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. Each processor provides a 32/64-bit DDR3/DDR3L/LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth®, GPS, hard drive, displays, and camera sensors.

The i.MX 6Solo/6DualLite processors are specifically useful for applications such as:

- Web and multimedia tablets
- Web and multimedia tablets

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NXP Reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products

- Color eReaders
- IPTV
- Human Machine Interfaces (HMI)
- Portable medical
- IP phones
- Home energy management systems

The i.MX 6Solo/6DualLite applications processors feature:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS requirements of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), a programmable smart DMA (SDMA) controller, and an asynchronous sample rate converter.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller two CAN ports, ESAI audio interface, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, and PCIe-II).
- Eink Panel Display Controller—The processors integrate EPD controller that supports E-INK color and monochrome with up to 1650x2332 resolution and 5-bit grayscale (32-levels per color channel).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure

software downloads. The security features are discussed in detail in the *i.MX 6Solo/6DualLite Security Reference Manual* (IMX6DQ6SDLSRM).

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on the web page nxp.com/imx6series. If the desired part number is not listed in Table 1, go to nxp.com/imx6series or contact a NXP representative for details.

Table 1. Example Orderable Part Numbers

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade[1]	Temperature Grade	Package
MCIMX6U8DVM10AB	DualLite	With VPU, GPU, EPDC, MLB 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U8DVM10AC	DualLite	With VPU, GPU, EPDC, MLB 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U8DVM10AD	DualLite	With VPU, GPU, EPDC, MLB 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5DVM10AB	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5DVM10AC	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5DVM10AD	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6U5DVM10CB	DualLite	HDCP enabled with VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6U5DVM10CC	DualLite	HDCP enabled with VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6U5DVM10CD	DualLite	HDCP enabled with VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5EVM10AB	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5EVM10AC	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U5EVM10AD	DualLite	With VPU, GPU, MLB, no EPDC 2x Arm Cortex-A9 64-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

Table 1. Example Orderable Part Numbers (continued)

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade[1]	Temperature Grade	Package
MCIMX6S8DVM10AB	Solo	With VPU, GPU, MLB, EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S8DVM10AC	Solo	With VPU, GPU, MLB, EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S8DVM10AD	Solo	With VPU, GPU, MLB, EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AB	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AC	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AD	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CB	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CC	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CD	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AB	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AC	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AD	Solo	With VPU, GPU, MLB, no EPDC 1x Arm Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

[1] If a 24 MHz input clock is used (required for USB), then the maximum SoC speed is limited to 996 MHz.

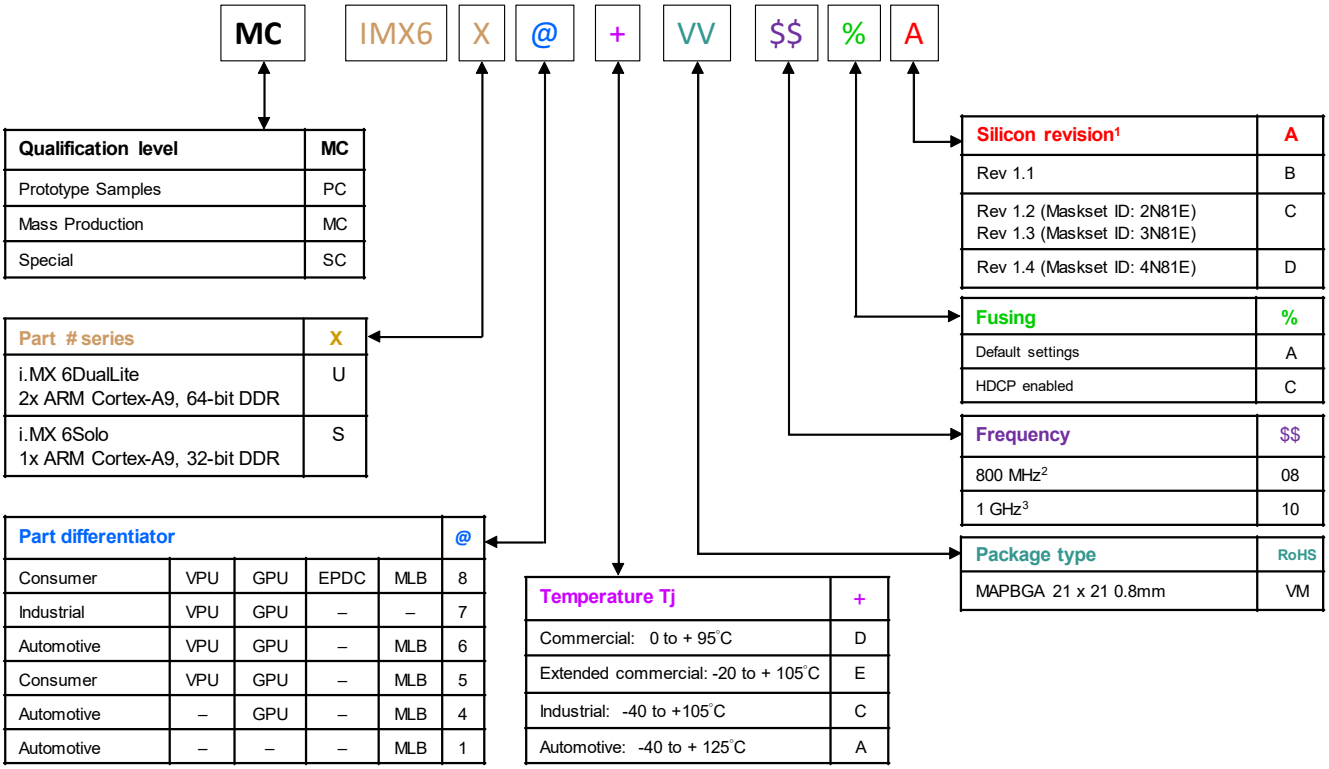
Figure 1 describes the part number nomenclature to identify the characteristics of a specific part number (for example, cores, frequency, temperature grade, fuse options, and silicon revision).

The primary characteristic that differentiates which data sheet applies to a specific part is the temperature grade (junction) field. The following list describes the correct data sheet to use for a specific part:

- The *i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors* data sheet (IMX6SDLAEC) covers parts listed with an “A (Automotive temp)”
- The *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* data sheet (IMX6SDLCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”

- The *i.MX 6Solo/6DualLite Applications Processors for Industrial Products* data sheet (IMX6SDLIEC) covers parts listed with "C (Industrial temp)"

For more information go to nxp.com/imx6series or contact a NXP representative for details.



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Solo and 6DualLite

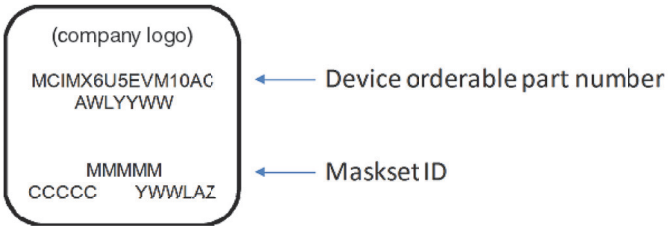


Figure 2. Example Part Marking

1.2 Features

The i.MX 6Solo/6DualLite processors are based on Arm Cortex-A9 MPCore Platform, which has the following features:

- The i.MX 6Solo supports single Arm Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual Arm Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:

  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The Arm Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache:
  - Used by one core in i.MX 6Solo
  - Shared by two cores in i.MX 6DualLite
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache), as per Table 8.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and DDR3L-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and DDR3L-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total of five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel (excluding EPDC).
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)

  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
  - EPDC, Color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
- Camera sensors:
  - Two parallel Camera ports (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 Serial port, supporting from 80 Mbps to 1 Gbps speed per data lane. The CSI-2 Receiver core can manage one clock lane and up to two data lanes. Each i.MX 6Solo/6DualLite processor has two lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed Phy
    - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block is capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I^2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Four eCSPI (Enhanced CSPI)
  - Four I^2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).

- — Four Pulse Width Modulators (PWM)
- — System JTAG Controller (SJC)
- — GPIO with interrupt capabilities
- — 8x8 Key Pad Port (KPP)
- — Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- — Two Controller Area Network (FlexCAN), 1 Mbps each
- — Two Watchdog timers (WDOG)
- — Audio MUX (AUDMUX)
- — MLB (MediaLB) provides interface to MOST Networks (MOST25, MOST50, MOST150) with the option of DTCP cipher accelerator

The i.MX 6Solo/6DualLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for Arm and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Solo/6DualLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Solo/6DualLite processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H
- GPU3Dv5—3D Graphics Processing Unit (OpenGL ES 2.0) version 5
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 16 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

1.3 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, etc.

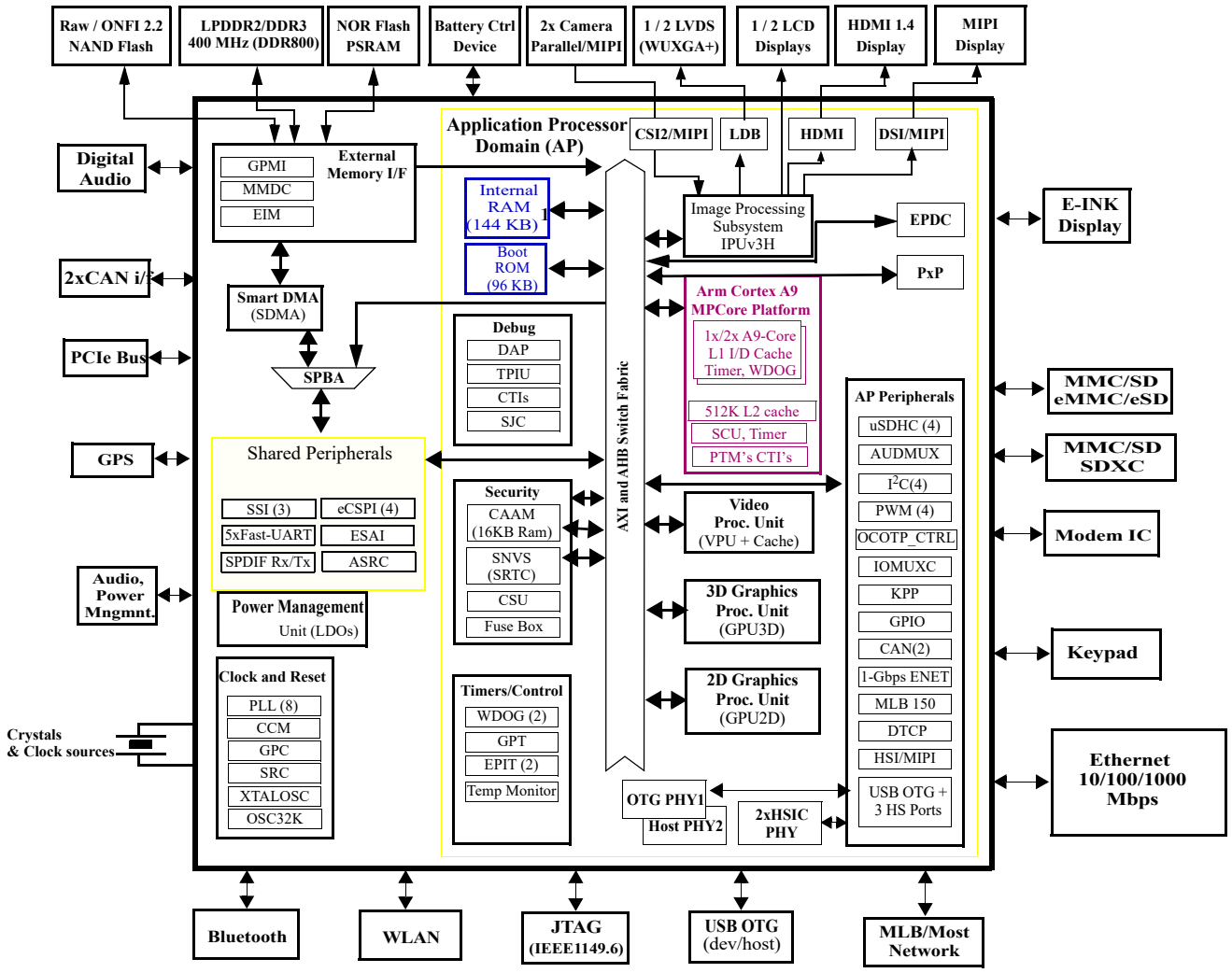
Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 3 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



[1] 144 KB RAM including 16 KB RAM inside the CAAM.

[2] For i.MX 6Solo, there is only one A9-core platform in the chip; for i.MX 6DualLite, there are two A9-core platforms.

Figure 3. i.MX 6Solo/6DualLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Solo/6DualLite processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Solo/6DualLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
APBH-DMA	NAND Flash and BCH ECC DMA controller	System Control Peripherals	DMA controller used for GPMI2 operation
Arm	Arm Platform	Arm	The Arm Core Platform includes 1x (Solo) Cortex-A9 core for i.MX 6Solo and 2x (Dual) Cortex-A9 cores for i.MX 6DualLite. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Solo/6DualLite processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details. **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes. It is available in both i.MX 6DualLite and i.MX 6Solo.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3 I^2C-4	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Solo/6DualLite processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Solo/6DualLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Solo/6DualLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-3 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Solo/6DualLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0. • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41 including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	Video Data Order Adapter (VDOA): used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.*MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for complete list of VPU’s decoding/encoding capabilities.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6Solo/6DualLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are provided in the *i.MX 6Solo/6DualLite Reference Manual* (IMX6SDLRM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N CLK2_P/CLK2_N	Two general purpose differential high speed clock Input/outputs are provided. Any or both of them could be used: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for PCIe, Video/Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals, for example it could be used as an output of the PCIe master clock (root complex use) See the i.MX 6Solo/6DualLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximum frequency range supported is 0...600 MHz. Alternatively one may use single ended signal to drive CLKx_P input. In this case corresponding CLKx_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLKx inputs/outputs could be disabled (if not used). If unused any or both of the CLKx_N/P pairs may remain unconnected.
XTALOSC_RTC_XTALI/ RTC_XTALO	If the user wishes to configure XTALOSC_RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between XTALOSC_RTC_XTALI and RTC_XTALO. Remember that the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTALOSC_RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTALOSC_RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTALOSC_RTC_XTALI the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock must not exceed VDD_SNVS_CAP level and the frequency must be <100 kHz under typical conditions.
XTALI/XTALO	• A 24.0 MHz crystal should be connected between XTALI and XTALO level and the frequency should be <32 MHz under typical conditions. See the Hardware Development Guide (IMX6DQ6SDLHDG), Design Checklist chapter, for details on crystal selection. • NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. • The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO remains unconnected. • The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. If this clock is used as a reference for USB and PCIe, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6Solo/6DualLite are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices).
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
NVCC_LVDS_2P5	The DDR pre-drivers share the NVCC_LVDS_2P5 ball with the LVDS interface. This ball can be shorted to VDD_HIGH_CAP on the circuit board.
VDD_FA FA_ANA	These signals are reserved for NXP manufacturing use only. User must tie both connections to GND.
GPANAIO	Analog output for NXP use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and must be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6Solo/6DualLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are not functional and must remain unconnected by the user.
SRC_POR_B	This cold reset negative logic input resets all modules and logic in the IC.
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for NXP factory use. This signal is internally connected to an on-chip pull-down device. This signal must either be tied to Vss or remain unconnected.
PCIE_REXT	The impedance calibration process requires connection of reference resistor 200 Ω 1% precision resistor on PCIE_REXT pad to ground.
CSI_REXT	MIPI CSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND
DSI_REXT	MIPI DSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 5 for a quick reference to the individual tables and sections.

Table 5. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 24
BGA Case 2240 Package Thermal Resistance	on page 25
Operating Ranges	on page 26
External Clock Sources	on page 28
Maximum Supply Currents	on page 29
Low Power Mode Supply Currents	on page 30
USB PHY Current Consumption	on page 32
PCIe 2.0 Power Consumption	on page 32

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 6 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6 shows the absolute maximum operating ratings.

Table 6. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.4	V
VDD_HIGH_IN supply voltage (LDO enabled)	VDD_HIGH_IN	-0.3	3.7	V
VDD_HIGH_CAP supply output voltage	VDD_HIGH_CAP	-0.3	2.85	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI and PCIe high PHY VPH supply voltage	HDMI_VPH PCIE_VPH	-0.3	2.85	V
HDMI and PCIe low PHY VP supply voltage	HDMI_VP PCIE_VP	-0.3	1.4	V
LVDS and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMII I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V
V_{in}/V_{out} input/output voltage range (non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.3 (See note 2)	V

Table 6. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
V_{in}/V_{out} input/output voltage range (DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.4 (See notes 1 & 2)	V
ESD immunity (HBM)	V_{esd_HBM}	—	2000	V
ESD immunity (CDM)	V_{esd_CDM}	—	500	V
Storage temperature range	$T_{storage}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 7 displays the thermal resistance data.

Table 7. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	38 23	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	30 20	°C/W °C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[1,5]	—	$R_{\theta JC}$	6	°C/W
Junction to Package Top[1,6]	Natural convection	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 8 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (*IMX6SDLRM*)*.

Table 8. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN	1.350[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.225 V minimum for operation up to 996 MHz.
		1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.25[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.125 V minimum for operation up to 396 MHz.
	VDD_SOC_IN	1.275[3,4]	—	1.5	V	VPU ≤ 328 MHz, VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) = 1.225 V[6] maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250	—	1.3	V	LDO bypassed for operation up to 996 MHz
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.125	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDD_SOC_IN	1.150[5]	—	1.21[6]	V	LDO bypassed for operation VPU ≤ 328 MHz
Standby/DSM mode	VDD_ARM_IN	0.9	—	1.3	V	Refer to Table 11, "Stop Mode Current and Power Consumption," on page 30.
	VDD_SOC_IN	0.9	—	1.225[6]	V	—
VDD_HIGH internal regulator	VDD_HIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[7]	2.9	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
Supply for RGMII I/O power group[8]	NVCC_RGMII	1.15	—	2.625	V	1.15 V–1.30 V in HSIC 1.2 V mode 1.43 V–1.58 V in RGMII 1.5 V mode 1.70 V–1.90 V in RGMII 1.8 V mode 2.25 V–2.625 V in RGMII 2.5 V mode

Table 8. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supply voltages[8]	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	—
	NVCC_LVDS_2P5[9] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.21	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.21	V	—
Junction temperature Extended commercial	T_J	-20	—	105	°C	See *i.MX 6Solo/6DualLite Product Lifetime Usage Estimates Application Note*, AN4725, for information on product lifetime for this processor.
Junction temperature Standard commercial	T_J	0	—	95	°C	See *i.MX 6Solo/6DualLite Product Lifetime Usage Estimates Application Note*, AN4725, for information on product lifetime for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 VDD_ARM_IN and VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

4 In LDO enabled mode, the internal LDO output set points must be configured such that the:

- VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.
- VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

5 In LDO bypassed mode, the external power supply must ensure that VDD_ARM_IN does not exceed VDD_SOC_IN by more than 100 mV. The VDD_ARM_IN supply voltage can be lower than the VDD_SOC_IN supply voltage. The minimum voltages shown in this table must be maintained.

6 When using VDD_SOC_CAP to supply the PCIE_VP and PCIE_VPTX, the maximum setting is 1.175V. If VDD_SOC_CAP requires setting to 1.2V or higher, the PCIE_VP and PCIE_VPTX must use an external supply to guarantee not to exceed the 1.21V maximum operating voltage.

7 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

8 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a pull-up or pull-down resistor applied to limit any non-connected gate current.

9 This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used.

4.1.4 External Clock Sources

Each i.MX 6Solo/6DualLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 9 shows the interface frequency requirements.

Table 9. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 9 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For XTALOSC_RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is used

The choice of a clock source must be based on real-time clock use and precision timeout.

4.1.5 Maximum Supply Currents

The Power Virus numbers shown in Table 10 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 10, however a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 10. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	i.MX 6DualLite: 996 MHz Arm clock based on Power Virus operation	2200	mA
	i.MX 6Solo: 996 MHz Arm clock based on Power Virus operation	1320	mA
VDD_SOC_IN	996 MHz Arm clock	1260	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	275[2]	µA
USB_OTG_VBUS/ USB_H1_VBUS (LDO 3P0)	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	—
NVCC_ENET	N=10	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_GPIO	N=24	Use maximum IO equation[5]	—
NVCC_CSI	N=20	Use maximum IO equation[5]	—
NVCC_EIM	N=53	Use maximum IO equation[5]	—
NVCC_JTAG	N=6	Use maximum IO equation[5]	—
NVCC_RGMII	N=6	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_SD2	N=6	Use maximum IO equation[5]	—
NVCC_SD3	N=11	Use maximum IO equation[5]	—
NVCC_NANDF	N=26	Use maximum IO equation[5]	—

Table 10. Maximum Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_LVDS2P5[6]	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.	—
MISC			
DDR_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown in Table 10. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

6 NVCC_LVDS2P5 is supplied by VDD_HIGH_CAP (by external connection) so the maximum supply current is included in the current shown for VDD_HIGH_IN. The maximum supply current for NVCC_LVDS2P5 has not been characterized separately.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
WAIT	• Arm, SoC, and PU LDOs are set to 1.225 • HIGH LDO set to 2.5 V • Clocks are gated. • DDR is in self refresh. • PLLs are active in bypass (24MHz) • Supply Voltages remain ON	VDD_ARM_IN (1.4V)	4.5	mA
		VDD_SOC_IN (1.4V)	23	
		VDD_HIGH_IN (3.0V)	13.5	
		Total	79	mW

Table 11. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Units
STOP_ON	• Arm LDO set to 0.9V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh.	VDD_ARM_IN (1.4V)	4	mA
		VDD_SOC_IN (1.4V)	22	
		VDD_HIGH_IN (3.0V)	8.5	
		Total	61.9	mW
STOP_OFF	• Arm LDO set to 0.9V • SoC LDO set to: 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4V)	4	mA
		VDD_SOC_IN (1.4V)	13.5	
		VDD_HIGH_IN (3.0V)	7.5	
		Total	47	mW
STANDBY	• Arm and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9V)	0.1	mA
		VDD_SOC_IN (0.9V)	5	
		VDD_HIGH_IN (3.0V)	5	
		Total	19.6	mW
Deep Sleep Mode (DSM)	• Arm and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9V)	0.1	mA
		VDD_SOC_IN (0.9V)	2	
		VDD_HIGH_IN (3.0V)	0.5	
		Total	3.4	mW
SNVS only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_VBUS valid detectors in typical condition. Table 12 shows the USB interface current consumption in power down mode.

Table 12. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 13 provides PCIe PHY currents under certain Tx operating modes.

Table 13. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.9 HDMI Power Consumption

Table 14 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 14. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The restrictions that follow must be observed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- The SRC_POR_B signal controls the processor POR and must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

NOTE

When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies must be powered or grounded. The input and output supplies for the remaining ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals must not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have three basic modes:

- Bypass. The regulation FET is switched fully on passing the external voltage, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 8 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, LVDS Phy, HDMI Phy, MIPI Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual (IMX6SDLRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 8 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB Phy, LVDS Phy, HDMI Phy, MIPI Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator

is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB_VBUS supply, when both are present. If only one of the USB_VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.4 PLL’s Electrical Characteristics

4.4.1 Audio/Video PLL’s Electrical Parameters

Table 15. Audio/Video PLL’s Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 16. 528 MHz PLL’s Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output

Table 16. 528 MHz PLL's Electrical Parameters (continued)

Parameter	Value
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 17. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 18. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 19. MLB PLL's Electrical Parameters

Parameter	Value
Lock time	<1 ms

4.4.6 Arm PLL

Table 20. Arm PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from VDD_HIGH_IN/VDD_SNVS_IN.

Table 21. OSC32K Main Characteristics

Characteristic	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K will work as well.
Current consumption	—	4 μA	—	The 4 μA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μA when ring oscillator is inactive, 20 μA when the ring oscillator is running. Another 1.5 μA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μA on vdd_rtc when the ring oscillator is not running.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

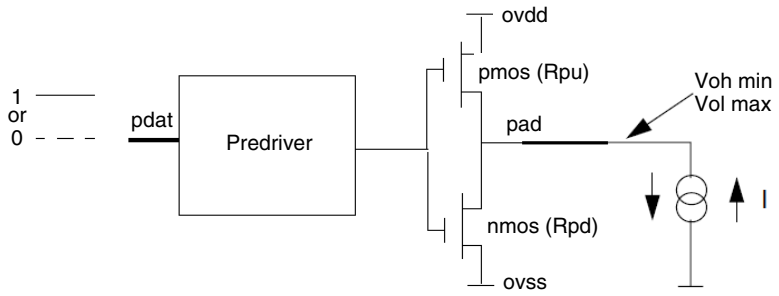


Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 22 shows the DC parameters for the clock inputs.

Table 22. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	—	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1[1]	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI_STARTUP}$	Power-on startup for 0.15msec with a driven 24 MHz clock at 1.1 V.[2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI. The 24 MHz oscillator cell is powered from NVCC_PLL_OUT.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 23 shows DC parameters for GPIO pads. The parameters in Table 23 are guaranteed per the operating ranges in Table 8, unless otherwise noted.

Table 23. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (DSE=001,010) Ioh= -1mA (DSE=011,100,101,110,111)	OVDD - 0.15	—	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (DSE=001,010) Iol= 1mA (DSE=011,100,101,110,111)	—	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7 × OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3 × OVDD	V
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=3.3V	VHYS_HighVDD	OVDD=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5 × OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5 × OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	uA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	uA

Table 23. GPIO DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD	—	1	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	uA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	uA
Keeper Circuit Resistance	R_Keeper	VI = 0.3 × OVDD, VI = 0.7 × OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 24. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9 × OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1 × OVDD	V
Input Reference Voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	V
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	
Differential Input Logic Low	Vil_diff	—	Note[3]	-0.26	
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	µA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

[3] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L Mode I/O DC Parameters

The parameters in Table 25 are guaranteed per the operating ranges in Table 8, unless otherwise noted. For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC).

Table 25. DDR3/DDR3L I/O DC Electrical Characteristics[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for DSE=001)	0.8 × OVDD[2]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for DSE=001)	—	0.2 × OVDD	V
High-level output voltage	VOH	Ioh= -1mA Voh (for all except DSE=001)	0.8 × OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except DSE=001)	—	0.2 × OVDD	V
Input Reference Voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	V
DC High-Level input voltage	Vih_DC	—	Vref[3]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	See Note[4]	V
Differential Input Logic Low	Vil_diff	—	See Note[3]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49 × OVDD	0.51 × OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	µA

[1] Note that the JEDEC DDR3 specification (JESD79_3D) supersedes any specification in this document.

[2] OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

[3] Vref – DDR3/DDR3L external reference voltage.

[4] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.4 RGMII I/O 2.5V I/O DC Electrical Parameters

The RGMII interface complies with the RGMII standard version 1.3. The parameters in Table 26 are guaranteed per the operating ranges in Table 8, unless otherwise noted.

Table 26. RGMII I/O 1.8V and 2.5V mode DC Electrical Characteristics[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level Output Voltage[1]	V_{OH}	Ioh= -0.1mA (DSE=001,010) Ioh= -1mA (DSE=011,100,101,110,111)	OVDD-0.15	—	V
Low-level Output Voltage[1]	V_{OL}	Iol= 0.1mA (DSE=001,010) Iol= 1mA (DSE=011,100,101,110,111)	—	0.15	V
Input Reference Voltage	V_{ref}	—	0.49 × OVDD	0.51 × OVDD	V
High-Level Input Voltage[2 3]	V_{IH}	—	0.7 × OVDD	OVDD	V
Low-Level Input Voltage[2 3]	V_{IL}	—	0	0.3 × OVDD	V
Input Hysteresis (OVDD=1.8V)	$V_{HYS_HighVDD}$	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=2.5V)	$V_{HYS_HighVDD}$	OVDD=2.5V	250	—	mV
Schmitt Trigger VT+[3 4]	V_{TH}^{+}	—	0.5 × OVDD	—	mV
Schmitt Trigger VT-[3 4]	V_{TH}^{-}	—	—	0.5 × OVDD	mV
Pull-up Resistor (22 kΩ PU)	R_{PU_22K}	Vin=0V	—	212	µA
Pull-up Resistor (22 kΩ PU)	R_{PU_22K}	Vin=OVDD	-—	1	µA
Pull-up Resistor (47 kΩ PU)	R_{PU_47K}	Vin=0V	—	100	µA
Pull-up Resistor (47 kΩ PU)	R_{PU_47K}	Vin=OVDD	—	1	µA
Pull-up Resistor (100 kΩ PU)	R_{PU_100K}	Vin=0V	—	48	µA
Pull-up Resistor (100 kΩ PU)	R_{PU_100K}	Vin=OVDD	—	1	µA
Pull-down Resistor (100 kΩ PD)	R_{PD_100K}	Vin=OVDD	—	48	µA
Pull-down Resistor (100 kΩ PD)	R_{PD_100K}	Vin=0V	—	1	µA
Keeper Circuit Resistance	R_{keep}		105	165	kΩ
Input Current (no pull-up/down)	I_{in}	VI = 0, VI = OVDD	-2.9	2.9	µA

1 Input Mode Selection "SW_PAD_CTL_GRP_DDR_TYPE_RGMII"='10' (1.8V Mode) "SW_PAD_CTL_GRP_DDR_TYPE_RGMII"='11' (2.5V Mode).

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled (register IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC[HYS]= 0).

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.6.6 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, "MediaLB 6-pin interface Electrical Characteristics" for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo	—	1.6	—	kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

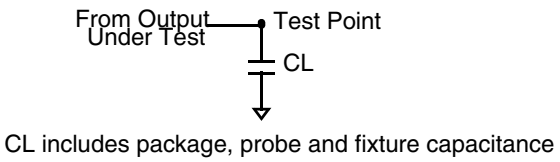


Figure 5. Load Circuit for Output

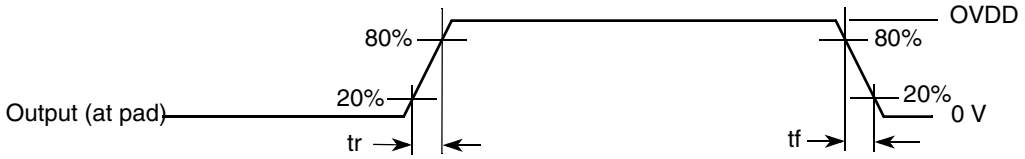


Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

[1] Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

[2] Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

[3] The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3, 4]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

[1] Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

[2] Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

[3] The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

[4] Extended range for Vix is only allowed for the clock and when the single-ended clock input signals CK and CK# are:
- monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 ±250 mV, and
- the differential slew rate of CK - CK# is larger than 3 V/ns

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

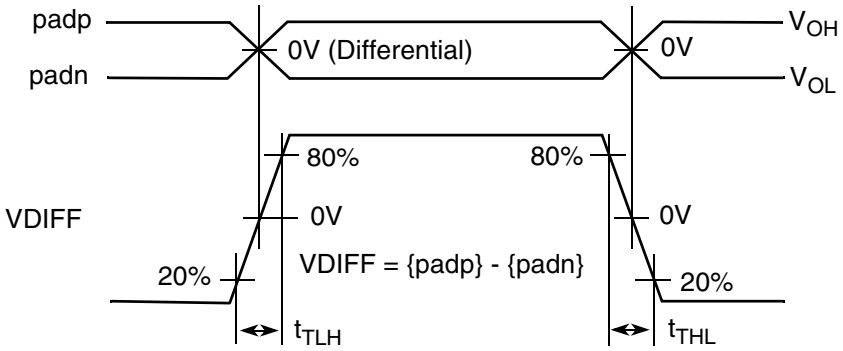


Figure 7. Differential LVDS Driver Transition Time Waveform

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 $t_{SKD} = | t_{PHLD} - t_{PLHD} |$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in Figure 8.

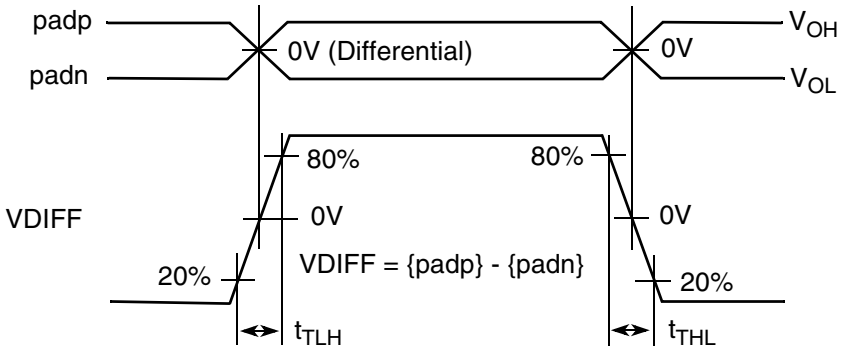


Figure 8. Differential MLB Driver Transition Time Waveform

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one ipp_clk_in* (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 9.

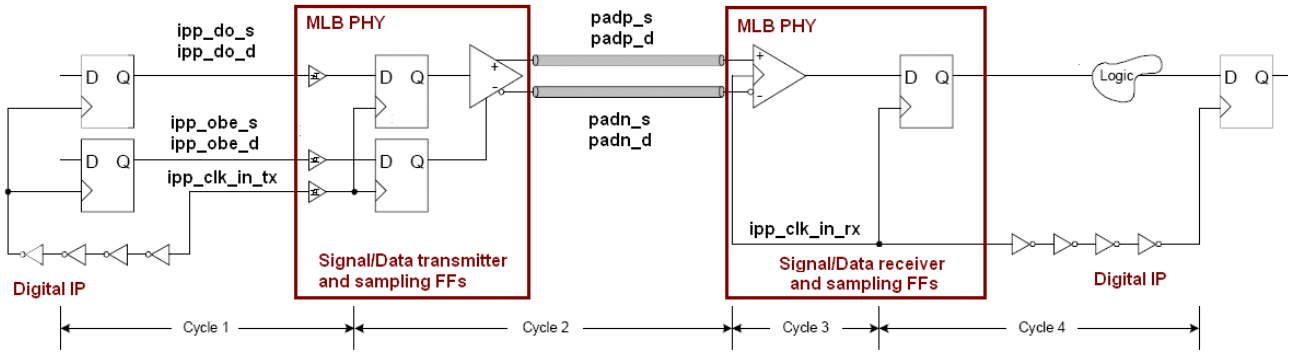


Figure 9. MLB 6-Pin Pipeline Diagram

Table 34 shows the AC parameters for MLB I/O.

4.8 Output Buffer Impedance Parameters

Table 34. I/O AC Parameters of MLB PHY

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 50 Ω between padp and padn	—	—	0.1	ns
Transition Low to High Time[2]	t_{TLH}		—	—	1	
Transition High to Low Time	t_{THL}		—	—	1	
MLB external clock Operating Frequency	fclk_ext	—	—	—	102.4	MHz
MLB PLL clock Operating Frequency	fclk_pll	—	—	—	307.2	MHz

1 $t_{SKD} = | t_{PHLD} - t_{PLHD} |$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

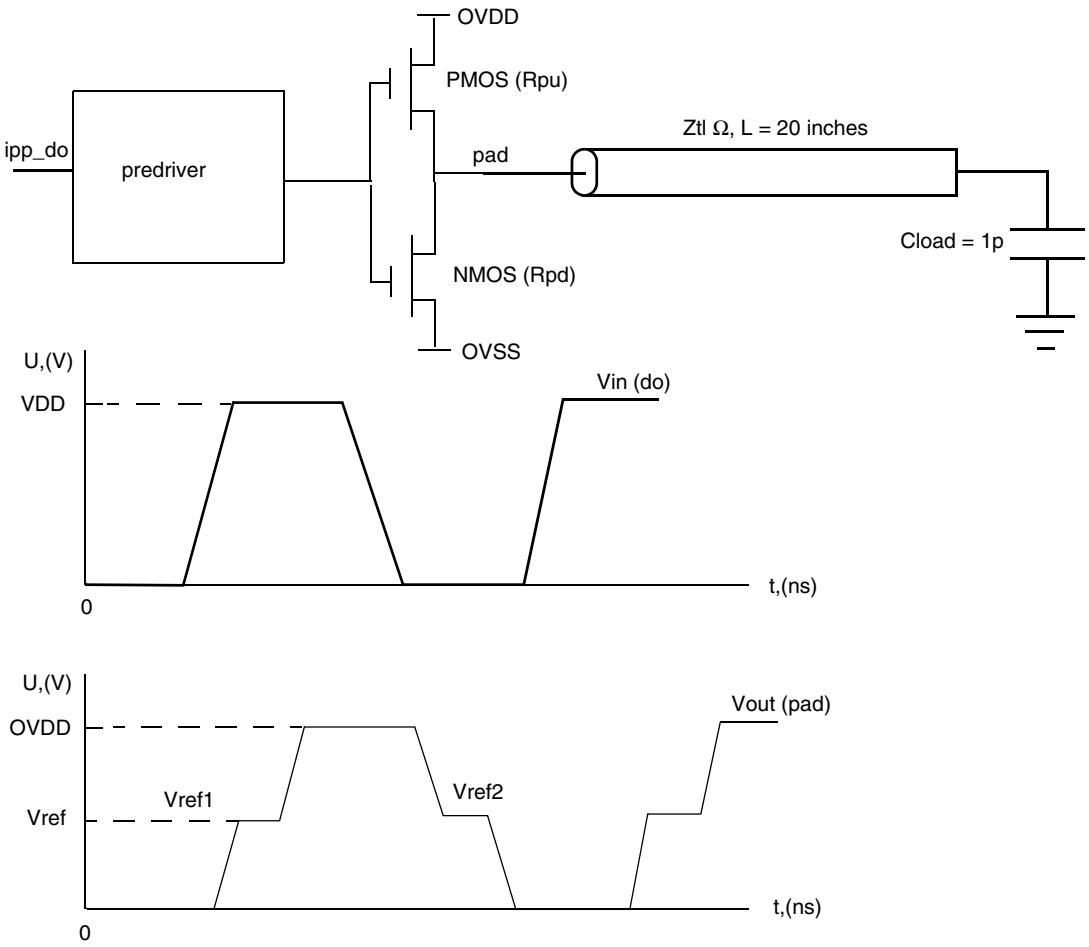
2 Measurement levels are 20-80% from output voltage.

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 10).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 10. Impedance Matching Load for Measurement

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC).

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

4.8.4 MLB I/O Differential Output Impedance

Table 38 shows MLB I/O differential output impedance of the i.MX 6Solo/6DualLite processors.

Table 38. MLB I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Zo	—	1.6	—	—	kΩ

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 11 shows the reset timing and Table 39 lists the timing parameters.

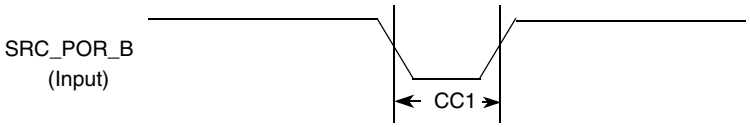


Figure 11. Reset Timing Diagram

Table 39. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 12 shows the WDOG reset timing and Table 40 lists the timing parameters.

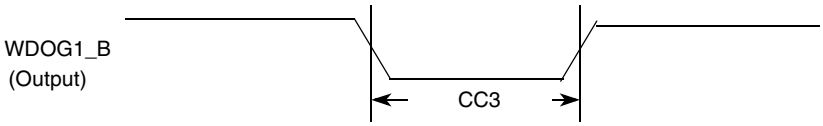


Figure 12. WDOG1_B Timing Diagram

Table 40. WDOG1_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	XTALOSC_RTC_XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Two system clocks are used with the EIM:

- ACLK_EIM_SLOW_CLK_ROOT is used to clock the EIM module.
  The maximum frequency for CLK_EIM_SLOW_CLK_ROOT is 132 MHz.
- ACLK_EXSC is also used when the EIM is in synchronous mode.
  The maximum frequency for ACLK_EXSC is 104 MHz.

Timing parameters in this section that are given as a function of register settings.

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 41 provides EIM interface pads allocation in different modes.

Table 41. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 13, Figure 14, and Table 42 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

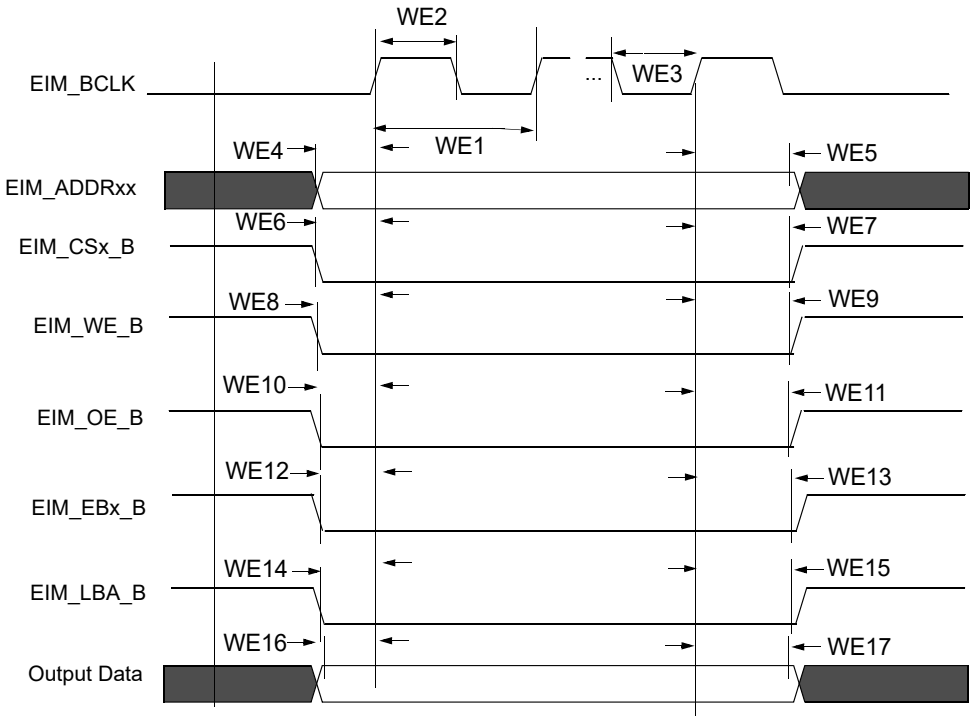


Figure 13. EIM Outputs Timing Diagram

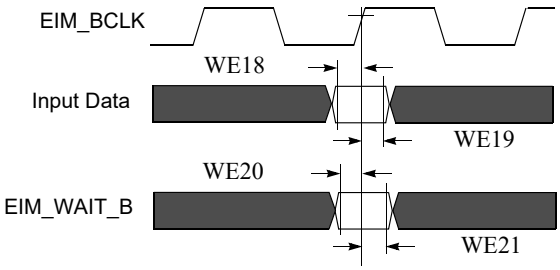


Figure 14. EIM Inputs Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 42. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

[1] t is the maximum EIM logic (ACLK_EXSC) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 104 MHz.

—Variable latency for read only is 104 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz ACLK_EXSC, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 15 to Figure 18 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

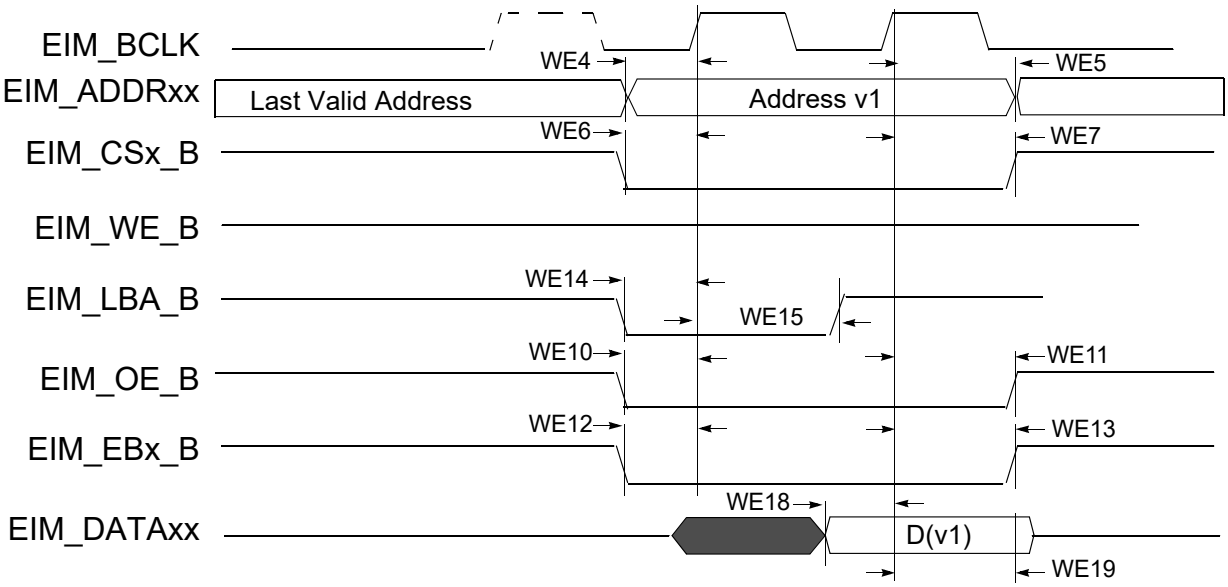


Figure 15. Synchronous Memory Read Access, WSC=1

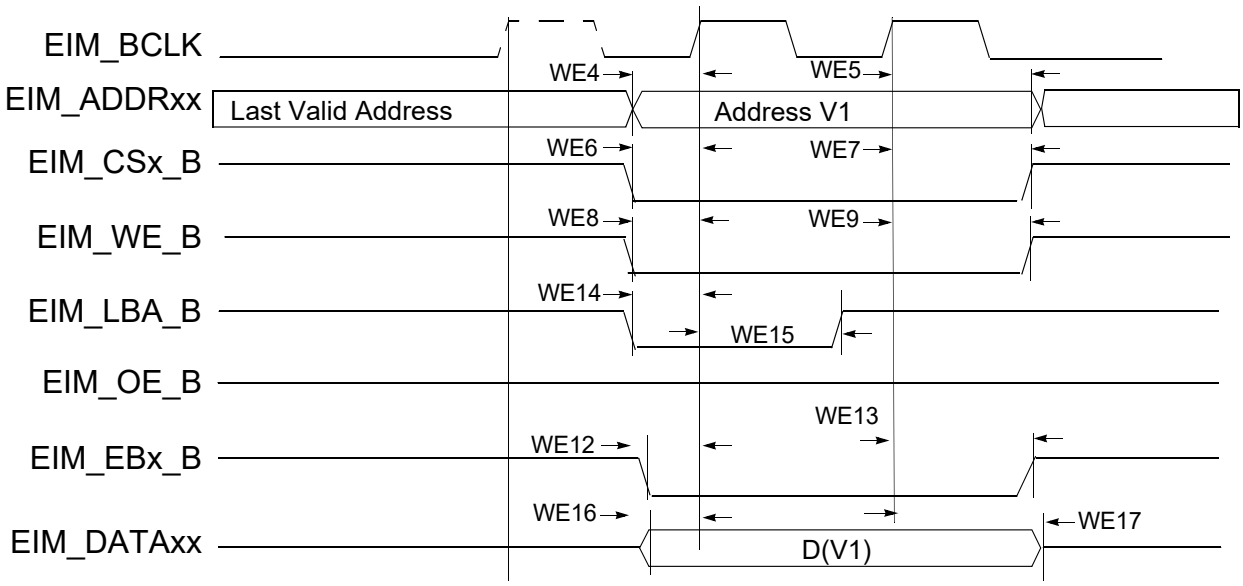


Figure 16. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

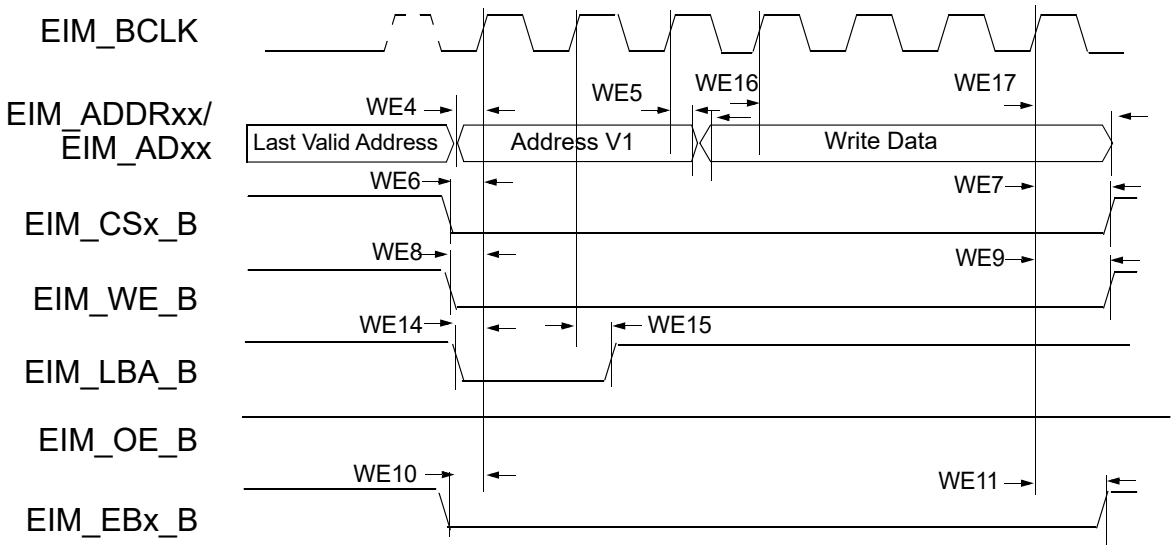


Figure 17. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

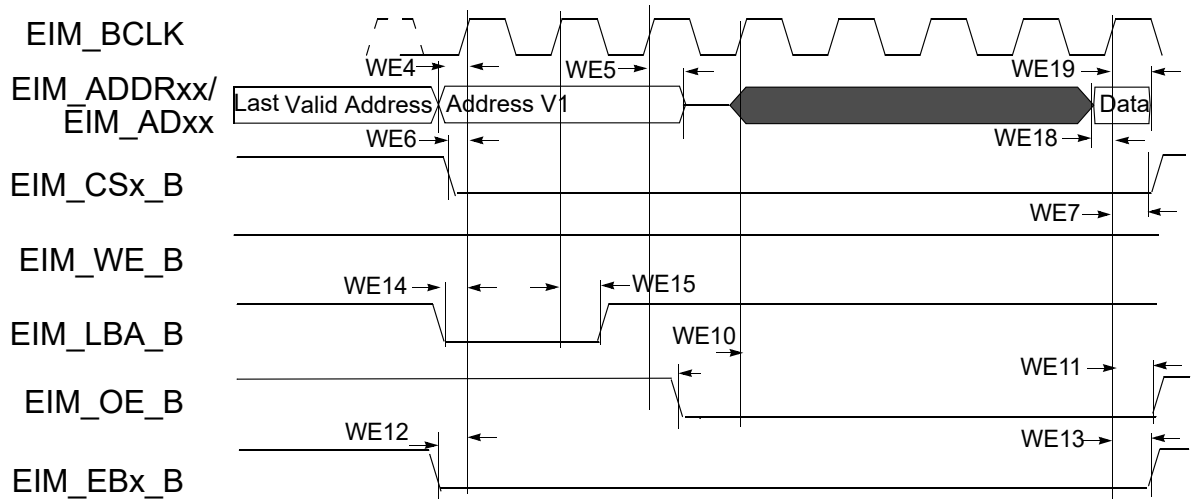


Figure 18. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 19 through Figure 23, and Table 43 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 19 through Figure 22 as RWSC, OEN and CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

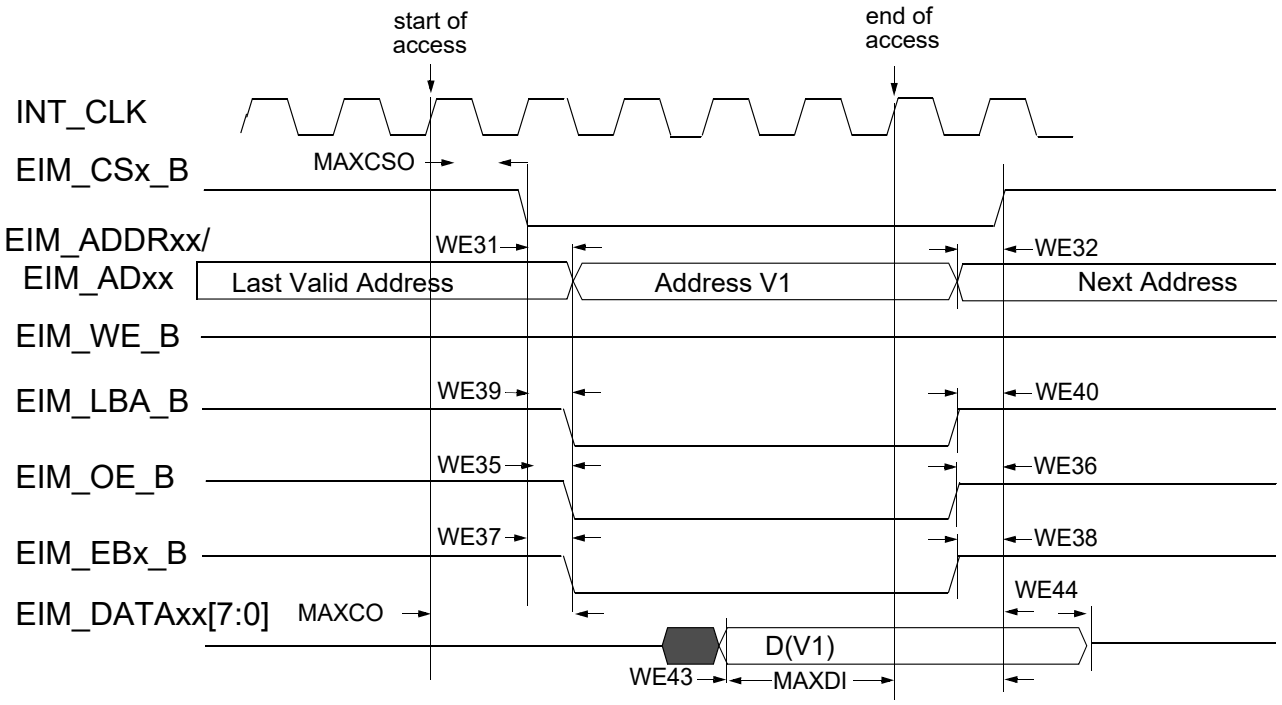


Figure 19. Asynchronous Memory Read Access (RWSC = 5)

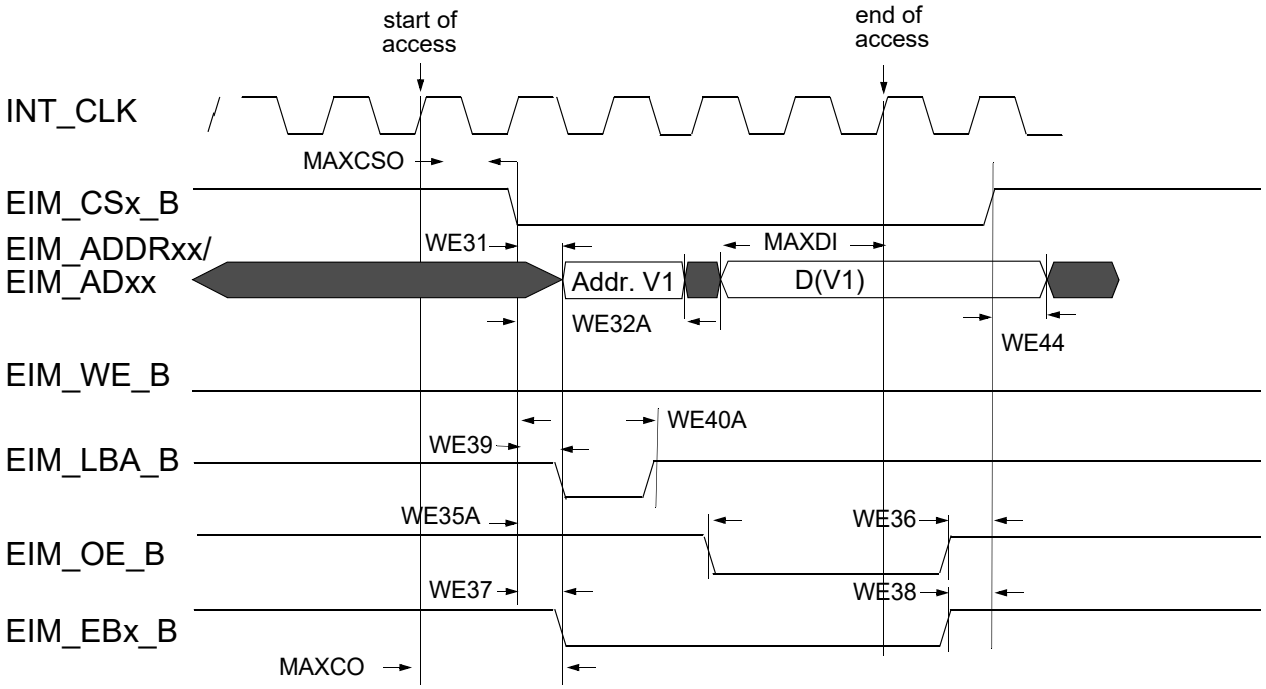


Figure 20. Asynchronous A/D Muxed Read Access (RWSC = 5)

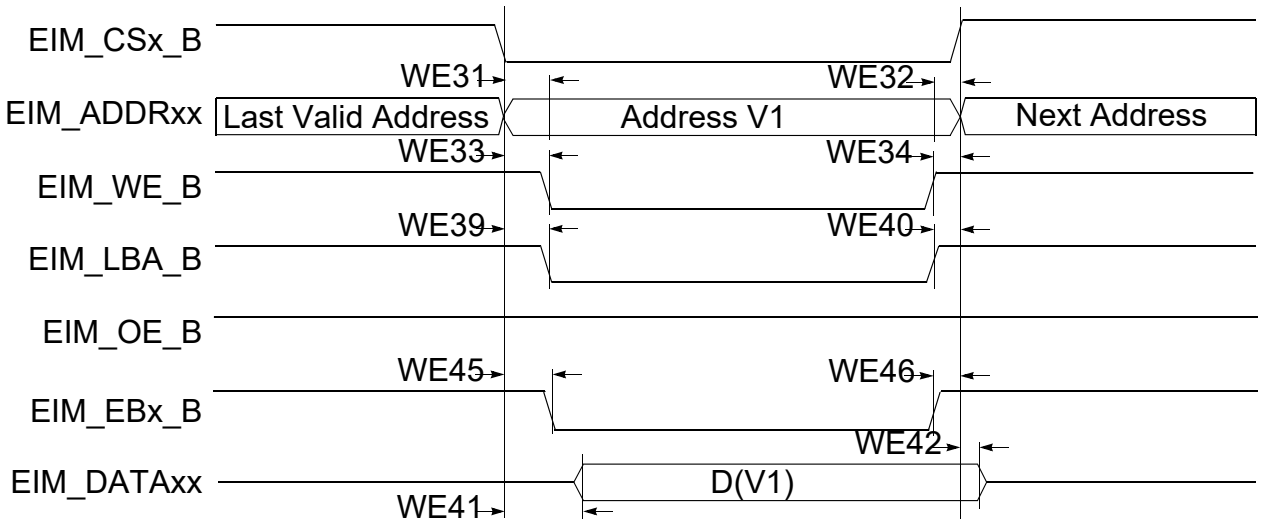


Figure 21. Asynchronous Memory Write Access

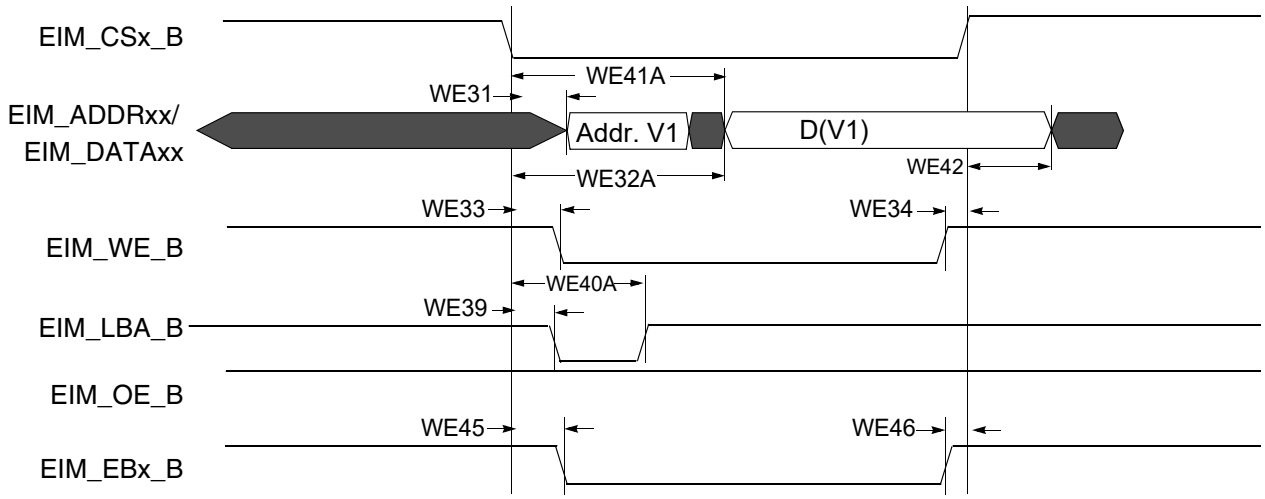


Figure 22. Asynchronous A/D Muxed Write Access

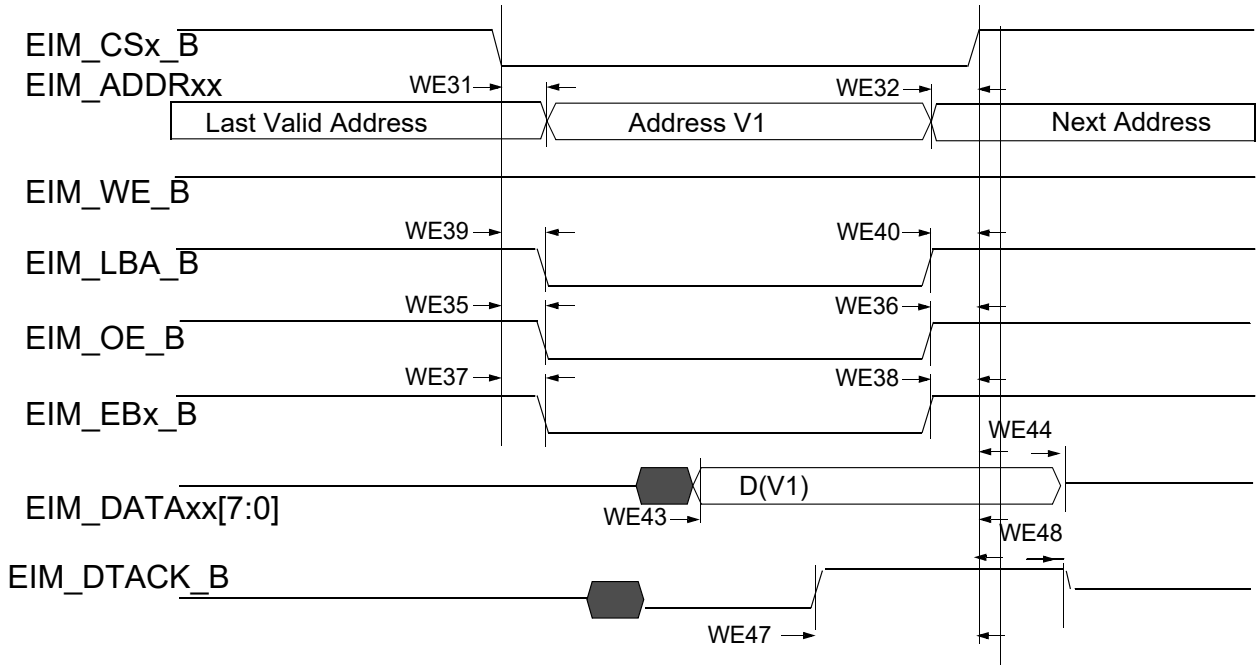


Figure 23. DTACK Mode Read Access (DAP=0)

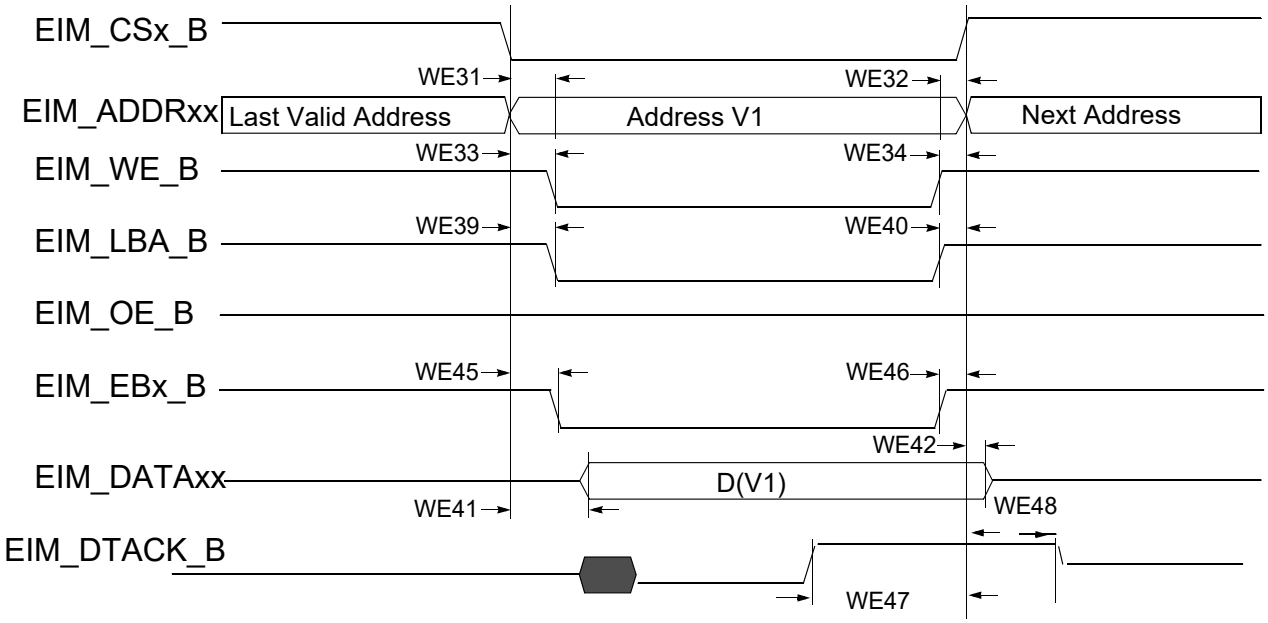


Figure 24. DTACK Mode Write Access (DAP=0)

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to EIM_CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A (muxed A/D	EIM_CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+ADH +1-RCSA)	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal FF	5	—	—	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal FF + 2 cycles for synchronization	10	—	—	—

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.
2 In this table, CSA means WCSA when write operation or RCSA when read operation.
3 In this table, CSN means WCSN when write operation or RCSN when read operation.
4 t is ACLK_EIM_SLOW_CLK_ROOT cycle time.
5 In this table, ADVN means WADVN when write operation or RADVN when read operation.
6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.9.4.1 MMDC Compatibility with JEDEC-compliant SDRAMs

The i.MX 6Solo/6DualLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

4.9.4.2 MMDC Supported DDR3/DDR3L/LPDDR2 Configurations

Table 44 and Table 45 show the supported DDR3/DDR3L/LPDDR2 configurations.

Table 44. i.MX 6Solo Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16/32-bit	16/32-bit	16/32-bit
Channel	Single	Single	Single
Chip selects	2	2	2

Table 45. i.MX 6DualLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2 (Dual channel)	LPDDR2 (Single channel)	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz	400 MHz
Bus width	32-bit per channel	16/32-bit	16/32/64-bit	16/32/64-bit
Channel	Dual	Single	Single	Single
Chip selects	2 per channel	2	2	2

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 25 through Figure 28 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 46 describes the timing parameters (NF1–NF17) that are shown in the figures.

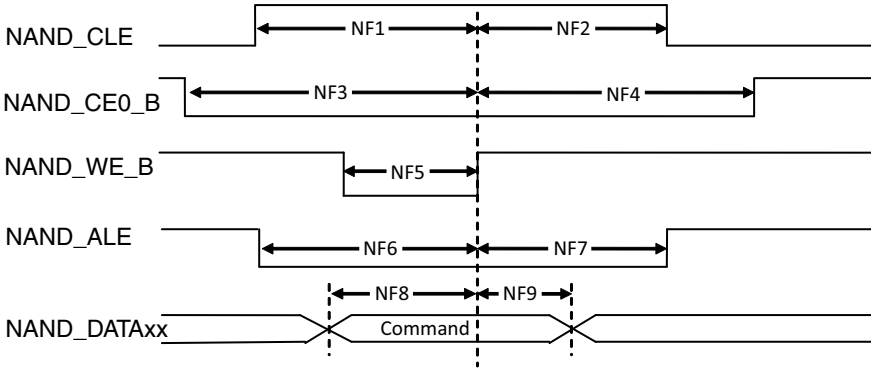


Figure 25. Command Latch Cycle Timing Diagram

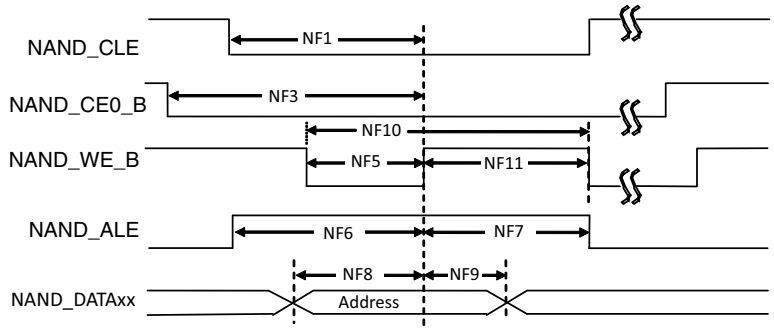


Figure 26. Address Latch Cycle Timing Diagram

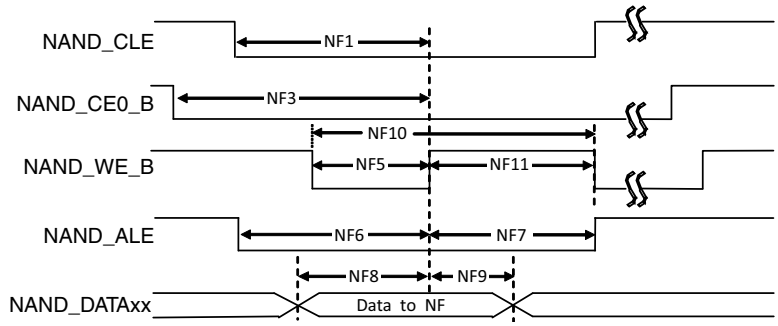


Figure 27. Write Data Latch Cycle Timing Diagram

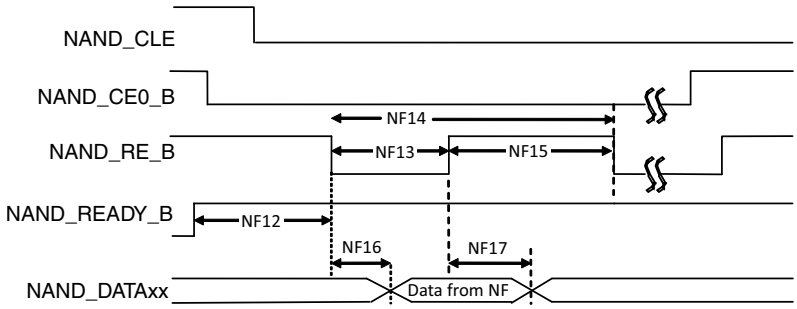


Figure 28. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

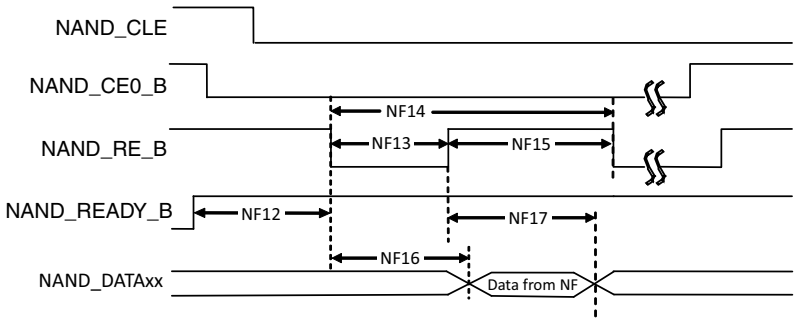


Figure 29. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 46. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see [3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see [2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see [2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see [2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see [2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see [2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 28), NF16/NF17 are different from the definition in non-EDO mode (Figure 27). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 30 to Figure 32 show the write and read timing of Source Synchronous Mode.

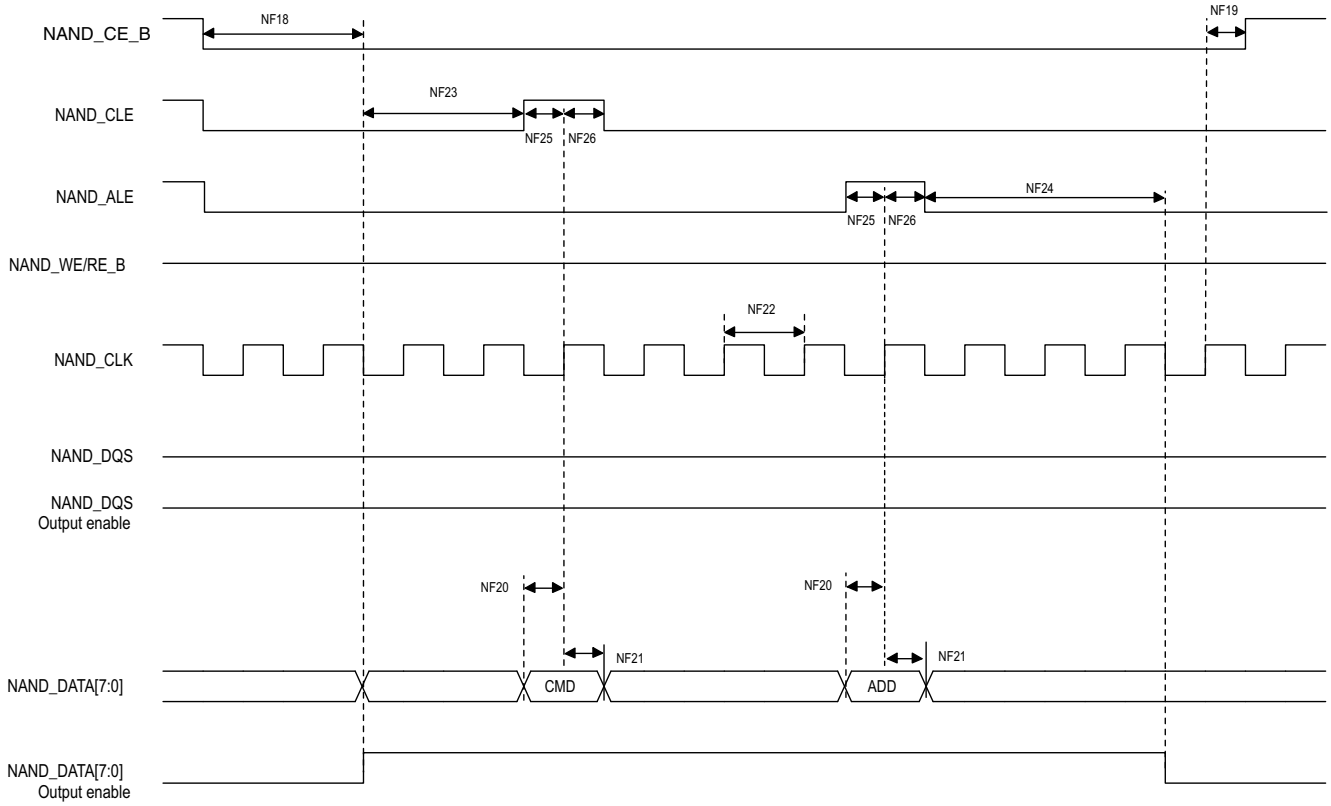


Figure 30. Source Synchronous Mode Command and Address Timing Diagram

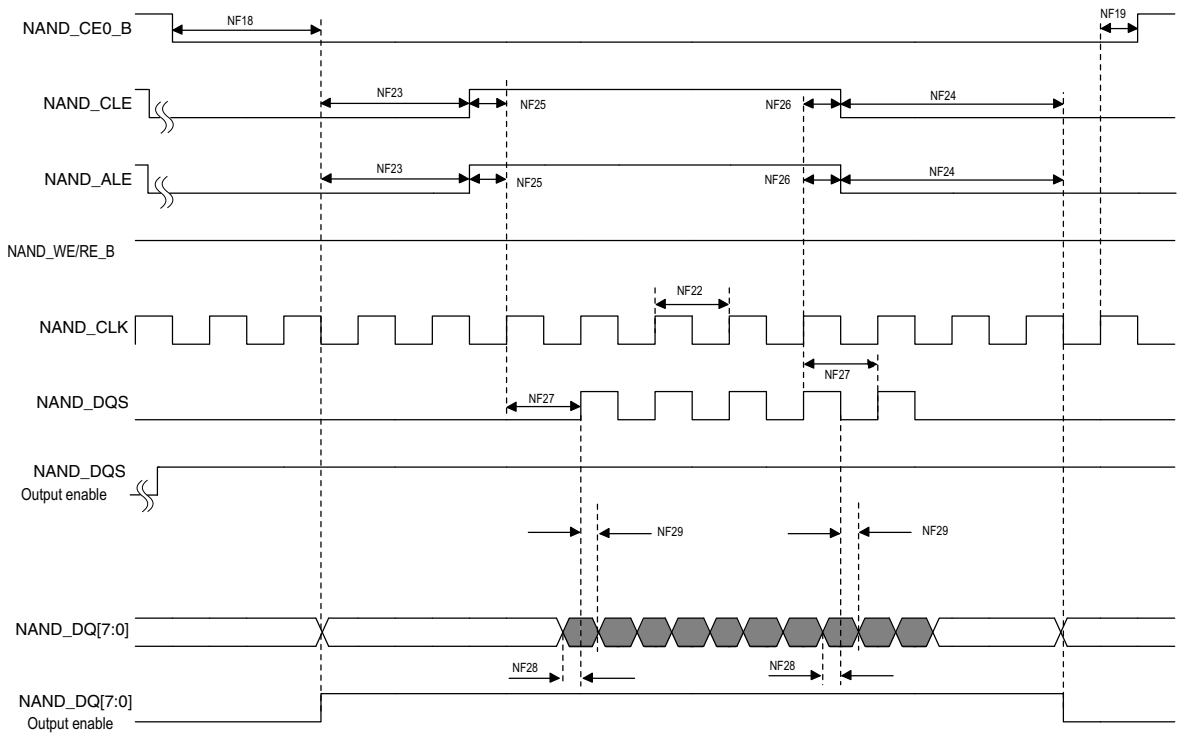


Figure 31. Source Synchronous Mode Data Write Timing Diagram

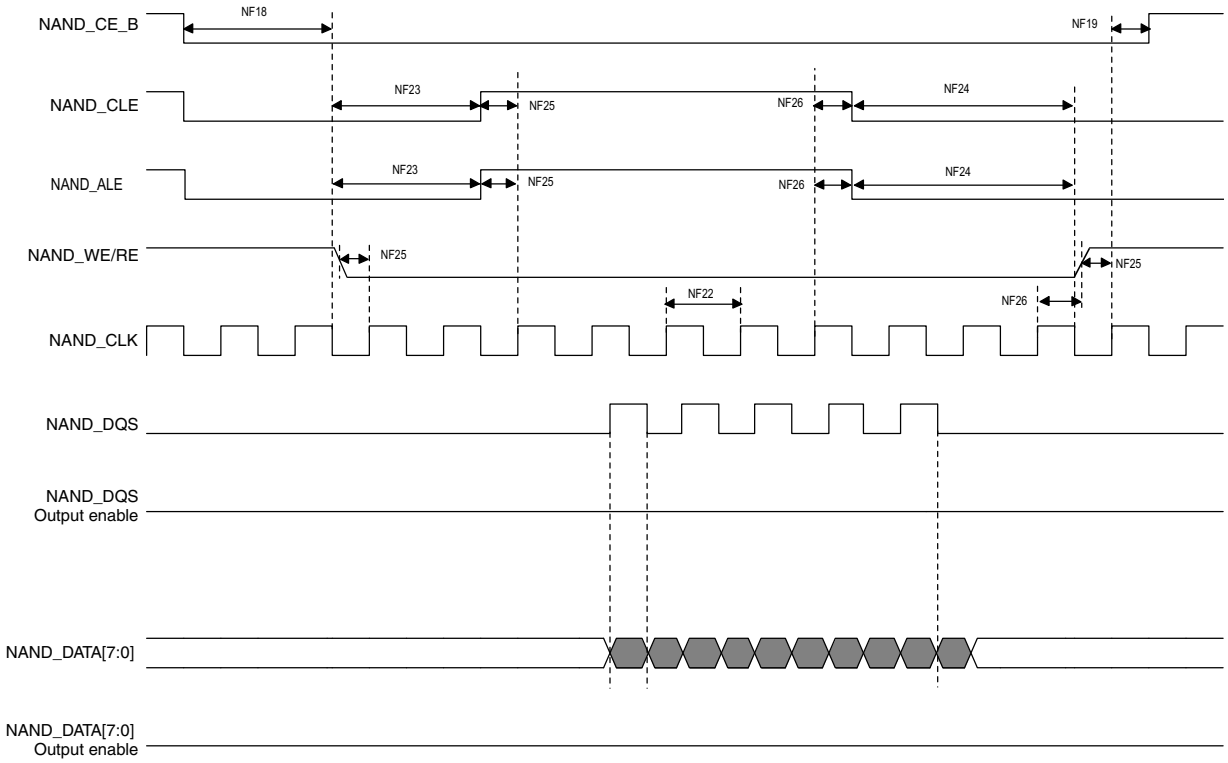


Figure 32. Source Synchronous Mode Data Read Timing Diagram

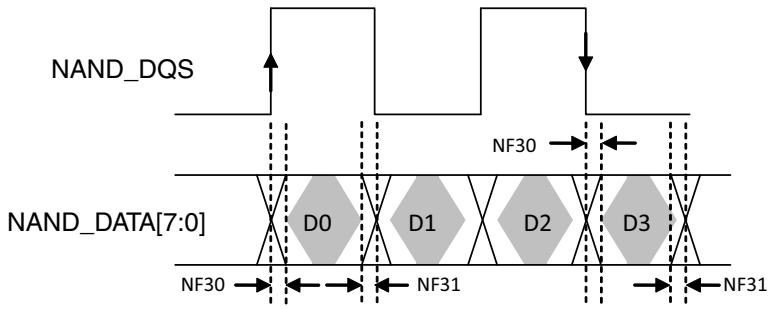


Figure 33. NAND_DQS/NAND_DQ Read Valid Window

Table 47. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see [2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see [2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see [2]]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see [2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see [2]]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		
NF29	Data write hold	—	0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	

[1] GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

[2] T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 33 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.10.3.2 Read and Write Timing

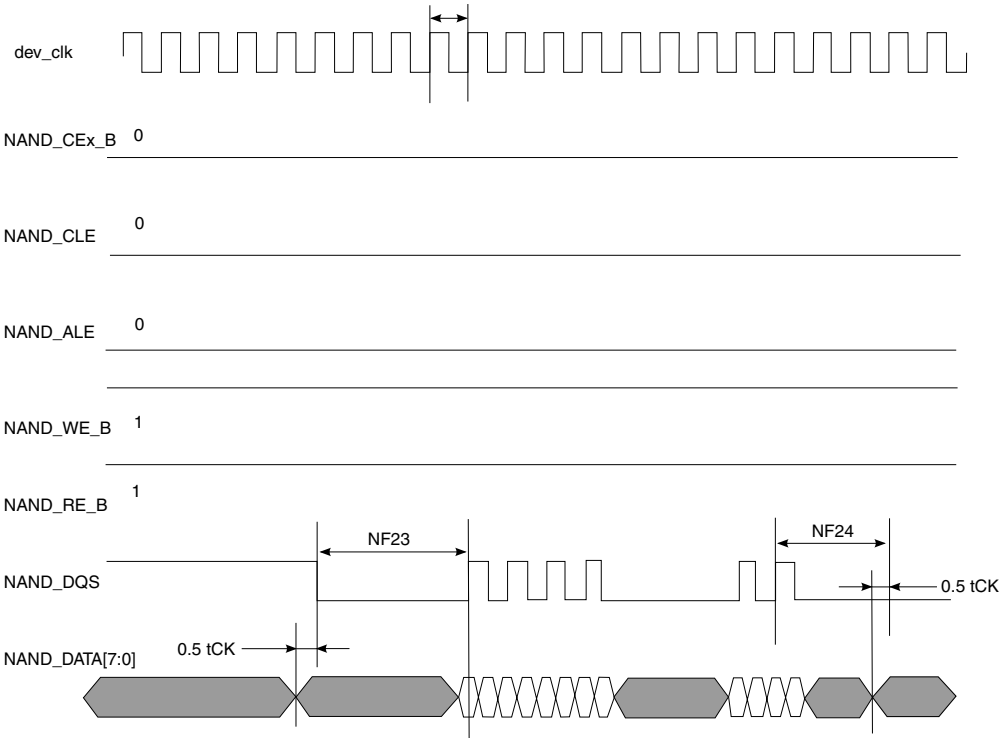


Figure 34. Samsung Toggle Mode Data Write Timing

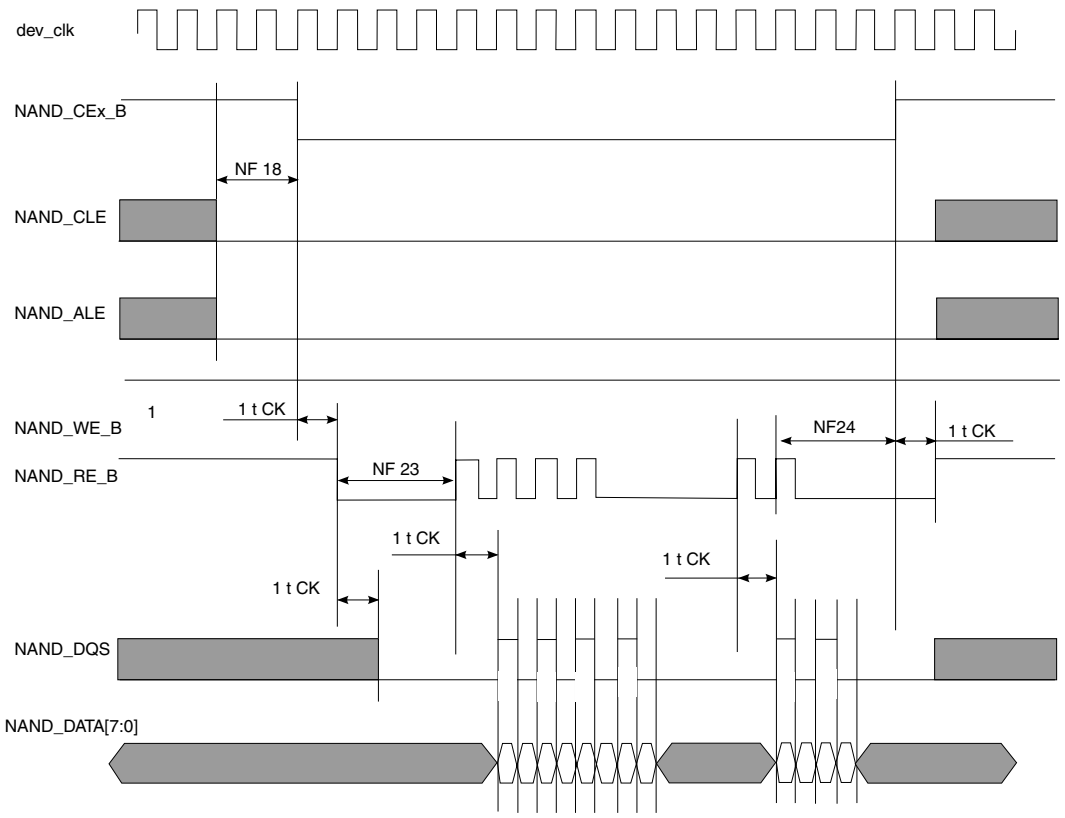


Figure 35. Samsung Toggle Mode Data Read Timing

Table 48. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see [3,2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see [2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see [2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see [2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see [2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see [4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see [5,2]]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see [2]]	—	ns

Table 48. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS).

6 Shown in Figure 34, Samsung Toggle Mode Data Write Timing diagram.

7 Shown in Figure 33, NAND_DQS/NAND_DQ Read Valid Window.

For DDR Toggle mode, Figure 33 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

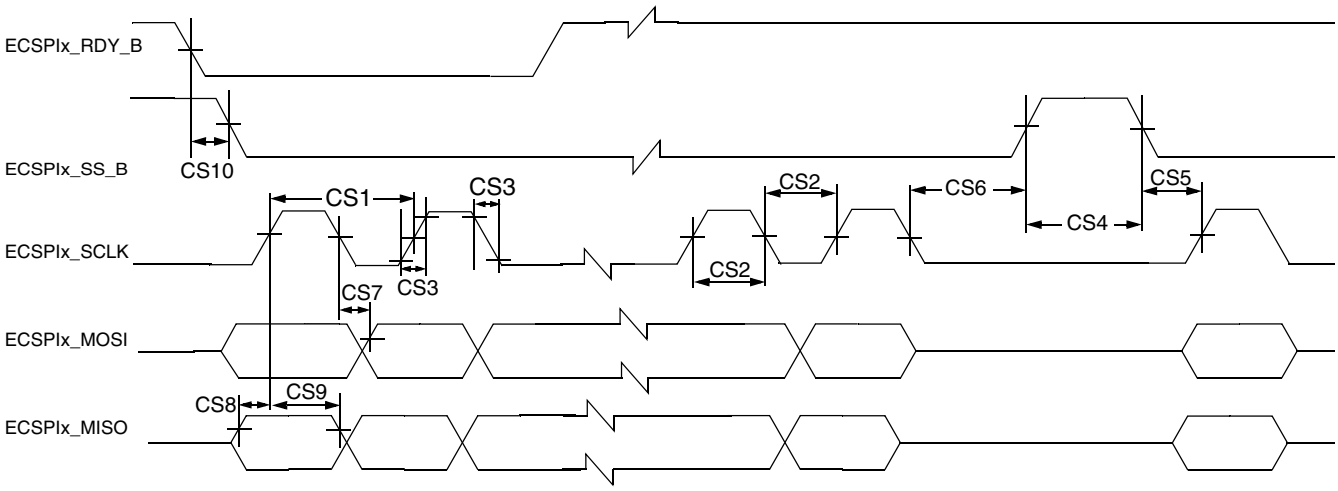
The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 36 depicts the timing of ECSPI in master mode. Table 49 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 36. ECSPI Master Mode Timing Diagram

Table 49. ECSPI Master Mode Timing Parameters

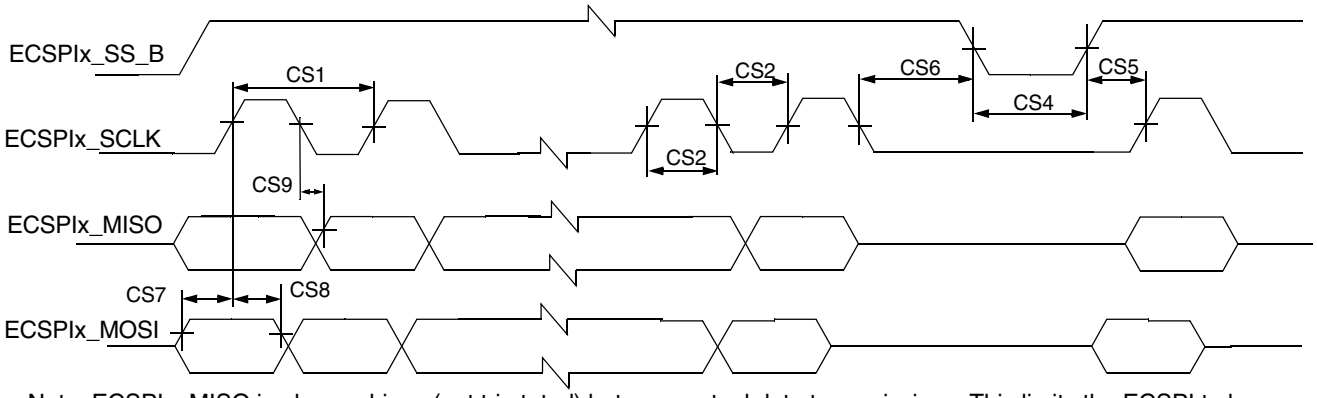
ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time •	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.11.2.2 ECSPI Slave Mode Timing

Figure 37 depicts the timing of ECSPI in slave mode. Table 50 lists the ECSPI slave mode timing characteristics.



Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 37. ECSPI Slave Mode Timing Diagram

Table 50. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF) •	t_{PDmiso}	4	19	ns

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 51 shows the interface timing values. The number field in the table refers to timing signals found in Figure 38 and Figure 39.

Table 51. Enhanced Serial Audio Interface (ESAI) Timing Parameters

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 51. Enhanced Serial Audio Interface (ESAI) Timing Parameters (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [6,7]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	2 x T_C	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

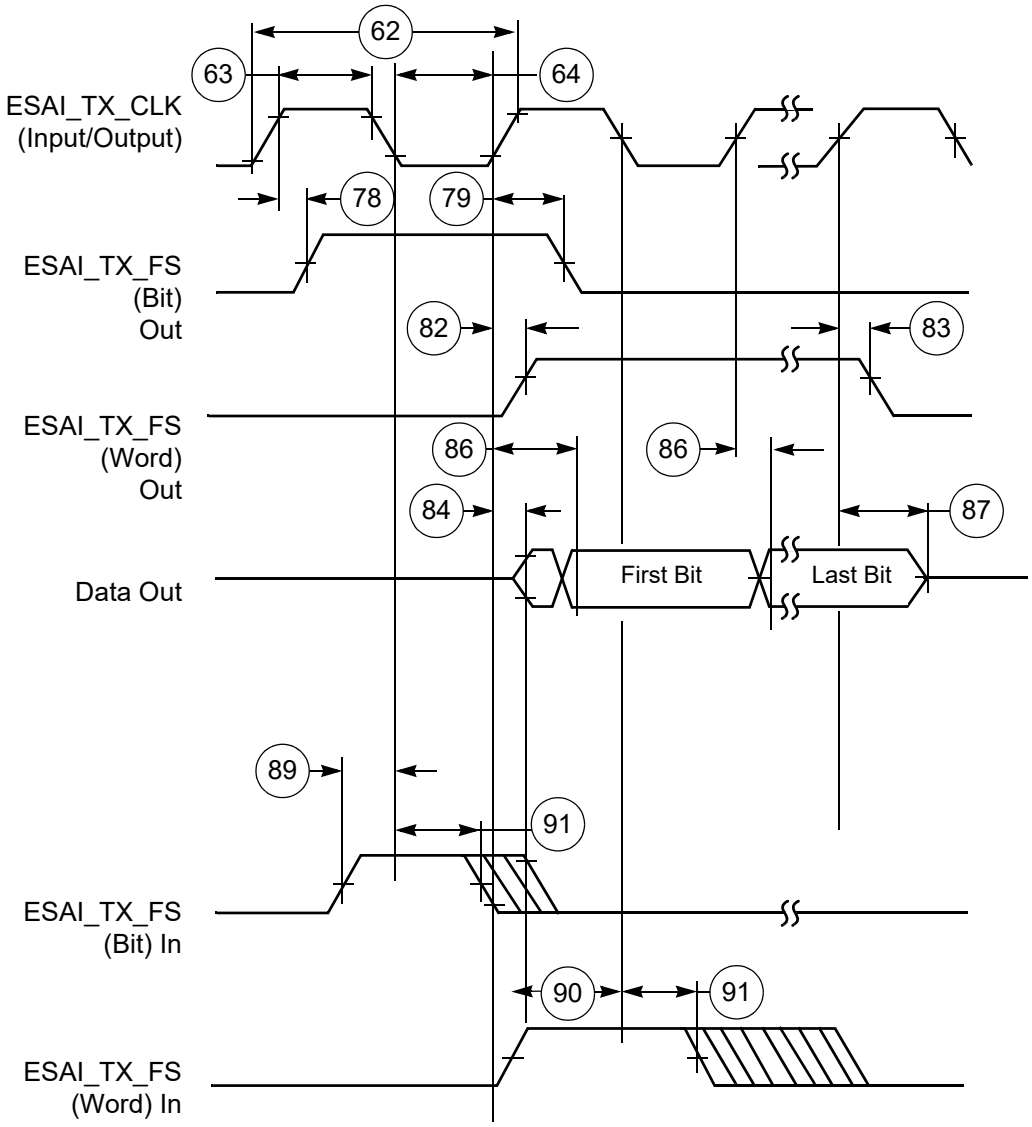


Figure 38. ESAI Transmitter Timing

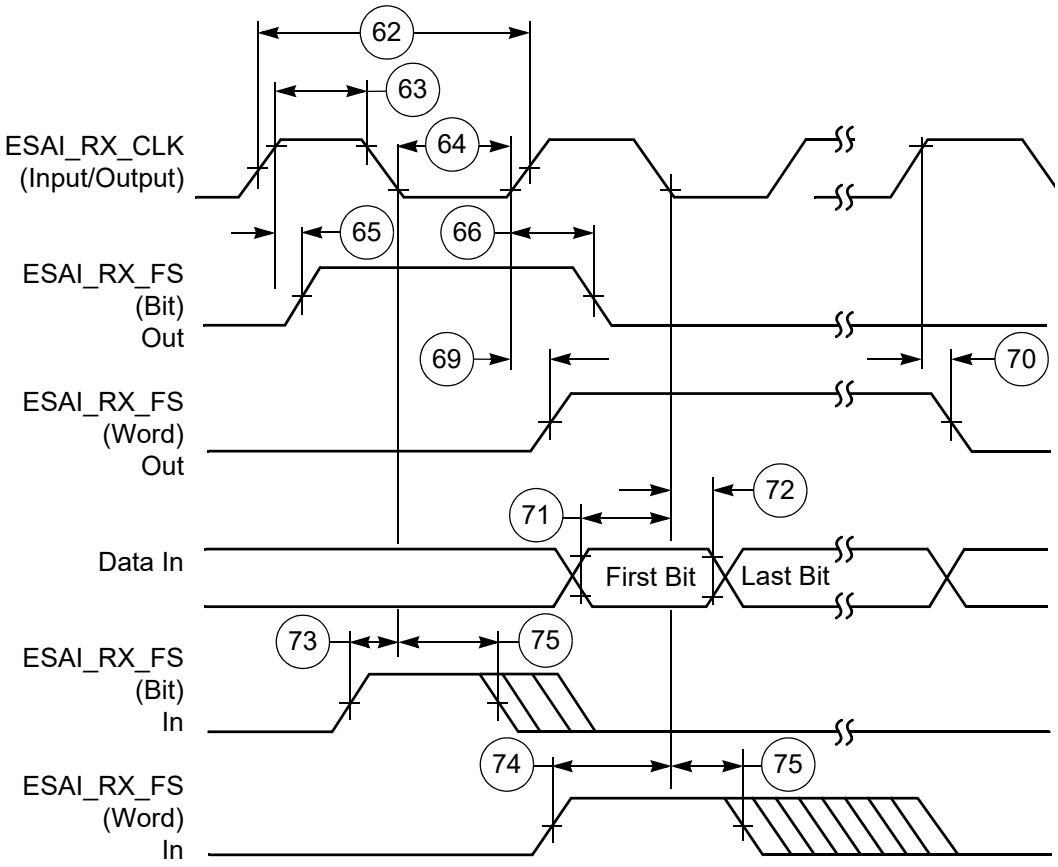


Figure 39. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 52 lists the SD/eMMC4.3 timing characteristics.

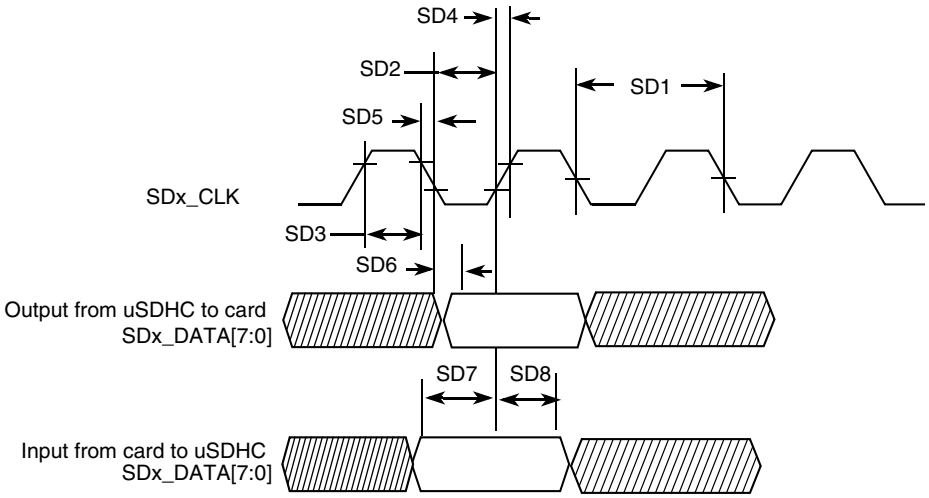


Figure 40. SD/eMMC4.3 Timing

Table 52. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 52. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 53 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

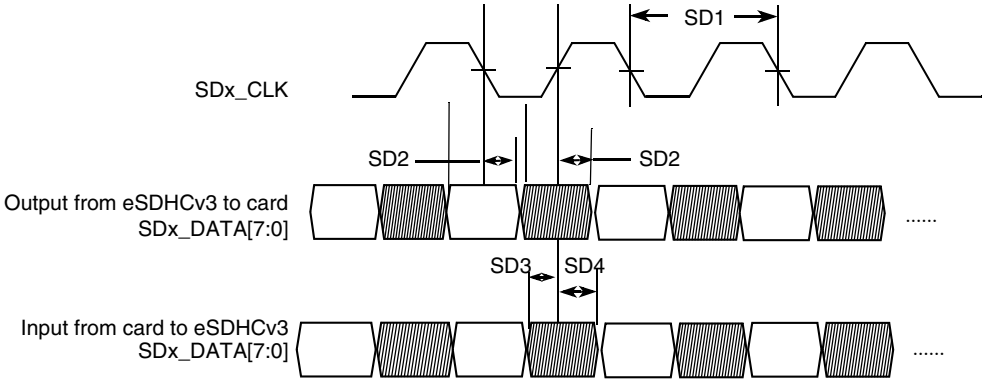


Figure 41. eMMC4.4/4.41 Timing

Table 53. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 1 Clock duty cycle will be in the range of 47% to 53%.

4.11.4.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 54 lists the SDR50/SDR104 timing characteristics.

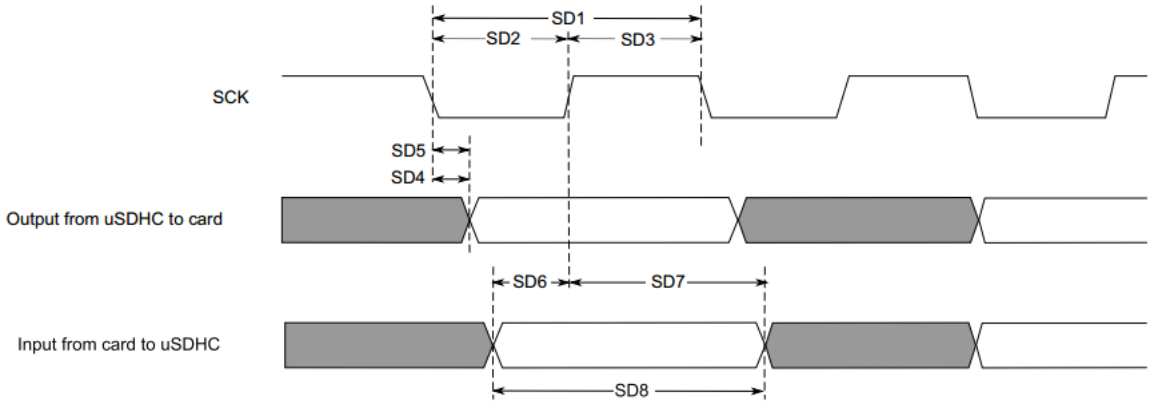


Figure 42. SDR50/SDR104 Timing

Table 54. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 23, "GPIO DC Parameters," on page 40.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 43 shows MII receive signal timings. Table 55 describes the timing parameters (M1–M4) shown in the figure.

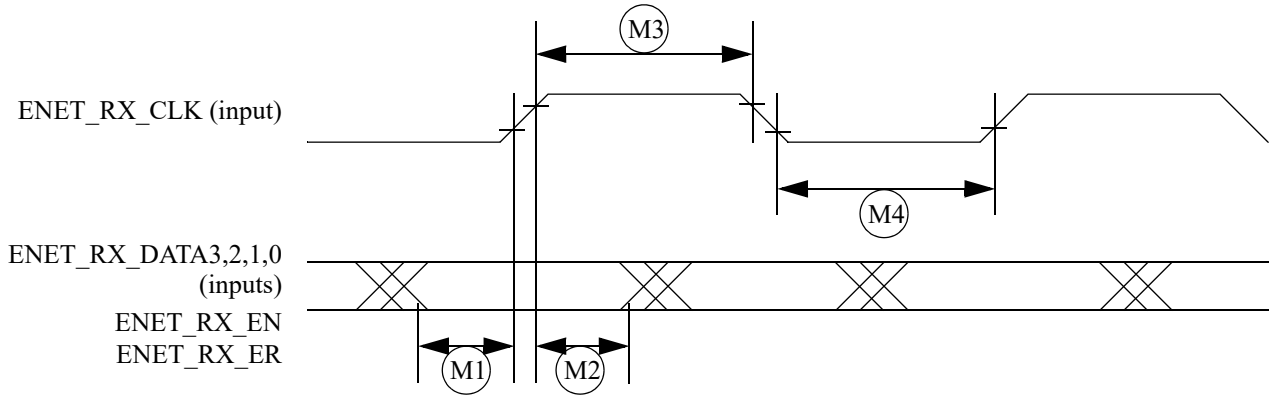


Figure 43. MII Receive Signal Timing Diagram

Table 55. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 44 shows MII transmit signal timings. Table 56 describes the timing parameters (M5–M8) shown in the figure.

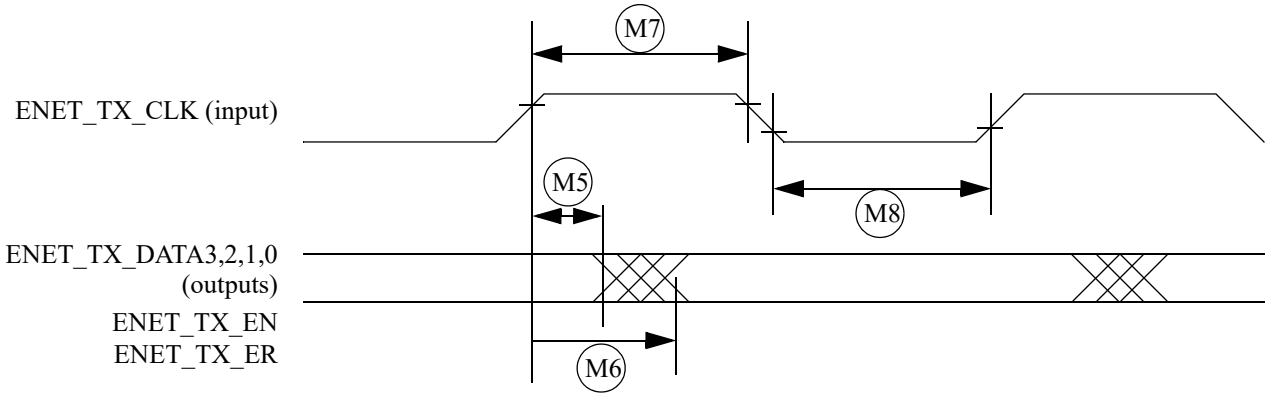


Figure 44. MII Transmit Signal Timing Diagram

Table 56. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 45 shows MII asynchronous input timings. Table 57 describes the timing parameter (M9) shown in the figure.

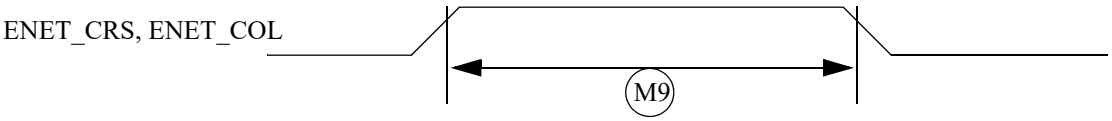


Figure 45. MII Async Inputs Timing Diagram

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min	Max	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 46 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

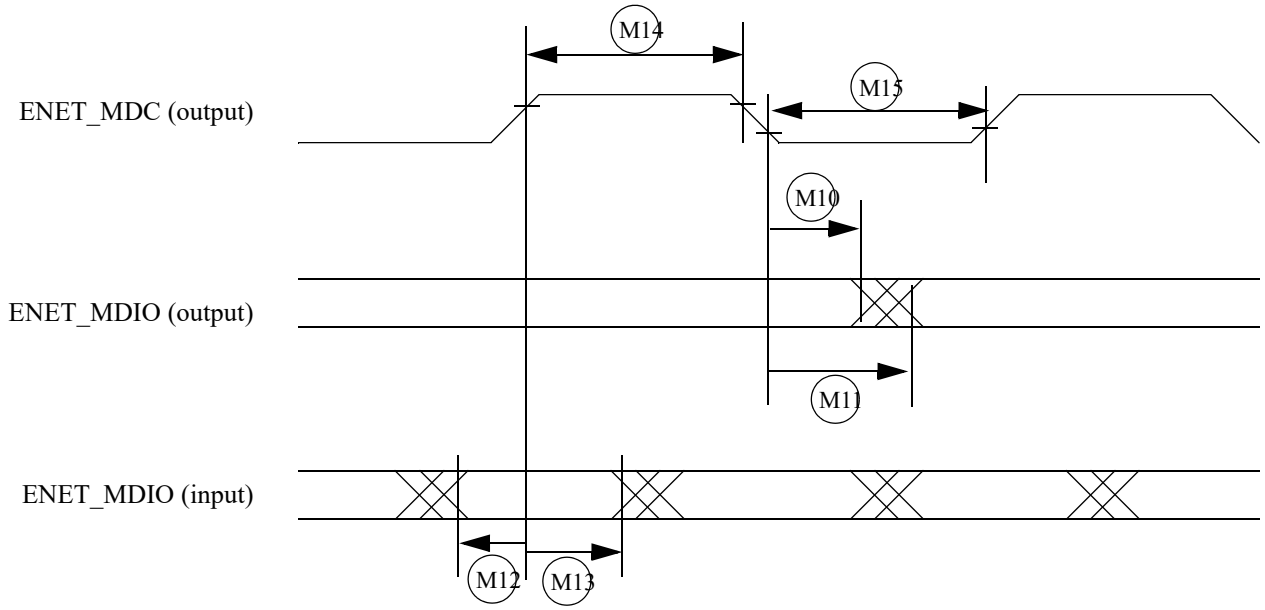


Figure 46. MII Serial Management Channel Timing Diagram

Table 58. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 47 shows RMII mode timings. Table 59 describes the timing parameters (M16–M21) shown in the figure.

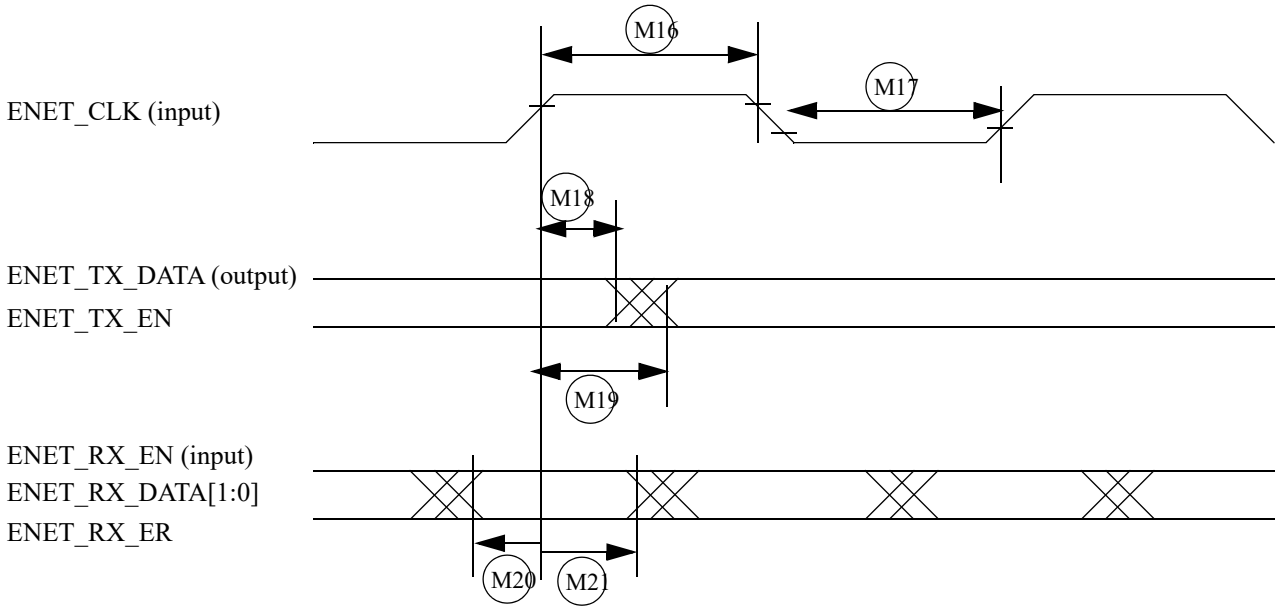


Figure 47. RMII Mode Signal Timing Diagram

Table 59. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.5.3 Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 60. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

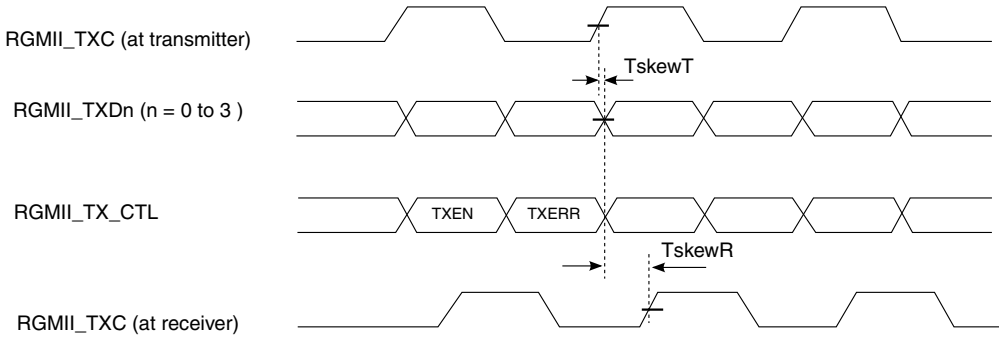


Figure 48. RGMII Transmit Signal Timing Diagram Original

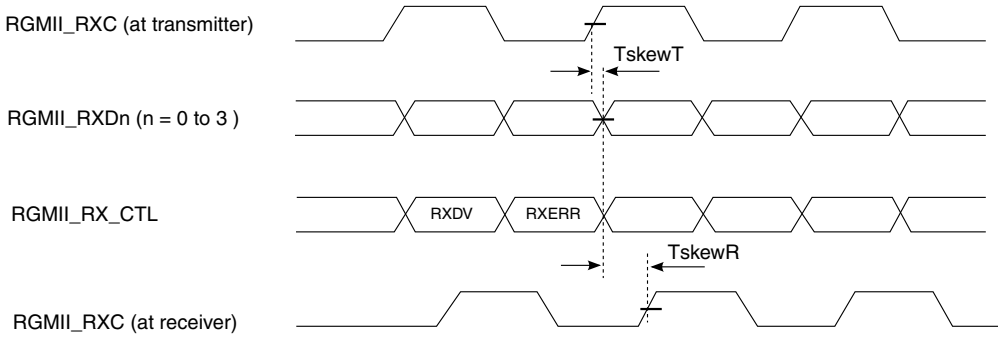


Figure 49. RGMII Receive Signal Timing Diagram Original

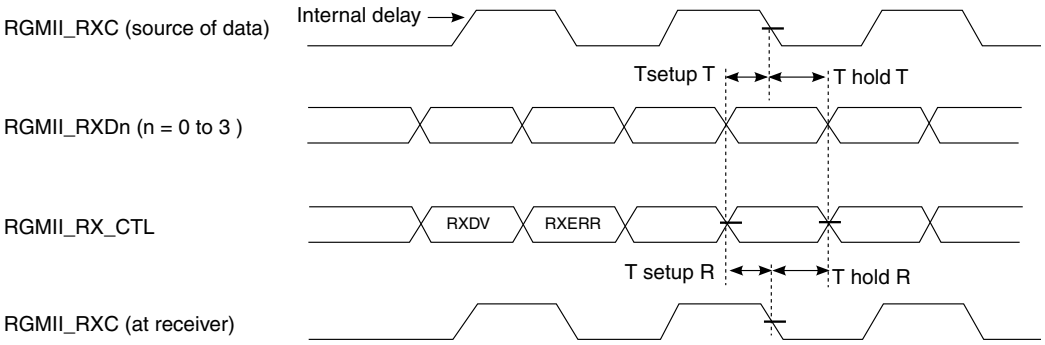


Figure 50. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

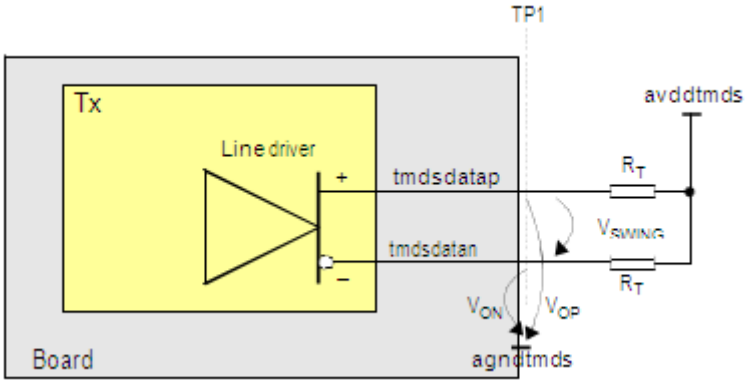


Figure 51. Driver Measuring Conditions

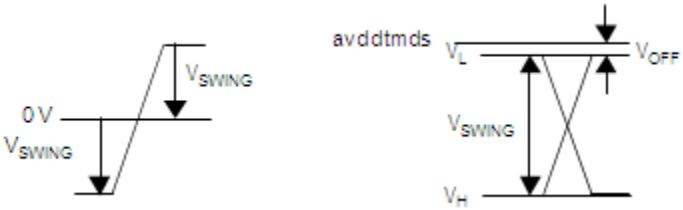


Figure 52. Driver Definitions

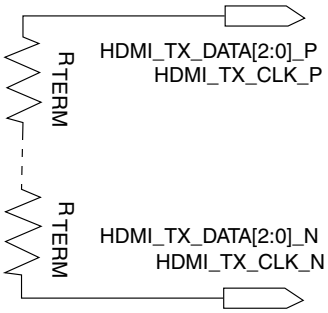


Figure 53. Source Termination

Table 61. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V
R_T	Termination resistance	—	45	50	55	Ω

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	—	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	—	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see Figure 53). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$^{VHPD}{}_{VL}$	Hot plug detect low range	—	0	—	0.8	V
$^{HPD}{}_{Z}$	Hot plug detect input impedance	—	10	—	—	kΩ
$^{HPD}{}_{t}$	Hot plug detect time delay	—	—	—	100	µs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 54 to Figure 58 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

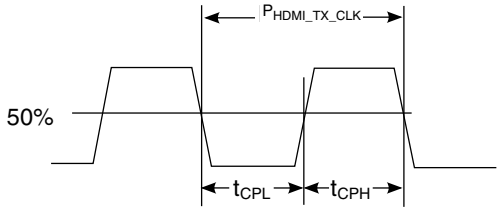


Figure 54. TMDS Clock Signal Definitions

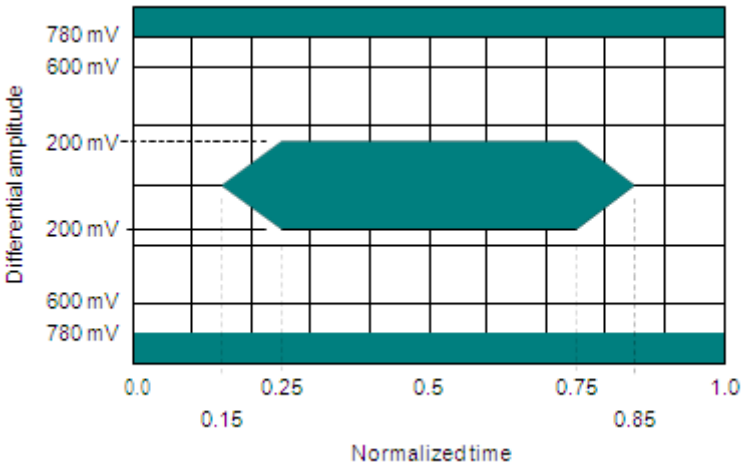


Figure 55. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

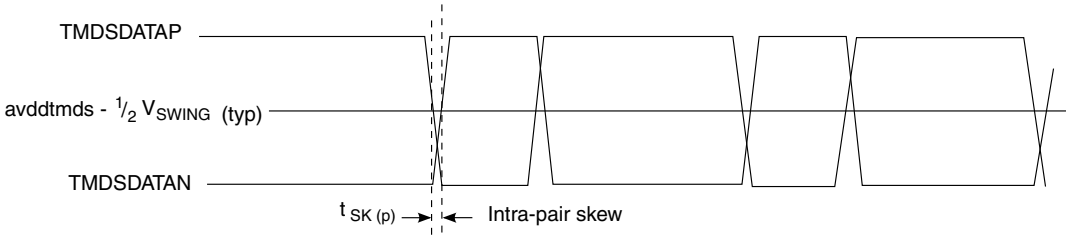


Figure 56. Intra-Pair Skew Definition

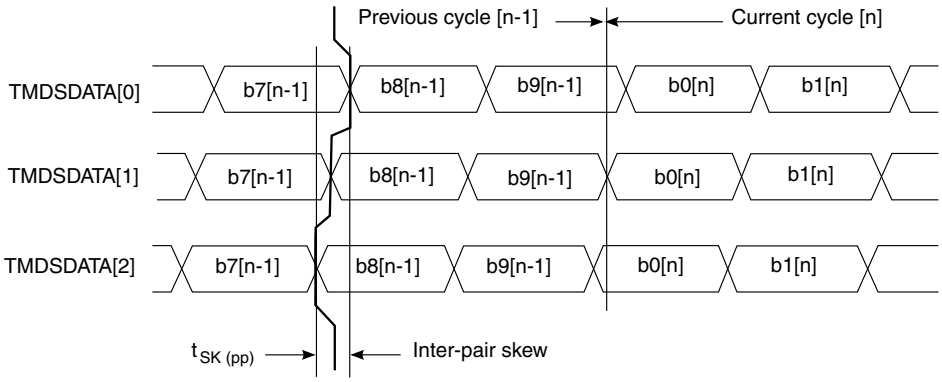


Figure 57. Inter-Pair Skew Definition

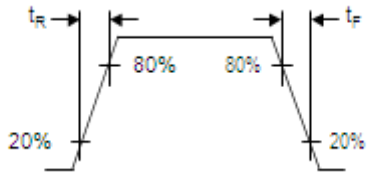


Figure 58. TMDS Output Signals Rise and Fall Time Definition

Table 62. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 54.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 54.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 54.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 54.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 56.	—	—	0.15	UI[1]
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 57.	—	—	1	UI[1]
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 58.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 58.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%

1 UI means TMDS clock unit.

2 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 59 depicts the timing of I²C module, and Table 63 lists the I²C module timing characteristics.

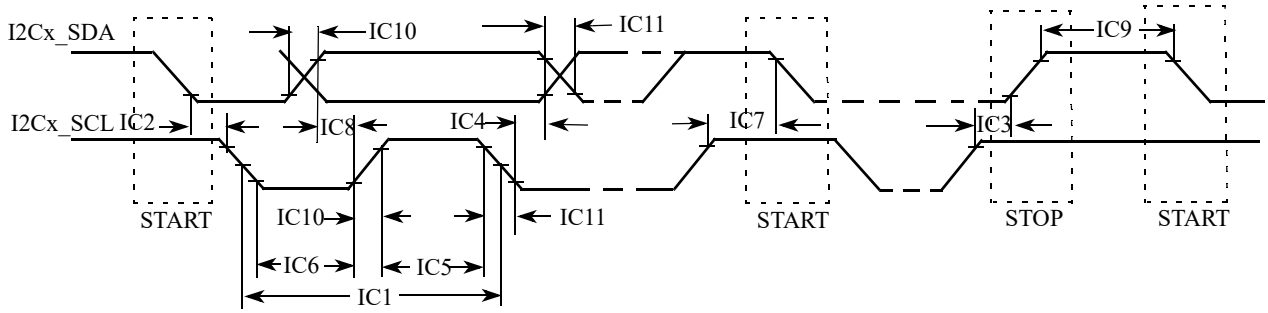


Figure 59. I²C Bus Timing

Table 63. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 64 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 64. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPUx_CSIx_DATA05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]

Table 64. Camera Input Signal Cross Reference, Format, and Bits Per Cycle (continued)

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_ DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_ DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_ DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_ DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_ DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_ DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 IPUx_CSIx stands for IPUx_CSI0 or IPUx_CSI1.
2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB 16 bits—Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr 16 bits—Supported as a “generic-data” input, with no on-the-fly processing.
7 YCbCr 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPUx_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPUx_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPUx_CSIx_DATA_EN bus.

4.11.10.2.2 Gated Clock Mode

The IPUx_CSIx_VSYNC, IPUx_CSIx_HSYNC, and IPUx_CSIx_PIX_CLK signals are used in this mode. See Figure 60.

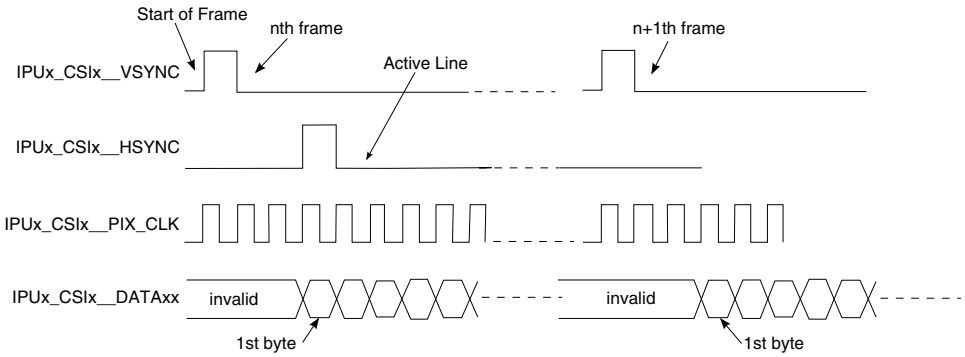


Figure 60. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPUx_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPUx_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPUx_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPUx_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the IPUx_CSIx_HSYNC timing repeats. For the next frame, the IPUx_CSIx_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the IPUx_CSIx_HSYNC signal, which is not used (see Figure 61). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPUx_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

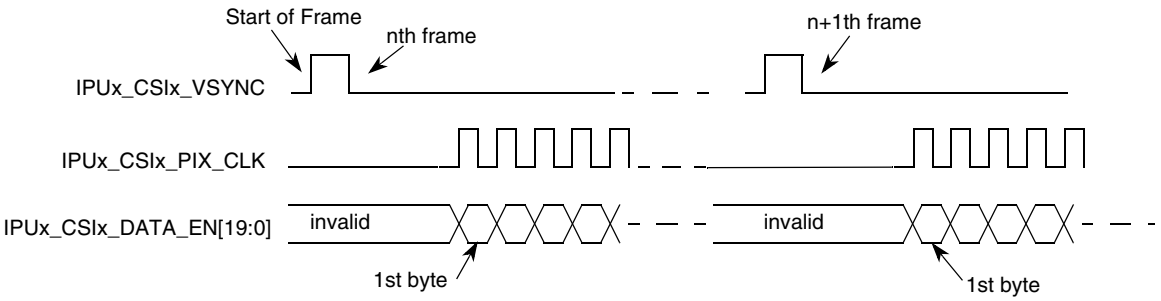


Figure 61. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 61 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPUx_CSIx_VSYNC; active-high/low IPUx_CSIx_HSYNC; and rising/falling-edge triggered IPUx_CSIx_PIX_CLK.

4.11.10.3 Electrical Characteristics

Figure 62 depicts the sensor interface timing. IPUx_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 65 lists the sensor interface timing characteristics.

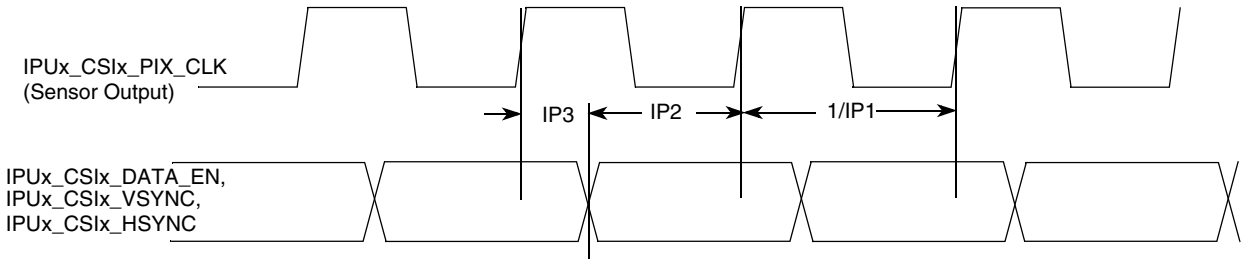


Figure 62. Sensor Interface Timing Diagram

Table 65. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 66 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 66. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

Table 66. Video Signal Cross-Reference (continued)

i.MX 6Solo/6DualLite	LCD							Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
DIx_DISP_CLK	PixCLK							—
DIx_PIN1	—							May be required for anti-tearing
DIx_PIN2	HSYNC							—
DIx_PIN3	VSYNC							VSYNC out

Table 66. Video Signal Cross-Reference (continued)

i.MX 6Solo/6DualLite	LCD							Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
DIx_PIN4	—							Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							
DIx_PIN6	—							
DIx_PIN7	—							
DIx_PIN8	—							
DIx_D0_CS	—							—
DIx_D1_CS	—							Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							—
DIx_PIN12	—							—
DIx_PIN13	—							Register select signal
DIx_PIN14	—							Optional RS2
DIx_PIN15	DRDY/DV							Data validation/blank, data enable
DIx_PIN16	—							Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 66 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The IPP_DISP_CLK is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The IPUx_DIx_PIN01—IPUx_DIx_PIN07 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any other independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The IPUx_DIx_D0_CS and IPUx_DIx_D1_CS pins are dedicated to provide chip select signals to two displays.
- The IPUx_DIx_PIN11—IPUx_DIx_PIN17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters.

The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 63 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPUx_DIx_PIN02 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPUx_DIx_PIN03 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

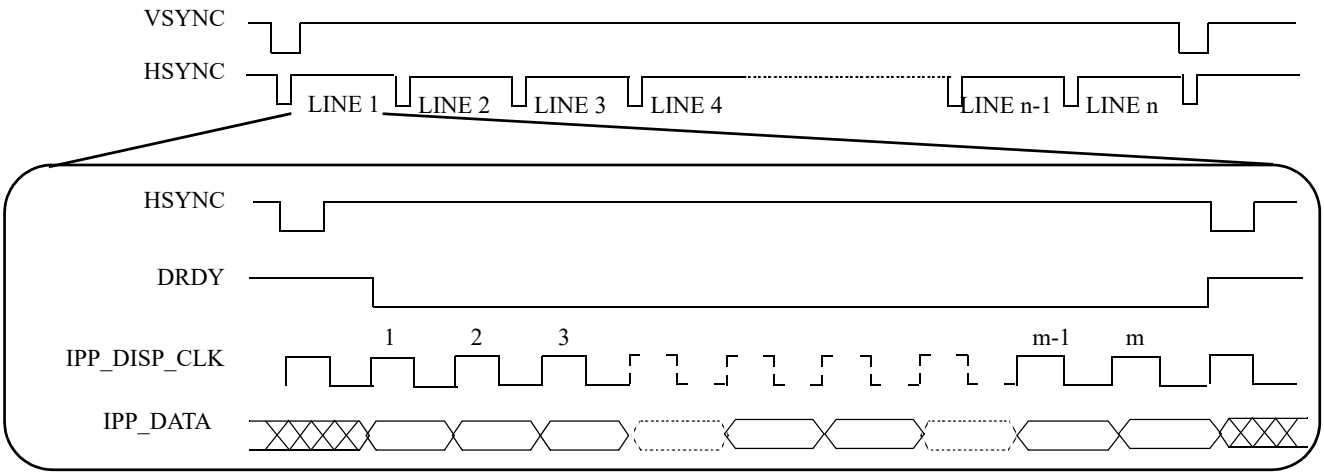


Figure 63. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 64 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by

corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

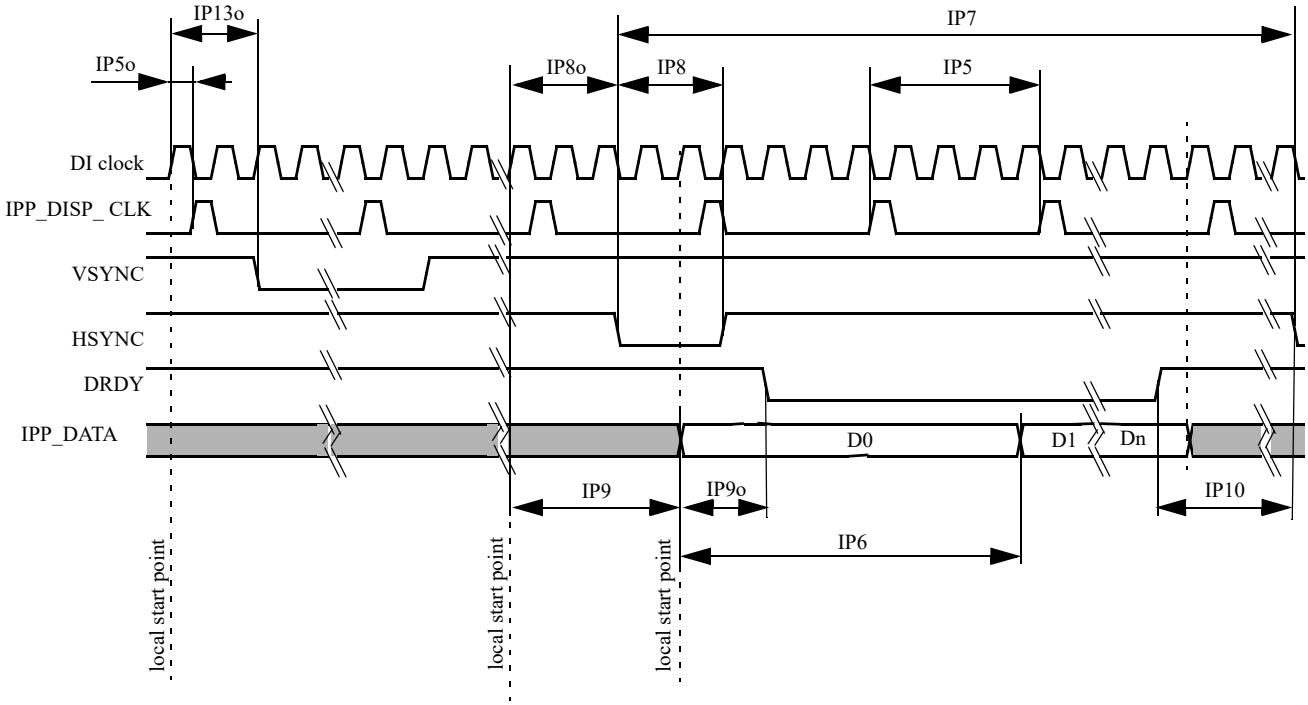


Figure 64. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 65 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

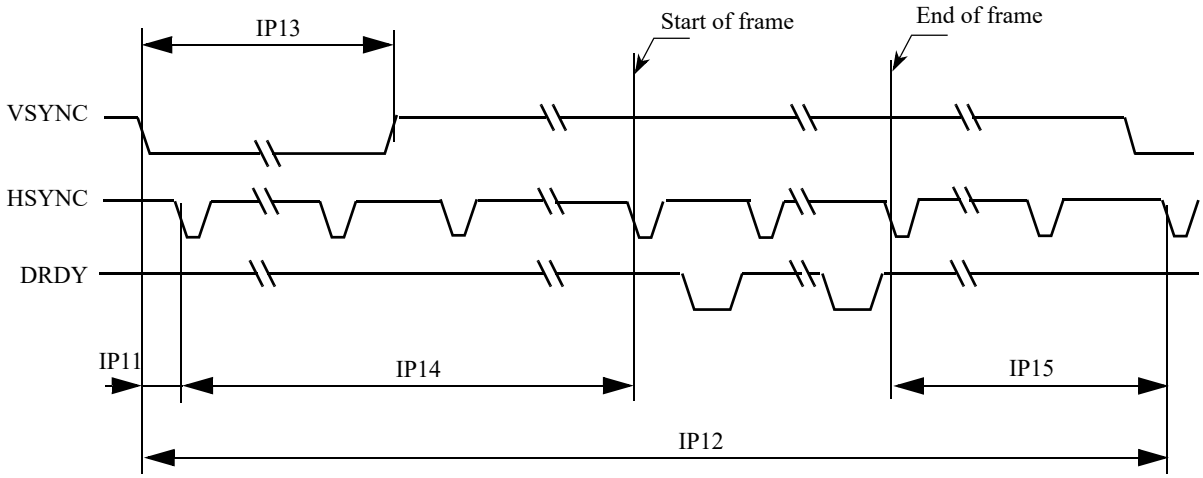


Figure 65. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 67 shows timing characteristics of signals presented in Figure 64 and Figure 65.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	Width of second Vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter	ns

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1]Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk}\left(floor\left[\dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximum accuracy of UP/DOWN edge of IPP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 66 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 68 lists the synchronous display interface timing characteristics.

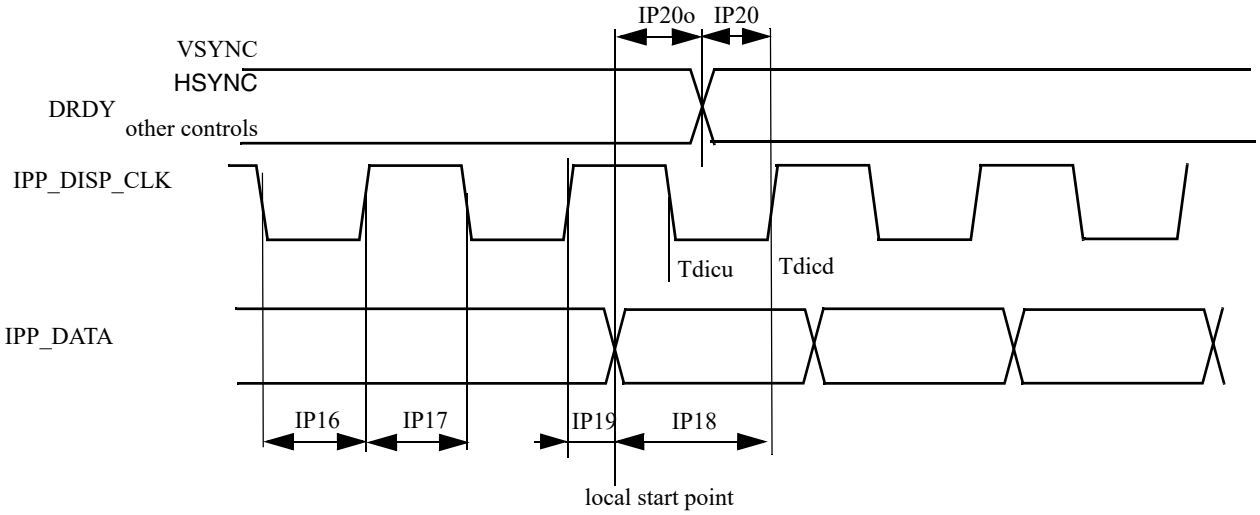


Figure 66. Synchronous Display Interface Timing Diagram—Access Level

Table 68. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$\mathrm{Tdicd} = \frac{1}{2}\left(T_{diclk} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP_CLK_DOWN}}{\mathrm{DI_CLK_PERIOD}}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$\mathrm{Tdicu} = \frac{1}{2}\left(T_{diclk} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP_CLK_UP}}{\mathrm{DI_CLK_PERIOD}}\right]\right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*".

Table 69. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications - Apply to DSI_CLK_P/DSI_CLK_N and DSI_DATA_P/DSI_DATA_N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V

Table 70. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns
HS Line Drivers DC Specifications						
$\lvert V_{OD} \rvert$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\lvert V_{OD} \rvert$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01\text{-}10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0\text{-}11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV

Table 70. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Z_{ID}	Differential input impedance	—	80	—	125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 67 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

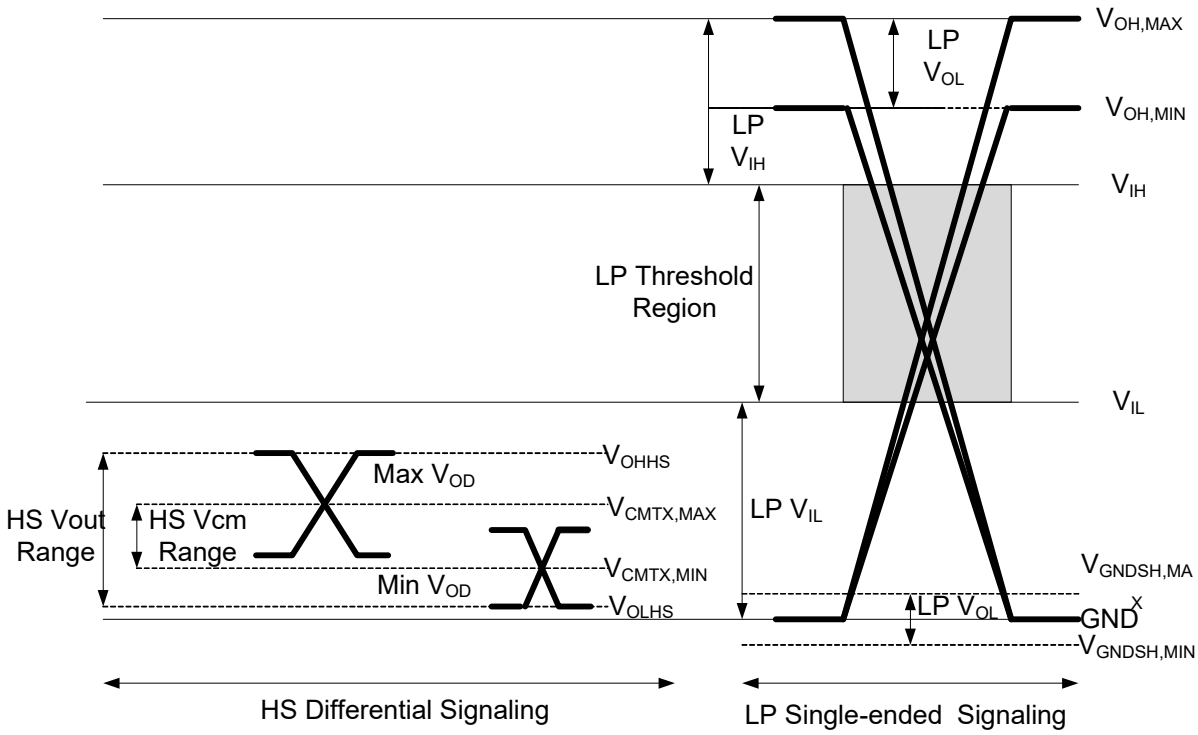


Figure 67. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

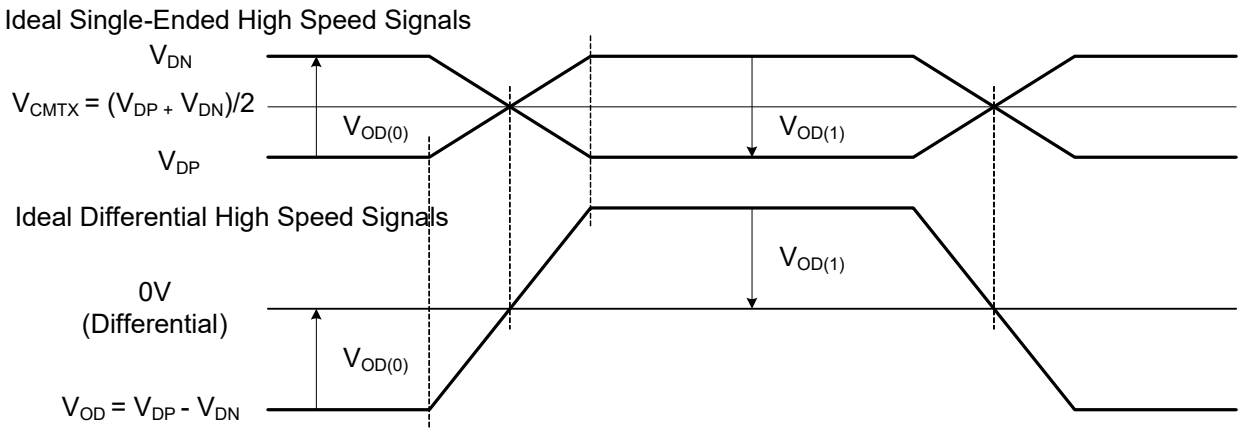


Figure 68. Ideal Single-ended and Resulting Differential HS Signals

4.11.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

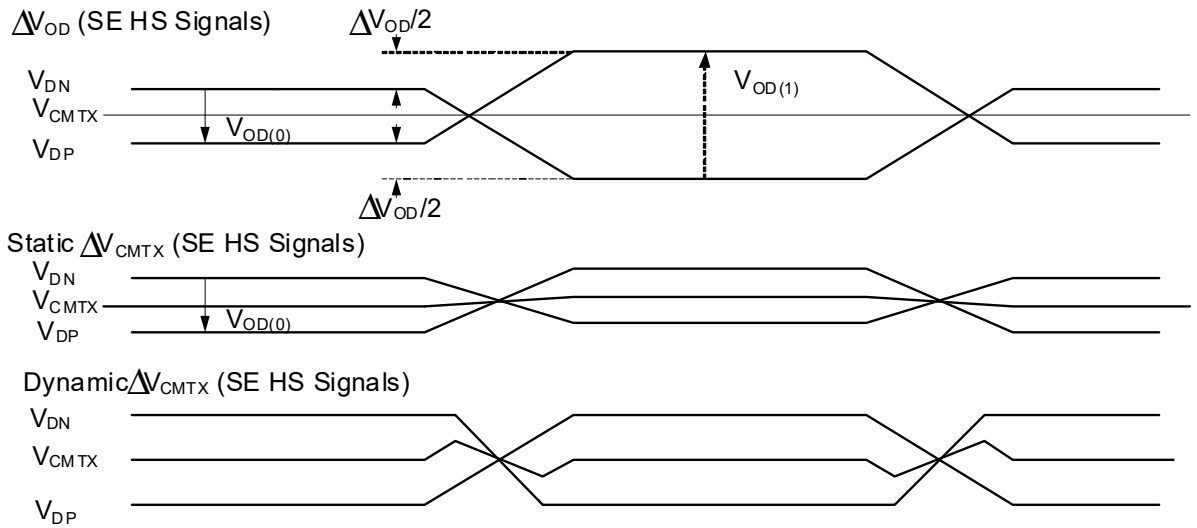


Figure 69. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 71. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps

Table 71. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}		30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—		—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—		ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz

Table 71. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load resistance	—	80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

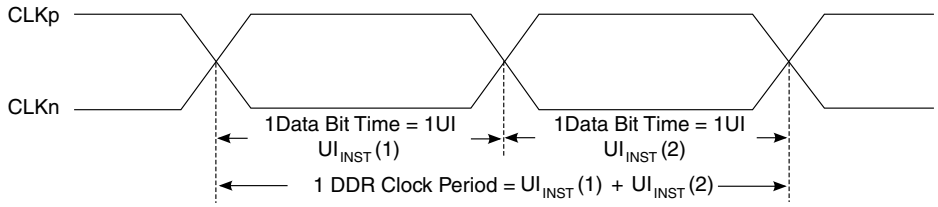


Figure 70. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 71:

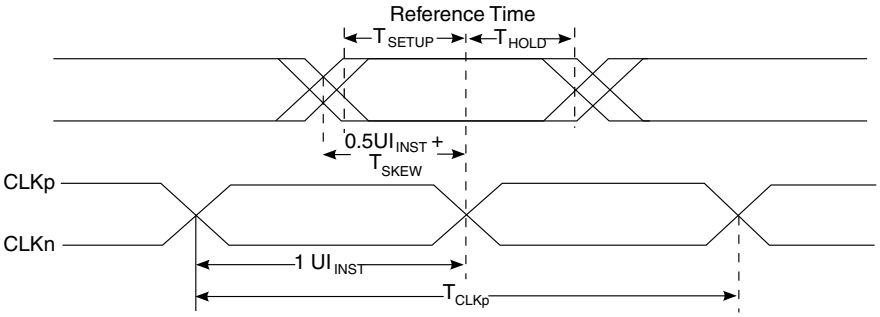


Figure 71. Data to Clock Timing Definitions

4.11.12.8 Reverse High-Speed Data Transmission Timing

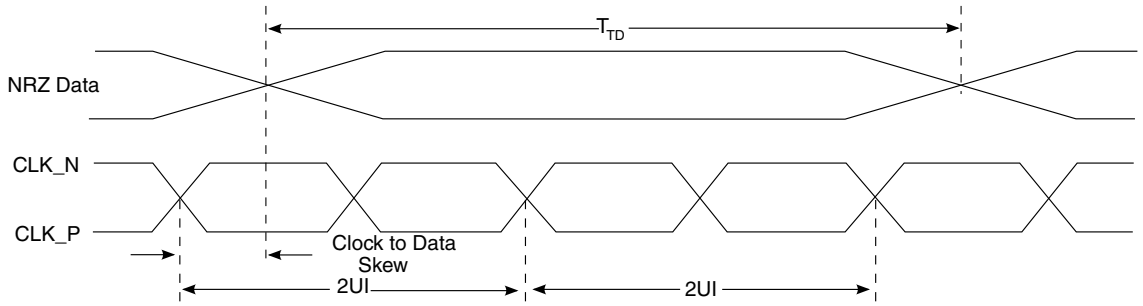


Figure 72. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.9 Low-Power Receiver Timing

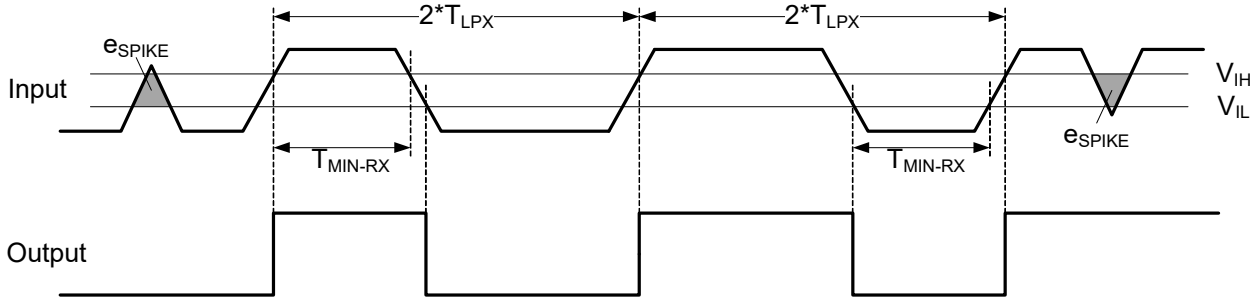


Figure 73. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

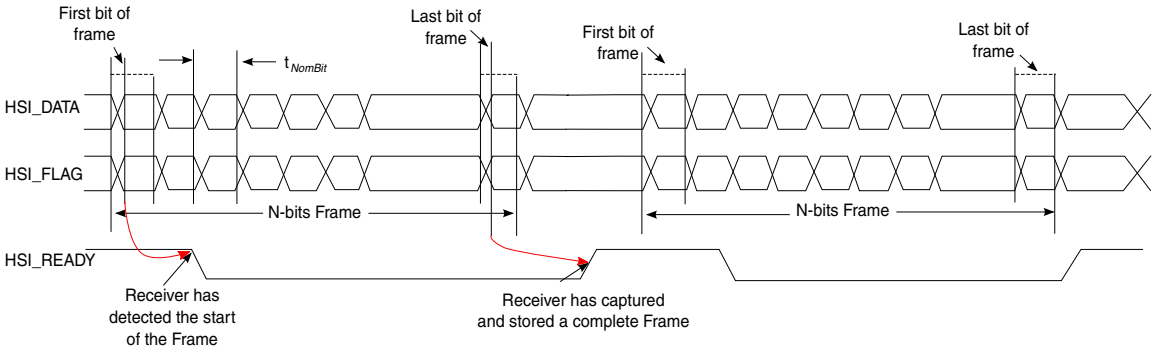


Figure 74. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

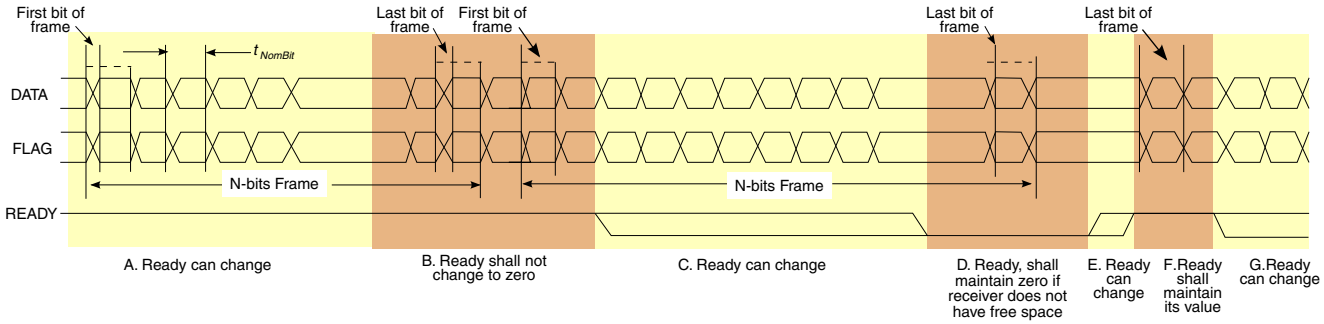


Figure 75. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

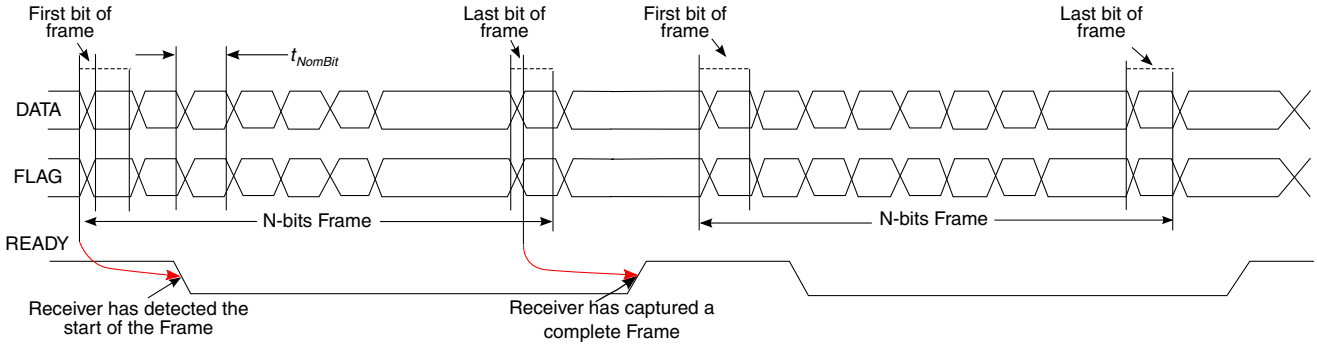


Figure 76. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

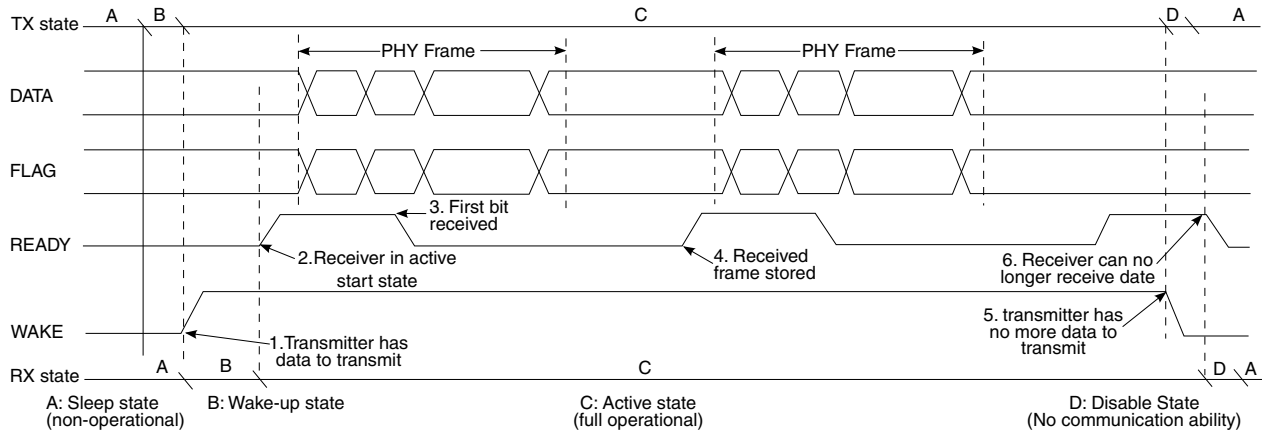


Figure 77. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

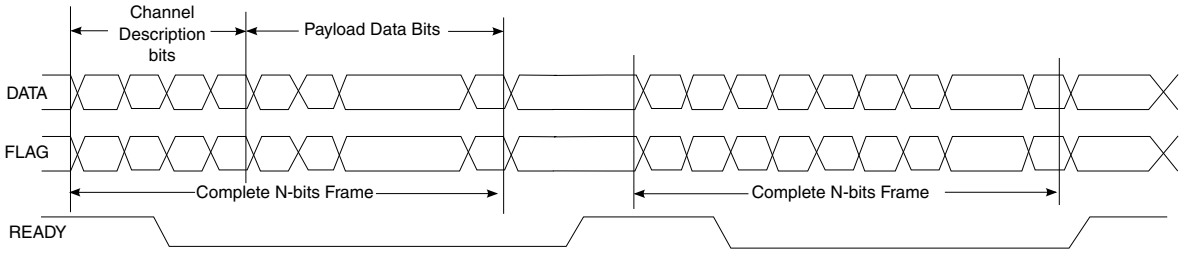


Figure 78. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

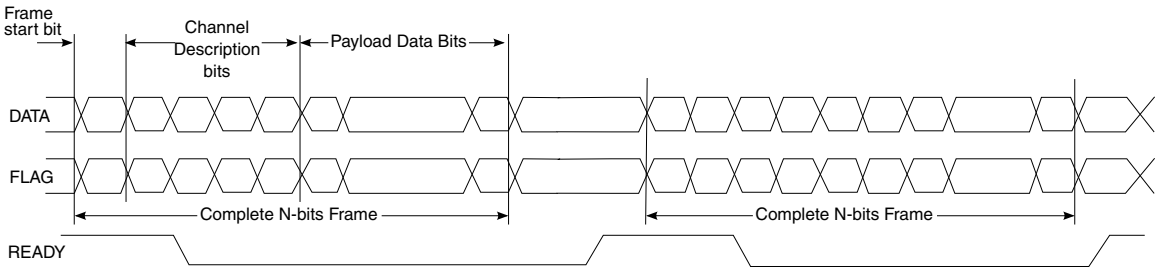


Figure 79. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

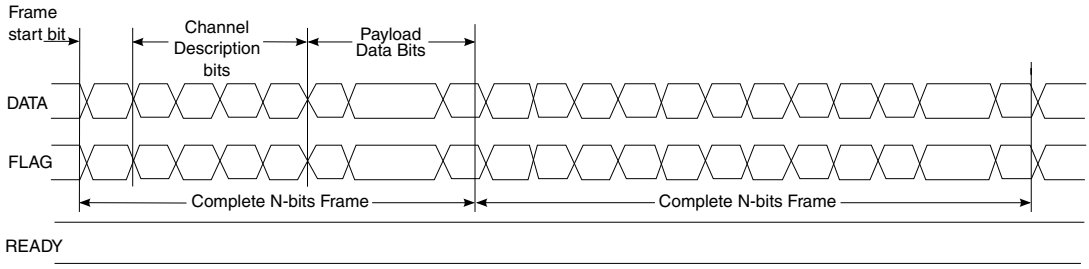


Figure 80. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

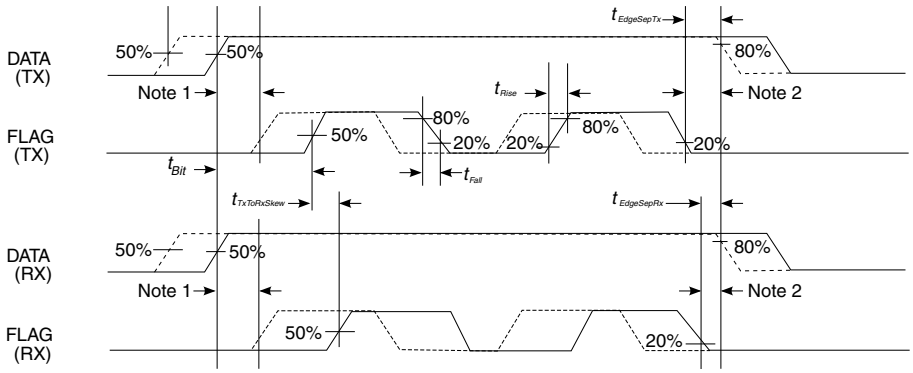
4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 72. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns

Table 72. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns



1 This case shows that the DATA signal has slowed down more compared to the FLAG signal
2 This case shows that the FLAG signal has slowed down more compared to the DATA signal.

Figure 81. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 73 lists the MediaLB 3-pin interface electrical characteristics.

Table 73. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = -6 mA	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < VDD$	—	±10	µA

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 74 lists the MediaLB 6-pin interface electrical characteristics.

Table 74. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\lvert V_{OCM, high} - V_{OCM, low} \rvert$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\lvert I_{OS} \rvert$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					
Differential clock input: • logic low steady-state • logic high steady-state • hysteresis	 V_{ILC} V_{IHC} V_{HSC}	See Note[4]	 — 50 -25	 -50 — 25	 mV mV mV
Differential signal/data input: • logic low steady-state • logic high steady-state	 V_{ILS} V_{IHS}	—	 — 50	 -50 —	 mV mV
Signal-ended input voltage (steady-state): • MLB_SIG_P, MLB_DATA_P • MLB_SIG_N, MLB_DATA_N	 V_{IN+} V_{IN-}	—	 0.5 0.5	 2.0 2.0	 V V

1 The signal-ended output voltage of a driver is defined as V_{O+} on MLB_CLK_P, MLB_SIG_P, and MLB_DATA_P. The signal-ended output voltage of a driver is defined as V_{O-} on MLB_CLK_N, MLB_SIG_N, and MLB_DATA_N.

2 Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-}.

3 Short circuit current is applicable when V_{O+} and V_{O-} are shorted together and/or shorted to ground.

4 The logic state of the receiver is undefined when -50 mV < V_{ID} < 50 mV.

4.11.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 82 show the timing of MediaLB 3-pin interface, and Table 75 and Table 76 lists the MediaLB 3-pin interface timing characteristics.

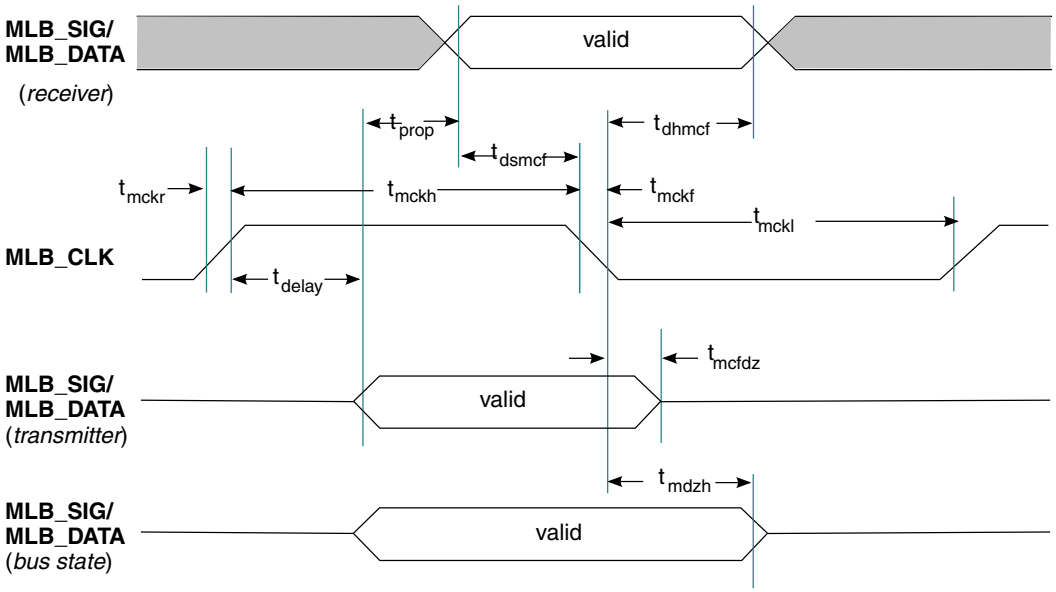


Figure 82. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 75. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK operating frequency[1]	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLB_CLK low time[2]	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLB_CLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLB_CLK low	t_{mdzh}	4	—	ns	—

Table 75. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	10	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	10.75	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 76; unless otherwise noted.

Table 76. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLB_CLK low time	t_{mckl}	6.1	—	ns	[2]
MLB_CLK high time	t_{mckh}	9.3	—	ns	—
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLB_CLK low	t_{mdzh}	2	—	ns	—
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	7	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	6	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 77 lists the MediaLB 6-pin interface timing characteristics, and Figure 83 shows the MLB 6-pin delay, setup, and hold times.

Table 77. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLB_SIG_P/_N (MLB_DATA_P/_N) output valid from transition of MLB_CLK_P/_N (low-to-high)[1]	t_{delay}	0.6	1.3	ns	—
Disable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{phz}	0.6	3.5	ns	—
Enable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{plz}	0.6	5.6	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) valid to transition of MLB_CLK_P/_N (low-to-high)	t_{su}	0.05	—	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) hold from transition of MLB_CLK_P/_N (low-to-high)[2]	t_{hd}	0.6			—

[1] t_{delay}, t_{phz}, t_{plz}, t_{su}, and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

[2] The transmitting device must ensure valid data on MLB_SIG_P/_N (MLB_DATA_P/_N) for at least $t_{hd(min)}$ following the rising edge of MLB_CLK_P/N; receivers must latch MLB_SIG_P/_N (MLB_DATA_P/_N) data within $t_{hd(min)}$ of the rising edge of MLB_CLK_P/_N.

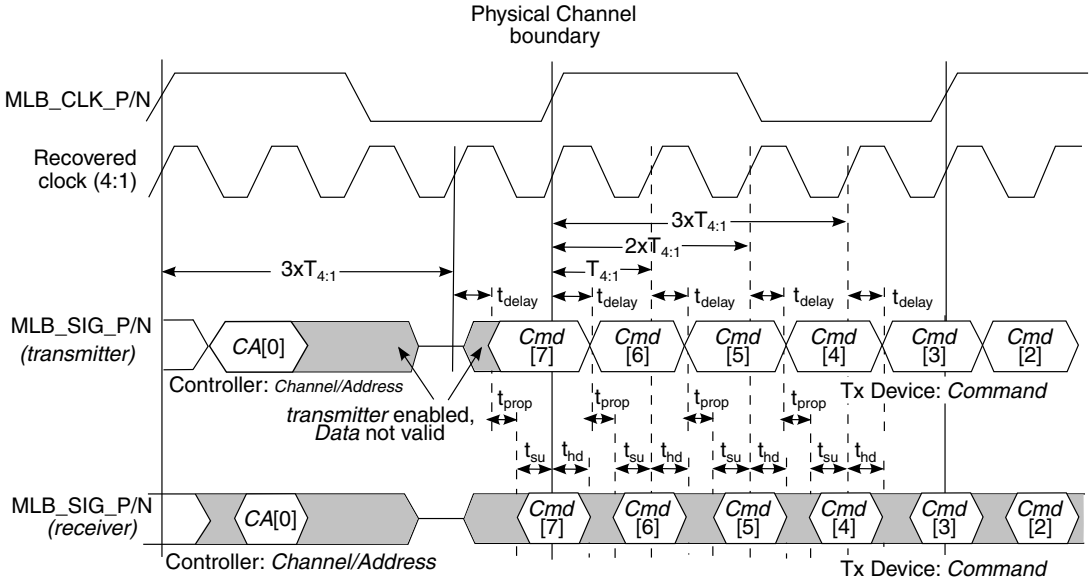


Figure 83. MLB 6-Pin Delay, Setup, and Hold Times

4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 84 depicts the timing of the PWM, and Table 78 lists the PWM timing parameters.

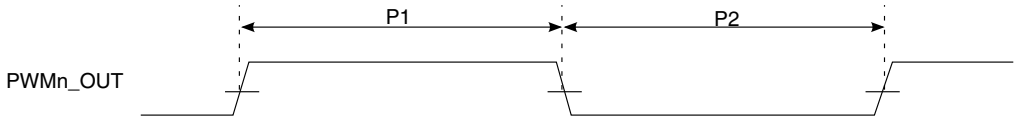


Figure 84. PWM Timing

Table 78. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 85 depicts the SJC test clock input timing. Figure 86 depicts the SJC boundary scan timing. Figure 87 depicts the SJC test access port. Signal parameters are listed in Table 79.

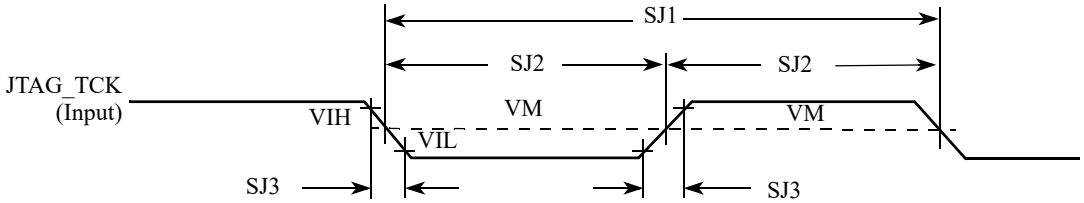


Figure 85. Test Clock Input Timing Diagram

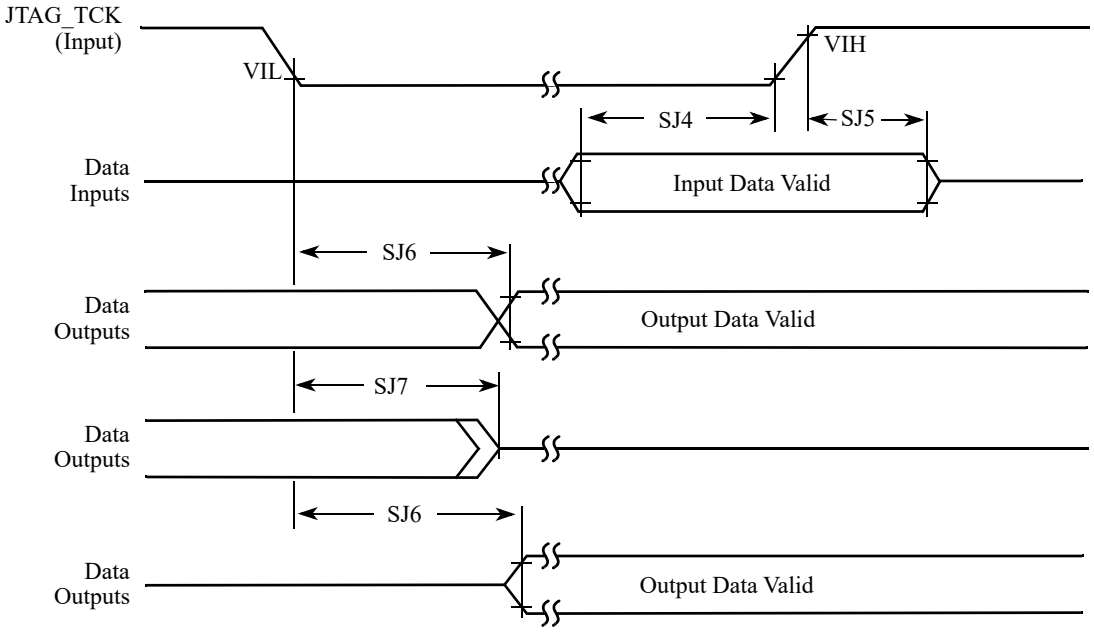


Figure 86. Boundary Scan (JTAG) Timing Diagram

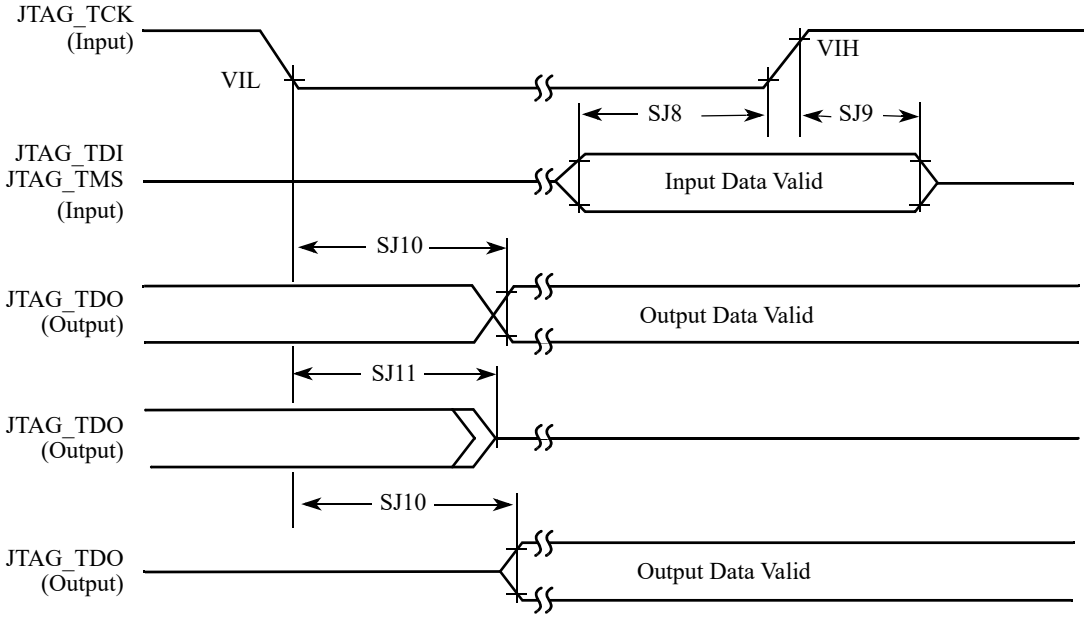


Figure 87. Test Access Port Timing Diagram

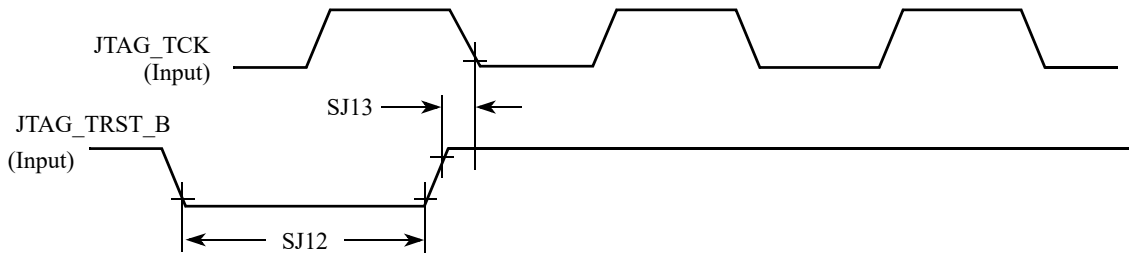


Figure 88. JTAG_TRST_B Timing Diagram

Table 79. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figure 89 and Figure 90 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 80. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

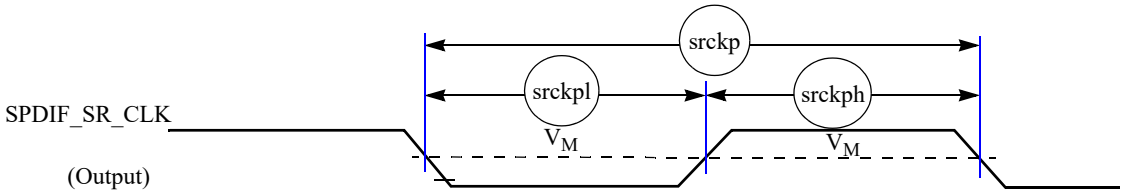


Figure 89. SPDIF_SR_CLK Timing Diagram

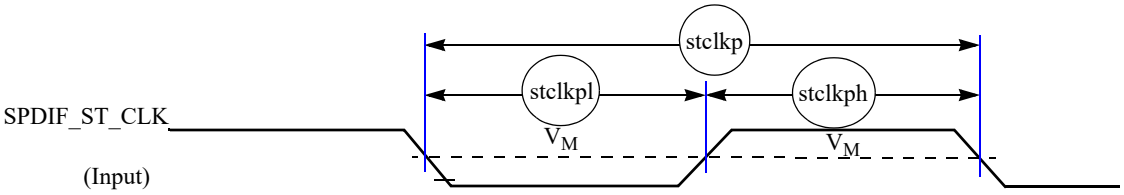


Figure 90. SPDIF_ST_CLK Timing Diagram

4.11.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 81.

Table 81. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External—AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External—EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External—EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 91 depicts the SSI transmitter internal clock timing and Table 82 lists the timing parameters for the SSI transmitter internal clock.

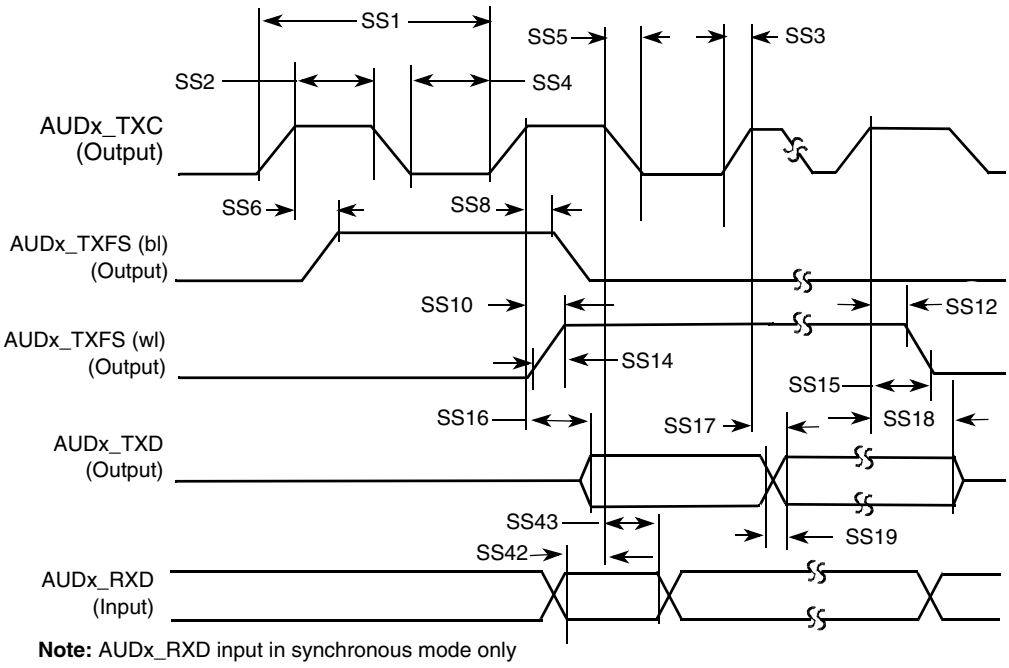


Figure 91. SSI Transmitter Internal Clock Timing Diagram

Table 82. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 92 depicts the SSI receiver internal clock timing and Table 83 lists the timing parameters for the receiver timing with the internal clock.

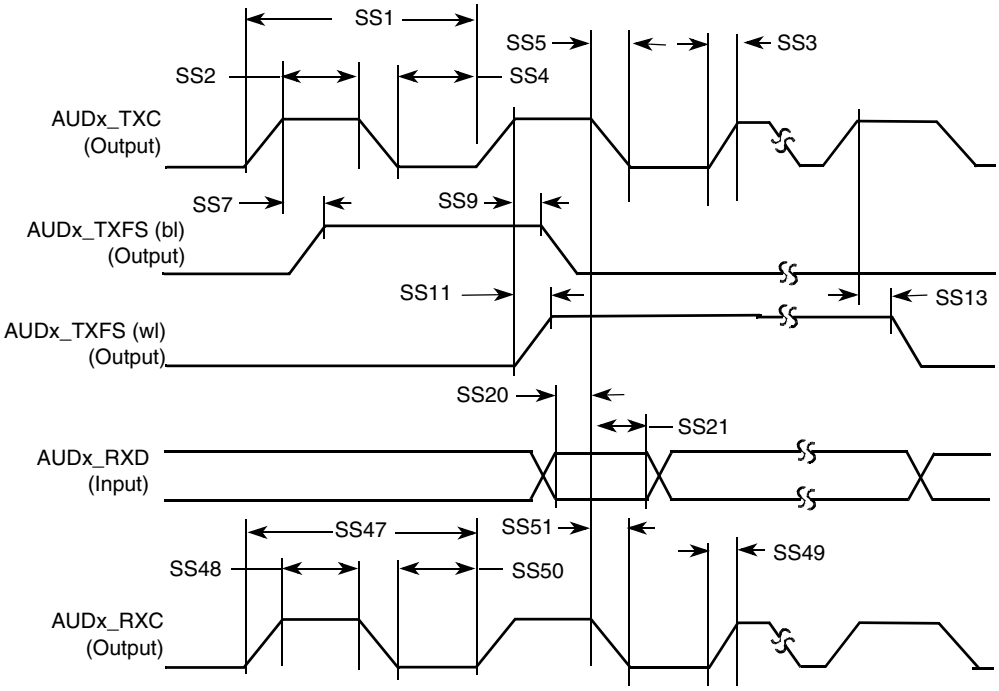


Figure 92. SSI Receiver Internal Clock Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 83. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 93 depicts the SSI transmitter external clock timing and Table 84 lists the timing parameters for the transmitter timing with the external clock.

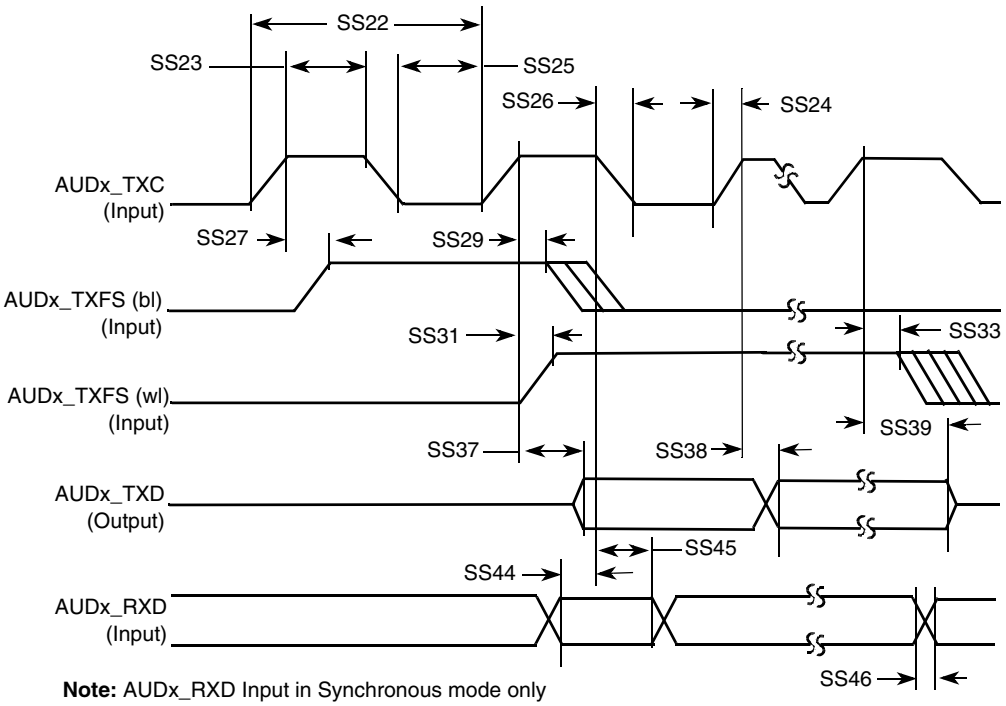


Figure 93. SSI Transmitter External Clock Timing Diagram

Table 84. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	-10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	-10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.19.4 SSI Receiver Timing with External Clock

Figure 94 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

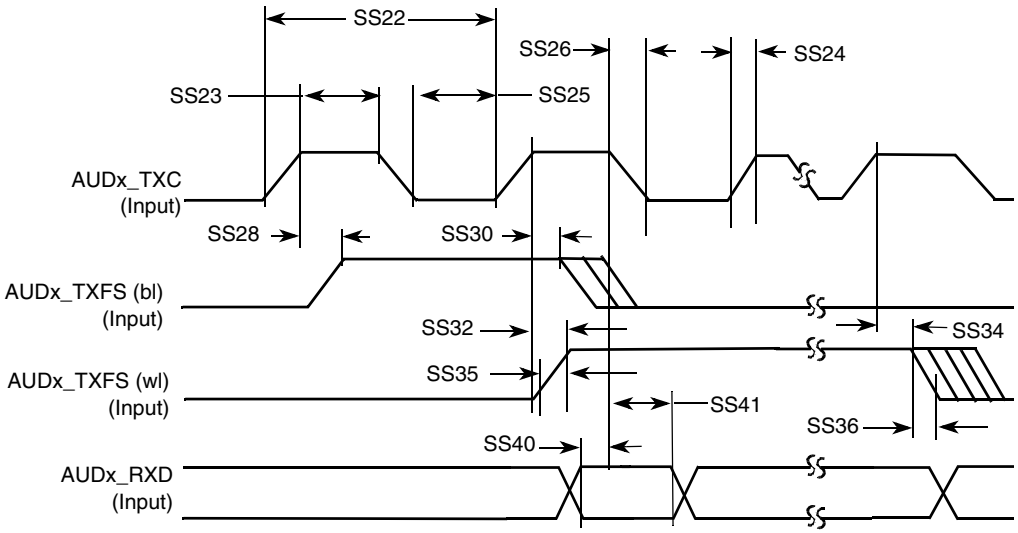


Figure 94. SSI Receiver External Clock Timing Diagram

Table 85. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	-10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	-10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters

4.11.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Solo/6DualLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_ B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.20.2.1 UART Transmitter

Figure 95 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 87 lists the UART RS-232 serial mode transmit timing characteristics.

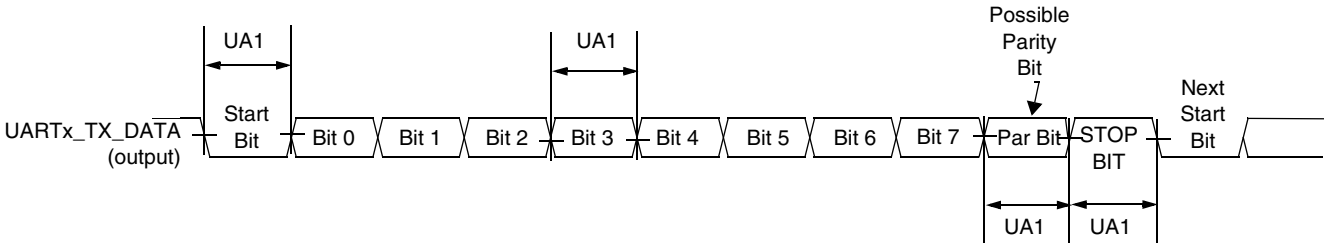


Figure 95. UART RS-232 Serial Mode Transmit Timing Diagram

Table 87. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.11.20.2.2 UART Receiver

Figure 96 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 88 lists serial mode receive timing characteristics.

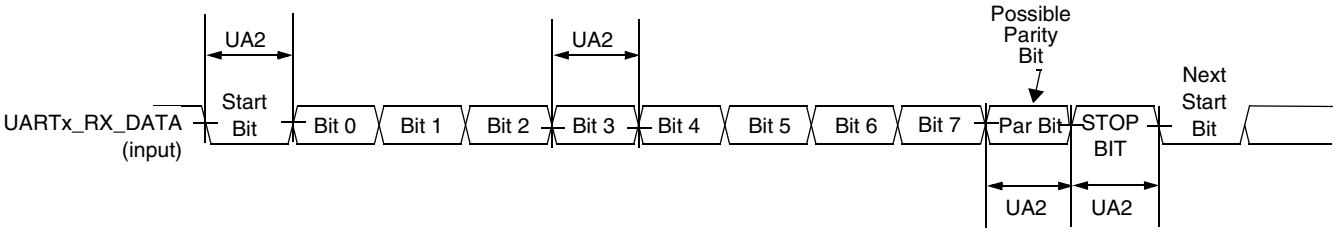


Figure 96. UART RS-232 Serial Mode Receive Timing Diagram

Table 88. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$[2] - $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 97 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 89 lists the transmit timing characteristics.

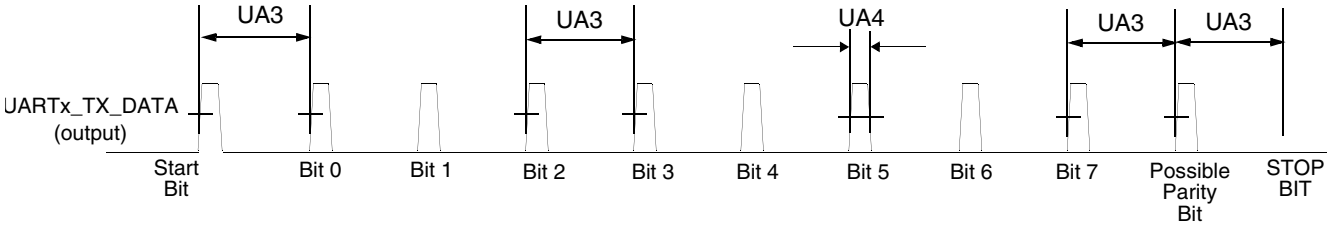


Figure 97. UART IrDA Mode Transmit Timing Diagram

Table 89. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$	$(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 98 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 90 lists the receive timing characteristics.

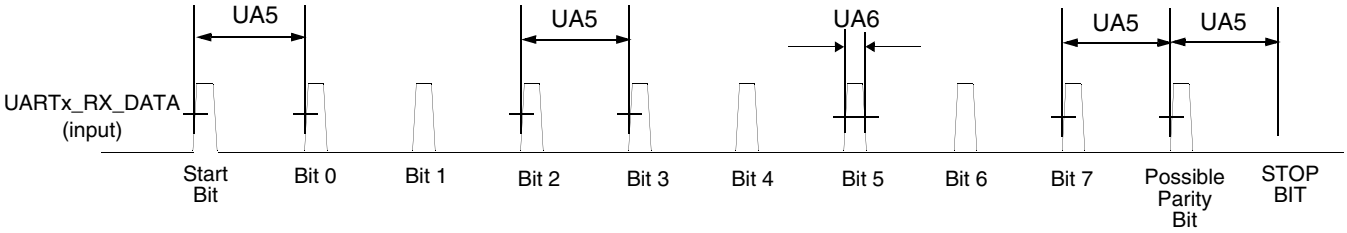


Figure 98. UART IrDA Mode Receive Timing Diagram

Table 90. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}$[2] - $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.21.1 Transmit Timing

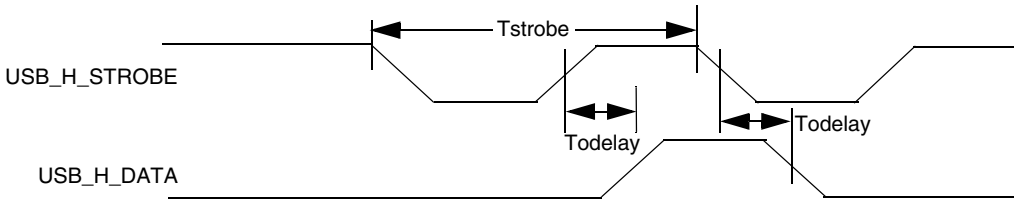


Figure 99. USB HSIC Transmit Waveform

Table 91. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.21.2 Receive Timing

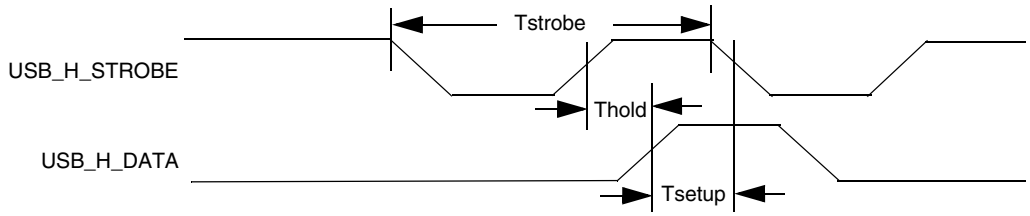


Figure 100. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification

— Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  — Revision 1.2, December 7, 2010
  — Portable device only

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 93 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 93. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	N/A
BOOT_MODE0	Input	N/A
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = ‘0’. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Device Interface Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interface Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3,DISP0_DAT4,DISP0_DAT5,DISP0_DAT6	—

Table 94. Interface Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD, SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, GPIO_1, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, GPIO_4, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, SD3_RST, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_ALE, NANDF_CS1	1, 4, or 8 bit
I^2C	I^2C-1	EIM_D28, EIM_D21	—
I^2C	I^2C-2	EIM_D16, EIM_EB2	—
I^2C	I^2C-3	EIM_D18, EIM_D17	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, etc.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

6.2 21x21 mm Package Information

6.2.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

Figure 101 shows the top, bottom, and side views of the 21×21 mm BGA package.

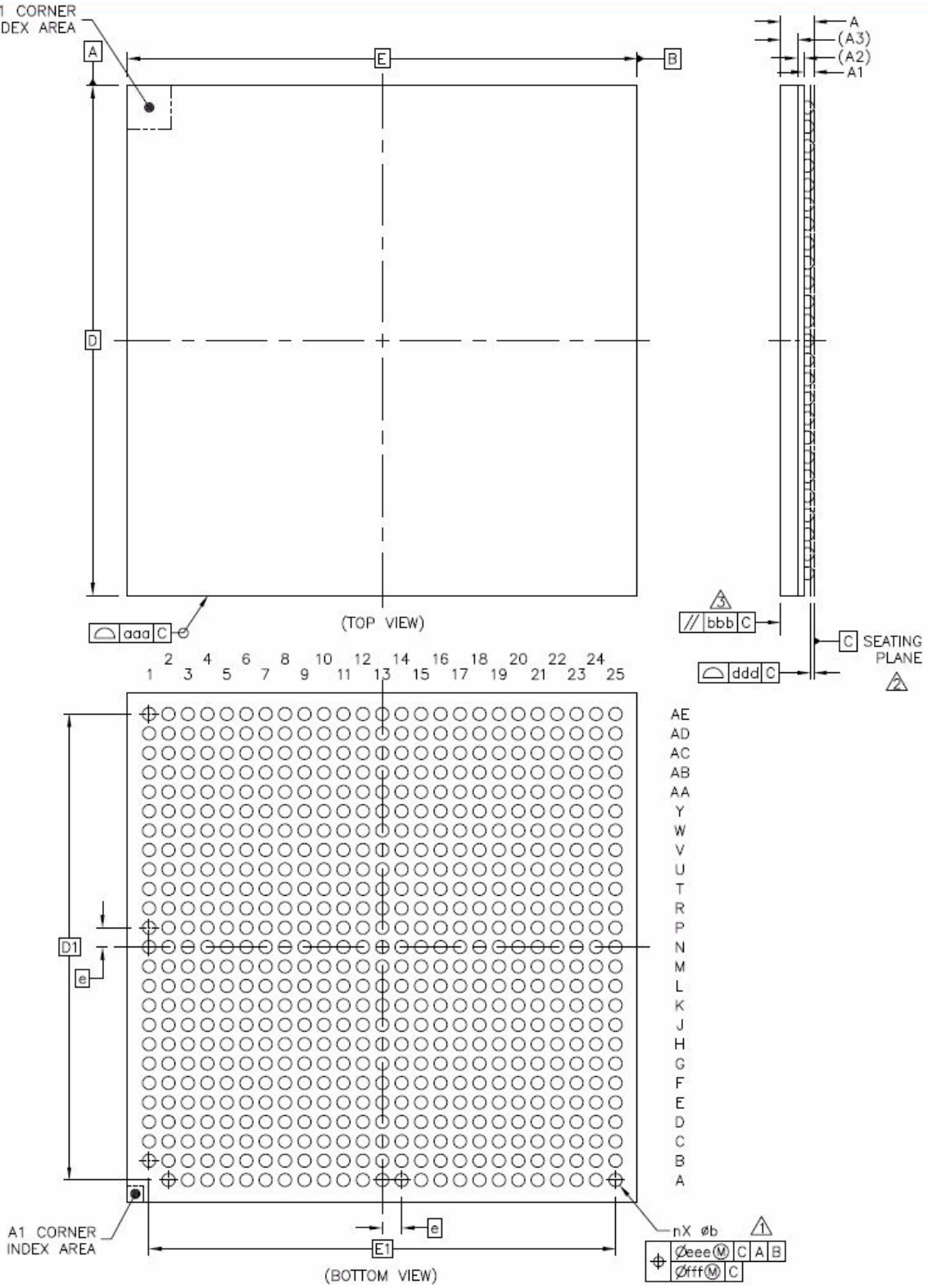


Figure 101. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 95 shows the 21 × 21 mm BGA package details.

Table 95. 21 x 21, 0.8 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	—	—	1.6
Stand Off	A1	0.36	—	0.46
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.7 REF		
Body Size	D	21 BSC		
	E	21 BSC		
Ball Diameter	—	0.5		
Ball Opening	—	0.4		
Ball Width	b	0.44	—	0.64
Ball Pitch	e	0.8 BSC		
Ball Count	n	624		
Edge Ball Center to Center	D1	19.2 BSC		
	E1	19.2 BSC		
Body Center to Contact Ball	SD	—		
	SE	—		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.2		
Coplanarity	ddd	0.15		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.08		

6.2.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 96 shows supplies contact assignments for the 21 x 21 mm package.

Table 96. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	—
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	—
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 96. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
PCIE_REXT	A2	—
PCIE_VP	H7	—
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H11, H13, J11, J13, K11, K13, L11, L13, M11, M13, N11, N13, P11, P13, R11, R13	Secondary supply for core (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K9, K14, L9, L14, M9, M14, N9, N14, P9, P14, R9, R14, T9, U9	Primary supply for the Arm core's regulator
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for VPU and GPUs (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for SoC and PU regulators (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V Domain (internal regulator output—requires capacitor if internal regulator is used)
USB_H1_VBUS	D10	Primary supply for the 3 V regulator
USB_OTG_VBUS	E9	Primary supply for the 3 V regulator
HDMI_DDCCEC	K2	Analog Ground (Ground reference for the Hot Plug Detect signal)
FA_ANA	A5	—
GPANAIO	C8	Analog output for NXP use only. This output must remain unconnected.
VDD_FA	B5	—

Table 96. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
ZQPAD	AE17	Connect ZQPAD to an external 240 Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.
NC	**For i.MX 6DualLite:** A12, A14, B12, B14, C14, E1, E2, F1, F2, G12, G13, N12 **For i.MX 6Solo:** A12, A14, B12, B14, C14, E1, E2, F1, F2, G12, G13, N12, W25, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y25, AA17, AA18, AA20, AA21, AA23, AA24, AA25, AB18, AB19, AB20, AB21, AB22, AB23, AB25, AC18, AC19, AC20, AC21, AC22, AC23, AC24, AC25, AD18, AD20, AD21, AD23, AD24, AD25, AE18, AE19, AE20, AE21, AE22, AE23, AE24	These signals are not functional and must remain unconnected by the user.

Table 97 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 97. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDDHIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDDHIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDDHIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	ANALOG	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	ANALOG	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	ANALOG	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	ANALOG	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	ANALOG	—	CSI_DATA1_N	—	—
CSI_D1P	D2	NVCC_MIPI	ANALOG	—	CSI_DATA1_P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	100 kΩ pull-up
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	100 kΩ pull-up
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	100 kΩ pull-up
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	100 kΩ pull-up
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	100 kΩ pull-up
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	100 kΩ pull-up
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	100 kΩ pull-up
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	100 kΩ pull-up
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	100 kΩ pull-up
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	100 kΩ pull-up
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	100 kΩ pull-up
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	100 kΩ pull-up
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	100 kΩ pull-up
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	100 kΩ pull-up
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	100 kΩ pull-up
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	100 kΩ pull-up
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	100 kΩ pull-up
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	100 kΩ pull-up
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	100 kΩ pull-up
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	100 kΩ pull-up
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	100 kΩ pull-up
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	100 kΩ pull-up
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	100 kΩ pull-up
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	100 kΩ pull-up
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	100 kΩ pull-up
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	100 kΩ pull-up
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	100 kΩ pull-up
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	100 kΩ pull-up
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	100 kΩ pull-up
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	100 kΩ pull-up
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	100 kΩ pull-up
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	100 kΩ pull-up
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	100 kΩ pull-up
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	100 kΩ pull-up
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	100 kΩ pull-up
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	100 kΩ pull-up
Note: DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.							
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	100 kΩ pull-up
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	—	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK1_P	Output	Low

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	—	—	DRAM_SDCLK1_N	—	—
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	Low
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	Low
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	—	—	DRAM_SDQS0_N	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	—	—	DRAM_SDQS1_N	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	—	—	DRAM_SDQS2_N	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	—	—	DRAM_SDQS3_N	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	—	—	DRAM_SDQS4_N	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	—	—	DRAM_SDQS5_N	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	—	—	DRAM_SDQS6_N	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	—	—	DRAM_SDQS7_N	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	DRAM_SDWE	Output	Low
DSI_CLK0M	H3	NVCC_MIPI	ANALOG	—	DSI_CLK_N	—	—
DSI_CLK0P	H4	NVCC_MIPI	ANALOG	—	DSI_CLK_P	—	—
DSI_D0M	G2	NVCC_MIPI	ANALOG	—	DSI_DATA0_N	—	—
DSI_D0P	G1	NVCC_MIPI	ANALOG	—	DSI_DATA0_P	—	—
DSI_D1M	H2	NVCC_MIPI	ANALOG	—	DSI_DATA1_N	—	—
DSI_D1P	H1	NVCC_MIPI	ANALOG	—	DSI_DATA1_P	—	—
EIM_A16	H25	NVCC_EIM	GPIO	ALT0	EIM_ADDR16	Output	Low
EIM_A17	G24	NVCC_EIM	GPIO	ALT0	EIM_ADDR17	Output	Low
EIM_A18	J22	NVCC_EIM	GPIO	ALT0	EIM_ADDR18	Output	Low
EIM_A19	G25	NVCC_EIM	GPIO	ALT0	EIM_ADDR19	Output	Low
EIM_A20	H22	NVCC_EIM	GPIO	ALT0	EIM_ADDR20	Output	Low
EIM_A21	H23	NVCC_EIM	GPIO	ALT0	EIM_ADDR21	Output	Low
EIM_A22	F24	NVCC_EIM	GPIO	ALT0	EIM_ADDR22	Output	Low
EIM_A23	J21	NVCC_EIM	GPIO	ALT0	EIM_ADDR23	Output	Low
EIM_A24	F25	NVCC_EIM	GPIO	ALT0	EIM_ADDR24	Output	Low
EIM_A25	H19	NVCC_EIM	GPIO	ALT0	EIM_ADDR25	Output	Low

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	EIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	EIM_CS0	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	EIM_CS1	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	GPIO3_IO16	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	GPIO3_IO17	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	GPIO3_IO18	Input	100 kΩ pull-up
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	GPIO3_IO19	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	GPIO3_IO20	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	GPIO3_IO21	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	GPIO3_IO22	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	GPIO3_IO23	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	GPIO3_IO24	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	GPIO3_IO25	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	GPIO3_IO26	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	GPIO3_IO27	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	GPIO3_IO28	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	GPIO3_IO29	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	GPIO3_IO30	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	GPIO3_IO31	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	EIM_AD00	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	EIM_AD01	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	EIM_AD10	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	EIM_AD11	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	EIM_AD12	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	EIM_AD13	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	EIM_AD14	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	EIM_AD15	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	EIM_AD02	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	EIM_AD03	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	EIM_AD04	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	EIM_AD05	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	EIM_AD06	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	EIM_AD07	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	EIM_AD08	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	EIM_AD09	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	EIM_EB0	Output	High

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_EB1	K23	NVCC_EIM	GPIO	ALT0	EIM_EB1	Output	High
EIM_EB2	E22	NVCC_EIM	GPIO	ALT5	GPIO2_IO30	Input	100 kΩ pull-up
EIM_EB3	F23	NVCC_EIM	GPIO	ALT5	GPIO2_IO31	Input	100 kΩ pull-up
EIM_LBA	K22	NVCC_EIM	GPIO	ALT0	EIM_LBA	Output	High
EIM_OE	J24	NVCC_EIM	GPIO	ALT0	EIM_OE	Output	High
EIM_RW	K20	NVCC_EIM	GPIO	ALT0	EIM_RW	Output	High
EIM_WAIT	M25	NVCC_EIM	GPIO	ALT0	EIM_WAIT	Input	100 kΩ pull-up
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	100 kΩ pull-up
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	100 kΩ pull-up
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	100 kΩ pull-up
ENET_REF_CLK[3]	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	100 kΩ pull-up
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	100 kΩ pull-up
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	100 kΩ pull-up
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	100 kΩ pull-up
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	100 kΩ pull-up
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	100 kΩ pull-up
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	100 kΩ pull-up
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	100 kΩ pull-down
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	100 kΩ pull-up
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	100 kΩ pull-up
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	100 kΩ pull-up
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	100 kΩ pull-up
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	100 kΩ pull-up
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	100 kΩ pull-up
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	100 kΩ pull-up
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	100 kΩ pull-up
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	100 kΩ pull-up
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	100 kΩ pull-up
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	100 kΩ pull-up
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	100 kΩ pull-up
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	J6	HDMI	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	K5	HDMI	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	K6	HDMI	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	J3	HDMI	—	—	HDMI_TX_DATA1_N	—	—

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
HDMI_D1P	J4	HDMI	—	—	HDMI_TX_DATA1_P	—	—
HDMI_D2M	K3	HDMI	—	—	HDMI_TX_DATA2_N	—	—
HDMI_D2P	K4	HDMI	—	—	HDMI_TX_DATA2_P	—	—
HDMI_HPD	K1	HDMI	—	—	HDMI_TX_HPD	—	—
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	JTAG_MODE	Input	100 kΩ pull-up
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	JTAG_TDO	Output	Low
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	JTAG_TRSTB	Input	47 kΩ pull-up
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO06	Input	100 kΩ pull-up
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	GPIO4_IO08	Input	100 kΩ pull-up
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO10	Input	100 kΩ pull-up
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO12	Input	100 kΩ pull-up
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO14	Input	100 kΩ pull-up
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO07	Input	100 kΩ pull-up
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO09	Input	100 kΩ pull-up
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	GPIO4_IO11	Input	100 kΩ pull-up
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	GPIO4_IO13	Input	100 kΩ pull-up
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO15	Input	100 kΩ pull-down
LVDS0_CLK_N	V4	NVCC_LVDS2P5	—	—	LVDS0_CLK_N	—	—
LVDS0_CLK_P	V3	NVCC_LVDS2P5	—	ALT0	LVDS0_CLK_P	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5	—	—	LVDS0_TX0_N	—	—
LVDS0_TX0_P	U1	NVCC_LVDS2P5	—	ALT0	LVDS0_TX0_P	Input	Keeper
LVDS0_TX1_N	U4	NVCC_LVDS2P5	—	—	LVDS0_TX1_N	—	—
LVDS0_TX1_P	U3	NVCC_LVDS2P5	—	ALT0	LVDS0_TX1_P	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5	—	—	LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS2P5	—	ALT0	LVDS0_TX2_P	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5	—	—	LVDS0_TX3_N	—	—
LVDS0_TX3_P	W1	NVCC_LVDS2P5	—	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5	—	—	LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS2P5	—	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5	—	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS2P5	—	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5	—	—	LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS2P5	—	ALT0	LVDS1_TX1_P	Input	Keeper

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
LVDS1_TX2_N	AB1	NVCC_LVDS2P5	—	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS2P5	—	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5	—	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS2P5	—	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP	—	—	MLB_CLK_N	—	—
MLB_CP	B11	VDDHIGH_CAP	—	—	MLB_CLK_P	—	—
MLB_DN	B10	VDDHIGH_CAP	—	—	MLB_DATA_N	—	—
MLB_DP	A10	VDDHIGH_CAP	—	—	MLB_DATA_P	—	—
MLB_SN	A9	VDDHIGH_CAP	—	—	MLB_SIG_N	—	—
MLB_SP	B9	VDDHIGH_CAP	—	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	100 kΩ pull-up
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	SRC_ONOFF	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open drain with PU(100K) enable
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	100 kΩ pull-down
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	100 kΩ pull-up
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	100 kΩ pull-up
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	100 kΩ pull-up
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	100 kΩ pull-up
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	100 kΩ pull-up
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	100 kΩ pull-up
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	100 kΩ pull-down
TEST_MODE	E12	VDD_SNVS_IN	GPIO	ALT0	TCU_TEST_MODE	Input	100 kΩ pull-down
USB_H1_DN	F10	VDDUSB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	E10	VDDUSB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	B8	VDDUSB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDDUSB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A6	VDDUSB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A7	NVCC_PLL_OUT	—	—	XTALI	—	—
XTALO	B7	NVCC_PLL_OUT	—	—	XTALO	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 23, "GPIO DC Parameters," on page 40
- Table 24, "LPDDR2 I/O DC Electrical Parameters," on page 41
- Table 25, "DDR3/DDR3L I/O DC Electrical Characteristics," on page 42

3 ENET_REF_CLK is used as a clock source for MII and RGMII modes only. RGMII mode uses either GPIO_16 or RGMII_TX_CTL as a clock source. For more information on these clocks, see the device Reference Manual and the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

Table 98. Signals with Differing Before Reset and After Reset States

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A16	Input	PD (100K)
EIM_A17	Input	PD (100K)
EIM_A18	Input	PD (100K)
EIM_A19	Input	PD (100K)

Table 98. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A20	Input	PD (100K)
EIM_A21	Input	PD (100K)
EIM_A22	Input	PD (100K)
EIM_A23	Input	PD (100K)
EIM_A24	Input	PD (100K)
EIM_A25	Input	PD (100K)
EIM_DA0	Input	PD (100K)
EIM_DA1	Input	PD (100K)
EIM_DA2	Input	PD (100K)
EIM_DA3	Input	PD (100K)
EIM_DA4	Input	PD (100K)
EIM_DA5	Input	PD (100K)
EIM_DA6	Input	PD (100K)
EIM_DA7	Input	PD (100K)
EIM_DA8	Input	PD (100K)
EIM_DA9	Input	PD (100K)
EIM_DA10	Input	PD (100K)
EIM_DA11	Input	PD (100K)
EIM_DA12	Input	PD (100K)
EIM_DA13	Input	PD (100K)
EIM_DA14	Input	PD (100K)
EIM_DA15	Input	PD (100K)
EIM_EB0	Input	PD (100K)
EIM_EB1	Input	PD (100K)
EIM_EB2	Input	PD (100K)
EIM_EB3	Input	PD (100K)
EIM_LBA	Input	PD (100K)
EIM_RW	Input	PD (100K)
EIM_WAIT	Input	PD (100K)
GPIO_17	Output	Drive state unknown (x)

Table 98. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.2.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 99 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo

	A	B	C	D	E	F	G	
1		PCIE_RXM	GND	CSI_D1M	NC	NC	DSI_D0P	1
2	PCIE_REXT	PCIE_RXP	JTAG_TRSTB	CSI_D1P	NC	NC	DSI_D0M	2
3	PCIE_TXM	PCIE_TXP	JTAG_TMS	GND	CSI_D0P	CSI_CLK0P	GND	3
4	GND	GND	GND	CSI_REXT	CSI_D0M	CSI_CLK0M	DSI_REXT	4
5	FA_ANA	VDD_FA	CLK2_N	CLK2_P	GND	GND	JTAG_TDI	5
6	USB_OTG_DP	USB_OTG_DN	GND	GND	GND	GND	JTAG_TDO	6
7	XTALI	XTALO	CLK1_N	CLK1_P	GND	GND	PCIE_VPH	7
8	GND	USB_OTG_CHD_B	GPANAIO	GND	NVCC_PLL_OUT	GND	PCIE_VPTX	8
9	MLB_SN	MLB_SP	RTC_XTALO	RTC_XTALI	USB_OTG_VBUS	VDDUSB_CAP	VDD_SNVS_CAP	9
10	MLB_DP	MLB_DN	GND	USB_H1_VBUS	USB_H1_DP	USB_H1_DN	GND	10
11	MLB_CN	MLB_CP	POR_B	PMIC_ON_REQ	TAMPER	PMIC_STBY_REQ	VDD_SNVS_IN	11
12	NC	NC	BOOT_MODE0	ONOFF	TEST_MODE	BOOT_MODE1	NC	12
13	GND	SD3_CMD	SD3_DAT5	SD3_DAT4	SD3_DAT6	SD3_DAT7	NC	13
14	NC	NC	NC	SD3_CLK	SD3_DAT0	SD3_DAT1	NVCC_SD3	14
15	SD3_DAT2	SD3_DAT3	NANDF_CLE	SD3_RST	NANDF_WP_B	NANDF_CS0	NVCC_NANDF	15
16	NANDF_ALE	NANDF_RB0	NANDF_CS1	NANDF_CS3	SD4_CLK	NANDF_D2	NVCC_SD1	16
17	NANDF_CS2	SD4_CMD	NANDF_D1	NANDF_D3	NANDF_D6	SD4_DAT2	NVCC_SD2	17
18	NANDF_D0	NANDF_D5	NANDF_D7	SD4_DAT0	SD4_DAT4	SD1_DAT3	NVCC_RGMII	18
19	NANDF_D4	SD4_DAT1	SD4_DAT5	SD4_DAT7	SD1_DAT2	SD2_CMD	GND	19
20	SD4_DAT3	SD4_DAT6	SD1_DAT1	SD1_CLK	SD2_DAT1	RGMII_TD1	EIM_D20	20
21	SD1_DAT0	SD1_CMD	SD2_CLK	RGMII_TXC	RGMII_TD2	EIM_D17	EIM_D19	21
22	SD2_DAT0	SD2_DAT3	RGMII_TD0	RGMII_RX_CTL	EIM_EB2	EIM_D24	EIM_D25	22
23	SD2_DAT2	RGMII_RD1	RGMII_TX_CTL	RGMII_RD3	EIM_D22	EIM_EB3	EIM_D28	23
24	RGMII_TD3	RGMII_RD2	RGMII_RD0	EIM_D18	EIM_D26	EIM_A22	EIM_A17	24
25	GND	RGMII_RXC	EIM_D16	EIM_D23	EIM_D27	EIM_A24	EIM_A19	25
	A	B	C	D	E	F	G	

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

R	P	N	M	L	K	J	H	
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	1
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	2
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	3
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	4
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	5
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	6
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	7
GND	GND	GND	GND	GND	GND	GND	GND	8
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	9
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	10
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	11
GND	GND	NC	GND	GND	GND	GND	GND	12
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	13
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	14
GND	GND	GND	GND	GND	GND	GND	GND	15
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	16
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	17
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND	18
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	19
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	20
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	21
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	22
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	23
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	24
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	25
R	P	N	M	L	K	J	H	

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

AC	AB	AA	Y	W	V	U	T	
DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	**1**
DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	**2**
DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	**3**
DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	**4**
DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	**5**
DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	**6**
DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	**7**
DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND	**8**
DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	**9**
DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	**10**
DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	**11**
DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND	**12**
DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	**13**
DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	**14**
DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	**15**
DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	**16**
DRAM_A13	DRAM_SDODT1	NC	NC	GND	NVCC_DRAM	GND	GND	**17**
NC	NC	NC	NC	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	**18**
NC	NC	GND	NC	GND	GND	GND	GND	**19**
NC	NC	NC	NC	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	**20**
NC	NC	NC	NC	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	**21**
NC	NC	GND	NC	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	**22**
NC	NC	NC	NC	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	**23**
NC	GND	NC	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	**24**
NC	NC	NC	NC	NC	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	**25**
AC	**AB**	**AA**	**Y**	**W**	**V**	**U**	**T**	

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

	AE	AD	
1	GND	DRAM_D5	1
2	DRAM_D1	DRAM_D0	2
3	DRAM_SDQS0	DRAM_SDQS0_B	3
4	DRAM_D7	GND	4
5	DRAM_D9	DRAM_D8	5
6	DRAM_SDQS1_B	DRAM_SDQS1	6
7	DRAM_	GND	7
8	DRAM_SDQS2_B	DRAM_SDQS2	8
9	DRAM_D24	DRAM_D29	9
10	DRAM_DQM3	GND	10
11	DRAM_D26	DRAM_D30	11
12	DRAM_A9	DRAM_A12	12
13	DRAM_A5	GND	13
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	14
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	15
16	DRAM_CAS	GND	16
17	ZQPAD	DRAM_CS1	17
18	NC	NC	18
19	NC	GND	19
20	NC	NC	20
21	NC	NC	21
22	NC	GND	22
23	NC	NC	23
24	NC	NC	24
25	GND	NC	25
	AE	AD	

Table 100 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite

	D	C	B	A	
1	CSI_D1M	GND	PCIE_RXM		1
2	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
3	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
4	CSI_REXT	GND	GND	GND	4
5	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
6	GND	GND	USB_OTG_DN	USB_OTG_DP	6
7	CLK1_P	CLK1_N	XTALO	XTALI	7
8	GND	GPANAIO	USB_OTG_CHD_B	GND	8
9	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
10	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
11	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
12	ONOFF	BOOT_MODE0	NC	NC	12
13	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
14	SD3_CLK	NC	NC	NC	14
15	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
16	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
17	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
18	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
19	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
20	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
21	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
22	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
23	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
24	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
25	EIM_D23	EIM_D16	RGMII_RXC	GND	25
	D	C	B	A	

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

M	L	K	J	H	G	F	E	
CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC	**1**
CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC	**2**
CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P	**3**
CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M	**4**
CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND	**5**
CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND	**6**
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND	**7**
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT	**8**
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS	**9**
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP	**10**
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER	**11**
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE	**12**
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6	**13**
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0	**14**
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B	**15**
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK	**16**
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6	**17**
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4	**18**
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2	**19**
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1	**20**
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2	**21**
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2	**22**
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22	**23**
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26	**24**
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27	**25**
M	**L**	**K**	**J**	**H**	**G**	**F**	**E**	

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

Y	W	V	U	T	R	P	N	
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4	**1**
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC	**2**
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7	**3**
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6	**4**
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9	**5**
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8	**6**
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI	**7**
DRAM_D21	GND	GND	GND	GND	GND	GND	GND	**8**
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	**9**
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND	**10**
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	**11**
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC	**12**
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	**13**
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN	**14**
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND	**15**
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	**16**
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP	**17**
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND	**18**
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	**19**
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3	**20**
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15	**21**
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK	**22**
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14	**23**
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15	**24**
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2	**25**
Y	**W**	**V**	**U**	**T**	**R**	**P**	**N**	

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

	AE	AD	AC	AB	AA	
1	GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	1
2	DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	2
3	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N	3
4	DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P	4
5	DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3	5
6	DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10	6
7	DRAM_D11	GND	DRAM_D15	DRAM_D16	GND	7
8	DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17	8
9	DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23	9
10	DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND	10
11	DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1	11
12	DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14	12
13	DRAM_A5	GND	DRAM_A6	DRAM_A8	GND	13
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2	14
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10	15
16	DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND	16
17	ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32	17
18	DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33	18
19	DRAM_D35	GND	DRAM_D39	DRAM_D38	GND	19
20	DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45	20
21	DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57	21
22	DRAM_D49	GND	DRAM_D48	DRAM_D52	GND	22
23	DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61	23
24	DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B	24
25	GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7	25
	AE	AD	AC	AB	AA	

7 Revision History

Table 101 provides the current revision history for this data sheet. Table 102 provides a revision history for previous revisions.

Table 101. i.MX 6Solo/6DualLite Data Sheet Document Rev. 9 History

Rev. Number	Date	Substantive Changes
9	10/2018	Changes to Revision 9 include the following: • Table 3, "Special Signal Considerations," on page 21: Corrected, – Row: NC, from “These signals are No Connected …” to read, “These signals are not functional and must remain unconnected by the user.” • Table 8, "Operating Ranges," on page 26: Corrected footnote 6: – Changed *from*: “When VDD_SOC_IN does not supply… then maximum setting can be 1.3V.” – Changed *to*: “When using VDD_SOC_CAP to supply the PCIE_VP and PCIE_VPTX, the maximum setting is 1.175V. …” • Table 53, "eMMC4.4/4.41 Interface Timing Specification," on page 80, – Row: SD2, uSDHC Output Delay: Changed t_{OD} from 2.5ns minimum to 2.8ns and 7.1ns maximum to 6.8ns. • Table 96, "21 x 21 mm Supplies Contact Assignments," on page 140: Corrected, – Last row: NC, from “—” to read, These signals are not functional and must remain unconnected by the user.
8	09/2017	• Replaced ipp_dse with DSE throughout. • Section 1, “Introduction: Replaced text “low voltage DDR3” with “DDR3L” in the features list of i.MX 6Solo/6DualLite applications processors. • Table 1, "Example Orderable Part Numbers," on page 3: Added orderable part numbers. • Figure 1: Updated to include Rev 1.4 in Silicon Revision section. • Section 2.1, “Block Diagram: Updated WEIM with EIM in the block diagram. • Table 2, "i.MX 6Solo/6DualLite Modules List," on page 11: Rearranged alphabetically. • Table 6, "Absolute Maximum Ratings," on page 24: – Removed VDD_HIGH_IN supply voltage (LDO bypass) parameter. – Max. value of VDD_HIGH_CAP supply output voltage corrected to 2.85V. • Table 22: Updated test condition of “XTALI input leakage current at startup” parameter; replaced 32KHz RTC with 24MHz. • Added Section 4.6.4, “RGMII I/O 2.5V I/O DC Electrical Parameters. • Section 4.8.2, “DDR I/O Output Buffer Impedance: Modified introductory text. • Corrected Figure 22, "Asynchronous A/D Muxed Write Access," on page 60. • Table 53, "eMMC4.4/4.41 Interface Timing Specification," on page 80: – Added the following footnote to Card Input Clock section: 1 Clock duty cycle will be in the range of 47% to 53%. – Min. value of uSDHC Input Setup Time reduced to 1.7ns.

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories

Rev. Number	Date	Substantive Changes
7	10/2016	• Figure 1, "Part Number Nomenclature—i.MX 6Solo and 6DualLite," on page 5: Added to Silicon Revision block: Revision 1.2 and 1.3 and associated Mask ID. • Table 6, "Absolute Maximum Ratings," on page 24: – NVCC_DRAM maximum value changed to 1.975 V. – Included footnote to NVCC_DRAM maximum value regarding maximum voltage allowance. – Added row to Vin/Vout I/O supply voltage, separating DDR pins and non-DDR pins and included footnote regarding maximum voltage allowance. • Table 8, "Operating Ranges," on page 26: Added footnotes within the Comments column for the Run Mode, LDO Enabled row; VDD_SOC_IN maximum values. • Section 4.6.3, “DDR I/O DC Parameters: Added reference for more DDR details to see the MMDC section. Moved JEDEC standard information to footnote. • Section 4.7.2, “DDR I/O AC Parameters: Added reference for more DDR details to see the MMDC section. Moved JEDEC standard information to footnote. • Table 44, "i.MX 6Solo Supported DDR3/DDR3L/LPDDR2 Configurations," on page 63: Changed LPDDR2 Channel column from “Dual” to “Single.” • Table 45, "i.MX 6DualLite Supported DDR3/DDR3L/LPDDR2 Configurations," on page 64: Added LPDDR2 Dual Channel column. • Table 95, "21 x 21, 0.8 mm BGA Package Details," on page 139: Correction to package total thickness. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: DRAM_SDCKL*n* rows, reverted to “Low” rather than “0” in the Value column.

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
6	8/2016	• Changed throughout: - LVDDR3 to DDR3L - Changed terminology from “floating” to “not connected”. • Table 2, "i.MX 6Solo/6DualLite Modules List," on page 11: - uSDHC1–4, SD/MMC and SDXC Enhanced Multi-Media Card/Secure Digital Host Controller row: Added new bullet at top: “Conforms to the SD Host Controller…”. - eCSPI1-4 row: removed from the Brief Description column, “with data rate up to 52Mbit/s.” - BCH row, removed from Brief Description column, “encryption/decryption”. • Table 3, "Special Signal Considerations," on page 21: - GPANAIO row, modified remarks to be NXP use only. - SRC_POR_B row: removed reference to internal POR which is not supported on device. - TEST_MODE row: modified remarks to be NXP use only and added tie to Vss or remain unconnected. • Table 6, "Absolute Maximum Ratings," on page 24” throughout table: clarified parameter descriptions including adding LDO state. Clarified symbol names. - Added row, RGMII I/O supply voltage. - Added VDD_HIGH_CAP supply voltage row for LDO output. - Added to USB supply voltage row: USB_OTG_CHD_B. - All maximum voltages increased (improved). • Section 4.1.2, “Thermal Resistance: added NOTE. • Table 8, "Operating Ranges," on page 26: Changed minimum parameter of Run mode: LDO enabled from 1.175 to 1.25 V. • Section 4.2.1, “Power-Up Sequence”: Removed references to the internal POR function. Internal POR is not supported. Removed fourth and fifth bullets. • Section 4.2.3, “Power Supplies Usage”: Added NOTE, “When the PCIE interface is not used…”. • Section 4.5.2, “OSC32K”: Removed battery resistor (coin cell) calculation. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters”: - Added 3 rows: Input capacitance; Startup current; and DC input current. - Added footnote to RTC_XTALI high-level DC input voltage at the Max parameter. - Added NOTE following table: “The Vil and Vih only apply when external clock source is used…”. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”: this new section added, replacing the original section 4.9.4 “DDR SRAM Specific Parameters (DDR3/DDR3L and LPDDR2)”. • Figure 36, "ECSPI Master Mode Timing Diagram," on page 73: Added note, “ECSPI_MOSI always…”. • Figure 37, "ECSPI Slave Mode Timing Diagram," on page 74: Added note, “ECSPI_MOSI always driven…”. • Figure 42, "SDR50/SDR104 Timing," on page 81: Aligned SD4 and SD5. • Table 54, "SDR50/SDR104 Interface Timing Specification," on page 81: - Corrected Clock High Time ID to SD3. - Changed SD2 and SD3 Min and max values to 0.46 and 0.54. - Changed SD5 Max to 0.74. • Table 64, "Camera Input Signal Cross Reference, Format, and Bits Per Cycle," on page 93: Changed RGB565 column heading from 2 to 1 cycle. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: - Table row: DRAM_SDCLK0 and DRAM_SDCLK1 changed Out of Reset Condition from Low to 0. - Added to ZQPAD row: requirement to add resistor to GND.
5	6/2015	• Table 8, “Operating Ranges,” Run mode: LDO enabled row; Changed comments for VDD_ARM_IN, from “1.05V minimum for operation up to 396MHz” to “1.125V minimum for operation up to 396MHz”. • Table 3, “Special Signal Considerations,” XTALI/XTALO row: Changed from “The crystal must be rated...”, to “See Hardware Development Guide”.

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
Rev. 4	12/2014	• Table 1, "Example Orderable Part Numbers," on page 3: Speed Grade footnote added as follows: If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz. • Table 1, "Example Orderable Part Numbers," on page 3: Added (4) devices; SCIMX6U5DVM10BC/CC and SCIMX6S5DVM10BC/CC. • Figure 1, “Part Number Nomenclature—i.MX 6Solo and 6DualLite”: Added Silicon Rev 1.3. to diagram • Table 2, Modules List, UART 1–5 Description changed: baud rate up from 5MHz to 5Mbps. • Added Figure 2, "Example Part Marking," on page 5. • Section 1.2, “Features”: under, *Miscellaneous IPs and interfaces*: Changed *UARTs* bullet, from “up to 4.0 Mbps”, to “up to 5.0 Mbps”. • Table 8, “Operating Ranges,” on page 29: — Changed *Run mode: VDD_ARM_IN* minimum value from 1.05 to 1.125V; for operation up to 396 MHz. and changed *LDO bypassed* maximum value from 1.225V to 1.21V; for *VDD_SOC_IN*. — Changed *PCIe supply voltages; PCIE_VP/PCIE_VPTX* maximum value from 1.225V to 1.21V • Table 10, "Maximum Supply Currents," on page 29; — Changed *VDD_ARM_IN* from single condition to include DualLite and Solo conditions with Maximum current values of 2200 and 1320 mA, respectively. — Added footnote for NVCC_LVDS2P5 supply. • Table 38, “Reset Timing Parameters”: Removed footnote regarding SRC_POR_B rise and fall times. • Section 4.9.3, “External Interface Module (EIM)”: Changed first paragraph to describe two systems clocks used with EIM: ACLK_EIM_SLOW_CLK_ROOT and ACLK_EXSC (for synchronous mode). • Table 31, “DDR I/O DDR3/DDR3L Mode AC Parameters”; Added footnote about extended range for Vix. • Table 48, “DDR3/DDR3L Timing Parameter Table,” on page 76; Added DDR0, tCK(avg) and parameter values. Changed symbol names DDR1 through DDR7 to include avg or base; changed minimum parameter values for DDR4–DDR7. Added footnote about tIS and tIH base values. • Figure 25, “DDR3 Command and Address Timing Parameters,” on page 76; Added DDR0. • Table 49, “DDR3/DDR3L Write Cycle,” on page 77; Changed symbol names of DDR17 and DDR18 to include base(AC150/DC100); Changed Units from tCK to tCK(avg). • Table 46, “LPDDR2 Write Cycle,” on page 64; Changed LP21 min/max parameter values from -0.25/+0.25 to 0.75/1.25. • Table 42, "EIM Bus Timing Parameters," on page 55: Changed footnotes regarding the system clocks used with EIM: from *axi_clk* to *ACLK_EXSC* or *ACLK_EIM_SLOW_CLK_ROOT.* • Table 49, “DDR3/DDR3L Write Cycle,” on page 77: Changed *DDR17* minimum value from 420 ps to 125 ps and *DDR18* from 345 ps to 150 ps. • Table 49, “DDR3/DDR3L Write Cycle,” on page 77: Added footnote 4. • Table 69, "LVDS Display Bridge (LDB) Electrical Specification," on page 105: Corrected Units for Output Voltage High and Output Voltage Low from mV to V. • Table 71, "Electrical and Timing Information," on page 108: Moved rows *tSETUP[RX]* and *tHOLD[RX]* to be directly under *HS Line Receiver AC Specifications* heading row. • Table 96, "21 x 21 mm Supplies Contact Assignments," on page 140: Removed A1 pin. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: Moved rows *DRAM_4*, *DRAM_5,* and *DRAM_6* out of the i.MX 6DualLite section (shaded gray) to the i.MX 6Solo section above DRAM_7 and (unshaded). • Table 99, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo," on page 156: Removed “NC” from A1 pin location. • Table 100, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite," on page 159: Removed “NC” from A1 pin location.

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
Rev. 3	02/2014	• Updates throughout for Silicon revision C, including: - Figure 1 Part number nomenclature diagram - Table 1 Example Orderable Part Numbers • Feature descriptions updated for: - Camera sensors: updated from one to two ports at up to 240 MHz peak. - Miscellaneous IPs and interfaces; SSI and ESAI. • Table 2, Modules List, uSDHC 1–4 description change: including SDXC cards up to 2 TB. • Table 2, Modules List, UART 1–5 description change: programmable baud rate up to 5 MHz. • Table 3, Special Signal Considerations: XTALOSC_RTC_XTALI/RTC_XTALO: ending paragraph removed. Was: “In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect XTALOSC_RTC_XTALI to GND and keep RTC_XTALO floating.” • Table 8, Operating Ranges for Run mode LDO bypassed: Added footnote regarding alternate maximum voltage on VDD_SOC_IN … this maximum can be 1.3V. • Table 8, Operating Ranges Standby/DSM mode: Added footnote regarding alternate maximum voltage on VDD_SOC_IN … this maximum can be 1.3V. • Table 8, Operating Ranges GPIO supply voltages: Corrected supply name to NVCC_NANDF • Table 8, Operating ranges: updated table footnotes for clarity. • Removed table “On-Chip LDOs and their On-Chip Loads.” • Section 4.1.4, External Clock Sources; added Note, “The internal RTC oscillator does not...”. • Section 4.1.5, Maximum Supply Currents: Reworded second paragraph about the power management IC to explain that a robust thermal design is required for the increased system power dissipation. • Table 10, Maximum Supply Currents: NVCC_RGMII Condition value corrected to N=6. • Table 10, Maximum Supply Currents: Corrected supply name NVCC_NANDF. • Table 10, Maximum Supply currents: Added row NVCC_LVDS2P5 • Section 4.2.1, Power-Up Sequence: Clarified wording of third bulleted item regarding POR control. • Section 4.2.1, Power-Up Sequence: Removed Note. • Section 4.2.1, Power-Up Sequence: Corrected bullet regarding VDD_ARM_CAP / VDD_SOC_CAP difference from 50 mV to 100 mV. • Section 4.5.2, OSC32K, second paragraph reworded to describe OSC32K automatic switching. • Section 4.5.2, OSC32K, added Note following second paragraph to caution use of internal oscillator. • Table 23, XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih minimum value to 0.8. • Table 23, XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih maximum value to 1.1. • Table 39, Reset Timing Parameters; removed rise/fall time requirement • Section 4.9.3, External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies.
Rev. 3 continued	2/2014	• Table 42, EIM Bus Timing Parameters; reworded footnotes for clarity. • Table 42, EIM Asynchronous Timing Parameters; removed comment from the Max heading cell. • Figure 60, Gated Clock Mode Timing Diagram: Corrected HSYNC trace behavior • Table 66, Video Signal Cross-Reference: Corrected naming of HSYNC and VSYNC • Section 4.11.22, USB PHY Parameters: Updated Battery Charging Specification bullet • Table 95, BGA Package Details: Corrected to read “21 x 21, 0.8 mm”. • Table 96, Supplies Contact Assignments: Corrected supply name NVCC_NANDF • Table 96, Supplies Contact Assignments: Updated NC rows to show i.MX 6DualLite vs. i.MX 6Solo • Table 97, Functional Contact Assignments: ALT5 Default function signal names corrected • Table 97, Functional Contact Assignments: PMIC_ON_REQ Out of Reset value corrected to “Open Drain with PU (100K) enabled” • Table 97, Functional Contact Assignments: TEST_MODE row included • Table 97, Functional Contact Assignments: VDD_ARM_IN and ZQPAD row removed

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
Rev. 2.2	8/2013	• 21x21 functional contact table: changed from NAND to NANDF • System Timing Parameters Table 39, *Reset timing parameter*, CC1 description, change from: “Duration of SRC_POR_B to be qualified as valid (<= 5 ns)” to: “Duration of SRC_POR_B to be qualified as valid” and added a footnote to the parameter with the following text: “SRC_POR_B rise and fall times must be 5 ns or less.”
Rev. 2.1	5/2013	Substantive changes throughout this document are as follows: • Incorporated standardized signal names. This change is extensive throughout. • Added reference to EB792, i.MX Signal Name Mapping. • Figures updated to align to standardized signal names. • Updated references to eMMC standard to include 4.41. • Added MediaLB (MLB) feature and DTCP module to the commercial temperature grade version. • Figure 1 Part Number Nomenclature: Updates to Part differentiator section to align with Table 1. • Table 1 “Orderable Part Numbers,” added Arm core information to the Options column: 2x “Arm Cortex-A9” 64-bit to 6DualLite 1x “Arm Cortex -A9” 32-bit to 6Solo • Table 2 Changed reference to Global Power Controller to read General Power Controller. • Table 8 “Operating Ranges,” added reference for information on product lifetime: i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note, AN4725. • Table 10 “Maximum Supply Currents,” updated footnote 2. • Table 11 Stop Mode Current and Power Consumption: Added SNVS Only mode. • Table 60 RGMII parameter TskewT minimum and maximum values corrected. • Table 60 RGMII parameter TskewR units corrected. • Table 97 Clarification of ENET_REF_CLK naming. • Added Table 98, "Signals with Differing Before Reset and After Reset States," on page 153. • Removed section, EIM Signal Cross Reference. Signal names are now aligned with reference manual. • Removed table from Section 3.2, “Recommended Connections for Unused Analog Interfaces and referenced the Hardware Development Guide. • Section 1.2, “Features added bulleted item regarding the SOC-level memory system. • Section 1.2, “Features Camera sensors: Changed Camera port to be up to 180 MHz peak. • Added Section 1.3, “Updated Signal Naming Convention • Section 4.2.1, “Power-Up Sequence” updated wording. • Section 4.3.2, “Regulators for Analog Modules” section updates. • Added Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters.” • Section 4.10, “General-Purpose Media Interface (GPMI) Timing” figures replaced, tables revised.

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