M32000D4AFP

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M32000D4AFP is a new generation microcomputer with a 32-bit CPU and built-in high capacity DRAM. Using this device it is possible to implement the complex applications of the multimedia age with high performance and low power consumption.

The M32000D4AFP contains 2M bytes of DRAM and 4K bytes of cache memory. The CPU is implemented with a RISC architecture and has a high performance figure of 52.4 MIPS (at an internal clock rate of 66.6 MHz). Memory for main storage is provided internally to the device eliminating external memory and associated control circuits thus reducing overall system noise and power consumption.

The CPU, internal DRAM and cache memory are connected by a 128-bit, 15 ns/cycle internal bus which virtually eliminates transfer bottlenecks in between the CPU and the memory. The M32000D4AFP internally multiplies the frequency of the input clock signals by four. For an internal operating frequency of 66.6 MHz the input clock frequency is 16.65MHz.

A 16-bit data and 24-bit address bus are the M32000D4AFP's external bus and the interface to external peripheral controllers. When the hold state is set, the internal DRAM can be accessed from an external device.

A 3-chip basic system configuration using the M32000D4AFP is the device itself plus an ASIC as a peripheral controller and a program ROM. Execution starts from the reset vector entry on the external ROM after power on, a program requiring high speed execution is then transferred to internal DRAM and this is then executed. The M32000D4AFP also has a slave mode additional to its master mode. When set to slave mode the M32000D4AFP can be used as a coprocessor. In this mode it does not access its external bus immediatly after reset, but waits for the master to start its operation.

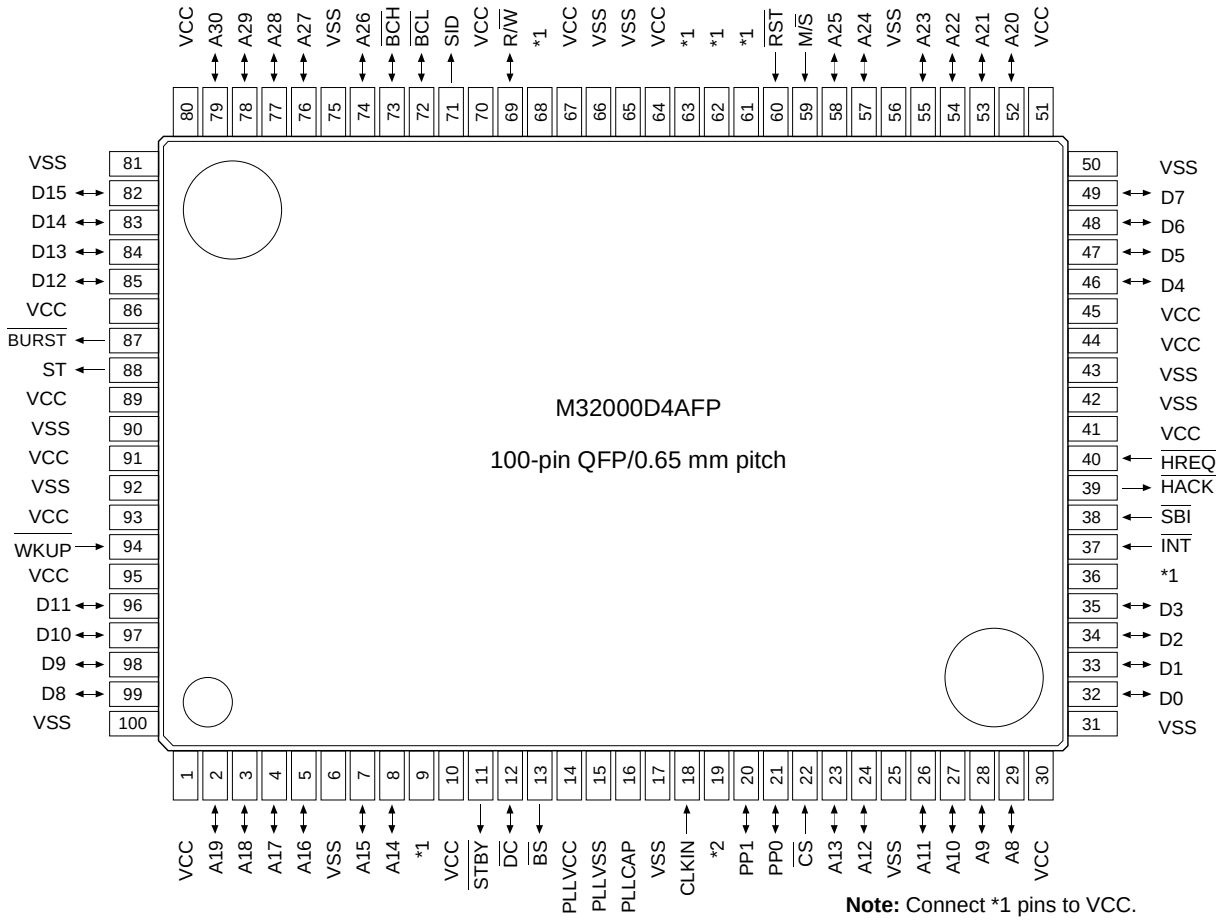
FEATURES

- CPU ..... M32R family CPU core
- Pipeline ..... 5 steps
- Basic bus cycle ..... 15 ns (at internal 66.6 MHz)
- Logical address space ..... 4G-byte linear
- External bus ..... data bus: 16 bits
  address bus: 24 bits
- Internal DRAM ..... 16M bits (2M bytes)
- Cache ..... 4K bytes (direct map)
- Register configuration ..... general-purpose registers: 32 bits x 16
  control registers: 32 bits x 5
- Instruction set ..... 83 instructions/6 addressing modes
- Instruction format ..... 16 bits/32 bits
- Multiply-accumulate operation unit (DSP function instruction)
- Internal memory controller
- Programmable I/O ports
- Power management function ..... standby mode
  /CPU sleep mode
- PLL clock generating circuit ..... four-time clock PLL circuit
- Operation mode ..... master/slave mode
- Interrupt input ..... $\overline{\text{INT}}$ and $\overline{\text{SBI}}$
- Power source ..... 3.3 V (±10 %)

APPLICATIONS

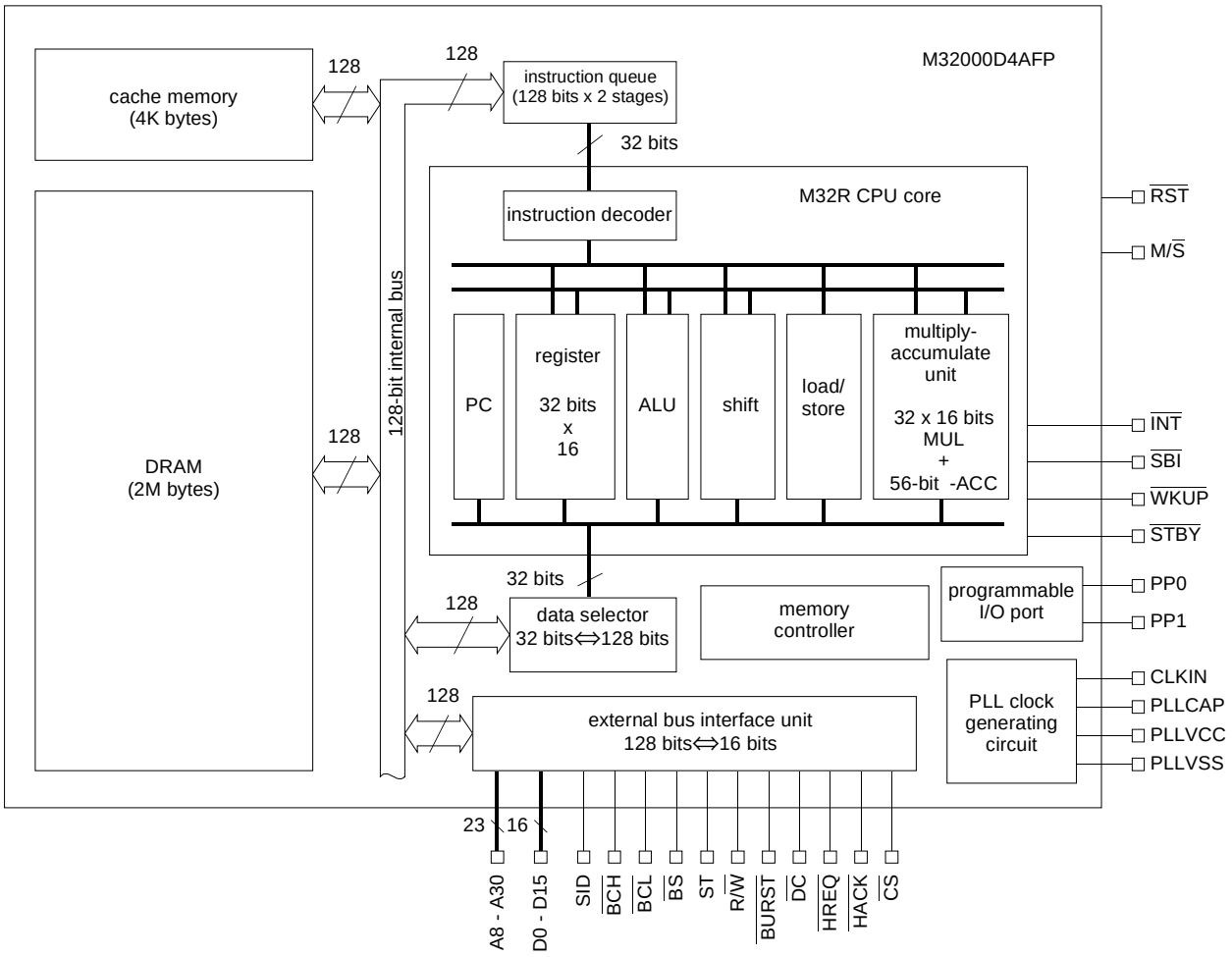
Portable equipment, Still camera, Navigation system,
Digital instrument, Printer, Scanner, FA equipment

PIN CONFIGURATION (TOP VIEW)



Note: Connect *1 pins to VCC.
Connect *2 pins to VSS.

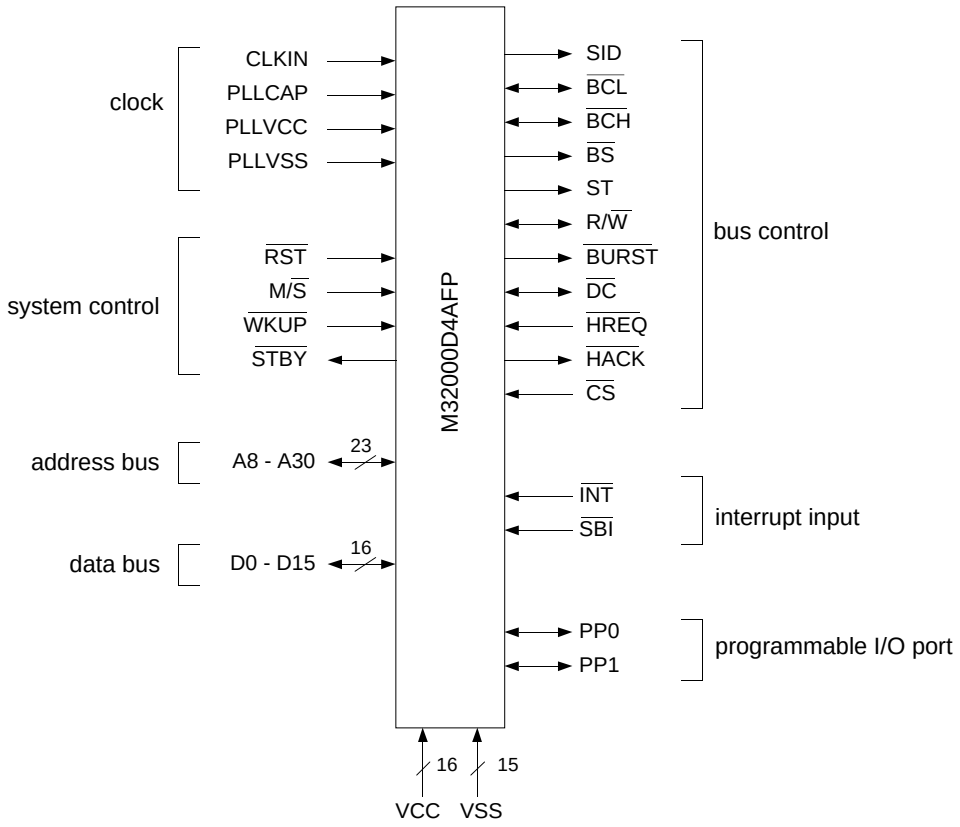
BLOCK DIAGRAM



FUNCTIONS

function block	characteristics
CPU core	• bus specification basic bus cycle: 15 ns (internal operation at 66.6 MHz) logical address space: linear 4G bytes external address bus: 24 bits (external output pin: A8 to A30, $\overline{BCH}$, $\overline{BCL}$) external data bus: 16 bits • implementation: 5-stage pipeline • core internal: 32 bits • register configuration general-purpose registers: 32 bits × 16 control registers: 32 bits × 5 • instruction set 16-bit/32-bit instruction format 83 instructions/6 addressing modes • multiply-accumulate operation built in
internal DRAM	• 16M bits (2M bytes)
cache memory	• 4K bytes (internal instruction/data cache mode, instruction cache mode, cache-off mode)
memory controller	• cache control • internal DRAM control, refresh control • power management function (standby mode, CPU sleep mode selection control)
programmable I/O port	• two programmable I/O ports

PIN FUNCTION DIAGRAM



PIN DESCRIPTION (1/3)

type	pin name	name	I/O	function
power source	VCC VSS	power source ground	– –	All power source pins should be connected to VCC. All ground pins should be connected to VSS.
clock	CLKIN	clock input	input	Clock input pin. The M32000D4AFP has an internal PLL multiplier circuit, and an input clock which is 1/4 of the internal operating frequency (when the internal operating frequency is 66.6 MHz, the CLKIN input is 16.65 MHz).
	PLLCAP	C connection for PLL	–	Connects a capacitor for the internal PLL.
	PLLVCC	power source for PLL	–	Power source for the internal PLL.
	PLLVSS	ground for PLL	–	Ground for the internal PLL.
system control	$\overline{RST}$	reset	input	Internally resets the M32000D4AFP. It is also used to return from standby mode and CPU sleep mode.
	M/$\overline{S}$	master/slave	input	Sets the M32000D4AFP default operation to either system bus master (M/$\overline{S}$ = "H") or bus slave (M/$\overline{S}$ = "L"). When the M32000D4AFP is set to bus slave, it does not carry out a reset vector entry fetch after a reset. The setting of M/$\overline{S}$ cannot be changed during operation. Keep at either an "H" or an "L" level.
	$\overline{WKUP}$	wakeup	input	Input pin to request return from standby mode. This is only accepted when $\overline{STBY}$ is "L" level. It generates the wakeup interrupt.
	$\overline{STBY}$	standby	output	Indicates that the M32000D4AFP has switched to standby mode. An "L" level is output while the device is in standby mode.
address bus	A8 to A30	address bus	I/O (Hi-z)*	The M32000D4AFP has a 24-bit address (A8 to A31) bus for a 16 MB address space. A31 is not output. During the write cycle, the valid byte positions on the 16-bit data bus are output as $\overline{BCH}$ or $\overline{BCL}$. During the read cycle, the 16-bit data bus is read, however,only data in the valid byte positions is transferred to the M32000D4AFP. Address bus pins are bidirectional. When accessing the internal DRAM from an external bus master while the M32000D4AFP is in the hold state, input the address from the system bus side.
data bus	D0 to D15	data bus	I/O (Hi-z)*	16-bit data bus for connecting to external devices.

* (Hi-z): This pin goes to high-impedance in the hold state.

PIN DESCRIPTION (2/3)

type	pin name	name	I/O	function
bus control	SID	space identifier	output (Hi-z)*	Space identifier between user space and I/O space. SID = "L": user space SID = "H": I/O space SID = undefined: when idle
	$\overline{BCH}$, $\overline{BCL}$	byte control	I/O (Hi-z)*	Indicates the valid byte positions of transferred data. $\overline{BCH}$ corresponds to the MSB side (D0 to D7), and $\overline{BCL}$ corresponds to the LSB side (D8 to D15). During a read bus cycle, both $\overline{BCH}$ and $\overline{BCL}$ are an "L" level. During a write bus cycle, either $\overline{BCH}$ and/or $\overline{BCL}$ is an "L" level depending on the byte(s) to be written. When accessing the internal DRAM from an external bus master, the byte control signal is input from the system bus side.
	$\overline{BS}$	bus start	output (Hi-z)*	When the M32000D4AFP drives an external bus cycle, $\overline{BS}$ goes to an "L" level at the start of the bus cycle. In burst transfer, $\overline{BS}$ goes to the "L" level for each transfer cycle. When accessing internal resources such as an internal DRAM or internal I/O register, $\overline{BS}$ is not output.
	ST	bus status	output (Hi-z)*	Indicates whether the bus cycle that the M32000D4AFP drives is an instruction fetch access cycle or an operand access cycle. ST = "L": for instruction fetch access ST = "H": for operand access ST = undefined: when idle
	R/$\overline{W}$	read/write	I/O (Hi-z)*	Outputs R/$\overline{W}$ to identify whether the external bus cycle a read or a write cycle. When accessing the internal DRAM from an external bus master, R/W is input from the external bus.
	$\overline{BURST}$	burst	output (Hi-z)*	The M32000D4AFP drives two consecutive bus cycles to access 32-bit data allocated on the 32-bit word boundary. For instruction fetches, it drives 8 (max.) consecutive cycles (8 cycles in instruction cache mode) to data on the 128-bit boundary. During these consecutive bus cycles, $\overline{BURST}$ goes to "L" level. When accessing 32-bit data, an "L" level followed by an "H" level is output from address A30, because the MSB-side 16 bits are accessed prior to the LSB-side 16 bits. When accessing 128-bit data, the addresses are output from an arbitrary 16-bit aligned address and wraparound within a 128-bit aligned boundary.

* (Hi-z): This pin goes to high-impedance in the hold state.

PIN DESCRIPTION (3/3)

type	pin name	name	I/O	function
bus control (cont.)	$\overline{DC}$*	data complete	I/O (Hi-z)	When the M32000D4AFP drives an external bus cycle, it automatically inserts wait cycles until $\overline{DC}$ is input by the slave device in the system bus. When the M32000D4AFP is in the hold state and the internal DRAM is accessed from an external bus master, the M32000D4AFP outputs $\overline{DC}$ to notify to the external bus master that the bus cycle to the internal DRAM has been completed.
	$\overline{HREQ}$	hold	input	Bus right request input pin of the system bus. When $\overline{HREQ}$ is an "L" level, the M32000D4AFP switches to the hold state.
	$\overline{HACK}$	hold acknowledge	output	Indicates that the M32000D4AFP has switched to the hold state and releases the bus right of the system bus to the requestor.
	$\overline{CS}$	chip select	input	Signal input to the M32000D4AFP when it is in the hold state to request access to the internal DRAM from an external bus master. When an "L"level is input to $\overline{CS}$, the M32000D4AFP access accesses the internal DRAMat the address input via the address pins.
interrupt controller	$\overline{SBI}$	system break interrupt	input	System break interrupt input pin. The SBI is not masked by the IE bit in the PSW register. It is also used to return from CPU sleep mode and to request the start of operation in slave mode.
	$\overline{INT}$	external interrupt	input	External interrupt request input pin. It is also used to return from CPU sleep mode and to request the start of operation the slave mode.
programm-able I/O port	PP0, PP1	port	I/O	Two programmable I/O ports.

* The $\overline{DC}$ pin becomes an output pin when the $\overline{CS}$ signal is input to the M32000D4AFP.

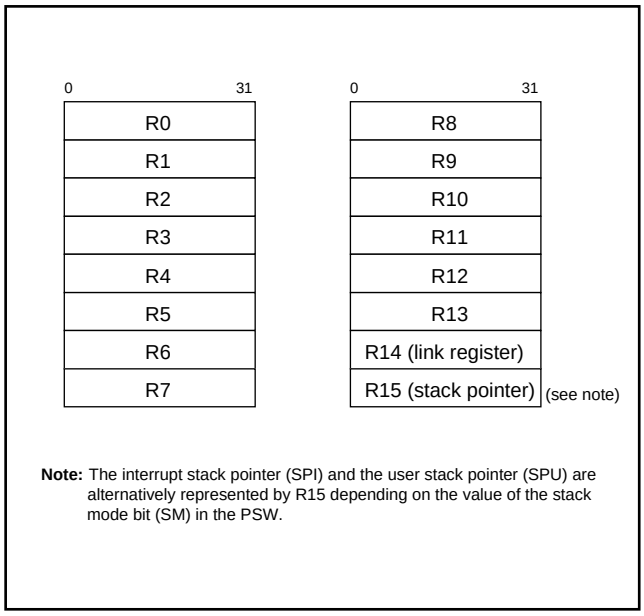
FUNCTIONAL DESCRIPTION

CPU

The M32R CPU has 16 general-purpose registers, 5 control registers, an accumulator and a program counter. The accumulator is of 64-bit width. The registers and program counter are of 32-bit width.

General-purpose registers

The 16 general-purpose registers (R0 - R15) are of 32-bit width and are used to retain data and base addresses. R14 is used as the link register and R15 as the stack pointer (SPI or SPU). The link register is used to store the return address when executing a subroutine call instruction. The interrupt stack pointer (SPI) and the user stack pointer (SPU) are alternatively represented by R15 depending on the value of the stack mode bit (SM) in the processor status word register (PSW).

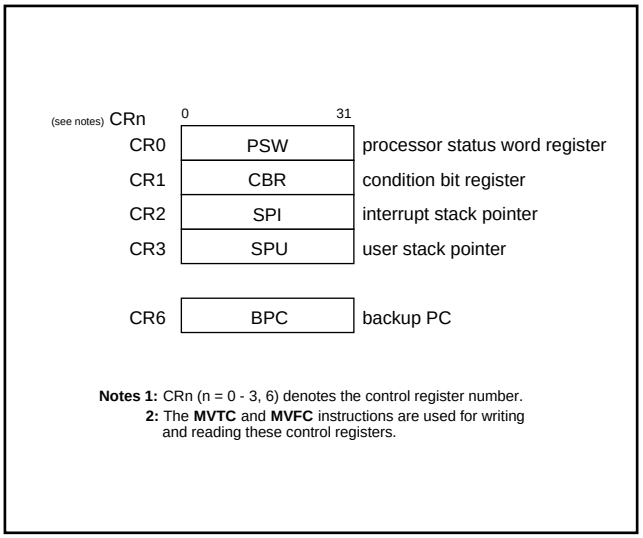


Note: The interrupt stack pointer (SPI) and the user stack pointer (SPU) are alternatively represented by R15 depending on the value of the stack mode bit (SM) in the PSW.

Fig. 1 General-purpose registers

Control registers

There are 5 control registers which are the processor status word register (PSW), the condition bit register (CBR), the interrupt stack pointer (SPI), the user stack pointer (SPU) and the backup PC (BPC). The **MVTC** and **MVFC** instructions are used for writing and reading these control registers.



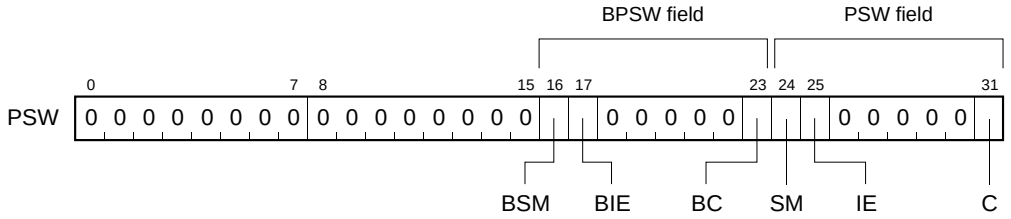
Notes 1: CRn (n = 0 - 3, 6) denotes the control register number.
2: The **MVTC** and **MVFC** instructions are used for writing and reading these control registers.

Fig. 2 Control registers

Processor status word register: PSW (CR0)

The processor status word register (PSW) shows the M32R CPU status. It consists of the current PSW field, and the BPSW field where a copy of the PSW field is saved when EIT occurs.

The PSW field is made up of the stack mode bit (SM), the interrupt enable bit (IE) and the condition bit (C). The BPSW field is made up of the backup stack mode bit (BSM), the backup interrupt enable bit (BIE) and the backup condition bit (BC).



D	bit name	function	init.	R	W
16	BSM (backup SM)	saves value of SM bit when EIT occurs	undefined	○	○
17	BIE (backup IE)	saves value of IE bit when EIT occurs	undefined	○	○
23	BC (backup C)	saves value of C bit when EIT occurs	undefined	○	○
24	SM (stack mode)	0: uses R15 as the interrupt stack pointer 1: uses R15 as the user stack pointer	0	○	○
25	IE (interrupt enable)	0: does not accept interrupt 1: accepts interrupt	0	○	○
31	C (condition bit)	indicates carry, borrow and overflow resulting from operations (instruction dependent)	0	○	○

Note: "init." ...initial state immediately after reset
"R" .... ○ : read enabled
"W" .... ○ : write enabled

Fig. 3 Processor status word register

Condition bit register

The condition bit register (CBR) is a separate read-only register which contains a copy of the current value of the condition bit (C) in the PSW. An attempt to write to the CBR with the **MVTC** instruction is ignored.

Interrupt stack pointer, User stack pointer

The interrupt stack pointer (SPI) and the user stack pointer (SPU) retain the current stack address. The SPI and SPU can be accessed as the general-purpose register R15. R15 switches between representing the SPI and SPU depending on the value of the stack mode bit (SM) in the PSW.

Backup PC

The backup PC (BPC) is the register where a copy of the PC value is saved when EIT occurs. Bit 31 is fixed at "0". When EIT occurs, the PC value immediately before EIT occurrence or that of the next instruction is set. The value of the BPC is reloaded to the PC when the **RTE** instruction is executed. However, the values of the lower 2 bits of the PC become "00" on returning (It always returns to the word boundary).

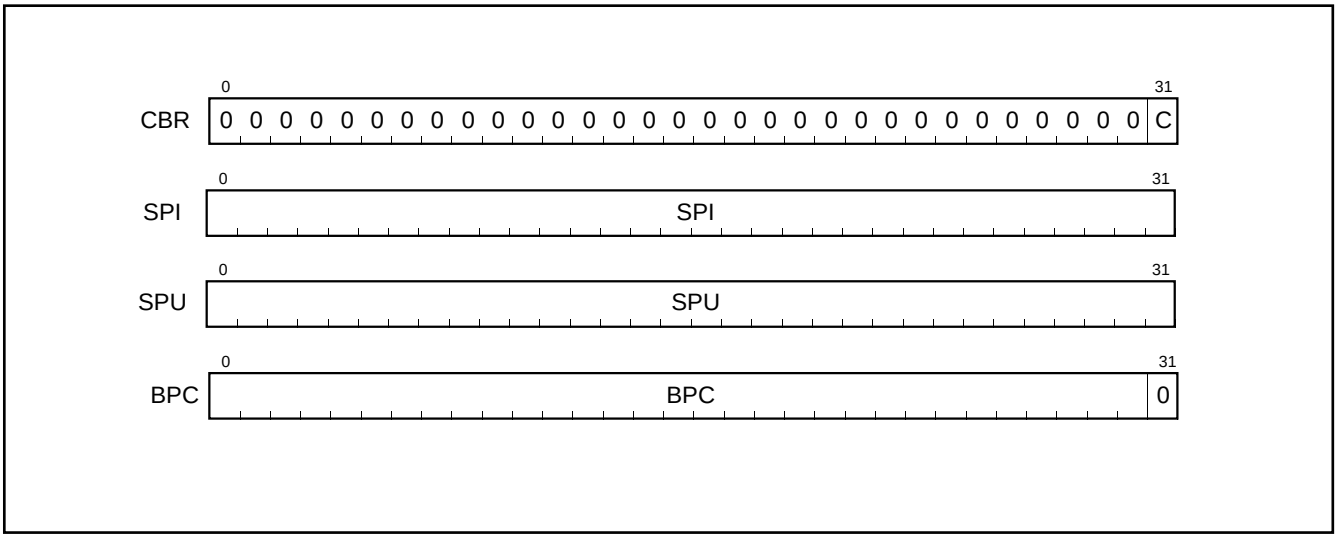


Fig. 4 Condition bit register, interrupt stack pointer, user stack pointer and backup PC

Accumulator

The accumulator (ACC) is a 64-bit register used for DSP type functions. Use the **MVTACHI** and **MVTACLO** instructions for writing to the accumulator. The high-order 32 bits (bit 0 - bit 31) can be set with the **MVTACHI** instruction and the low-order 32 bits (bit 32 - bit 63) can be set with the **MVTACLO** instruction. Use the **MVFACHI**, **MVFACLO** and **MVFACMI** instructions for reading from the accumulator. The high-order 32 bits (bit 0 - bit 31) are read with the **MVFACHI** instruction, the low order 32 bits (bit 32 - bit 63) with the **MVFACLO** instruction and the middle 32 bits (bit 16 - bit 47) with the **MVFACMI** instruction.

Program counter

The program counter (PC) is a 32-bit counter that retains the address of the instruction being executed. Since the M32R CPU instruction starts with even-numbered addresses, the LSB (bit 31) is always "0".

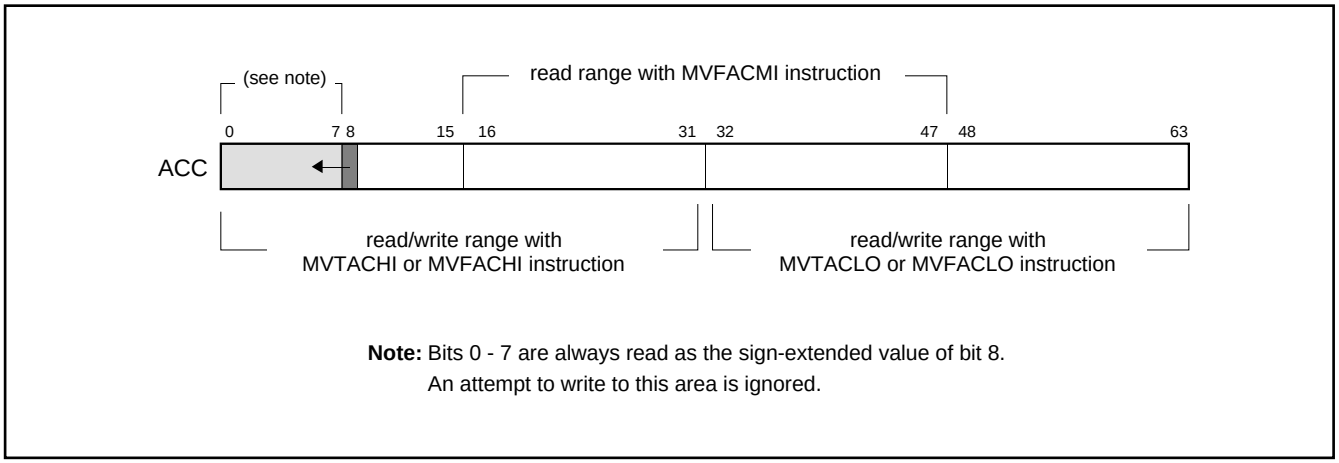


Fig. 5 Accumulator

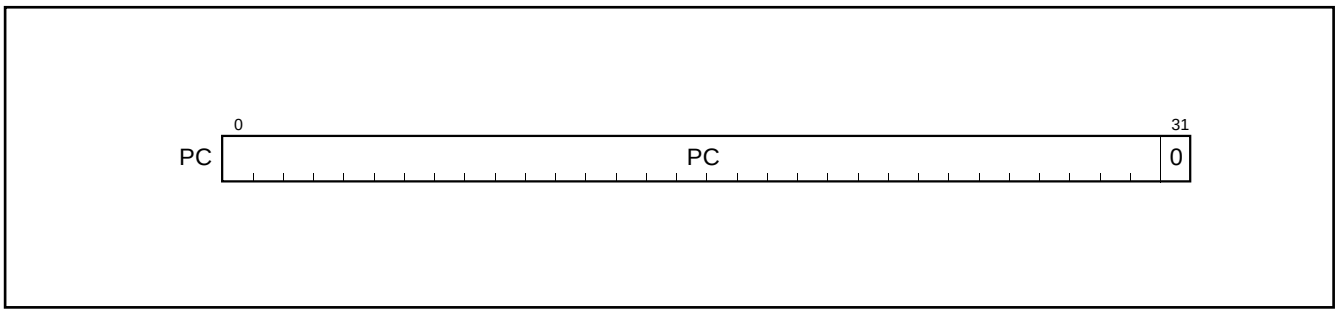


Fig. 6 Program counter

Data types

Signed and unsigned integers of byte (8 bits), halfword (16 bits), and word (32 bits) types are supported as data in the M32R CPU instruction set. A signed integer is represented in a 2's complement format.

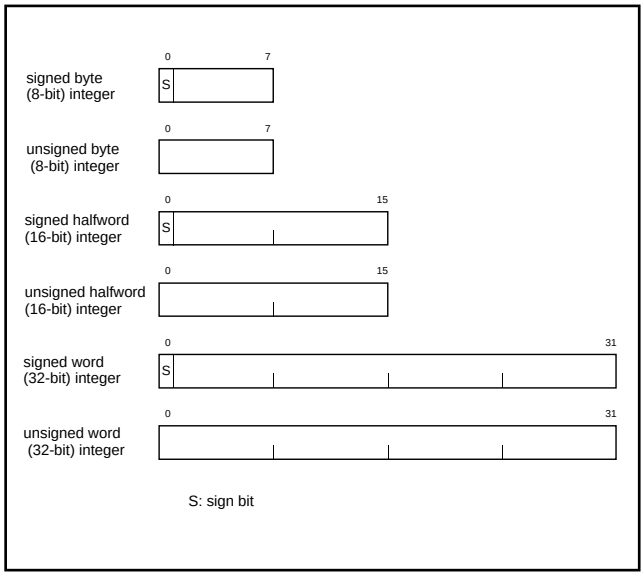


Fig. 7 Data type

Data formats

Data size of a register of the M32R CPU is always a word (32 bits). Byte (8 bits) and halfword (16 bits) data in memory are sign-extended (the **LDB** and **LDH** instructions) or zero-extended (the **LDUB** and **LDUH** instructions) to 32 bits, and loaded into the register.

Word (32 bits) data in a register is stored to memory by the **ST** instruction. Halfword (16 bits) data in the LSB side of a register is stored to memory by the **STH** instruction. Byte (8 bits) data in the LSB side of a register is stored to memory by the **STB** instruction.

Data stored in memory can be one of these types: byte (8 bits), halfword (16 bits) or word (32 bits).

Although the byte data can be located at any address, the halfword data and the word data can only be located on the halfword boundary and the word boundary, respectively. If an attempt is made to access data in memory which is not located on the correct boundary, an address exception occurs.

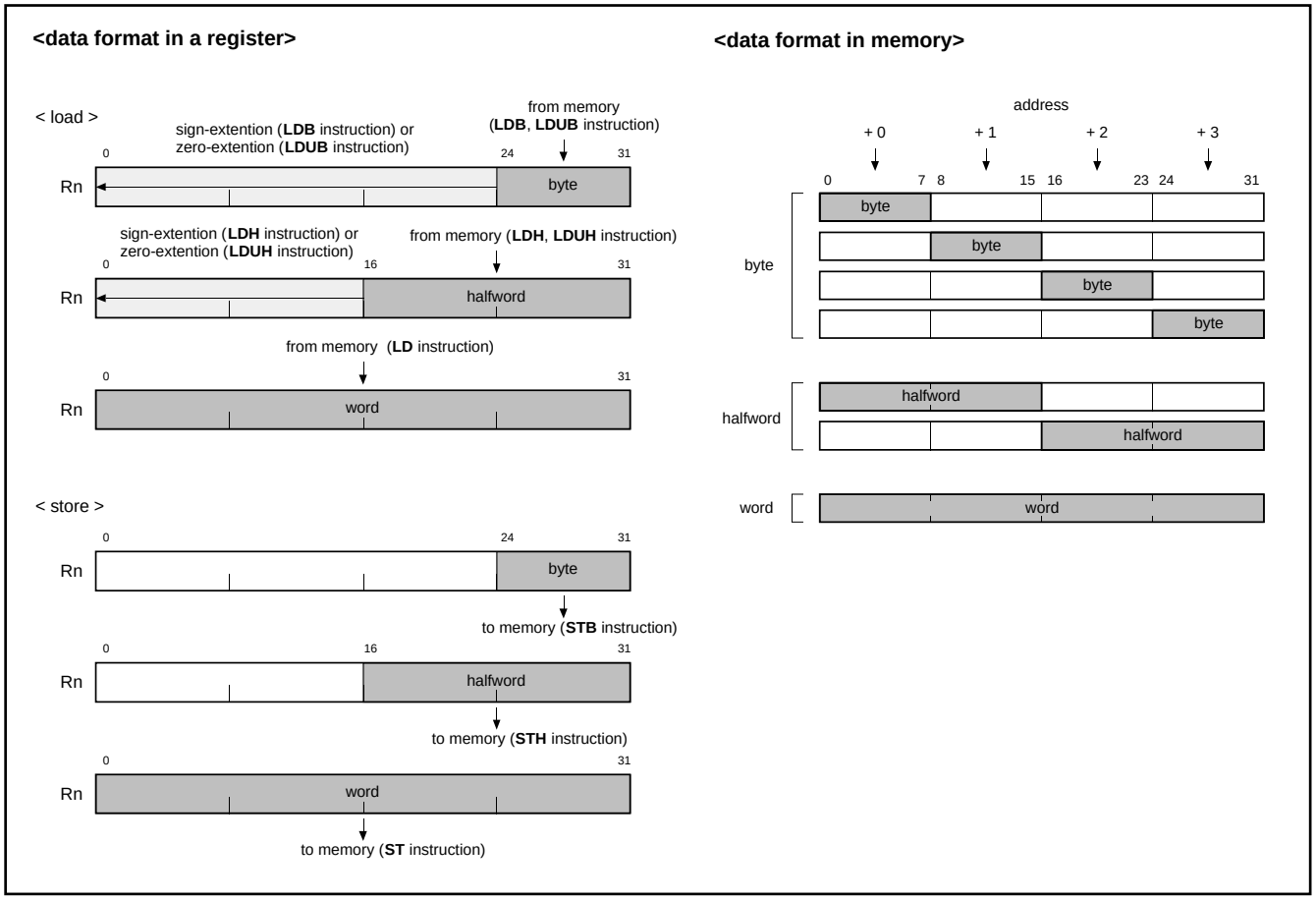


Fig. 8 Data format

Address space

The M32000D4AFP logical address is 32-bit wide and offers 4 GB linear space. The M32000D4AFP has address spaces allocated as shown below.

The user space is specified by SID = 0 (H'0000 0000 to H'7FFF FFFF). The area available to the user is 16 MB from address H'0000 0000 to address H'00FF FFFF.

The I/O space is specified by SID = 1 (H'8000 0000 to H'FFFF FFFF). The area available to the user is 16 MB from address H'FF00 0000 to address H'FFFF FFFF. The I/O space cannot be cached.

These areas below are allocated in each space.

- User space
  - internal DRAM area
  - external area
- I/O space
  - user I/O area
  - system area
  - internal I/O area

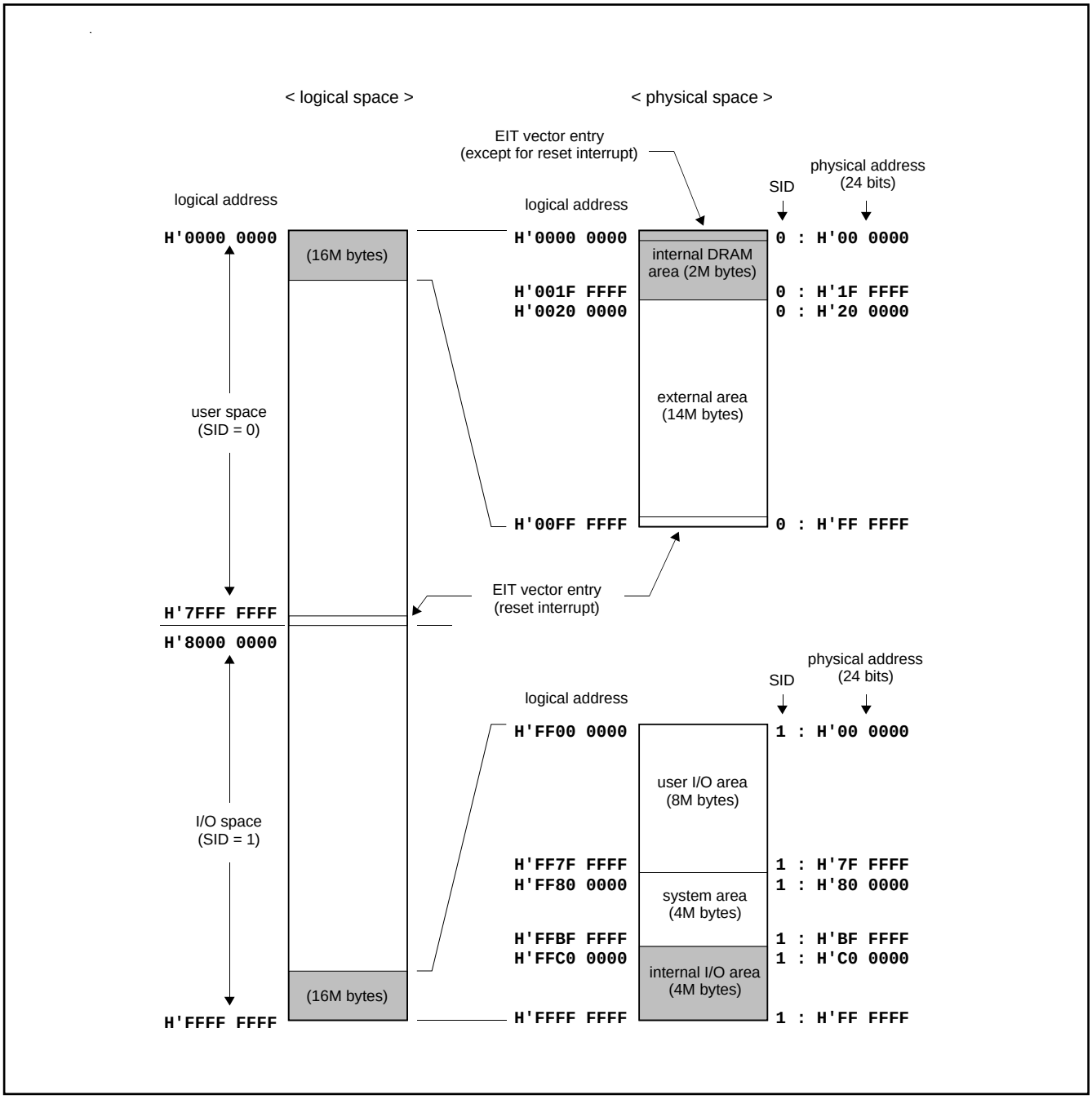
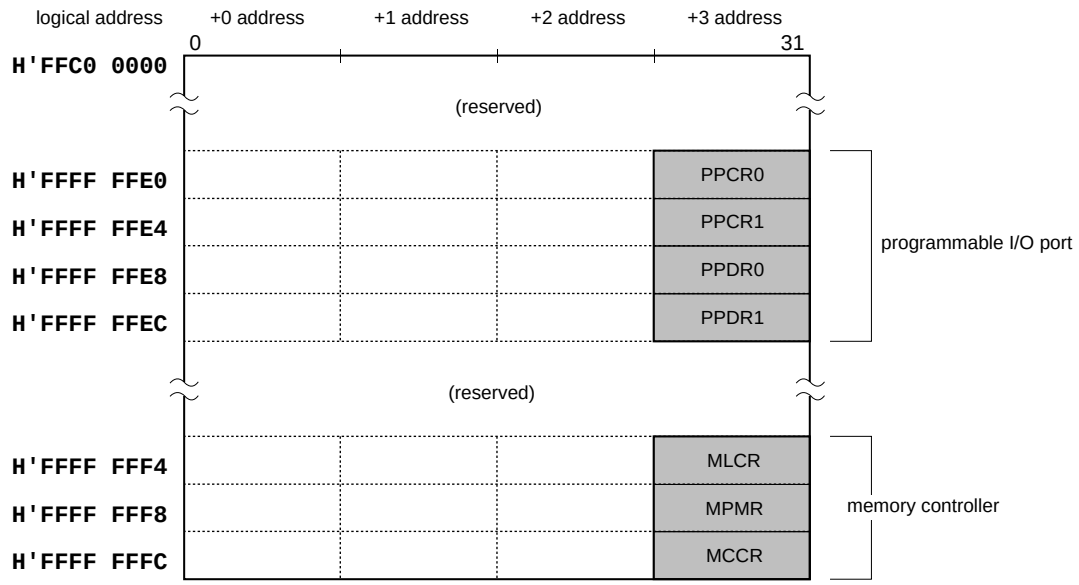


Fig. 9 Address space

The internal DRAM (2 MB) is allocated from address H'0000 0000 to address H'001F FFFF. The EIT vector entry (other than the reset interrupt) is allocated in the address H'0000 0000 to address H'0000 008F of this area.
The internal DRAM is connected to the M32R CPU via a 4 KB cache memory with a 128-bit bus. When the M32000D4AFP is in the hold state, the internal DRAM can be accessed from an external bus master by inputting control signals.
The external area consists of 14 MB from address H'0020 0000 to address H'00FF FFFF. When this space is accessed, the control signals to access external devices are output. The bottom 16 bytes in this area (H'00FF FFF0 to H'00FF FFFF) are the reset interrupt EIT vector entry.

The user I/O area is 8 MB from address H'FF00 0000 to address H'FF7F FFFF. When this space is accessed, the control signals to access external devices are output. The system area is 4 MB from address H'FF80 0000 to address H'FFBF FFFF. This area is reserved for development tools such as in-circuit emulators or debug monitors. The user cannot use this area.
The internal I/O area is 4 MB from address H'FFC0 0000 to address H'FFFF FFFF. The memory controller and programmable I/O port registers are allocated in this area.



PPCR0: programmable I/O port direction control register 0
PPCR1: programmable I/O port direction control register 1
PPDR0: programmable port data register 0
PPDR1: programmable port data register 1

MLCR: lock control register
MPMR: power management control register
MCCR: cache control register

Fig. 10 Internal I/O space memory map

EIT

While the CPU is executing a program, sometimes it is necessary to suspend execution, because a certain event occurs, and execute another program. These kinds of events are referred to as EIT (Exception, Interrupt, Trap).

• Exception

The event is related to the context being executed. It is generated by errors or violations that occur during instruction execution. With the M32000D4AFP, the address exception (AE) and reserved instruction exception (RIE) are of this type.

• Interrupt

The event is not related to the context being executed. It is generated by an external hardware signal. With the M32000D4AFP, the external interrupt (EI), system break interrupt (SBI), wakeup interrupt (WI) and reset interrupt (RI) are of this type.

• Trap

This is a software interrupt which is generated by executing the TRAP instruction. It is intentionally added to the program by the programmer, as a system call.

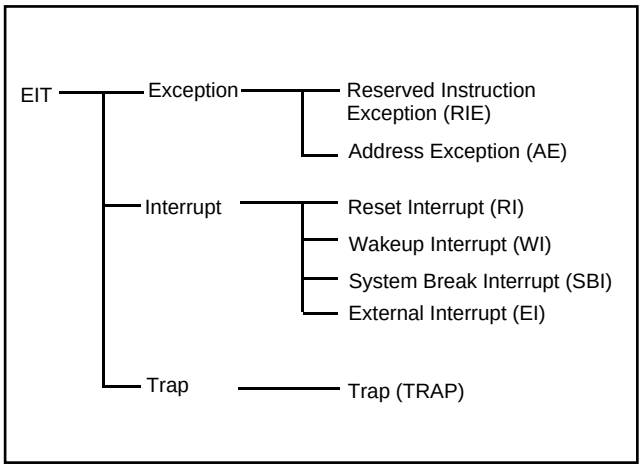


Fig. 11 EIT events

EIT events are shown below.

• Reserved instruction exception (RIE)

The reserved instruction exception (RIE) occurs when execution of a reserved instruction (unimplemented instruction) is detected.

• Address exception (AE)

The address exception (AE) occurs if an attempt is made to access an unaligned address with either a load instruction or a store instruction.

• Reset interrupt (RI)

The reset interrupt (RI) is always accepted when the $\overline{RST}$ signal is input. It has the highest priority.

• Wakeup interrupt (WI)

The wakeup interrupt (WI) is accepted when the $\overline{WKUP}$ signal is input while the M32000D4AFP is in standby mode. It is only used to return from standby mode.

• System break interrupt (SBI)

The system break interrupt (SBI) is an interrupt request from the $\overline{SBI}$ pin. It is used when a break in power source or an error from an external watchdog timer is detected. It is also used to return from CPU sleep mode and to start an M32000D4AFP set to slave mode.

• External interrupt (EI)

The external interrupt (EI) is an interrupt request from the $\overline{INT}$ pin. It is used by an interrupt from the external peripheral I/O and can be masked by the IE bit in the PSW register. It is also used to return from CPU sleep mode and to start an M32000D4AFP set to slave mode.

• Trap

The trap (TRAP) is a software interrupt which is generated by executing the TRAP instruction. A total of 16 EIT vector entries are available for operands 0 to 15 of the TRAP instruction.

Internal memory system

The memory system built into the M32000D4AFP has the following characteristics.

- internal 16M-bit (2M-byte) DRAM
- internal 4K-byte cache memory
- CPU, cache and internal DRAM are connected by a 128-bit bus
- selectable cache memory operation mode
  - – internal instruction/data cache mode
  - – instruction cache mode
  - – cache-off mode

cache control register (MCCR) < address: H'FFFF FFFF>

D24	D25	D26	D27	D28	D29	D30	D31
CP						CM0	CM1

<at reset: H'01>

D	bit name	function	R	W
24	CP (cache purge)	0: no purge 1: purge	0	○
25 - 29	Not assigned.		0	×
30, 31	CM0, CM1 (cache mode)	00: cache mode is not changed 01: cache-off mode 10: internal instruction/data cache mode 11: instruction cache mode	○	○

R = 0 ... "0" when reading R = ○ ... read enabled
W = ○ ... write enabled W = × : write disabled

Fig. 12 Cache control register

When the internal instruction/data cache mode is selected, the cache memory functions as a cache for both instruction and data from the internal DRAM, and caches all bus access to the DRAM. This mode is for a system which uses the internal DRAM as main memory. Transfer between the M32R CPU, cache memory and internal DRAM is always carried out in blocks of 128 bits. Caching is carried out by the direct map method. Writing is by the copy back method.

When the M32000D4AFP access destination is an external space, data transfer between the M32R CPU and the external device is carried out via the bus interface unit (BIU). The BIU has a 128-bit data buffer which converts the bus width between the 128-bit bus in the M32000D4AFP and the external bus. Caching is not applicable in this case of data transfer.

When accessing the internal DRAM from an external bus master, and a cache hit occurs (the accessed data is inside the cache), data transfer between the cache memory and the external bus via the BIU is carried out. When a cache miss occurs, (the accessed data is not inside the cache) data transfer is carried out between the internal DRAM and the external bus via the BIU without cache replacement.

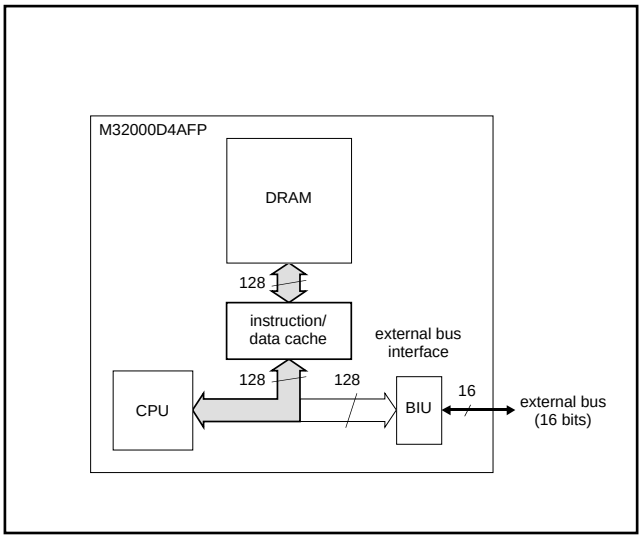


Fig. 13 Internal instruction/data cache mode

When the instruction cache mode is selected, the cache functions as an instruction cache for the internal DRAM or the external memory, and caching is carried out for instruction fetch access. This mode is designed for use when an external ROM is used as program memory and the internal DRAM is used as data memory, or when instructions are located in the internal DRAM. Caching is carried out by the direct map method. When instruction codes in the user space are overwritten by the external bus master or another source, instruction code coherency in the cache memory is not guaranteed. Furthermore, caching is not applied when accessing the internal DRAM from the external bus master.

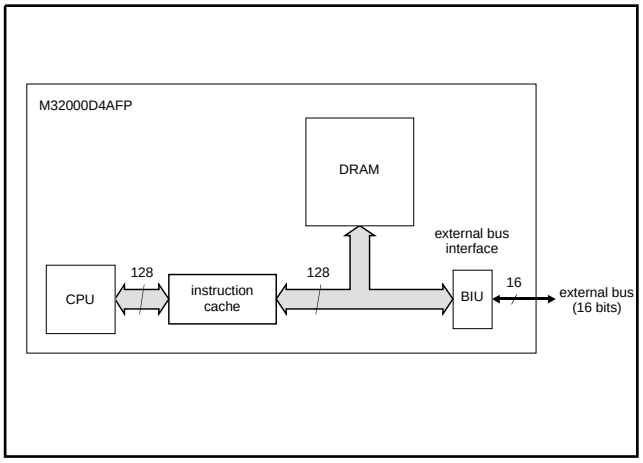


Fig. 14 Instruction cache mode

When the cache-off mode is selected, the M32000D4AFP internal memory system is configured as follows. In this mode, caching is not applied, and all bus cycles are directly to the internal DRAM or external bus.

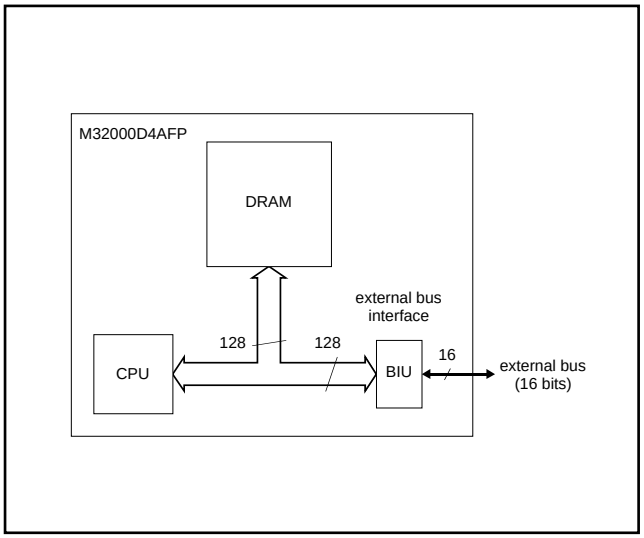


Fig. 15 Cache-off mode

Bus interface unit (BIU)

The M32000D4AFP has the following signals related to the external bus.

• Address (A8 to A30)

The M32000D4AFP has a 24-bit address bus (A8 to A31) corresponding to a 16 MB address space. Of these, A31 (the LSB) is not output externally. In write cycles, the validity of the two bytes output on the 16-bit data bus is indicated by $\overline{BCH}$ and/or $\overline{BCL}$. In read cycles, the 16-bit data bus is always read, however, only data in the valid byte position in the M32000D4AFP is transferred. The address pins are bidirectional. If the M32000D4AFP is in the hold state and the internal DRAM is accessed from an external bus master, the address signal is input from the system bus side.

• Space identifier (SID)

The space identifier is used to specify user space and I/O space.

user space: SID = "L"
I/O space: SID = "H"
hold: SID = high-impedance
idle: SID = undefined

• Byte control ($\overline{BCH}$, $\overline{BCL}$)

Byte control signals indicate the byte position of valid data transferred of the external bus cycle. $\overline{BCH}$ corresponds to the MSB side (D0 to D7), and $\overline{BCL}$ corresponds to the LSB side (D8 to D15). During the bus read cycle, both $\overline{BCH}$ and $\overline{BCL}$ are an "L" level. During the bus write cycle, $\overline{BCH}$ and/or $\overline{BCL}$ go to an "L" level depending on the bytes to be written. If the M32000D4AFP is in the hold state and the internal DRAM is accessed from an external bus master, the byte control signal is input from the system bus side.

• Data bus (D0 to D15)

The M32000D4AFP has a 16-bit data bus to access external devices. If the M32000D4AFP is in the hold state and the internal DRAM is accessed from an external bus master, the data bus is used as a data I/O bus from the system bus side.

• Bus start ($\overline{BS}$)

When the M32000D4AFP drives the bus cycle to the system bus, an "L" level is output to $\overline{BS}$ at the start of the bus cycle. Also, for a burst transfer, the $\overline{BS}$ signal is output for each transfer cycle. The $\overline{BS}$ signal is not output when accessing internal resources such as the internal DRAM or internal I/O registers.

• Bus status (ST)

The ST signal identifies whether the bus cycle the M32000D4AFP is driving is an instruction fetch cycle or an operand access cycle.

instruction fetch access: ST = "L"
operand access: ST = "H"
hold: ST = high-impedance
idle: ST = undefined

• Read/write (R/$\overline{W}$)

The M32000D4AFP outputs a R/$\overline{W}$ signal to identify whether the external bus cycle is a read or write operation. When accessing the internal DRAM from an external bus master, a R/$\overline{W}$ signal is input from the system bus side.

read bus cycle: R/$\overline{W}$ = "H"
write bus cycle: R/$\overline{W}$ = "L"

• Burst ($\overline{BURST}$)

The M32000D4AFP drives two consecutive bus cycles to access 32-bit data located on the 32-bit boundary. In instruction fetching, it drives a maximum of 8 (fixed to 8 cycles in instruction cache mode) consecutive read cycles to access data located on the 128-bit boundary. While driving these consecutive bus cycles, the M32000D4AFP outputs "L" level to $\overline{BURST}$. When accessing 32-bit data, the address of the MSB-side 16 bits are output before the address of the LSB side 16 bits. When accessing 128-bit data, the addresses are output for every access cycle from the arbitrary 16-bit aligned addresses to wraparound within the 128-bit boundary.

• Data complete ($\overline{DC}$)

When starting an external bus cycle, the M32000D4AFP automatically inserts wait cycles until the $\overline{DC}$ signal is input from external. Wait control using the $\overline{DC}$ signal is effective also for bus cycles during burst transfer. When the M32000D4AFP is in the hold state and if the $\overline{CS}$ signal is input, the M32000D4AFP outputs the $\overline{DC}$ signal to notify the external bus master that internal DRAM access is complete.

• Hold control ($\overline{HREQ}$, $\overline{HACK}$)

The hold state is the state when the external bus access stops and all pins go to a high-impedance state. However, the internal DRAM can be accessed while the external bus is in the hold state. To put the M32000D4AFP into the hold state, input an "L" level to $\overline{HREQ}$. When the hold request is accepted and the M32000D4AFP enters the hold state, an "L" level is output from $\overline{HACK}$.

• Internal DRAM access control ($\overline{CS}$)

The internal DRAM can be accessed when $\overline{CS}$ is driven to an "L" level after the M32000D4AFP enters the hold state ($\overline{HACK}$ = "L"). To access the internal DRAM from external, the following signals from the system bus side should be controlled.

• A8 to A30

Input internal DRAM addresses to be read or written.

• $\overline{BCH}$, $\overline{BCL}$

Specify the byte position of data to be written into the internal DRAM. $\overline{BCH}$ corresponds to the MSB side (D0 to D7), and $\overline{BCL}$ corresponds to the LSB side (D8 to D15).

• R/$\overline{W}$

Specify read or write operation. When reading, R/$\overline{W}$ = "H". When writing, R/$\overline{W}$ = "L".

• D0 to D15

16-bit data I/O bus.

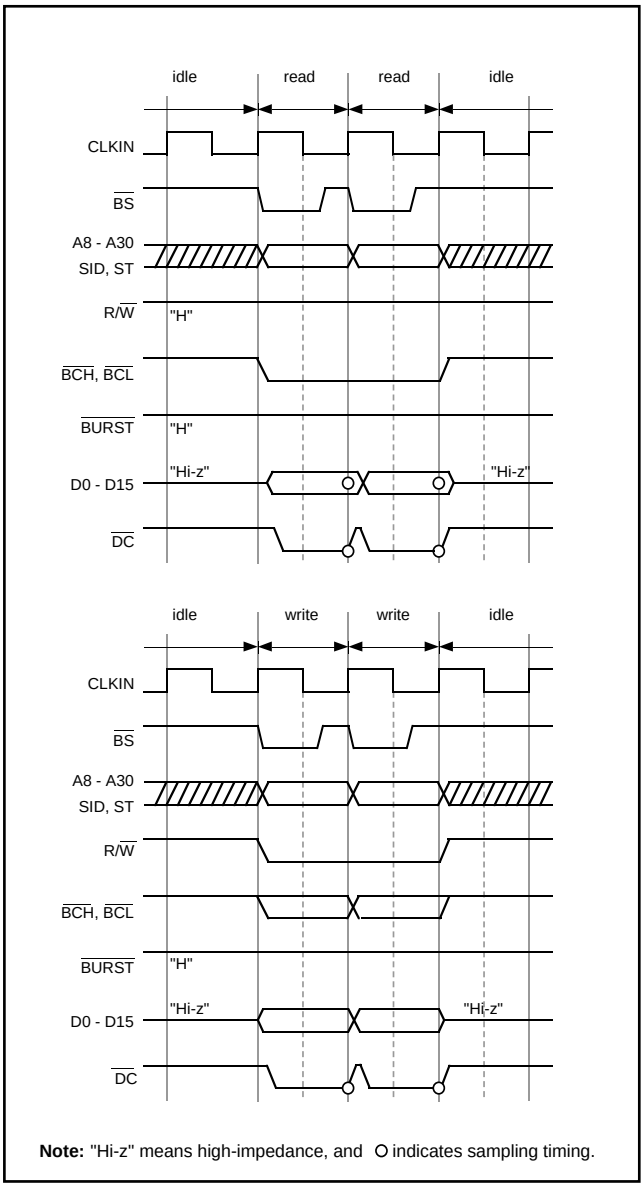
• $\overline{DC}$

This signal notifies to an external bus master that the internal DRAM access is complete. When access is complete, an "L" level is output to $\overline{DC}$.

Table 1 Pin condition in hold state

pin name	pin condition or operation
A8 - A30, SID, $\overline{BCH}$, $\overline{BCL}$ ST, R/$\overline{W}$, $\overline{BS}$, $\overline{BURST}$	high-impedance
D0 - D15	output when internal DRAM is read by an external bus master ($\overline{CS}$ = "L", R/$\overline{W}$ = "H"), otherwise high-impedance
$\overline{DC}$	output when internal DRAM is accessed by an external bus master ($\overline{CS}$ = "L"), otherwise high-impedance
$\overline{HACK}$	output "L"
other pins	normal operation

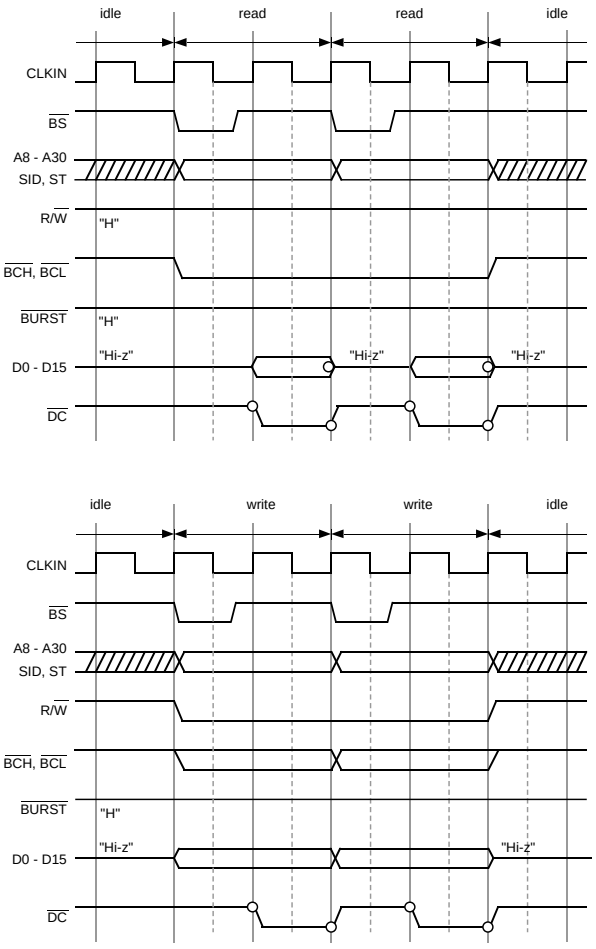
Read and write operations of the M32000D4AFP are carried out using the address bus, data bus, and the R/$\overline{W}$, $\overline{BCH}$, $\overline{BCL}$ and $\overline{DC}$ signals. When reading, the R/$\overline{W}$ signal goes to an "H" level, and the $\overline{BCH}$ and $\overline{BCL}$ signals go to an "L" level. The CPU reads the data in the valid byte positions. When writing, an "L" level is output from R/$\overline{W}$, and $\overline{BCH}$ and $\overline{BCL}$ are output according to the valid byte positions, so as to specify the byte positions for writing into an external device.



Note: "Hi-z" means high-impedance, and O indicates sampling timing.

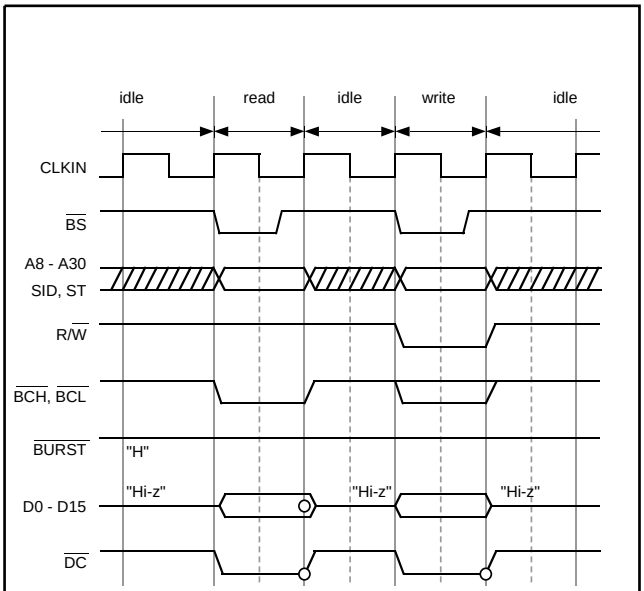
Fig. 16 Read/write timing (two no-wait accesses)

When an "L" level is input to $\overline{DC}$, the next bus cycle is processed and wait cycles are inserted until this point. When a write cycle comes immediately after a read cycle, the M32000D4AFP inserts an idle cycle to prevent a collision with data on the system bus. The same applies to write cycles (burst write access) immediately after a burst read cycle.



Note: "Hi-z" means high-impedance, and ○ indicates sampling timing.
Keep $\overline{DC}$ signal at the "H" level when waits are inserted.

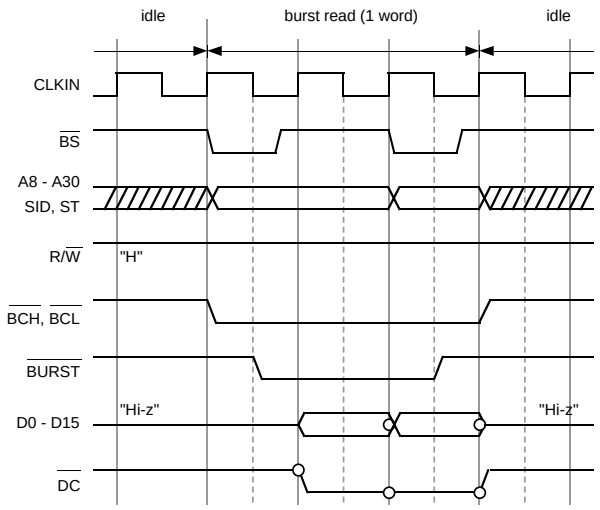
Fig. 17 Read/write timing (two one-wait accesses)



Note: "Hi-z" means high-impedance, and ○ indicates sampling timing.

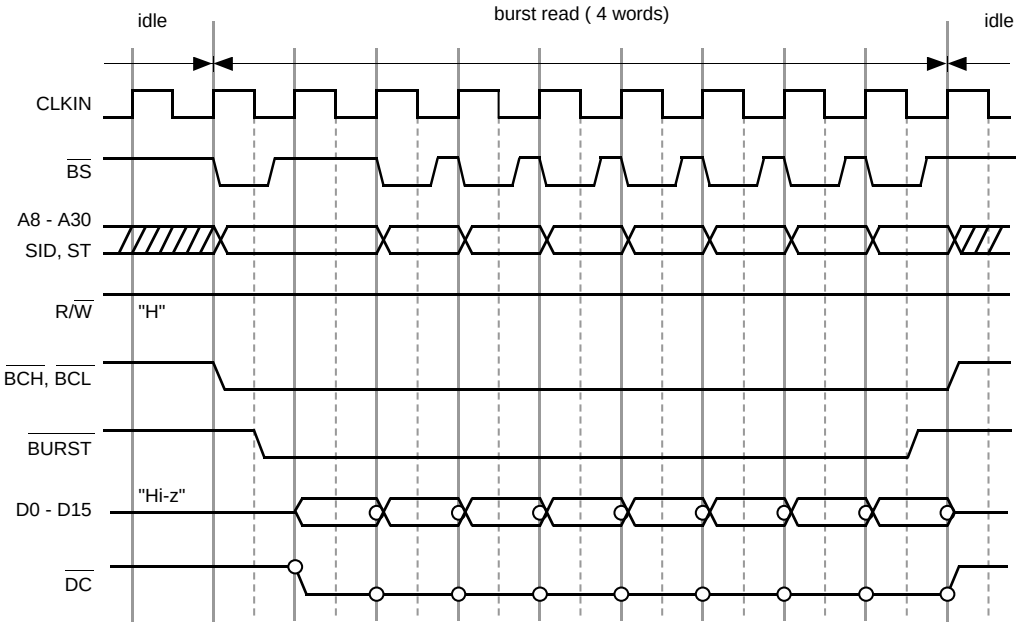
Fig. 18 Automatic idle cycle insertion between consecutive read and write cycles

The M32000D4AFP outputs the $\overline{\text{BURST}}$ signal and carries out a burst transfer when reading "the word-size data aligned on the 32-bit boundary" or "a maximum 4 words of instructions aligned on the 128-bit boundary". The $\overline{\text{BURST}}$ signal is synchronized with the CLKIN falling edge of the first bus access cycle and output "L" level. It returns to an "H" level synchronized with the first CLKIN falling edge of the last bus access cycle. Addresses A8 to A30 are output for each cycle.
When burst reading 32-bit data, the MSB-side 16-bit read bus cycle is carried out first followed by the LSB-side 16-bit read bus cycle.
When the cache memory operation mode is the instruction cache mode, and burst reading of the instructions within the 128-bit boundary for cache replacement occurs, the bus cycle is driven a fixed 8 times from an arbitrary 32-bit boundary address and to wraparound within the 128-bit boundary. When other than the instruction cache mode is selected and burst reading a set of instructions of less than 128 bits, consecutive bus cycles are driven from an arbitrary 32-bit boundary address as the top to the 128-bit line (A28 to A30 = "111").



Note: "Hi-z" means high-impedance, and O indicates sampling timing.
Wait cycles can be inserted even when burst transferring by setting $\overline{\text{DC}}$ = "H".

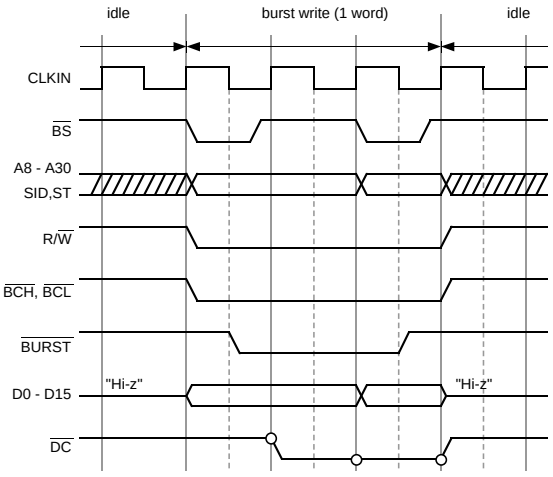
Fig. 19 1-word (32-bit) burst read timing (1-0 wait)



Note: "Hi-z" means high-impedance, and O indicates sampling timing.
Wait cycles can be inserted even when burst transferring by setting $\overline{\text{DC}}$ = "H".

Fig. 20 4-word (128-bit) burst read timing (1-0-0-0-0-0-0-0 wait)

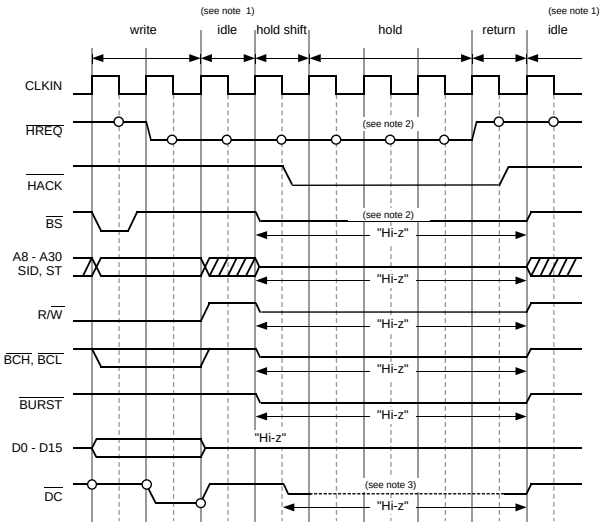
When writing word-size data aligned on the 32-bit boundary, the M32000D4AFP carries out a burst-transfer by outputting the $\overline{\text{BURST}}$ signal. When burst-writing 32-bit data, the MSB-side 16-bit write bus cycle is driven first, followed by the LSB-side 16-bit write bus cycle. The $\overline{\text{BURST}}$ signal is synchronized with the CLKIN falling edge of the first bus access cycle, and "L" level is output. It returns to "H" level in synchronization with the CLKIN falling edge of the last bus access cycle. Addresses A8 to A30 are output for each cycle.



Note: "Hi-z" means high-impedance, and O indicates sampling timing.
Wait cycles can be inserted even when burst transferring by setting $\overline{\text{DC}}$ = "H".

Fig. 21 1-word (32-bit) burst write timing (1-0 wait)

When an "L" level is input to $\overline{\text{HREQ}}$, the M32000D4AFP switches to the hold state and outputs an "L" level to $\overline{\text{HACK}}$. While the M32000D4AFP is in the hold state, bus related pins go to a high impedance state, and data transfer is carried out on the system bus. To return to normal operation mode from the hold state, the $\overline{\text{HREQ}}$ signal should be changed to an "H" level.



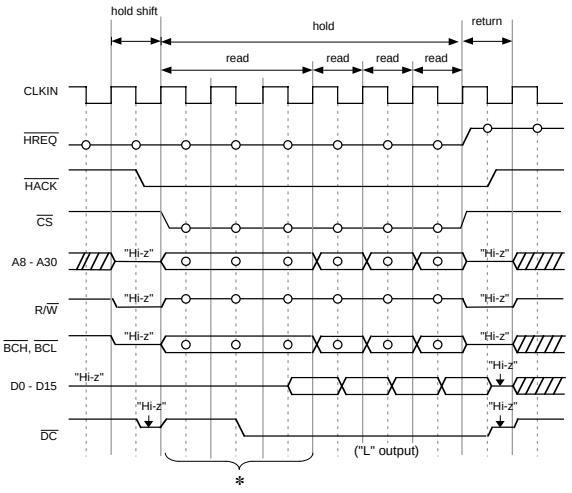
Notes 1: Before switching to the hold state, an idle cycle of 1 CLKIN clock period is always inserted.
After returning from the hold state, an idle cycle of 1 to 5 CLKIN clock periods is always inserted.
2: "Hi-z" means high impedance, and O indicates sampling timing.
3: While the M32000D4AFP is in the hold state, the $\overline{\text{DC}}$ signal is driven and output when the $\overline{\text{CS}}$ signal is input.

Fig. 22 Bus arbitration timing

When the M32000D4AFP is in the hold state and an "L" level is input to $\overline{CS}$, the M32000D4AFP interprets it as a bus access request to the internal DRAM. In this case, when the R/$\overline{W}$ signal is an "H" level, the memory controller drives a read cycle to the internal DRAM. In the read cycle, the 16-bit data for the address specified with A8 to A30, is output from D0 to D15 regardless of the $\overline{BCH}$ and $\overline{BCL}$ settings. Also the $\overline{DC}$ signal is output.

The M32000D4AFP reads 128 bits of data from the block on the 128-bit boundary including the requested address into the 128-bit buffer of the bus interface unit. 3 to 7 CLKIN clock periods are necessary for the first bus access, however, when reading consecutive address within the 128-bit boundary, the subsequent read bus cycles are completed in 1 CLKIN clock period because a read from the internal DRAM does not take place.

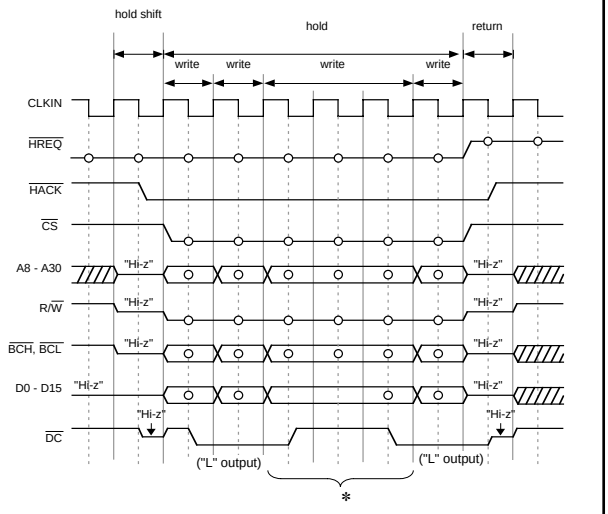
Once the external bus master read cycle has been driven, it cannot be aborted. When an "L" level is input to $\overline{CS}$ and an access has started, the values of this and other control signals should be held during the wait cycles (that is while $\overline{DC}$ = "H"). After $\overline{DC}$ outputs an "L" level (access complete), return $\overline{CS}$ to the "H" level between the CLKIN falling edge corresponding to the last read cycle and the following CLKIN falling edge. Return $\overline{HREQ}$ to the "H" level to return the M32000D4AFP to the normal operation mode from the hold state either at the same time as or after $\overline{CS}$ is returned to the "H" level.



Note: "Hi-z" means high impedance, and O indicates sampling timing.
The value of the R/$\overline{W}$ signal that controls the data direction of the bus interface cannot be changed during $\overline{CS}$="L". Hold this value while $\overline{CS}$="L".
Also, where marked above with *, 3 to 7 CLKIN clock periods are necessary for the first read operation (also when reading crosses an 128-bit boundary) when reading from the internal DRAM. Hold the input value of the address or other control signals during these wait cycle periods ($\overline{DC}$ = "H"). Consecutive read operations within an 128-bit boundary are completed in 1 CLKIN clock period.
During these wait cycle period, $\overline{CS}$ cannot be returned to an "H" level (the access cannot be aborted). $\overline{CS}$ can only be returned to an "H" level after $\overline{DC}$ is driven to "L".

Fig. 23 Read bus cycle to internal DRAM

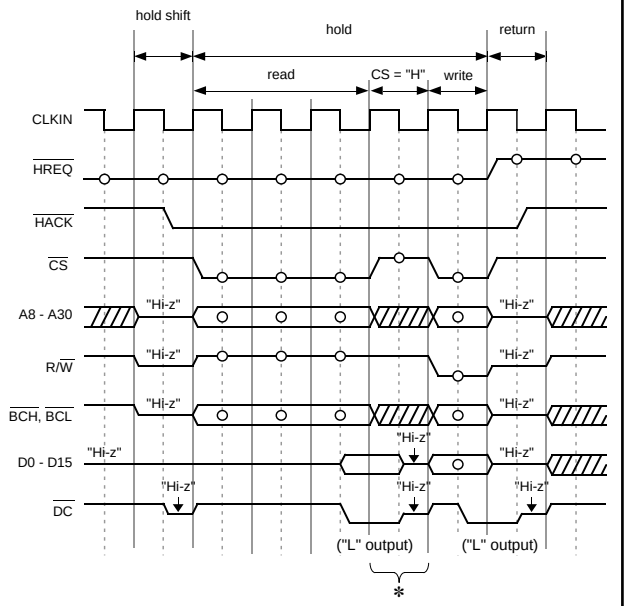
When the M32000D4AFP is in the hold state and an "L" level is input to $\overline{CS}$, the M32000D4AFP interprets it as a bus access request to the internal DRAM. In this case, when the R/$\overline{W}$ signal is at an "L" level, the memory controller drives a write cycle to the internal DRAM. Byte data control is specified by the $\overline{BCH}$ and $\overline{BCL}$ signals. Only data in the byte positions for which an "L" level is input to $\overline{BCH}$ or $\overline{BCL}$ are written. When writing is complete, an "L" level $\overline{DC}$ signal is output. The M32000D4AFP stores the requested data in the 128-bit data buffer of the BIU, before writing to the internal DRAM. This reduces the number of accesses to the internal DRAM when a request to writing to consecutive addresses is made, and improves bus cycle throughput. Consecutive write cycles within an 128-bit boundary are completed in 1 CLKIN clock period. 3 to 7 CLKIN clock periods are necessary for a write access crossing an 128-bit boundary when writing to the internal DRAM. Once the external bus master write cycle has been driven, it cannot be aborted. When an "L" level is input to $\overline{CS}$ and an access has started, the values of this and other control signals should be held during the wait cycles (that is while $\overline{DC}$ = "H"). After $\overline{DC}$ outputs an "L" level (access complete), return $\overline{CS}$ to the "H" level between the CLKIN falling edge corresponding to the last write cycle and the following CLKIN falling edge. Return $\overline{HREQ}$ to the "H" level to return the M32000D4AFP to the normal operation mode from the hold state either at the same time as or after $\overline{CS}$ is returned to the "H" level.



Note: "Hi-z" means high impedance, and ○ indicates sampling timing.
The value of the R/$\overline{W}$ signal that controls the data direction of the bus interface cannot be changed during $\overline{CS}$="L". Hold this value while $\overline{CS}$="L".
Also, where marked above with ✻, 3 to 7 CLKIN clock periods are necessary for writing operation to internal DRAM crossing an 128-bit boundary. Hold the input value of the address or other control signals during these wait cycle periods ($\overline{DC}$ = "H"). Consecutive writing operations within an 128-bit boundary are completed in 1 CLKIN clock period. During these wait cycle period, $\overline{CS}$ cannot be returned to "H" level (the access cannot be aborted). $\overline{CS}$ can only be returned to a "H" level after $\overline{DC}$ is driven to "L".

Fig. 24 Write bus cycle to internal DRAM

When the external bus master makes an access, the value of the R/$\overline{W}$ signal that controls the data direction of the bus interface cannot be changed during $\overline{CS}$="L". Therefore, read cycles and write cycles cannot be mixed while $\overline{CS}$ = "L". When starting a write cycle following after a read cycle and starting a read cycle following a write cycle, keep the $\overline{CS}$ signal at an "H" level for at least 1 CLKIN.



Note: "Hi-z" means high-impedance, and ○ indicates sampling timing.
Also, where marked above with ✻, keep $\overline{CS}$ signal to "H" at least 1 CLKIN when starting a write bus cycle after a read bus cycle or a read bus cycle after a write bus cycle.

Fig. 25 Read/write bus cycle

Master/slave mode

The M32000D4AFP has an M/$\overline{S}$ (master/slave) pin for multiprocessor configuration use.

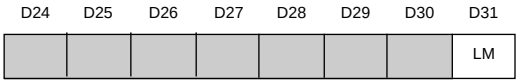
• master mode (M/$\overline{S}$ = "H")

This is normal operation mode. Set the M/$\overline{S}$ pin to an "H" level. It is used when the M32000D4AFP is used as the main CPU in a system.

• slave mode (M/$\overline{S}$ = "L")

This operation mode is for when the M32000D4AFP is used as a coprocessor. Set the M/$\overline{S}$ pin to an "L" level. When set to slave mode, the M32000D4AFP does not start operation even after a reset, until an interrupt request or the SBI is input. Processing is carried out by communicating with the master M32000D4AFP, using the two programmable I/O ports and the external interrupt signal.

lock control register (MLCR) < address: H'FFFF FFF7>



<at reset: H'00>

D	bit name	function	R	W
24 - 30	Not assigned.		0	×
31	LM (lock mode)	0: $\overline{HREQ}$ exclusive lock mode 1: $\overline{CS}$ exclusive lock mode	○	○

R = 0 ... "0" when reading R = ○ ... read enabled
W = ○ ... write enabled W = × : write disabled

Fig. 26 Lock control register

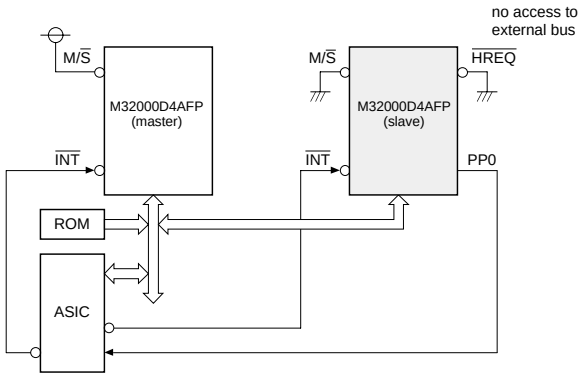
• Coprocessor only configuration example

The slave M32000D4AFP accesses only the internal DRAM and never the external bus. M/$\overline{S}$ and $\overline{HREQ}$ are fixed at the "L" level. The slave M32000D4AFP executes the instructions that the master M32000D4AFP downloads to the internal DRAM. The data transfer request (processing complete) from the slave M32000D4AFP is notified to the master M32000D4AFP by inputting the interrupt request via the programmable I/O port. The data transaction is carried out when the master M32000D4AFP accesses the internal DRAM in the slave M32000D4AFP.

• Common bus coprocessor configuration example

In this configuration, the slave M32000D4AFP can also access the external bus. Communications between the master and slave CPUs is carried out using the programmable I/O ports and the interrupt request input.

<coprocessor only configuration>



<common bus coprocessor configuration>

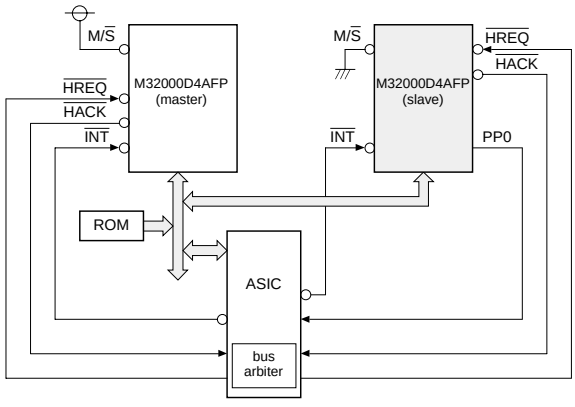


Fig. 27 Master/slave system configuration example

Power management function

The M32000D4AFP has the following two low-power consumption modes.

- standby mode
- CPU sleep mode

power management (MPMR) < address: H'FFFF FFFB>

D24	D25	D26	D27	D28	D29	D30	D31
						PM0	PM1

<at reset: H'00>

D	bit name	function	R	W
24 - 29	Not assigned.		0	×
30, 31	PM0, PM1 (low power consumption mode)	00: normal operation mode 01: (reserved) 10: CPU sleep mode 11: standby mode	○	○

R = 0 ... "0" when reading R = ○ ... read enabled
W = ○ ... write enabled W = × : write disabled

Fig. 28 Power management control register

In standby mode, all clock supply stops and only the contents of the internal DRAM are retained. The power requirement is only that which the internal DRAM needs for refreshing itself. When set to standby mode, the M32000D4AFP waits for the current bus operation to be completed. It then purges the cache memory and switches the internal DRAM to self-refresh mode. After that, the PLL and all clock supplies stop and the $\overline{\text{STBY}}$ signal goes to an "L" level to indicate the completion of the switch to standby mode. Input an "L" level to $\overline{\text{WKUP}}$ or $\overline{\text{RST}}$ to return from standby mode to normal operation mode. The contents of the internal DRAM are retained upon return using the $\overline{\text{WKUP}}$ signal.

In CPU sleep mode, clock supply to the M32R CPU stops. In this mode, the internal DRAM, cache memory, memory controller and external bus interface continue to operate and the internal DRAM can be accessed from the external bus. Input an "L" level to $\overline{\text{INT}}$, $\overline{\text{SBI}}$ or $\overline{\text{RST}}$ to return to normal operation mode from CPU sleep mode. The contents of the cache memory, internal DRAM, general-purpose registers and programmable I/O control register are retained upon return using the $\overline{\text{INT}}$ or $\overline{\text{SBI}}$ signals.

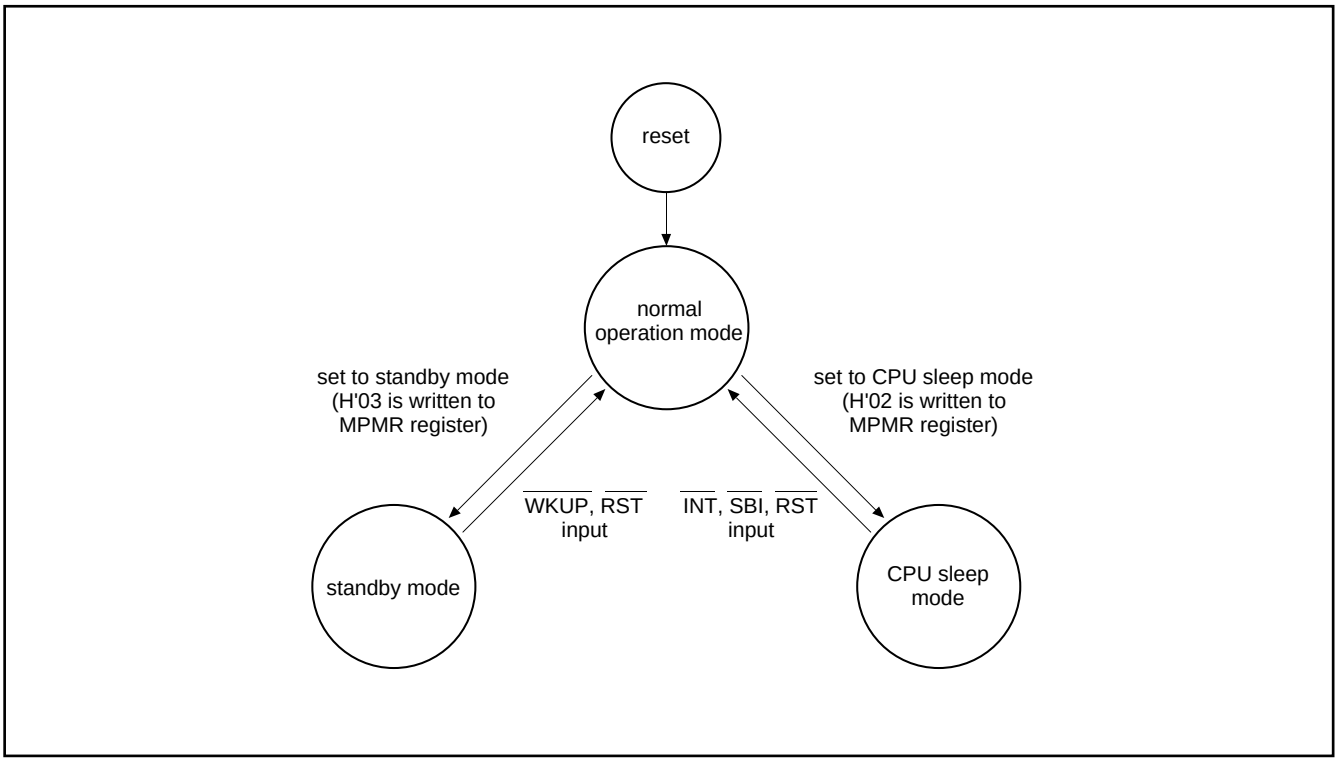


Fig. 29 State transition for low power consumption mode

Programmable I/O port

The M32000D4AFP has two programmable I/O ports (PP0, PP1). Each port can be set as input or output.

programmable I/O port direction control register 0 (PPCR0)
< address: H'FFFF FFE3>



programmable I/O port direction control register 1 (PPCR1)
< address: H'FFFF FFE7>



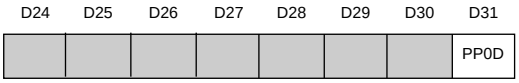
<at reset: H'00>

D	bit name	function	R	W
24 - 30	Not assigned.		0	×
31	PP0C, PP1C (port I/O direction)	0: input port 1: output port	○	○

R = 0 ... "0" when reading R = ○ ... read enabled
W = ○ ... write enabled W = × : write disabled

Fig. 30 Programmable I/O port direction control register

programmable I/O port data register 0 (PPDR0)
< address: H'FFFF FFEB>



programmable I/O port data register 1 (PPDR1)
< address: H'FFFF FFEF>



<at reset: B'0000 000?>

D	bit name	function	R	W
24 - 30	Not assigned.		0	×
31	PP0D, PP1D (port data)	0: data = "0" 1: data = "1"	○	○

R = 0 ... "0" when reading R = ○ ... read enabled
W = ○ ... write enabled W = × : write disabled

Fig. 31 Programmable I/O port data register

Reset

When an "L" level is input to $\overline{RST}$, the M32000D4AFP switches to the reset state. The reset state is released when an "H" level is input to $\overline{RST}$, and the program is executed from the EIT vector entry of the reset interrupt. All internal resources including the internal PLL (4x clock generator) are initialized. In order to stabilize PLL oscillation, the "L" input to $\overline{RST}$ should last a minimum of 2 ms after the clock input to CLKIN stabilizes and VCC stabilizes to the specified voltage level.

Table 2 Internal state after reset

internal resources		state
DRAM		undefined
cache memory		invalid (purged all)
general purpose registers (R0 - R15)		undefined
control registers	PSW (CR0)	B'0000 0000 0000 0000 ??00 000? 0000 0000 (BSM, BIE, and BC are undefined)
	CBR (CR1)	H'0000 0000
	SPI (CR2)	undefined
	SPU (CR3)	undefined
	BPC (CR6)	undefined
	PC	master mode: execute from address H'7FFF FFF0 slave mode: wait for interrupt input at address H'7FFF FFF0 • execute from address H'0000 0010 by inputting $\overline{SBI}$ signal • execute from address H'0000 0080 by inputting $\overline{INT}$ signal
	ACC (accumulator)	undefined
I/O registers	PPCR0, PPCR1	H'00 (input)
	PPDR0, PPDR1	B'0000 000? (depends on input pin state)
	MLCR	H'00 ($\overline{HREQ}$ exclusive lock mode)
	MPMR	H'00 (normal operation)
	MCCR	H'01 (cache-off mode)

Clock generating circuit

The M32000D4AFP has a clock multiplier circuit and operates at four times the input frequency. The internal operation frequency becomes 66.6 MHz when a 16.65 MHz clock is input to CLKIN. A capacitor (C) should be connected to the PLLCAP pin, and the clock is input to the CLKIN pin. The PLLVCC and PLLVSS pins should be connected to the power source or the ground, respectively.

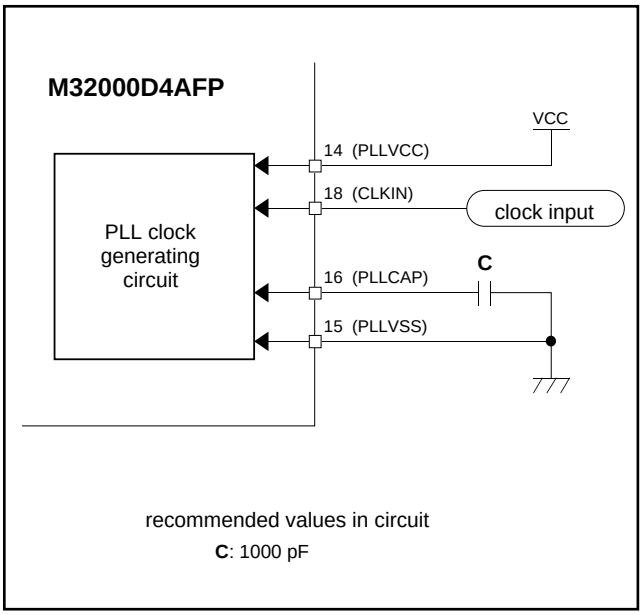


Fig. 32 Oscillation circuit

ADDRESSING MODE

M32R family supports the following addressing modes.

< register direct >

The general-purpose register or the control register to be processed is specified.

< register indirect >

The contents of the register specify the address in memory to be accessed. This mode can be used by all load/store instructions.

< register relative indirect >

(The contents of the register) + (16-bit immediate value which is sign-extended to 32 bits) specify the address in memory to be accessed.

< register indirect and register update >

- 4 is added to the register contents
  (the contents of the register before update specify the address in memory to be accessed) [**LD** instruction]
- 4 is added to the register contents
  (the contents of the register after update specify the address in memory to be accessed) [**ST** instruction]
- 4 is subtracted from the register contents
  (the contents of the register after update specify the address in memory to be accessed) [**ST** instruction]

< immediate >

The 4-, 5-, 8-, 16- or 24-bit immediate value.

< PC relative >

(The contents of PC) + (8, 16, or 24-bit displacement which is sign-extended to 32 bits and 2 bits left-shifted) specify the address in memory to be accessed.

INSTRUCTION FORMAT

There are two major instruction formats: two 16-bit instructions packed together within a word boundary, and a single 32-bit instruction.

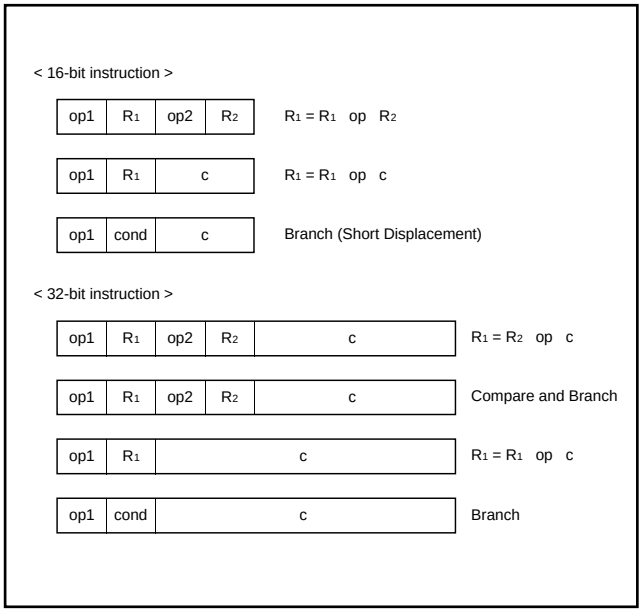


Fig. 33 Instruction format

INSTRUCTION SET

A total of 83 instructions are implemented.

<Load/store instructions>

The load/store instructions carry out data transfers between a register and a memory.

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

<Transfer instructions>

The transfer instructions carry out data transfers between registers or a register and an immediate value.

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

<Operation instructions>

Compare, arithmetic/logic operation, multiply and divide, and shift are carried out between registers.

• compare instructions

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• arithmetic operation instructions

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add with overflow checking
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract with overflow checking
SUBX	Subtract with borrow

• logic operation instructions

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

• multiply/divide instructions

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

• shift instructions

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

<Branch instructions>

The branch instructions are used to change the program flow.

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

<EIT-related instructions>

The EIT-related instructions carry out the EIT events (Exception, Interrupt and Trap). Trap initiation and return from EIT are EIT-related instructions.

TRAP	Trap
RTE	Return from EIT

<DSP function instructions>

The DSP function instructions carry out multiplication of 32 bits × 16 bits and 16 bits × 16 bits or multiply and add operation; there are also instructions to round off data in the accumulator and carry out transfer of data between the accumulator and a general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order halfword
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
			Min.	Max.	
VCC	Power source voltage		–0.5	4.6	V
VI	Input voltage		–0.5	4.6	V
VO	Output voltage		–0.5	4.6	V
PD	Power consumption	TOPR = 25 °C		1000	mW
TOPR	Operating temperature		0	70	°C
TSTG	Storage temperature		–65	150	°C

RECOMMENDED OPERATING CONDITIONS (VCC = 3.3 V ± 0.3 V, TOPR = 0 to 70 °C unless otherwise noted)

Symbol	Parameter		Ratings			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage		3.0		3.6	V
VIH	"H" input voltage	All inputs except following	2.0		VCC+0.3	V
		$\overline{\text{RST}}$ pin	0.8VCC		VCC+0.3	V
VIL	"L" input voltage	All inputs except following	–0.3		0.8	V
		$\overline{\text{RST}}$ pin	–0.3		0.2VCC	V
IOH (see note)	"H" output current				2	mA
IOL (see note)	"L" output current				2	mA
CL	output load capacity				50	pF

Note: IOH and IOL represent the maximum values of DC current load. Intermittent current that is generated during output need not to be considered as long as the output load capacity is within the specified range.

DC CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (VCC = 3.3 V ± 0.3 V, TOPR = 0 to 70 °C unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage	IOH = –2 mA	2.4			V
VOL	"L" output voltage	IOL = 2 mA			0.4	V
IOZ	Output current in off state	VO = 0 to VCC	–10.0		10.0	µA
IIH	"H" input current	VIH = 0 to VCC +0.3 V			10.0	µA
IIL	"L" input current	VIH = 0 to VCC +0.3 V			–10.0	µA
ICC	Power source current	Average in normal operation mode VCC = 3.3 V		140	220	mA
		Average in CPU sleep mode VCC = 3.3 V		100	170	mA
		Average in standby mode VCC = 3.3 V			2000	µA
C	Pin capacitance	All pins			15	pF

AC CHARACTERISTICS
TIMING REQUIREMENTS (VCC = 3.3 ± 0.3 V, CL = 50 pF, TOPR = 0 to 70 °C unless otherwise noted)

(1) Input transition time

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tr(INPUT)	Input rise transition time	CMOS input		5	ns	①
		$\overline{RST}$ pin		2	ms	
tf(INPUT)	Input fall transition time	CMOS input		5	ns	②
		$\overline{RST}$ pin		2	ms	

(2) Clock, reset and wakeup timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tc(CLKIN)	Clock input cycle time		60	100	ns	⑤
tw(CLKINH)	External clock input “H” pulse width		1/4CLKIN		ns	⑥
tw(CLKINL)	External clock input “L” pulse width		1/4CLKIN		ns	⑦
tr(CLKIN)	External clock input rising time			5	ns	⑧
tf(CLKIN)	External clock input falling time			5	ns	⑨
tw(RST)	Reset input “L” pulse width		2		ms	⑩
tw(WKUP)	Wakeup input “L” pulse width		2		ms	⑪

(3) Read and write timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tsu(D-CLKIN)	Data input set-up time before CLKIN		5.5		ns	㉚
th(CLKIN-D)	Data input hold time after CLKIN		2		ns	㉛
tsu(DCH-CLKIN)	$\overline{DC}$ input “H” set-up time before CLKIN		10		ns	㊱
th(CLKIN-DCH)	$\overline{DC}$ input “H” hold time after CLKIN		2		ns	㊲
tsu(DCL-CLKIN)	$\overline{DC}$ input “L” set-up time before CLKIN		10		ns	㊳
th(CLKIN-DCL)	$\overline{DC}$ input “L” hold time after CLKIN		2		ns	㊴

(4) Arbitration and external bus master read/write timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tsu(HREQ-CLKIN)	$\overline{\text{HREQ}}$ input set-up time before CLKIN		5		ns	㊵
th(CLKIN-HREQ)	$\overline{\text{HREQ}}$ input hold time after CLKIN		2		ns	㊶
tsu(CS-CLKIN)	$\overline{\text{CS}}$ input set-up time before CLKIN		7		ns	㊽
th(CLKIN-CS)	$\overline{\text{CS}}$ input hold time after CLKIN		2		ns	㊾
tsu(A-CLKIN)	Address input set-up time before CLKIN		5		ns	㊿
th(CLKIN-A)	Address input hold time after CLKIN		3		ns	(51)
tsu(D-CLKINL)	Data input set-up time before CLKIN		5		ns	(52)
th(CLKINL-D)	Data input hold time after CLKIN		3		ns	(53)

(5) Interrupt control unit timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tw(INT)	$\overline{\text{INT}}$ input pulse width (see note)		tc(CLKIN)		ns	(63)
tw(SBI)	$\overline{\text{SBI}}$ input pulse width (see note)		tc(CLKIN)		ns	(64)

Note: Both $\overline{\text{INT}}$ and $\overline{\text{SBI}}$ are level-sense inputs. Keep them at an "L" level until the interrupt is accepted.

(6) I/O port timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tw(PORTINL)	Port input “L” pulse width		30		ns	(69)
tw(PORTINH)	Port input “H” pulse width		30		ns	(70)

SWITCHING CHARACTERISTICS (VCC = 3.3 ± 0.3 V, CL = 50 pF, TOPR = 0 to 70 °C unless otherwise noted)

(1) Output transition time

Symbol	Parameter	Test conditions	Limits			Unit	Reference number
			Min.	Typ.	Max.		
tr(OUTPUT)	Output rising transition time				8	ns	③
tf(OUTPUT)	Output falling transition time				8	ns	④

(2) Read and write timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
td(CLKIN-BSHX)	$\overline{BS}$ = "H" effective time after CLKIN		0		ns	⑫
td(CLKIN-BSL)	$\overline{BS}$ = "L" delay time after CLKIN			12	ns	⑬
td(CLKIN-BSLX)	$\overline{BS}$ = "L" effective time after CLKIN		tc(CLKIN)/4		ns	⑭
td(CLKIN-BSH)	$\overline{BS}$ = "H" delay time after CLKIN			tc(CLKIN)/4+8	ns	⑮
td(CLKIN-AV)	Address delay time after CLKIN			16	ns	⑯
td(CLKIN-AX)	Address effective time after CLKIN		0		ns	⑰
td(CLKIN-BCV)	$\overline{BCH}$, $\overline{BCL}$ delay time after CLKIN			16	ns	⑱
td(CLKIN-BCX)	$\overline{BCH}$, $\overline{BCL}$ effective time after CLKIN		0		ns	⑲
td(CLKIN-SIDV)	SID delay time after CLKIN			16	ns	⑳
td(CLKIN-SIDX)	SID effective time after CLKIN		0		ns	㉑
td(CLKIN-STV)	ST delay time after CLKIN			16	ns	㉒
td(CLKIN-STX)	ST effective time after CLKIN		0		ns	㉓
td(CLKIN-RWV)	R/$\overline{W}$ delay time after CLKIN			16	ns	㉔
td(CLKIN-RWX)	R/$\overline{W}$ effective time after CLKIN		0		ns	㉕
td(CLKIN-BURSTHX)	$\overline{BURST}$ = "H" effective time after CLKIN		0		ns	㉖
td(CLKIN-BURSTL)	$\overline{BURST}$ = "L" delay time after CLKIN			12	ns	㉗
td(CLKIN-BURSTLX)	$\overline{BURST}$ = "L" effective time after CLKIN		0		ns	㉘
td(CLKIN-BURSTH)	$\overline{BURST}$ = "H" delay time after CLKIN			12	ns	㉙
td(CLKIN-DZX)	Data output enable time after CLKIN		0		ns	㉜
td(CLKIN-DV)	Data output delay time after CLKIN			18	ns	㉝
td(CLKIN-DVX)	Data output effective time after CLKIN		0		ns	㉞
td(CLKIN-DXZ)	Data output disable time after CLKIN			16	ns	㉟

(3) Arbitration and external bus master read/write timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
td(CLKIN-HACKHX)	$\overline{HACK}$ = "H" effective time after CLKIN		0		ns	㊷
td(CLKIN-HACKL)	$\overline{HACK}$ = "L" delay time after CLKIN			12	ns	㊸
td(CLKIN-HACKLX)	$\overline{HACK}$ = "L" effective time after CLKIN		0		ns	㊹
td(CLKIN-HACKH)	$\overline{HACK}$ = "H" delay time after CLKIN			12	ns	㊺
td(CLKIN-AZ)	Address output disable time after CLKIN			16	ns	㊻
td(CLKIN-AZX)	Address output enable time after CLKIN		0		ns	㊼
td(CLKIN-DZX)	Data output enable time after CLKIN		0		ns	㊿
td(CLKIN-DV)	Data output delay time after CLKIN			18	ns	(55)
td(CLKIN-DXZ)	Data output disable time after CLKIN			16	ns	(56)
td(CLKIN-DVX)	Data output effective time after CLKIN		0		ns	(57)
td(CS-DCZX)	$\overline{DC}$ output enable time after $\overline{CS}$		0		ns	(58)
td(CLKIN-DCHX)	$\overline{DC}$ = "H" effective time after CLKIN		0		ns	(59)
td(CLKIN-DCL)	$\overline{DC}$ = "L" delay time after CLKIN			16	ns	(60)
td(CLKIN-DCXZ)	$\overline{DC}$ output disable time after CLKIN			16	ns	(61)
td(CLKIN-DCLX)	$\overline{DC}$ = "L" effective time after CLKIN		0		ns	(62)

(4) Standby timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
td(CLKIN-STBYHX)	$\overline{STBY}$ = "H" effective time after CLKIN		0		ns	(65)
td(CLKIN-STBYL)	$\overline{STBY}$ = "L" delay time after CLKIN (see note)			tc(CLKIN)n/4+15	ns	(66)
td(CLKIN-STBYLX)	$\overline{STBY}$ = "L" effective time after CLKIN		0		ns	(67)
td(CLKIN-STBYH)	$\overline{STBY}$ = "H" delay time after CLKIN (see note)			tc(CLKIN)n/4+15	ns	(68)

Note: The $\overline{STBY}$ signal is synchronized with the internal clock, therefore its timing changes at 0, 90, 180 and 270 (n=0, 1, 2, 3) degree phase of CLKIN.

(5) I/O port timing

Symbol	Parameter	Test conditions	Limits		Unit	Reference number
			Min.	Max.		
tw(PORTOUTL)	Port output "L" pulse width (see note)		12		ns	(71)
tw(PORTOUTH)	Port output "H" pulse width (see note)		12		ns	(72)

Note: The minimum pulse width value is that where the output is changed within 1 clock of the internal clock. Software processing time to write to the port data register is not included.

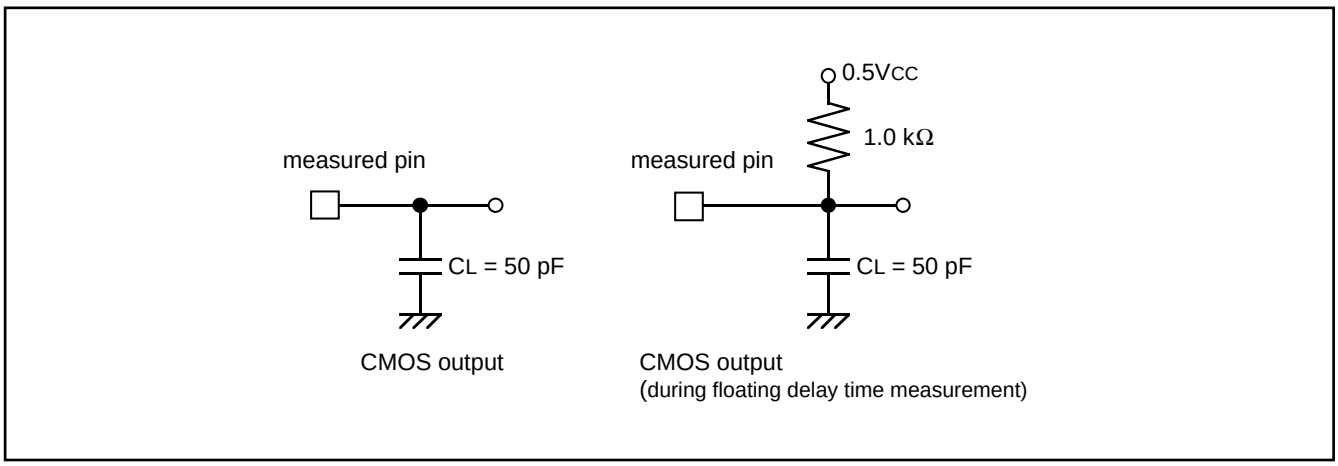


Fig. 34 Output switching characteristic measurement circuit

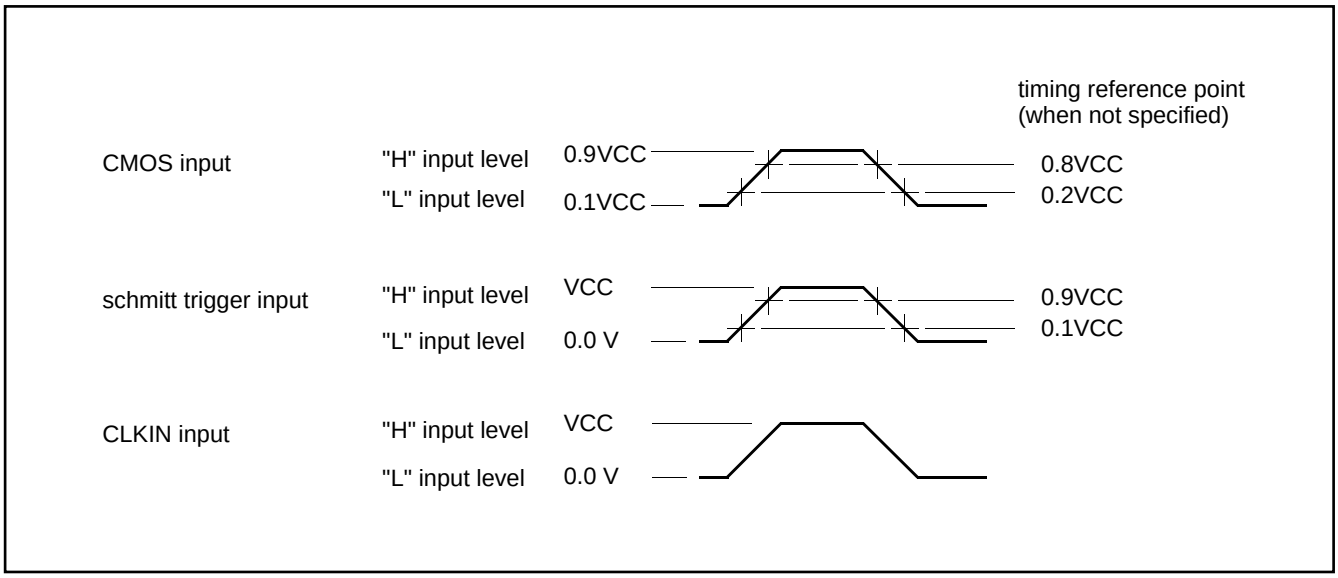


Fig. 35 Input waveform and timing reference point during characteristic measurement

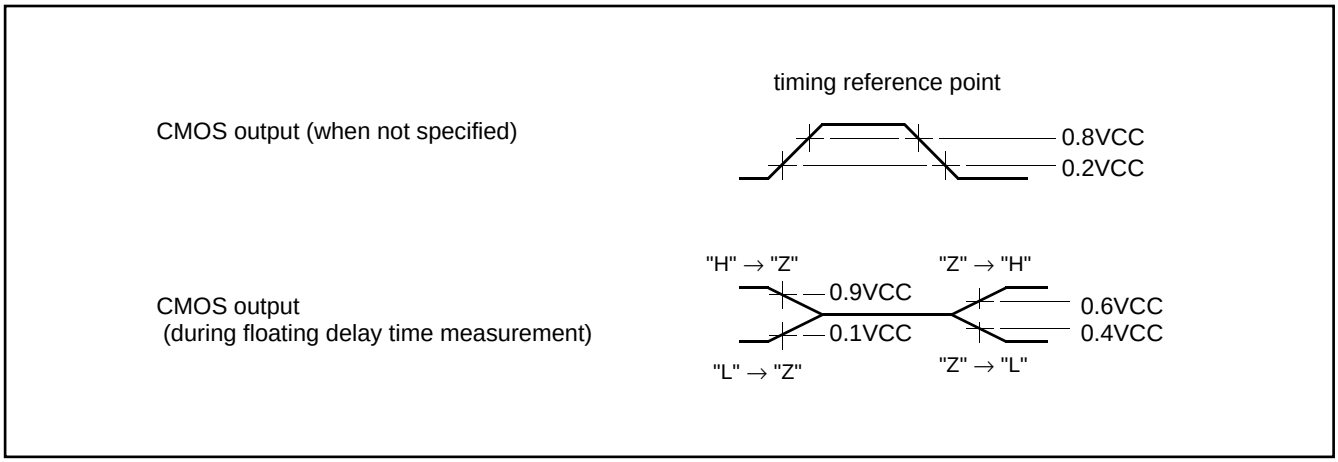


Fig. 36 Output timing measurement point during characteristic measurement

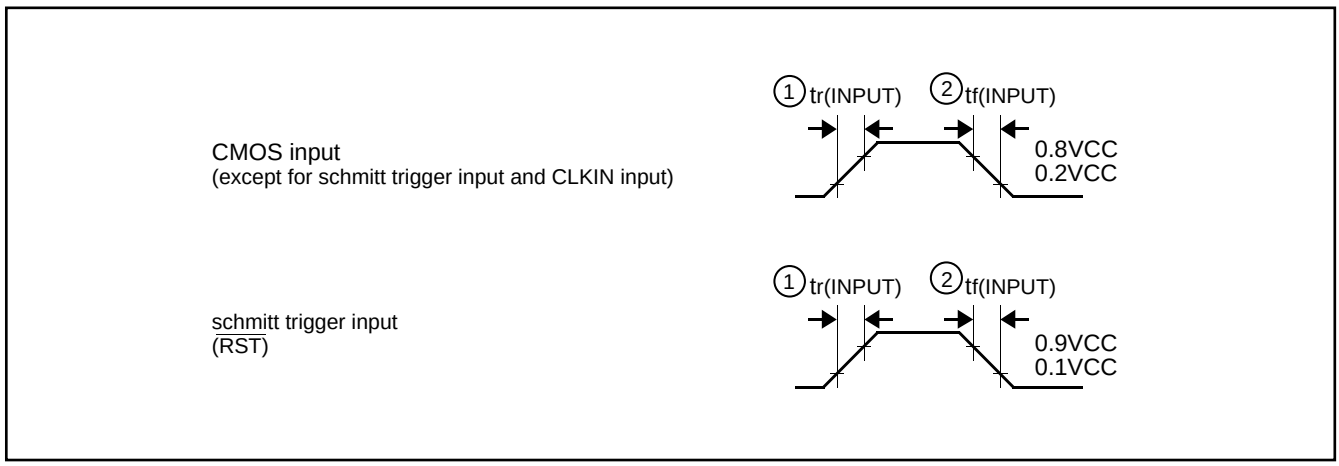


Fig. 37 Input transition time

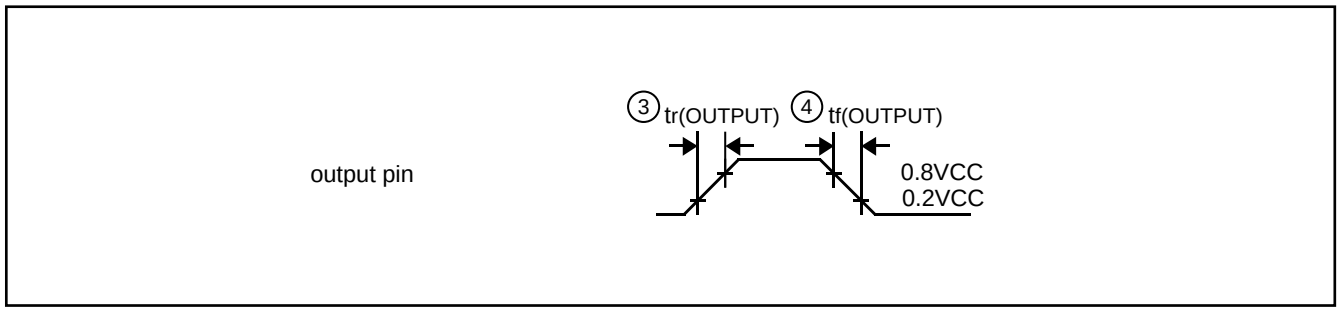
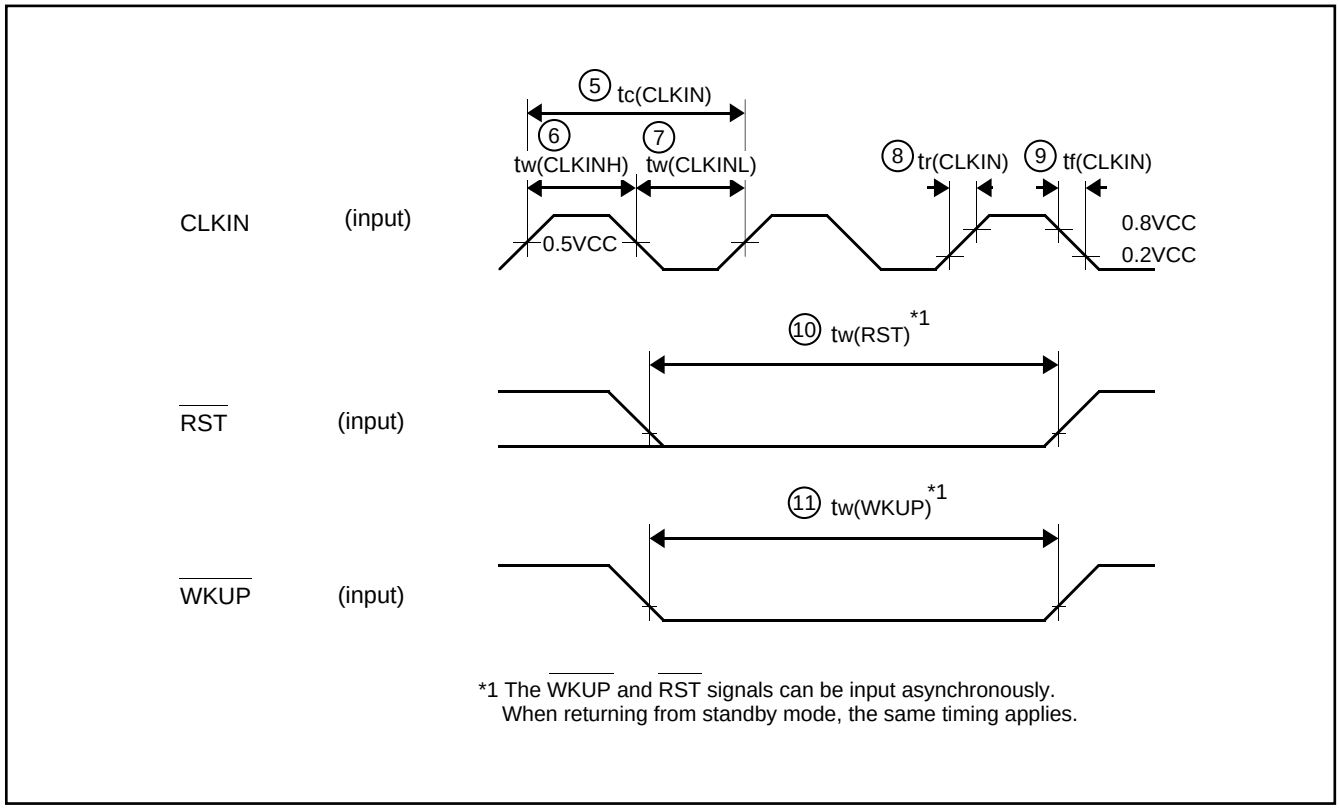
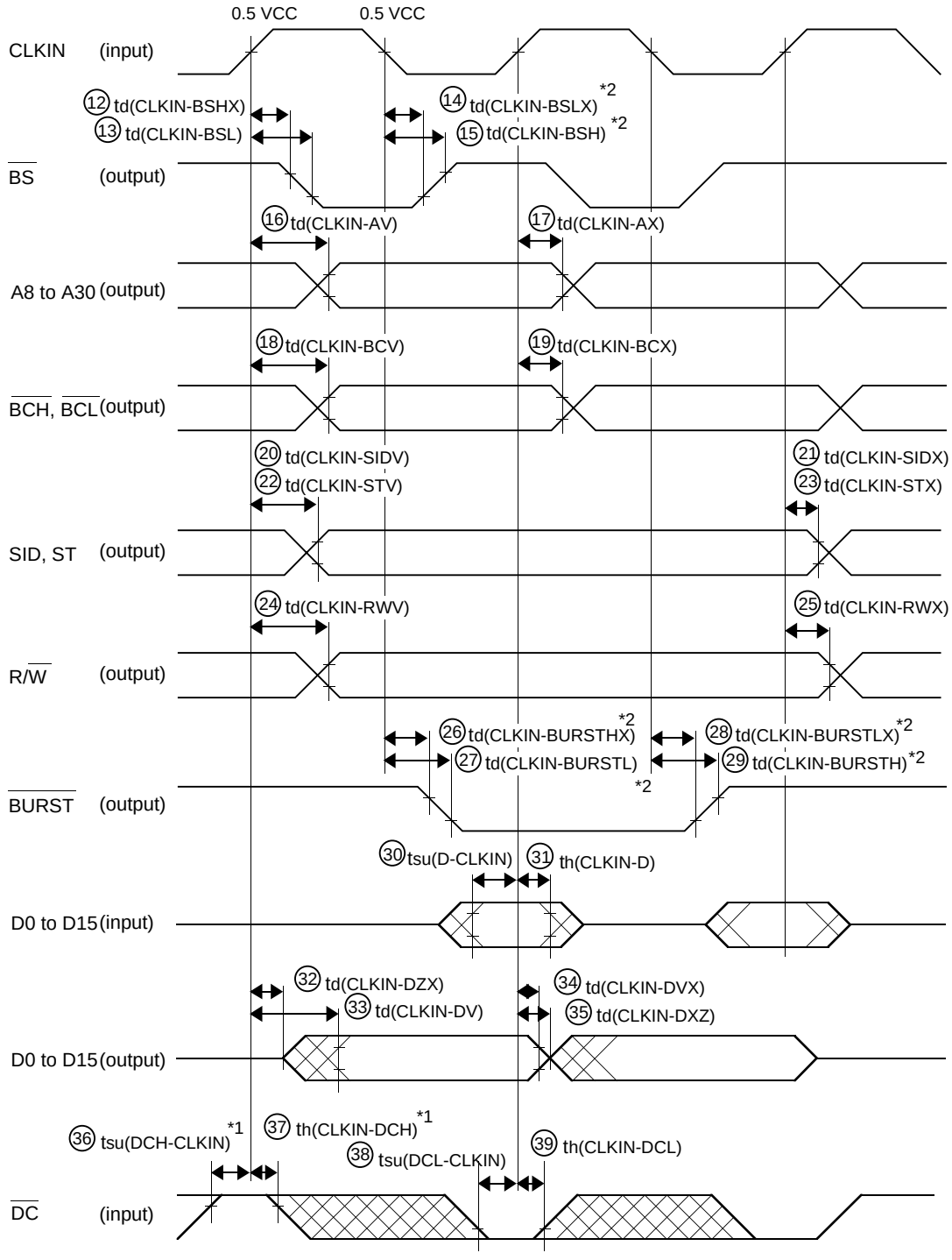


Fig. 38 Output transition time



*1 The WKUP and RST signals can be input asynchronously.
When returning from standby mode, the same timing applies.

Fig. 39 Clock reset and wakeup timing



*1 The set up/hold of $\overline{DC}$ = "H" may vary depending on the wait cycle insertion.

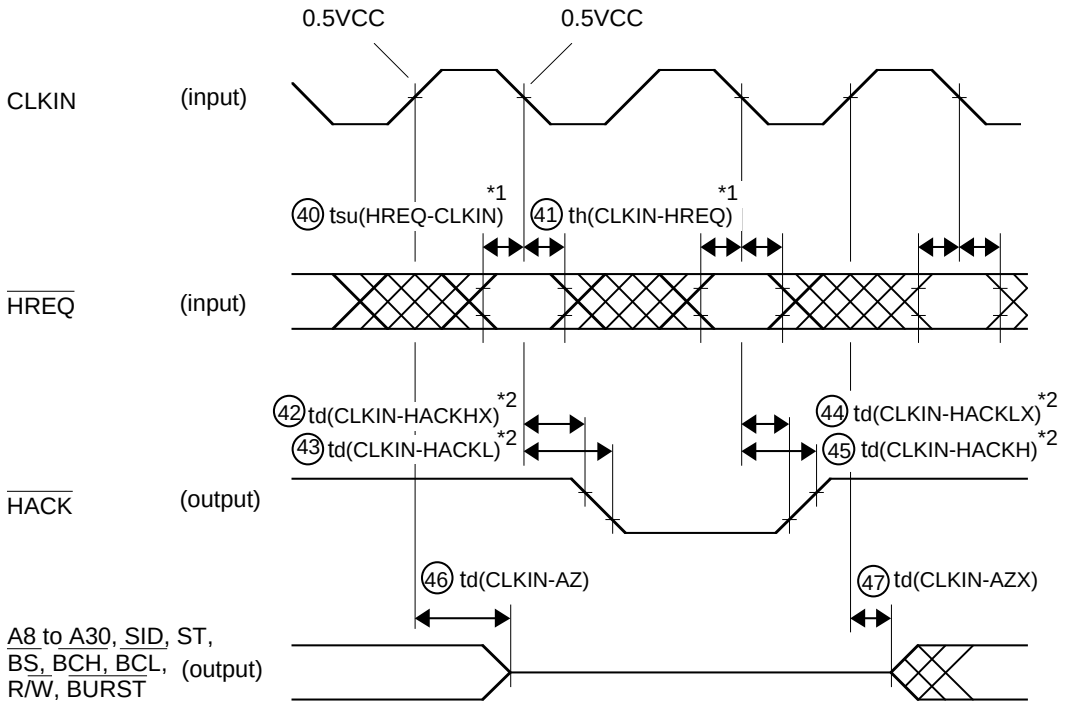
*2 All switching characteristics and timing requirements based on the falling edge of CLKIN are calculated according to the internal CLKIN (duty ratio is 50%) . When designing external peripheral circuits, the correction for the duty cycle of the actual CLKIN is necessary.

[example]

$\overline{BS}$ signal transition ("L" –> "H") when inputting 16.65 MHz clock whose duty ratio is 45 - 55% (± 5%) to CLKIN:

- minimum value of td(CLKIN-BSLX) = (value in table) – (correction value) = 15 – (60 x 5/100) = 12 [ns]
- maximum value of td(CLKIN-BSH) = (value in table) + (correction value) = (60/4 + 8) + (60 x 5/100) = 26 [ns]

Fig. 40 Read/write timing



*1 The HREQ signal can be input asynchronously.

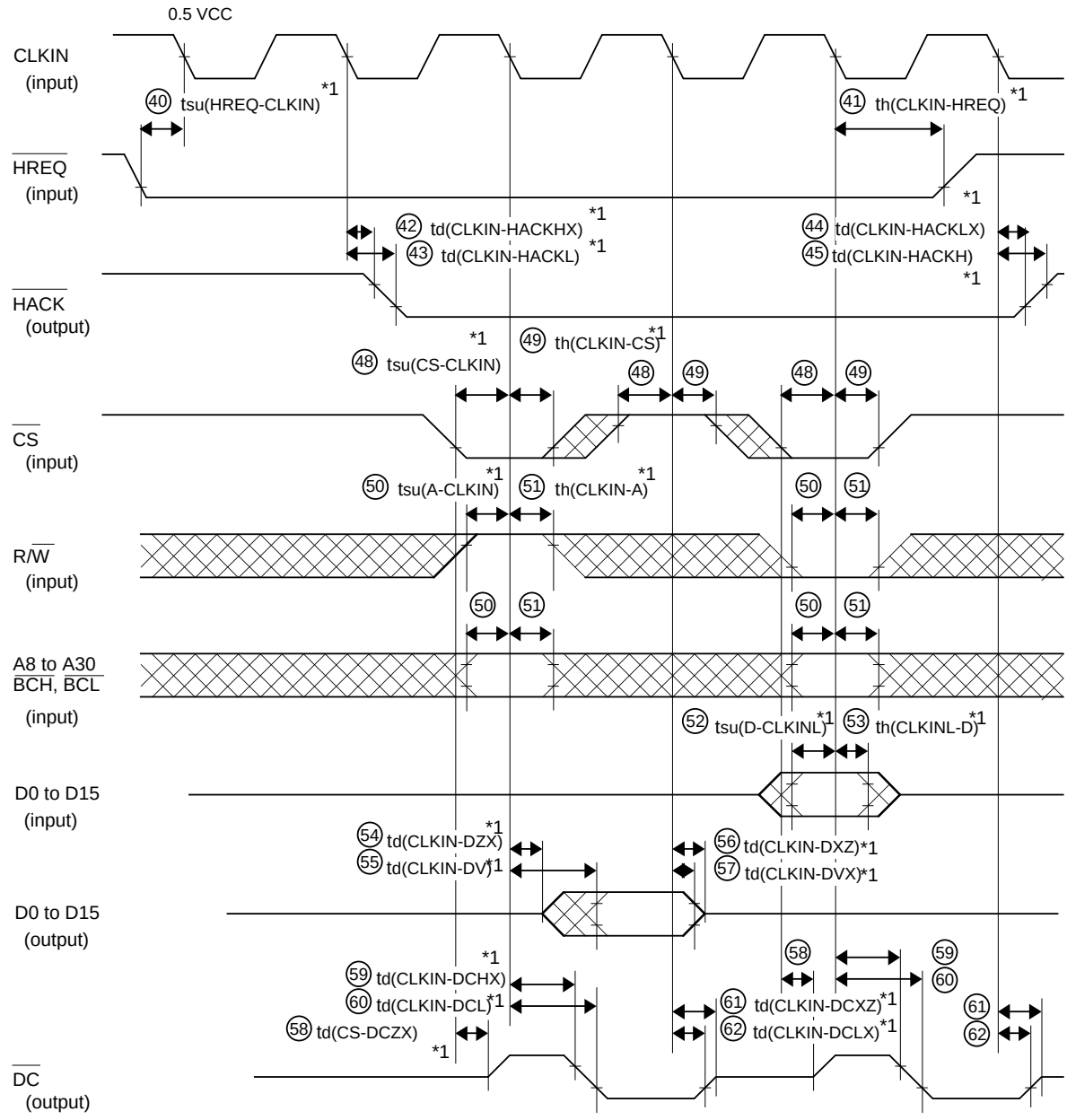
*2 All switching characteristics and timing requirements based on the falling edge of CLKIN are calculated according to the internal CLKIN (duty ratio is 50%) . When designing external peripheral circuits, the correction for the duty cycle of the actual CLKIN is necessary.

[example]

HACK signal transition ("H" –> "L") when inputting 16.65 MHz clock whose duty ratio is 45 - 55% (± 5%) to CLKIN:

- minimum value of td(CLKIN-HACKHX) = (value in table) – (correction value) = 0 – (60 x 5/100) = –3 [ns]
- maximum value of td(CLKIN-HACKL) = (value in table) + (correction value) = 12 + (60 x 5/100) = 15 [ns]

Fig. 41 Bus arbitration timing

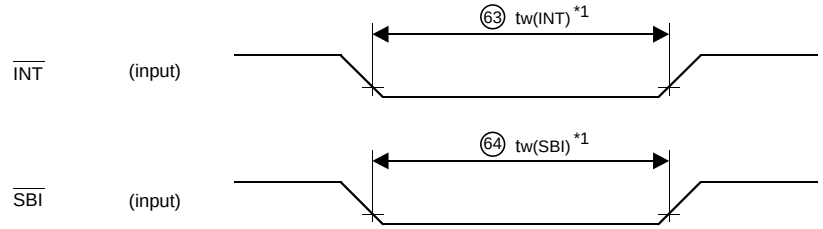


*1 All switching characteristics and timing requirements based on the falling edge of CLKIN are calculated according to the internal CLKIN (duty ratio is 50%) . When designing external peripheral circuits, the correction for the duty cycle of the actual CLKIN is necessary.

[example]
CS signal transition ("L" –> "H") when inputting 16.65 MHz clock whose duty ratio is 45 - 55% (± 5%) to CLKIN:

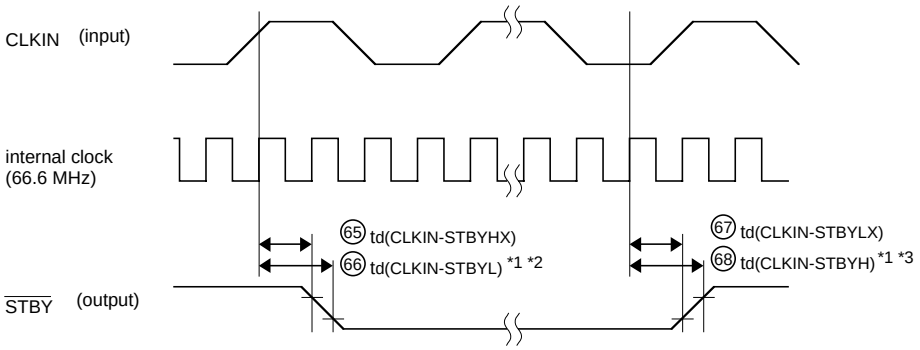
- minimum value of tsu(CS-CLKIN) = (value in table) + (correction value) = 10 + (60 x 5/100) = 13 [ns]
- minimum value of th(CLKIN-CS) = (value in table) + (correction value) = 2 + (60 x 5/100) = 5 [ns]

Fig. 42 External bus master read/write timing



*1 The $\overline{INT}$ and $\overline{SBI}$ signals can be input asynchronously.
When returning from CPU sleep mode, the same timing applies.
This timing value is "a value necessary for sampling the input to pins", however, not "a value that guarantees the interrupt acceptance".
The interrupt request is a level-sensed input , and should be kept "L" until it is accepted.

Fig. 43 Interrupt input timing



*1 The $\overline{STBY}$ signal is synchronized with the internal clock therefore, its timing changes at 0, 90, 180 and 270 degree phase of CLKIN.
*2 The $\overline{STBY}$ goes to an "L" level when switched to the standby mode.
*3 When returning from standby mode, the $\overline{STBY}$ signal goes to an "H" level 1 CLKIN after sampling that $\overline{WKUP}$ has returned from "L" to "H", or 3 CLKINs after sampling that $\overline{RST}$ = "L".

Fig. 44 Standby timing

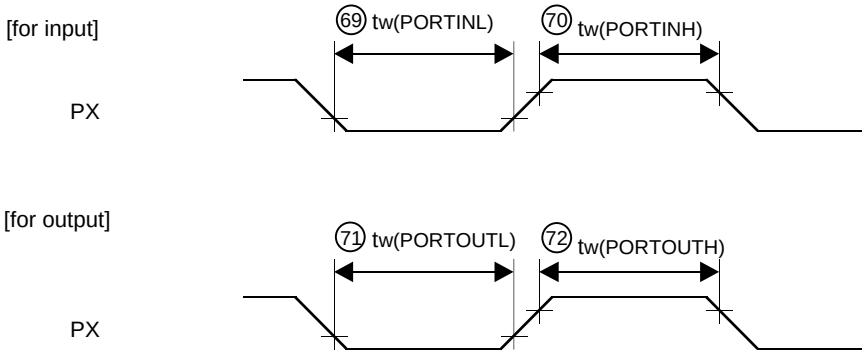


Fig. 45 I/O port timing

M32000D4AFP

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

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REVISION DESCRIPTION LIST	M32000D4AFP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	970901
1.1	• "After $\overline{DC}$ outputs an ~ CLKIN falling edge." revised (line 18, page 24). • Notes in Figure 23 revised (page 24). • "After $\overline{DC}$ outputs an ~ CLKIN falling edge." revised (line 19, page 25). • Notes in Figure 24 revised (page 25). • Table 2 revised (page 28). • (3) Arbitration and external bus master read/write timing Symbol | Parameter | td(CS-DCZX) | $\overline{DC}$ output enable time after $\overline{CS}$ | corrected (page 37). •"(58) td(CS-DCZX)*1 " in Fig. 42 corrected (page 42). • Notes in Figure 44 revised (page 43).	980501
1.2	• Figure 23 revised (page 24).	980911