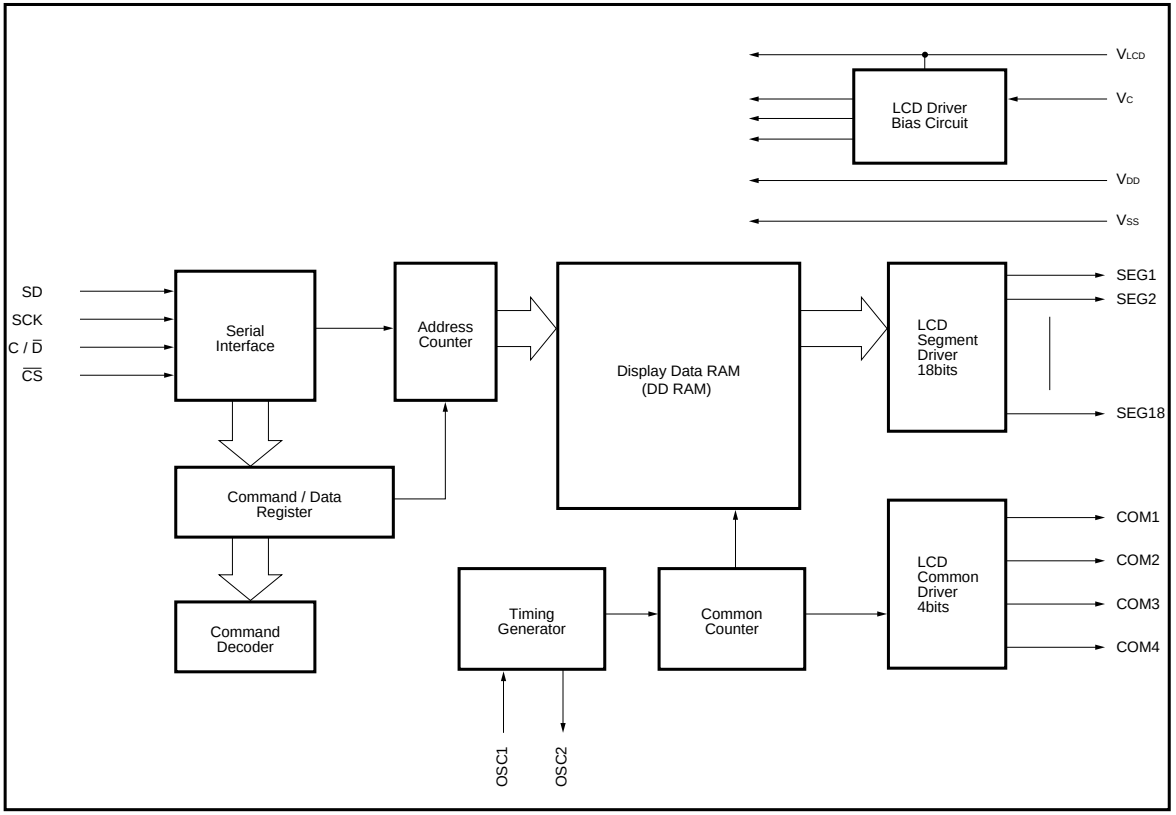
Segment-type LCD driver
BU9729K

The BU9729K is a driver for segmented liquid crystal displays, which enables connection with a microcomputer through a serial interface. 4-bit common output and an internal power supply circuit for LCD drive make it possible to configure a low-cost display system.

●Applications
Movie projectors, car audio equipment, telephones

●Features
1) Serial interface (8-bit length).
2) Display RAM: 72bits, internal (up to 72 segments can be displayed).
3) Internal power supply circuit for liquid crystal drive.
4) Display duty: 1 / 4.
5) Low-voltage and low-current operation supported.

●Block diagram



●Pin assignments

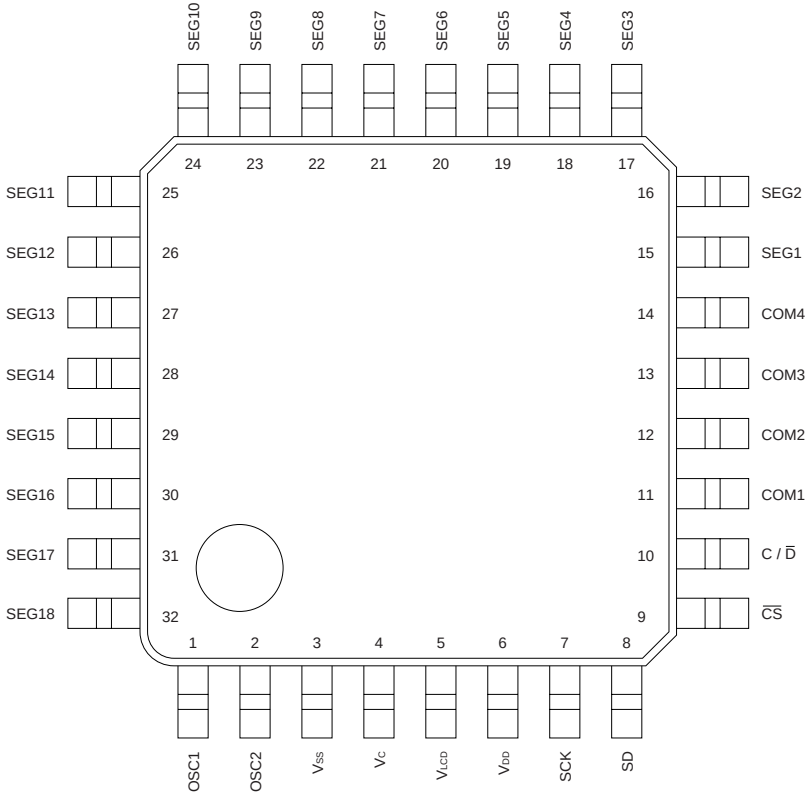


Fig.1

●Pin descriptions

Pin name	Pin No.	I / O	Function
OSC1 OSC2	1 2	I O	These are the I / O pins for the internal oscillator. Resistance should be connected between the pins when the internal clock is operating. When an external clock is operating, input should be done from OSC1, and OSC2 should be left open.
V_{SS}	3	—	This is the V_{SS} pin.
V_C V_{LCD}	4 5	—	This is the power supply pin for LCD drive. The condition $V_{LCD} \geqq V_C \geqq V_{SS}$ must be satisfied.
V_{DD}	6	—	This is the V_{DD} pin.
SCK	7	I	This is the shift lock input pin for serial data. The contents of the SD pin are read one bit at a time at the rising edge of this pin.
SD	8	I	This is the serial data input pin. Display data and commands are input here. When this is "0", display data is not displayed, and when "1", the data is displayed.
$\overline{CS}$	9	I	This is the chip select signal input pin. When this is LOW, SD input can be received. The SCK counter is incremented at the timing at which $\overline{CS}$ goes from HIGH to LOW.
C / $\overline{D}$	10	I	This is the signal input which recognizes whether the SD input consists of commands or display data. When the SCK of the eighth clock rises, this pin judges the input to be display data if the level is LOW, and a command if the level is HIGH.
COM1 ~ COM4	11 ~ 14	O	These are the common output pins for LCD drive. They are connected to the commons of the LCD panel.
SEG1 ~ SEG18	15 ~ 32	O	These are the segment output pins for LCD drive. They are connected to the segments of the LCD panel.

●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage 1	V_{DD}	– 0.3 ~ + 7.0	V
Power supply voltage 2	V_{LCD}	– 0.3 ~ + 7.0*1	V
Power dissipation	Pd	400*2	mW
Operating temperature	Topr	– 20 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C
Input voltage	V_{IN}	– 0.3 ~ V_{DD} + 0.3	V
Output voltage	V_{OUT}	– 0.3 ~ V_{DD} + 0.3	V

*1 The condition $V_{LCD} \geqq V_C \geqq V_{SS}$ must be satisfied.

*2 Reduced by – 4.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage 1	V_{DD}	2.5	—	5.5	V	—
Power supply voltage 2	V_{LCD}	2.5	—	5.5	V	The condition $V_{LCD} \geqq V_C \geqq V_{SS}$ must be satisfied.
Oscillation frequency	f_{OSC}	—	36	—	kHz	R_f = 470kΩ

●Electrical characteristics

DC characteristics (unless otherwise noted, V_{DD} = 2.5V to 5.5V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Applicable pin
Input high level voltage	V_{IH1}	0.8 × V_{DD}	—	V_{DD}	V	—	OSC1, SD, SCK, C / $\overline{D}$, $\overline{CS}$
Input low level voltage	V_{IL1}	0	—	0.2 × V_{DD}	V	—	—
LCD driver on-resistance*1	R_{ON}	—	—	30	kΩ	$\lvert\Delta V_{ON}\rvert$ = 0.1V	SEG1 ~ 32, COM1 ~ 4
Input high level current 2	I_{IL2}	—	—	2	µA	V_{IN} = 0	OSC1, SD, SCK, C / $\overline{D}$, $\overline{CS}$
Input low level current	I_{IH}	– 2	—	—	µA	V_{IN} = V_{DD}	OSC1, SD, SCK, C / $\overline{D}$,$\overline{CS}$
Input capacitance	C_I	—	5	—	pF	—	SD,SCK, C / $\overline{D}$, $\overline{CS}$
Current consumption	I_{DD}	—	0.05	1	µA	While quiescent*2	V_{DD}
		—	8	25	µA	When "ALL OFF" is displayed	
		—	40	80	µA	For display operations*3	
		—	100	250	µA	For access operations*4	

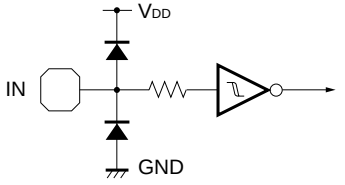
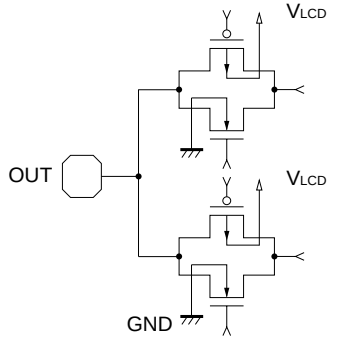
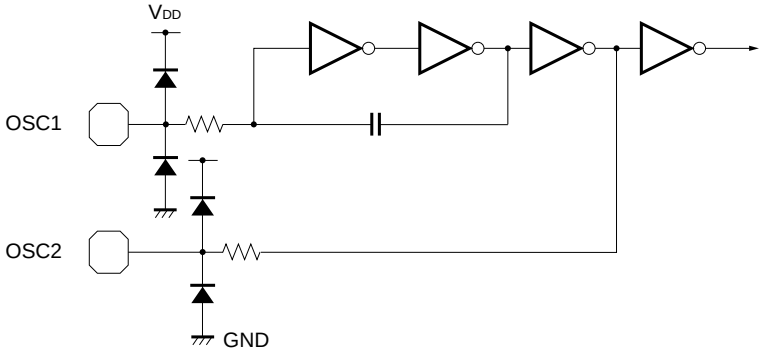
*1 The internal power supply impedance is not included in the LCD driver on-resistance.
*2 All input is fixed at either V_{DD} or V_{SS}.
*3 Except for R_f = 470kΩ and OSC1, all input is fixed at V_{DD} or V_{SS}.
*4 R_f = 470kΩ, fSCK = 200kHz.

AC characteristics (unless otherwise noted, V_{DD} = 2.5V to 5.5V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCK rise time	t_{TLH}	—	—	100	ns	—
SCK fall time	t_{THL}	—	—	100	ns	—
SCK cycle time	t_{CYC}	800	—	—	ns	—
Command wait time	t_{WAIT}	800	—	—	ns	—
SCK pulse width HIGH	t_{WH1}	300	—	—	ns	—
SCK pulse width LOW	t_{WL1}	300	—	—	ns	—
Data setup time	t_{SU1}	100	—	—	ns	—
Data hold time	t_{H1}	100	—	—	ns	—
$\overline{CS}$ pulse width HIGH	t_{WH2}	300	—	—	ns	—
$\overline{CS}$ pulse width LOW	t_{WL2}	6400	—	—	ns	—
$\overline{CS}$ setup time	t_{SU2}	100	—	—	ns	—
$\overline{CS}$ hold time	t_{H2}	100	—	—	ns	—
C / $\overline{D}$ setup time	t_{SU3}	100	—	—	ns	—
C / $\overline{D}$ hold time	t_{H3}	100	—	—	ns	8th rise of SCK used as reference
C / $\overline{D}$-$\overline{CS}$ time*5	t_{CCH}	100	—	—	ns	$\overline{CS}$ rise used as reference
C / $\overline{D}$-SCK time*5	t_{SCH}	100	—	—	ns	8th fall of SCK used as reference

*5 Should satisfy either one of these conditions.

●Input / output circuits

Pin name	I / O	Equivalent circuit	Pin name	I / O	Equivalent circuit
SD SCK C / $\overline{D}$ $\overline{CS}$	I		SEG1 ~ SEG18 COM1 ~ COM4	O	
OSC1 OSC2	I O				

●Timing charts

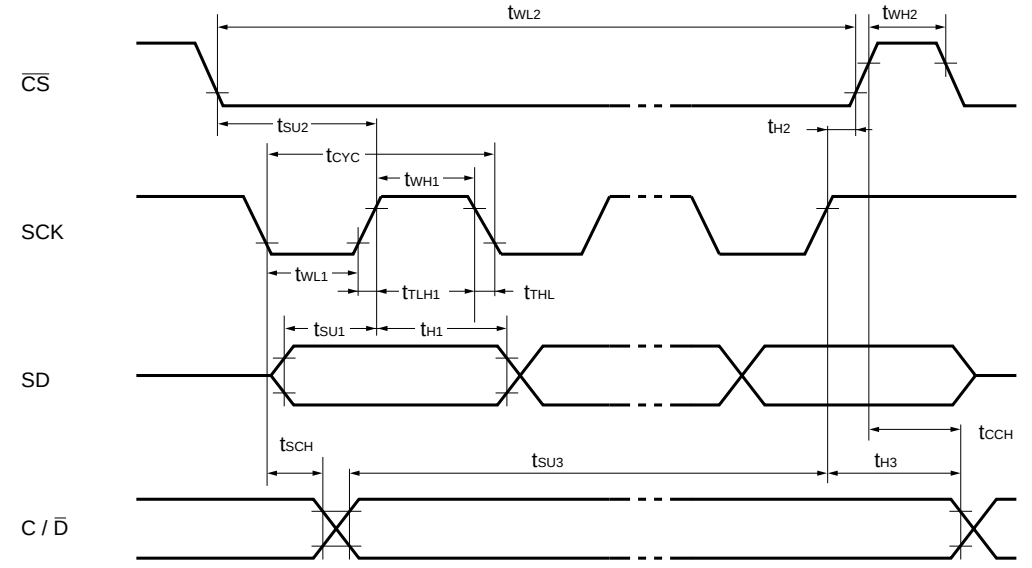


Fig. 2 Interface timing

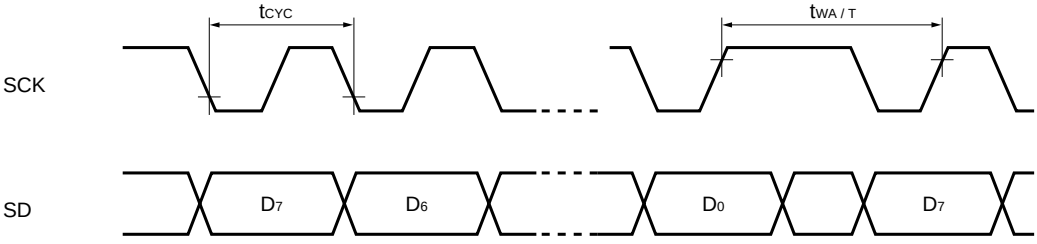


Fig. 3 Command cycle

●Data format

Serial data is transmitted using four-line clock synchronous transmission. Serial data with a length of eight bits is input synchronized to SCK. If C / $\overline{D}$ is HIGH at the rise of the 8 × nth clock of SCK, the serial data is recognized as a command, and if C / $\overline{D}$ is LOW, the serial data is recognized as display data.

Serial data is input sequentially, starting from the MSB.

●Detailed explanation of commands

The following commands (C / $\overline{D}$ is HIGH at the 8 × nth clock of SCK) are available for the BU9729K.

(1) Address Set

MSB							LSB
0	0	0	A	A	A	A	A

Address data displayed in binary format as AAAAA is set for the address counter.
The address is incremented by two each time input of the display data (8 bits of data) is completed.

(2) Display On

MSB							LSB
0	0	1	*	*	*	*	*

*: Don't Care

All displays light, regardless of the contents of the display data RAM (DDRAM). At this point, the contents of the DDRAM do not change.

(3) Display Off

MSB							LSB
0	1	0	*	*	*	*	*

*: Don't Care

All displays go out, regardless of the contents of the DDRAM.
At this point, the contents of the DDRAM do not change.

(4) Display Start

MSB							LSB
0	1	1	*	*	*	*	*

*: Don't Care

The display begins, in accordance with the contents of the DDRAM.

(5) Display Data RAM (DDRAM) Write

MSB							LSB
1	0	0	*	D	D	D	D

*: Don't Care

The binary 4-bit data DDDD is written to the DDRAM.
The address is that specified by the Address Set command. After this command is executed, the address is automatically incremented by + 1.

(6) Reset

MSB							LSB
1	1	0	*	*	*	*	*

*: Don't Care

This command should be executed after the power supply has been turned on and before any other command is executed. This command causes the BU9729K to initialize the following:

Display Off
Address Counter Reset

●Description of functions

(1) Register

The BU9729K has an 8-bit command / data register. Serial data is read in 8-clock units of SCK.
If the data read into the register is displayed data (C / $\overline{D}$ is LOW at the eighth clock of SCK), it is written to the DDRAM. If it is command data (C / $\overline{D}$ is HIGH at the eighth clock of SCK), it is output to the command decoder to control the BU9729K.

(2) Address counter

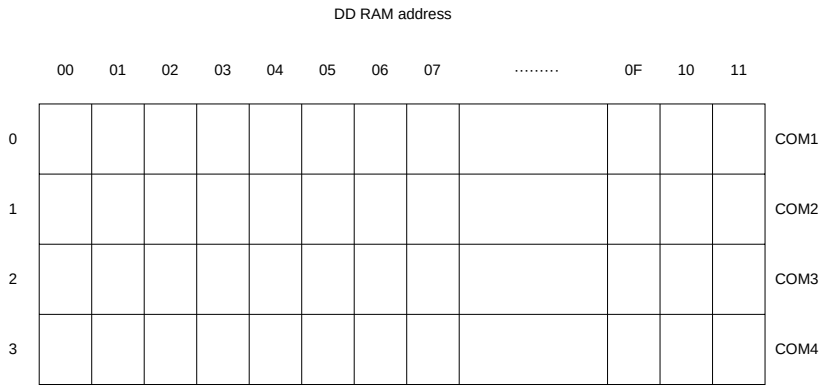
The address counter indicates DDRAM addresses. When the Address Set command is written to a command or data register, the address data is sent automatically to the address counter.
After data has been written to the DDRAM, the address counter increments automatically by either + 1 or + 2. The amount by which the counter increments is determined automatically, based on the following status.

DDRAM 8-bit writing (C / $\overline{D}$ is LOW at the eighth clock of SCK) $\rightarrow$ + 2
DDRAM 4-bit writing (C / $\overline{D}$ is HIGH at the eighth clock of SCK) $\rightarrow$ + 1

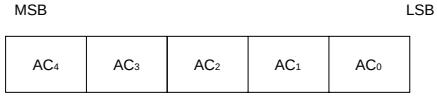
When the address counter has counted to the address 11H, it becomes 00H the next time it is incremented.

(3) Display data RAM (DDRAM)

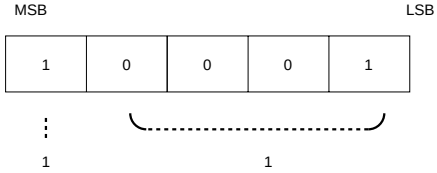
The display data RAM (DDRAM) is used to store display data. It has a capacity of 18 addresses $\times$ 4 bits.
The relationship between the DDRAM and the display position is shown below.



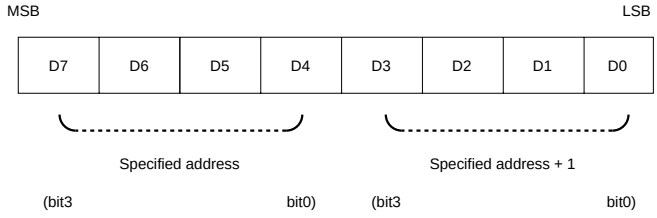
DDRAM addresses set for the address counter are in hexadecimal format, and are displayed as shown below.



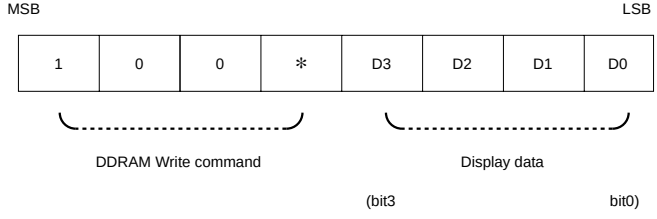
(Example) When the DDRAM address is "11" (display position: SEG18)



Display data input to the command / data register (C / $\overline{D}$ = LOW) is divided into the first four bits and the last four bits, with the specified DDRAM address being written to the first four, and the specified address + 1 being written to the last four. The four bits of display data are written sequentially to the bits of the DDRAM, starting from the MSB on both sides.



When a DDRAM Write command is input (C / $\overline{D}$ = HIGH), the four bits of display data in the DDRAM Write command are written to the specified DDRAM address. The four bits are written sequentially, starting from the MSB, to the bits of the DDRAM, starting with the MSB of the DDRAM.



(4) Timing generator

Connecting Rf between OSC1 and OSC2 causes oscillation of the internal oscillator circuit and generates a display timing signal. Operation can also be initiated by inputting an external clock.

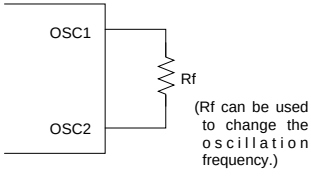


Fig. 4 Rf oscillator circuit

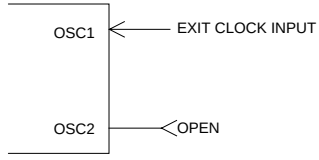


Fig. 5 External clock input

(5) LCD driver power supply

The LCD driver power supply is generated by the BU9729K. $V_1 = 2 \cdot V_C / 3$, $V2 = V_C / 3$ is generated internally.

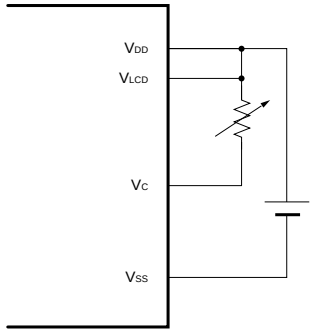


Fig. 6 Example of power supply connection

(6) LCD drive circuit

The LCD drive circuit is configured of 4 common drivers and 18 segment drivers. When oscillation begins, any effective common output automatically outputs a selective waveform, while the others output non-selective waveforms. Segment output automatically outputs drive waveforms, based on the display data and common counter. The common and segment output waveforms are shown in the following examples.

●LCD drive waveforms

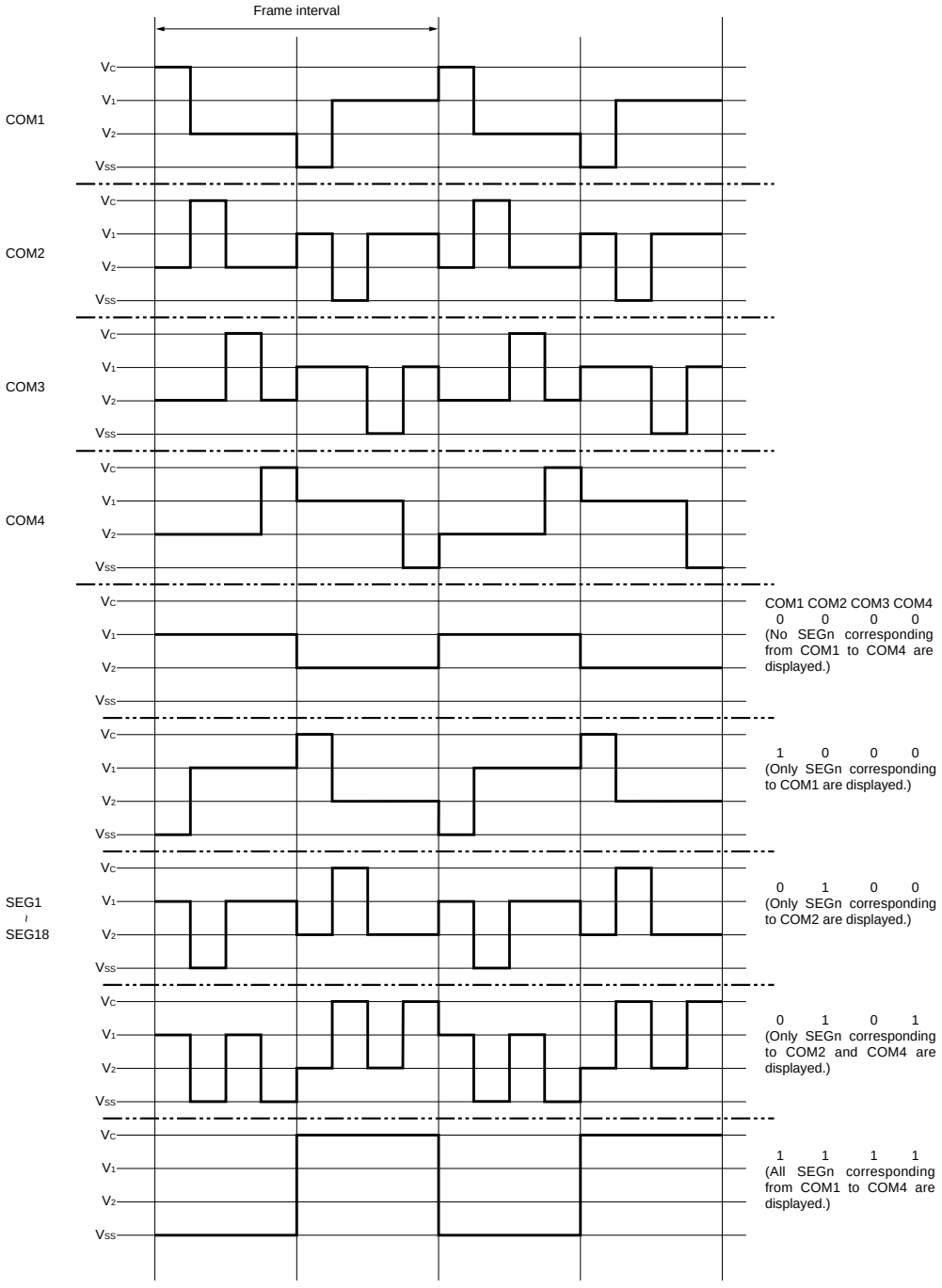
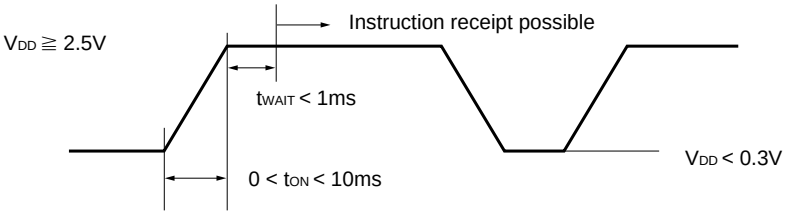
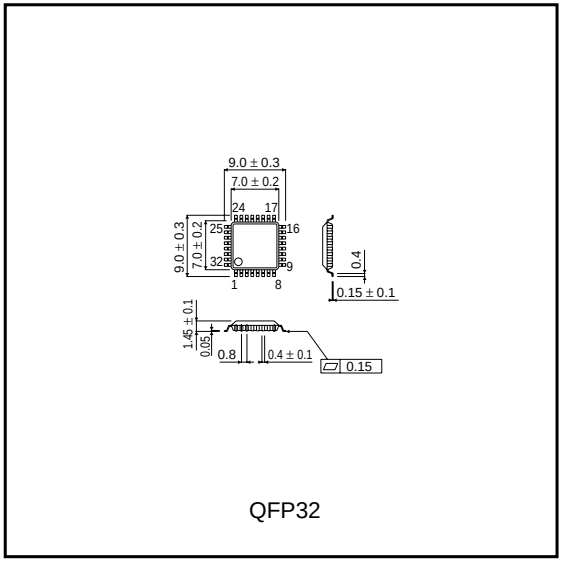


Fig. 7

V_{DD} has to satisfy the following conditions.



●External dimensions (Units: mm)



QFP32