

DATA SHEET

TDA9952

10-bit, 3.0 V, 25 Msps
analog-to-digital interface for
CCD cameras

Preliminary specification
Supersedes data of 2001 Jul 04

2002 Aug 21

10-bit, 3.0 V, 25 Msps analog-to-digital interface for CCD cameras

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FEATURES

- Sample rate = 25 Msps; 10-bit resolution
- Single 3.0 V supply operation (2.2 to 3.6 V operation for the digital outputs)
- Low power consumption: only 115 mW at 2.7 V
- Power consumption in standby mode: 4.5 mW (typical value)
- Programmable gain amplifier: gain range = 36 dB in 0.1 dB steps
- Correlated double sampling
- Internal input buffer for the correlated double sampling
- Fully programmable via a 3-wire serial interface
- 8-bit DAC included for external analog settings
- TTL-compatible inputs and CMOS-compatible outputs.

GENERAL DESCRIPTION

The TDA9952 is a 10-bit analog-to-digital interface for CCD cameras. The device consists of a Correlated Double Sampling (CDS) circuit, a digitally Programmable Gain Amplifier (PGA), a black level clamp and a 10-bit Analog-to-Digital Converter (ADC).

An internal CDS input buffer is incorporated in order to avoid using an external buffer that would consume more power and therefore optimizing the application for low noise, low power working.

The PGA gain, the ADC clamp level and other settings are controlled via a 3-wire serial digital interface.

An additional DAC is provided for system controls.

The TDA9952 operates from a single 3 V power supply (2.7 V minimum) and dissipates 135 mW (typical value).

APPLICATIONS

- Video camcorders
- Digital still cameras
- PC-cameras.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES		
	NAME	DESCRIPTION	VERSION
TDA9952HL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2
TDA9952HN	HVQFN48	plastic, heatsink very thin quad flat package; no leads; 48 terminals; body $7 \times 7 \times 0.85$ mm	SOT619-1

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.2	2.5	3.6	V
I_{CCA}	analog supply current	all clamps active	–	43	–	mA
I_{CCD}	digital supply current	$f_{pix} = 25$ MHz	–	2.0	–	mA
I_{CCO}	digital outputs supply current	$f_{pix} = 25$ MHz; $C_L = 10$ pF; input ramp response time is 800 μ s	–	0.5	–	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	maximum CDS input voltage (peak-to-peak value)	$V_{CC} = 2.85$ V	650	–	–	mV
		$V_{CC} \geq 3.0$ V	800	–	–	mV
$f_{pix(max)}$	maximum pixel rate		25	–	–	MHz
$f_{pix(min)}$	minimum pixel rate	$O_{CCD(max)} = \pm 100$ mV	–	–	1	MHz
		$O_{CCD(max)} = \pm 200$ mV	–	–	2	MHz
DR_{PGA}	PGA dynamic range		–	36	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output (RMS value)	PGA code = 00; see Fig.8	–	0.4	–	LSB
$E_{in(rms)}$	equivalent input noise voltage (RMS value)	PGA code = 383	–	145	–	μ V
P_{tot}	total power consumption	$V_{CCA} = V_{CCD} = 3$ V; $V_{CCO} = 2.5$ V	–	135	–	mW
		$V_{CCA} = V_{CCD} = 2.7$ V; $V_{CCO} = 2.2$ V	–	115	–	mW
		standby mode	–	4.5	–	mW

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BLOCK DIAGRAM

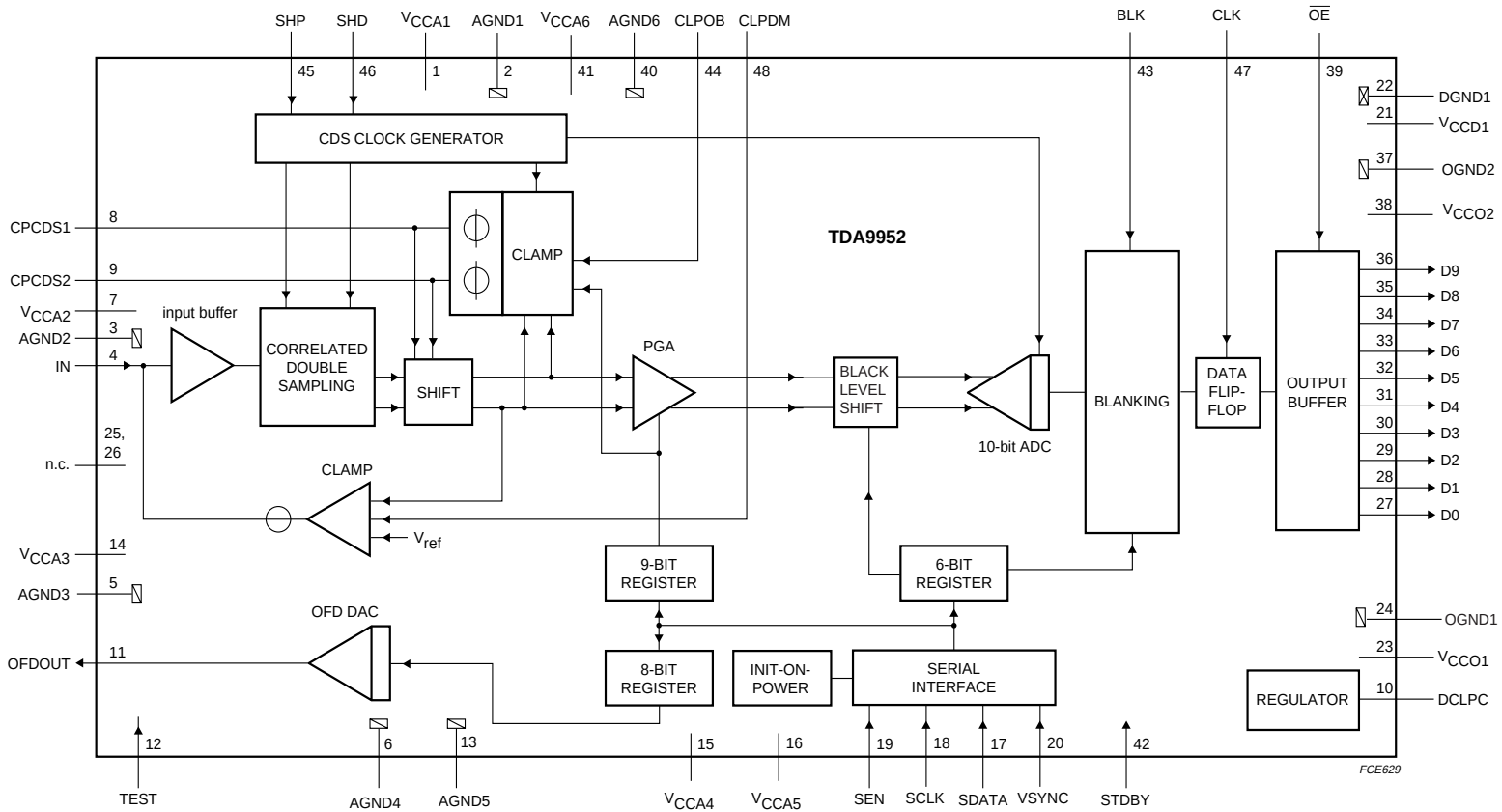


Fig.1 Block diagram.

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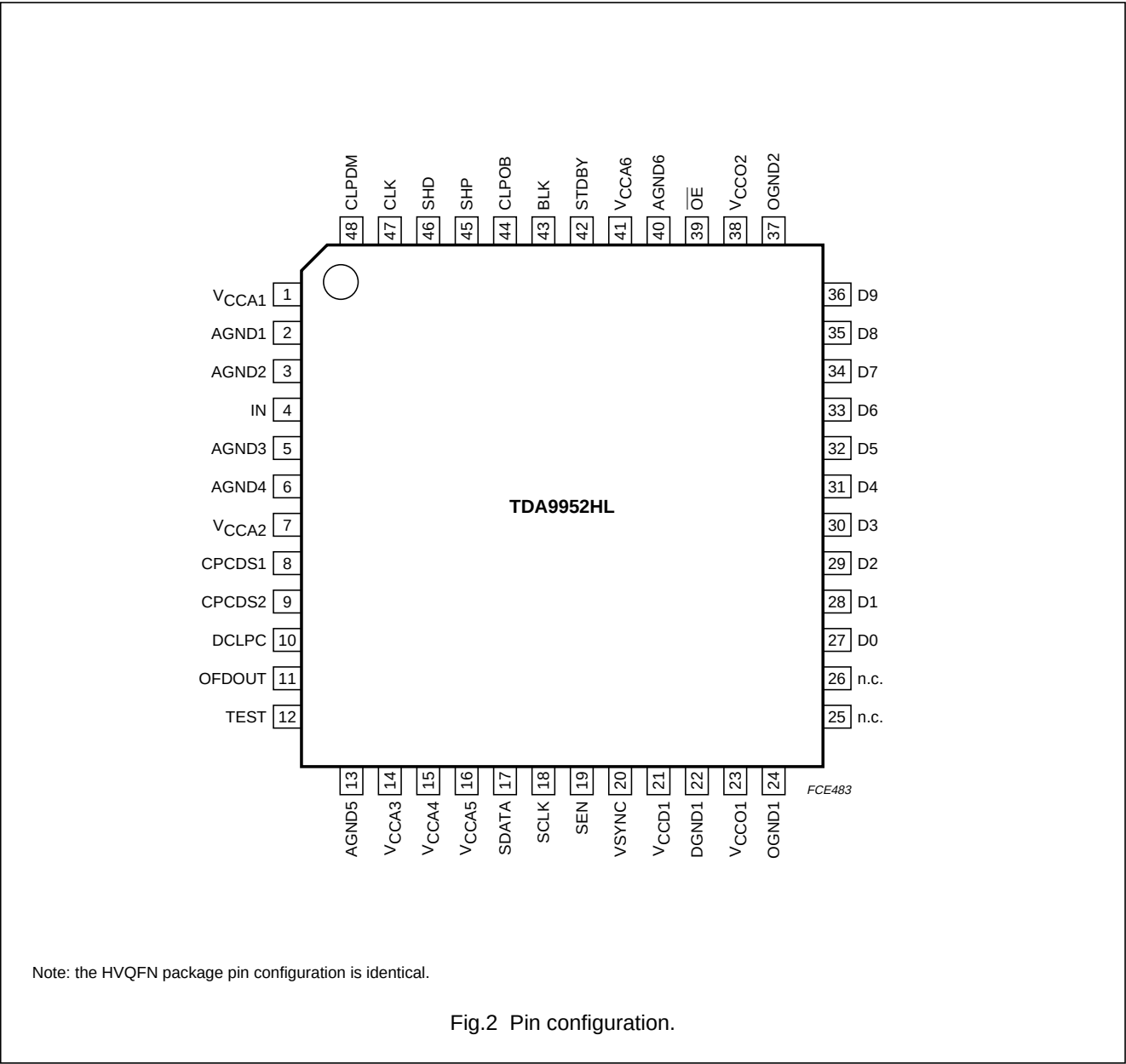
PINNING

SYMBOL	PIN	DESCRIPTION
V _{CCA1}	1	analog supply voltage1
AGND1	2	analog ground 1
AGND2	3	analog ground 2
IN	4	input signal from CCD
AGND3	5	analog ground 3
AGND4	6	analog ground 4
V _{CCA2}	7	analog supply voltage 2
CPCDS1	8	clamp storage capacitor pin 1
CPCDS2	9	clamp storage capacitor pin 2
DCLPC	10	regulator decoupling pin
OFDOUT	11	analog output of the additional 8-bit control DAC
TEST	12	test mode input pin (should be connected to AGND5)
AGND5	13	analog ground 5
V _{CCA3}	14	analog supply voltage 3
V _{CCA4}	15	analog supply voltage 4
V _{CCA5}	16	analog supply voltage 5
SDATA	17	serial data input for serial interface control
SCLK	18	serial clock input for serial interface
SEN	19	strobe pin for serial interface
VSYNC	20	vertical sync pulse input
V _{CCD1}	21	digital supply voltage 1
DGND1	22	digital ground 1
V _{CCO1}	23	digital output supply voltage 1
OGND1	24	digital output ground 1
n.c.	25	not connected
n.c.	26	not connected
D0	27	ADC digital output 0 (LSB)
D1	28	ADC digital output 1
D2	29	ADC digital output 2
D3	30	ADC digital output 3
D4	31	ADC digital output 4
D5	32	ADC digital output 5
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9 (MSB)
OGND2	37	digital output ground 2
V _{CCO2}	38	digital output supply voltage 2
OE	39	output enable control input (LOW: outputs active; HIGH: outputs in high-impedance)
AGND6	40	analog ground 6

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SYMBOL	PIN	DESCRIPTION
V _{CCA6}	41	analog supply voltage 6
STDBY	42	standby mode control input (LOW: TDA9952 active; HIGH: TDA9952 standby)
BLK	43	blanking control input
CLPOB	44	clamp pulse input at optical black
SHP	45	preset sample-and-hold pulse input
SHD	46	data sample-and-hold pulse input
CLK	47	data clock input
CLPDM	48	clamp pulse input at dummy pixel



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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	-0.3	+4.5	V
V_{CCD}	digital supply voltage	note 1	-0.3	+4.5	V
V_{CCO}	digital outputs supply voltage	note 1	-0.3	+4.5	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		-0.5	+0.5	V
	between V_{CCA} and V_{CCO}		-0.5	+1.2	V
	between V_{CCD} and V_{CCO}		-0.5	+1.2	V
V_i	input voltage	referenced to AGND	-0.3	+6.5	V
I_o	data output current		-	± 10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-20	+75	°C
T_j	junction temperature		-	150	°C

Note

1. All supplies are connected together.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

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CHARACTERISTICS

$V_{CCA} = V_{CCD} = 3.0\text{ V}$; $V_{CCO} = 2.5\text{ V}$; $f_{\text{pix}} = 25\text{ MHz}$; $T_{\text{amb}} = -20\text{ to }+75\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V _{CCA}	analog supply voltage		2.7	3.0	3.6	V
V _{CCD}	digital supply voltage		2.7	3.0	3.6	V
V _{CCO}	digital outputs supply voltage		2.2	2.5	3.6	V
I _{CCA}	analog supply current	all clamps active	–	43	–	mA
I _{CCD}	digital supply current		–	2.0	–	mA
I _{CCO}	digital outputs supply current	C _L = 10 pF on all data outputs; input ramp of 800 μs duration	–	0.5	–	mA
P _{tot}	total power consumption	V _{CCA} = V _{CCD} = 3 V; V _{CCO} = 2.5 V	–	135	–	mW
		V _{CCA} = V _{CCD} = 2.7 V; V _{CCO} = 2.2 V	–	115	–	mW
		standby mode	–	4.5	–	mW
Digital inputs						
PINS SHP, SHD AND CLK (REFERENCED TO DGND)						
V _{IL}	LOW-level input voltage		0	–	0.8	V
V _{IH}	HIGH-level input voltage		2.0	–	5.5	V
I _i	input current	0 ≤ V _i ≤ 5.5 V	–3	–	+3	μA
C _i	input capacitance		–	–	2	pF
PINS CLPDM, CLPOB, SEN, SCLK, SDATA STBY, $\overline{\text{OE}}$, BLK AND VSYNC						
V _{IL}	LOW-level input voltage		0	–	0.8	V
V _{IH}	HIGH-level input voltage		2.0	–	5.5	V
I _i	input current	0 ≤ V _i ≤ 5.5 V	–2	–	+2	μA
Clamps						
GLOBAL CHARACTERISTICS OF THE CLAMP LOOPS						
t _{W(clamp)}	clamp active pulse width in number of pixels	PGA code = 383 for maximum 6 LSB error for a CPCDS capacitance of 1 μF; clamp code = 32	15	–	–	pixels
INPUT CLAMP (DRIVEN BY CLPDM)						
g _{m(CDS)}	CDS input clamp transconductance		–	15	–	mS

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling (CDS)						
$V_{i(CDS)(p-p)}$	maximum CDS input voltage (peak-to-peak value)	$V_{CC} = 2.85\text{ V}$	650	–	–	mV
		$V_{CC} \geq 3.0\text{ V}$	800	–	–	mV
$V_{reset(max)}$	maximum CDS input reset pulse		–	–	1.5	V
$I_{i(IN)}$	input current into pin IN	at floating gate level	–	–	3	μA
C_i	input capacitance		–	2	–	pF
$t_{CDS(min)}$	CDS control pulses minimum active time	$V_{i(CDS)(p-p)} = 800\text{ mV}$; black-to-white transition in 1 pixel with 98.5% V_i recovery	11	–	–	ns
$t_{h(IN;SHP)}$	CDS input hold time (pin IN) compared to control pulse SHP	Figs 3 and 4	3	–	–	ns
$t_{h(IN;SHD)}$	CDS input hold time (pin IN) compared to control pulse SHD	Figs 3 and 4	3	–	–	ns
Programmable Gain Amplifier (PGA)						
DR_{PGA}	PGA dynamic range		–	36	–	dB
ΔG_{PGA}	PGA gain step		0.08	0.10	0.12	dB
ADC						
DNL	differential non linearity	ramp input	–	± 0.5	± 0.9	LSB
ADC_{res}	ADC resolution		–	10	–	bits
Total chain characteristics (CDS + PGA + ADC)						
$f_{pix(max)}$	maximum pixel rate		25	–	–	MHz
$f_{pix(min)}$	minimum pixel rate	$O_{CCD(max)} = \pm 100\text{ mV}$	–	–	1	MHz
		$O_{CCD(max)} = \pm 200\text{ mV}$	–	–	2	MHz
$O_{CCD(max)}$	maximum offset voltage between CCD floating level and CCD dark pixel level		–200	–	+200	mV
t_{CLKH}	CLK pulse width HIGH		15	–	–	ns
t_{CLKL}	CLK pulse width LOW		15	–	–	ns
$t_{d(SHD;CLK)}$	time delay between SHD and CLK	Figs 3 and 4	–	10	–	ns
$t_{su(BLK;SHD)}$	set-up time of BLK compared to SHD	Figs 3 and 4	5	–	–	ns
$V_{i(IN)}$	video input voltage for ADC full-scale output	PGA code = 00	–	800	–	mV
		PGA code = 383	–	12.7	–	mV

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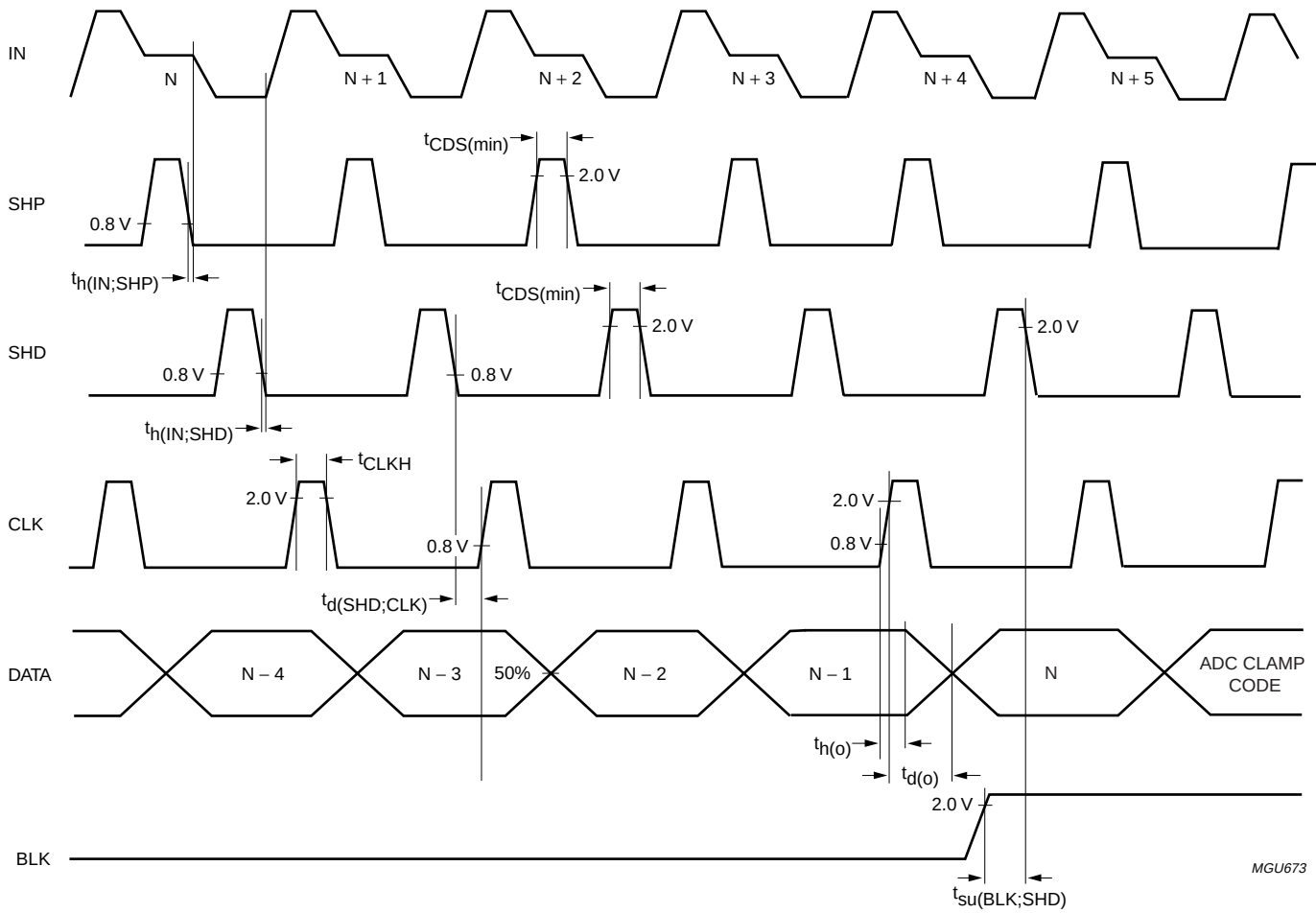
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$N_{\text{tot(rms)}}$	total noise from CDS input to ADC output (RMS value)	Fig.8; note 1 PGA code = 00 PGA code = 96	– –	0.4 0.6	– –	LSB LSB
$E_{\text{in(rms)}}$	equivalent input noise voltage (RMS value)	PGA code = 383 PGA code = 96	– –	145 170	– –	μV μV
Digital-to-Analog Converter (OFD DAC)						
$V_{\text{OFDOUT(p-p)}}$	output voltage (peak-to-peak value)	$R_L = 1 \text{ M}\Omega$	–	1.0	–	V
$V_{\text{OFDOUT(0)}}$	DC output voltage for code 0	Fig.5	–	V_{AGND}	–	V
$V_{\text{OFDOUT(255)}}$	DC output voltage for code 255	Fig.5	–	$V_{\text{AGND}} + 1.0$	–	V
T_{CDAC}	DAC output temperature coefficient		–	250	–	ppm/K
Z_{OFDOUT}	DAC output impedance		–	2000	–	Ω
I_{OFDOUT}	DAC output current drive	static	–	–	100	μA
Digital outputs $f_{\text{pix}} = 25 \text{ MHz}$; $C_L = 10 \text{ pF}$; see Figs 3 and 4						
V_{OH}	HIGH-level output voltage	$I_{\text{OH}} = -1 \text{ mA}$	$V_{\text{CCO}} - 0.5$	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	$I_{\text{OL}} = 1 \text{ mA}$	0	–	0.5	V
I_{OZ}	output current in 3-state mode	$0.5 \text{ V} < V_o < V_{\text{CCO}}$	–20	–	+20	μA
$t_{\text{h(o)}}$	output hold time		5	–	–	ns
$t_{\text{d(o)}}$	output delay time	$V_{\text{CCO}} = 3.6 \text{ V}$; $V_{\text{CCD}} = 3.6 \text{ V}$	–	10	13	ns
		$V_{\text{CCO}} = 2.5 \text{ V}$; $V_{\text{CCD}} = 3.0 \text{ V}$	–	12	15	ns
		$V_{\text{CCO}} = 2.2 \text{ V}$; $V_{\text{CCD}} = 2.7 \text{ V}$	–	13	16	ns
C_L	output load capacitance		–	–	20	pF
Serial interface						
$f_{\text{SCLK(max)}}$	maximum clock frequency of serial interface		10	–	–	MHz

Note

- Noise figure includes the internal input buffer circuit.

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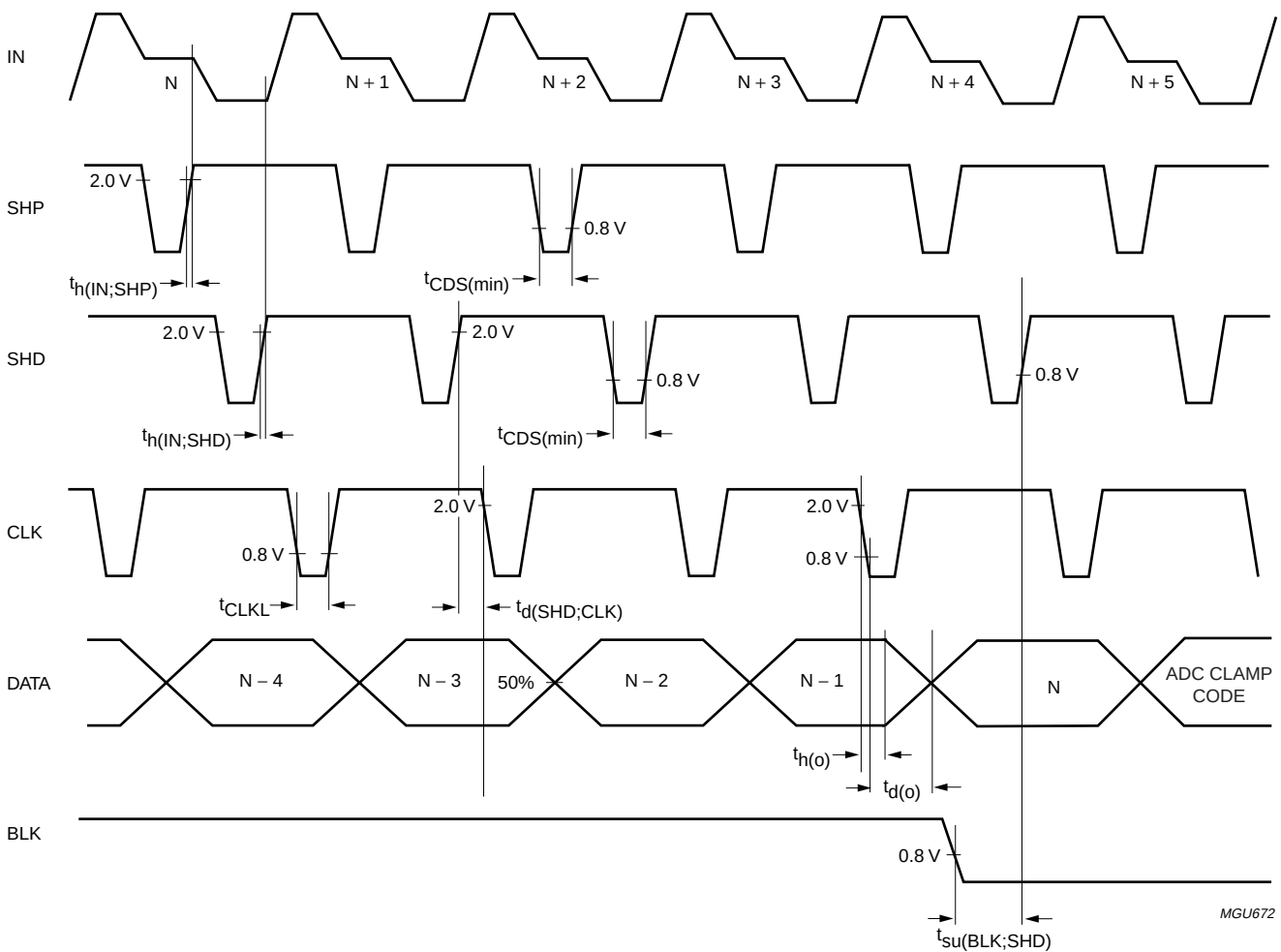
SHP and SHD should be aligned at optimum with the CCD signal. Samples are taken at falling edge.
Recommended placement for CLK rising edge is between the falling edge of SHD and the rising edge of SHP.

Fig.3 Pixel frequency timing diagram; all polarities active HIGH.

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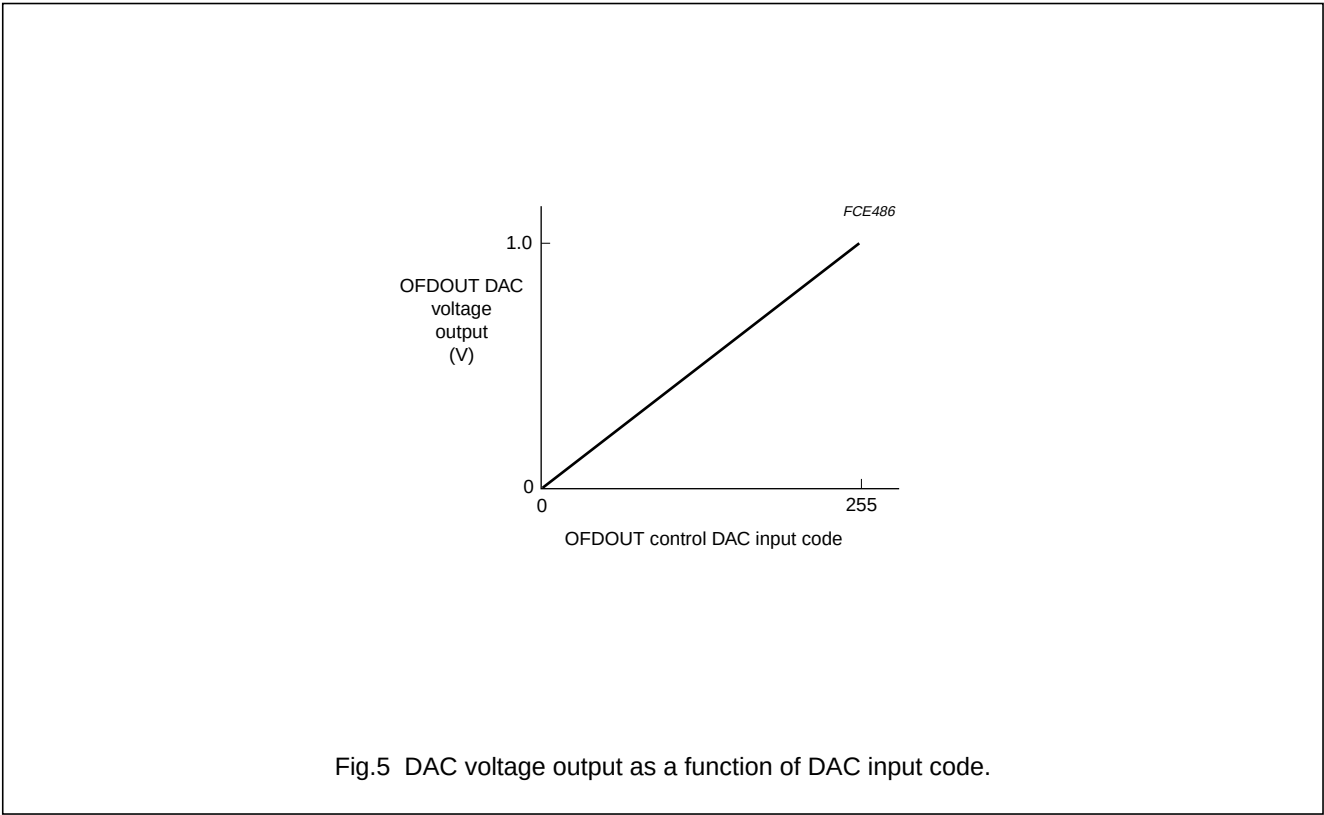
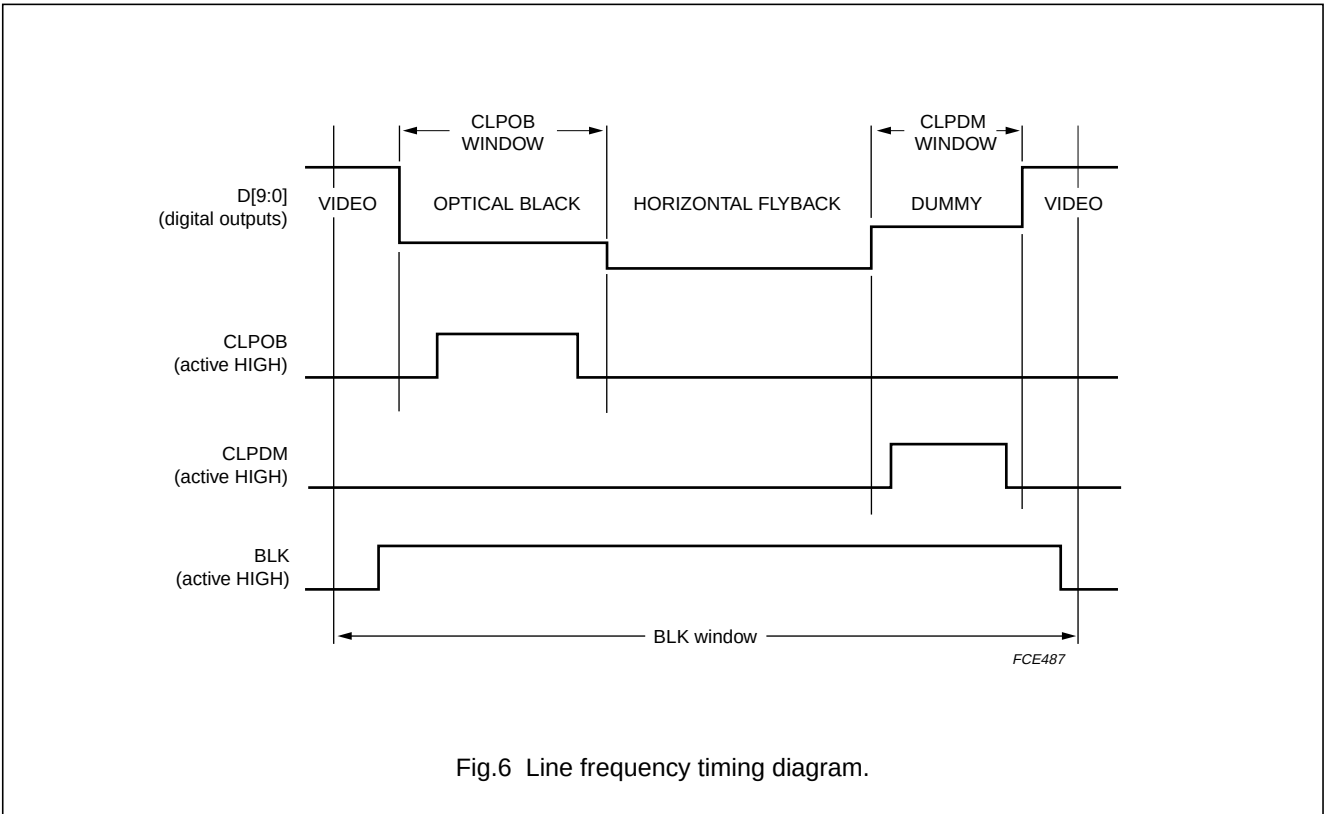


SHP and SHD should be aligned at optimum with the CCD signal. Samples are taken at rising edge.
 Recommended placement for CLK falling edge is between the rising edge of SHD and the falling edge of SHP.

Fig.4 Pixel frequency timing diagram; all polarities active LOW.

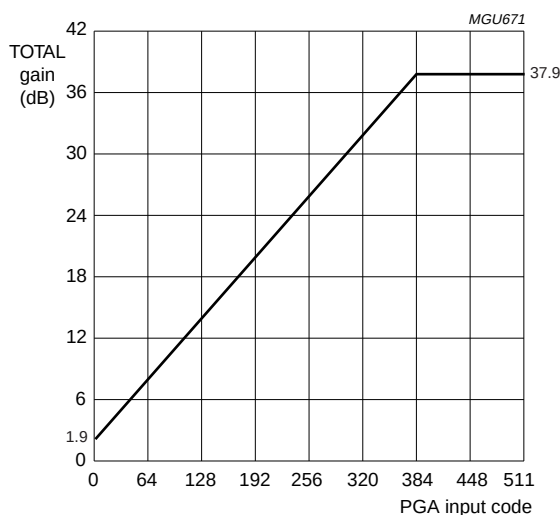
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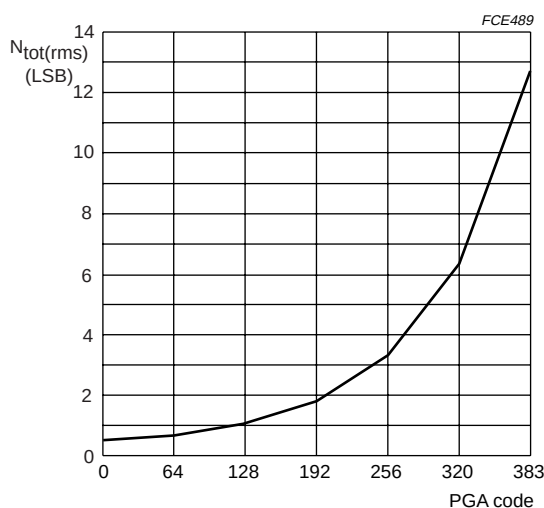
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$$\text{Gain(dB)} = 1.9 + 36 \times \left(\frac{\text{PGAcode}}{383} \right) [\text{dB}]$$

Full-scale at the ADC input is reached at $V_{(CDS)(p-p)} = 800 \text{ mV}$; PGA code 0.

Fig.7 Total gain from CDS input to ADC input as a function of PGA control code.



Noise measurement at ADC outputs:

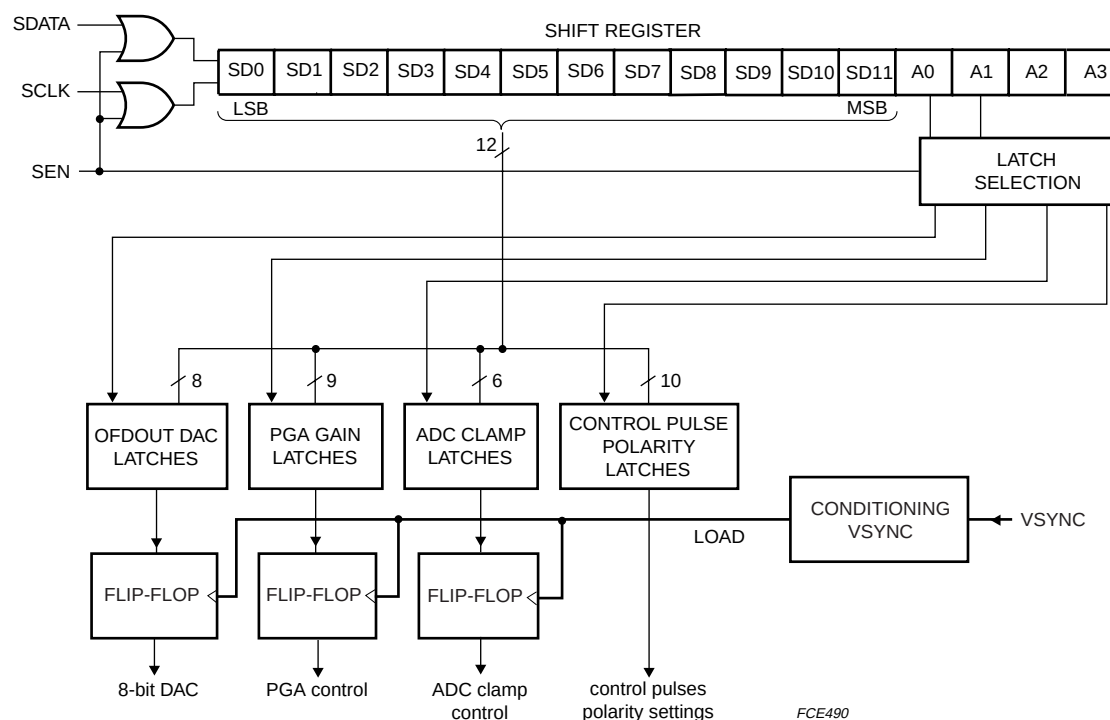
Coupling capacitor at input is grounded, so only noise contribution of the front-end is evaluated. Front-end works at 25 Mpixels with line of 1024 pixels whose first 40 are used to run CLPOB and the last 40 for CLPDM. Data at the ADC outputs are measured during the other pixels. As a result of this, the standard deviation of the codes statistic is computed, resulting in the noise. No quantization noise is taken into account because there is no input.

Fig.8 Typical total noise performance as a function of PGA gain.

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SERIAL INTERFACE

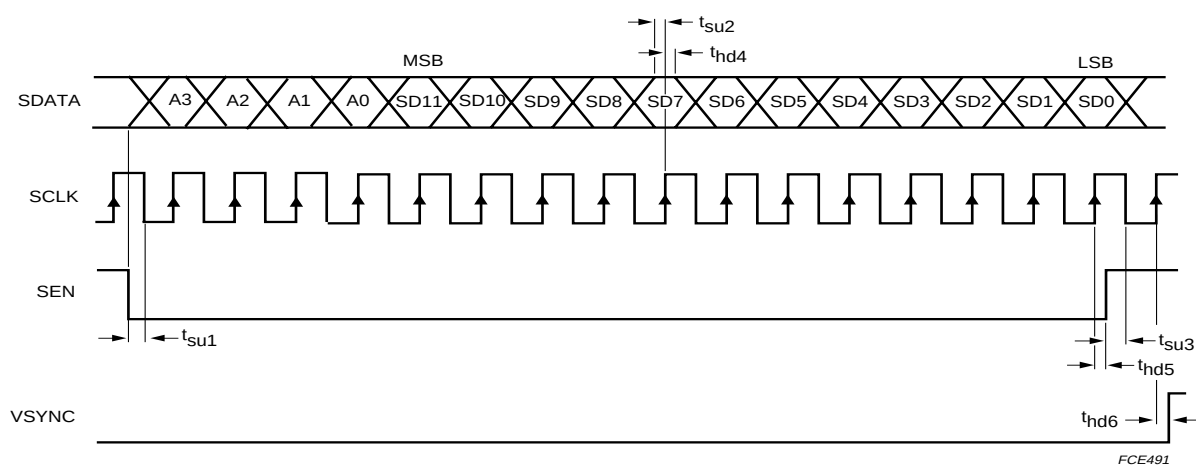


First logical layer (DFF) is clocked by first falling SCLK edge after rising SEN edge.
 Second logical layer is clocked by LOAD signal; this signal depends on VSYNC signal.
 If vertical sync signal is not available, VSYNC should be connected to SEN.

Fig.9 Serial interface block diagram.

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$t_{SU1} = t_{SU2} = t_{SU3} = 10 \text{ ns (minimum)}$; $t_{HD4} = t_{HD5} = t_{HD6} = 10 \text{ ns (minimum)}$.

Fig.10 Loading sequence of control input data via the serial interface.

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Table 1 Serial interface programming

ADDRESS BITS				DATA BITS SD11 TO SD0
A3	A2	A1	A0	
0	0	0	0	PGA gain control (SD8 to SD0)
0	0	0	1	DAC OFDOUT output control (SD7 to SD0)
0	0	1	0	ADC clamp reference control (SD5 to SD0); from code 0 to 63
0	0	1	1	control pulses (pins SHP, SHD, CLPDM, CLPOB, BLK and CLK) polarity settings; SD2, SD6, SD7 and SD9 should be set to logic 1; for SD6 and SD7 see Tables 3 and 4
other addresses				test modes (not to be used in normal applications)

Table 2 Polarity settings

PIN	DATA BIT	ACTIVE EDGE OR LEVEL
SHP and SHD	SD4	1 = HIGH; 0 = LOW
CLK	SD5	1 = rising; 0 = falling
CLPDM	SD0	1 = HIGH; 0 = LOW
CLPOB	SD1	1 = HIGH; 0 = LOW
BLK	SD3	1 = HIGH; 0 = LOW
VSYNC	SD8	0 = rising; 1 = falling

Table 3 Standby control using pin STDBY or serial interface

DATA BIT SD7	PIN STDBY	I _{CCA} + I _{CCD} (typical)
1	HIGH	1.5 mA
	LOW	45 mA
0	HIGH	45 mA
	LOW	1.5 mA

Table 4 Output enable selection using output enable pin OE or serial interface)

DATA BIT SD6	PIN OE	ADC DIGITAL OUTPUTS D9 TO D0
1	LOW	active binary
	HIGH	high-impedance
0	LOW	high-impedance
	HIGH	active binary

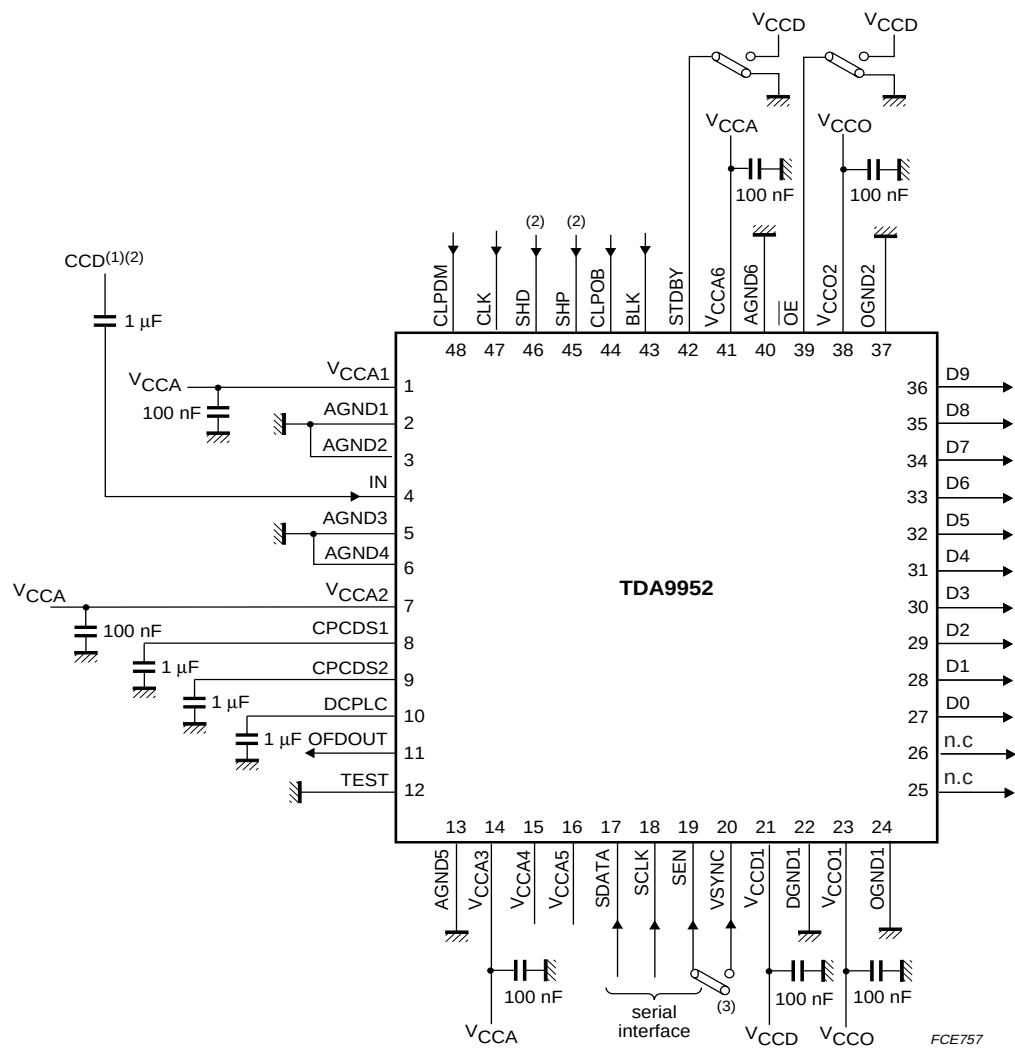
When power supplies increase from zero, an init-on-power block initializes the circuit as follows:

- PGA gain code is set to 000
- Clamp code is set to 00
- All polarity settings are set to logic 1
- Input OFD is set to logic 0.

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APPLICATION INFORMATION

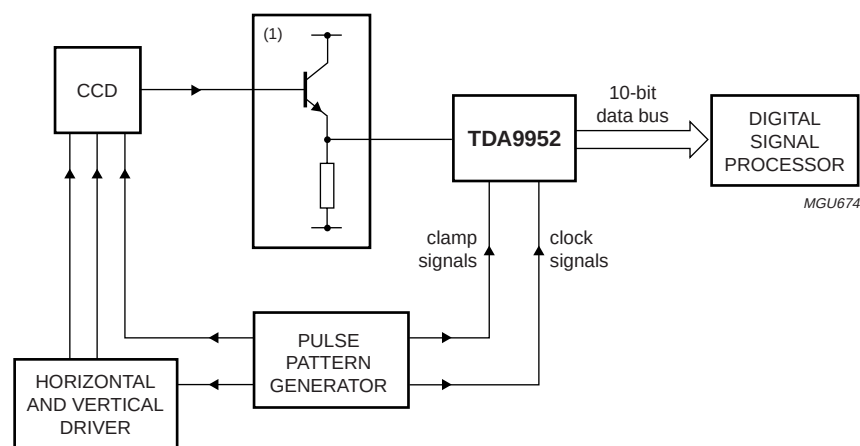


- (1) As an internal input buffer is incorporated, depending on the CCD output impedance, an external input buffer may not be necessary and consequently power savings can be made.
- (2) Input signals IN, SHD and SHP must be adjusted to comply with timing signals $t_{h(IN; SHP)}$ and $t_{h(IN; SHD)}$ (see Chapter "Characteristics").
- (3) Pins SEN and VSYNC should be connected together when the vertical sync signal is not available.

Fig.11 Application diagram.

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(1) The external input buffer can be omitted for CCDs with low output impedance; for CCDs with high output impedance, a small current (around 1 mA) is needed.

Fig.12 Typical imaging application.

Power and grounding recommendations

Care should be taken to minimize the noise when designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.

The connections between the CCD interface and the CDS input should be as short as possible and a ground ring protection around these connections can be beneficial.

Separate analog and digital supplies provide the best performance. If it is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins. The decoupling capacitors must be placed as close as possible to the IC package.

In a two-ground system, in order to minimize the noise through the package and die parasitics, the following recommendation must be implemented:

- The ground pin associated with the digital outputs must be connected to the digital ground plane and special care should be taken to avoid feedthrough in the analog ground plane. The analog and digital ground planes must be connected together with an inductor as closely as possible to the IC in order for them to have the same DC voltage.
- The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as a return path for digital signals.

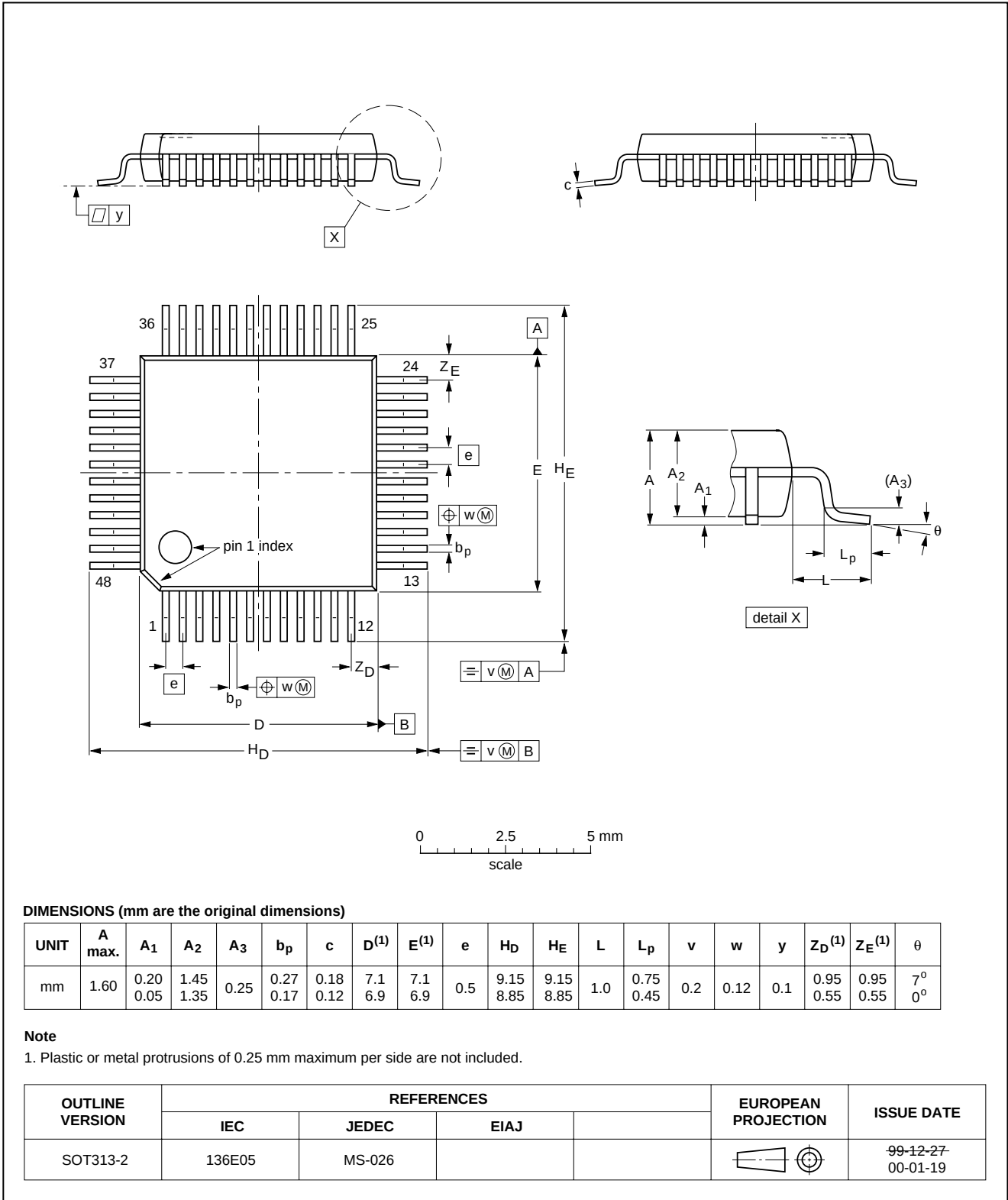
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PACKAGE OUTLINES

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

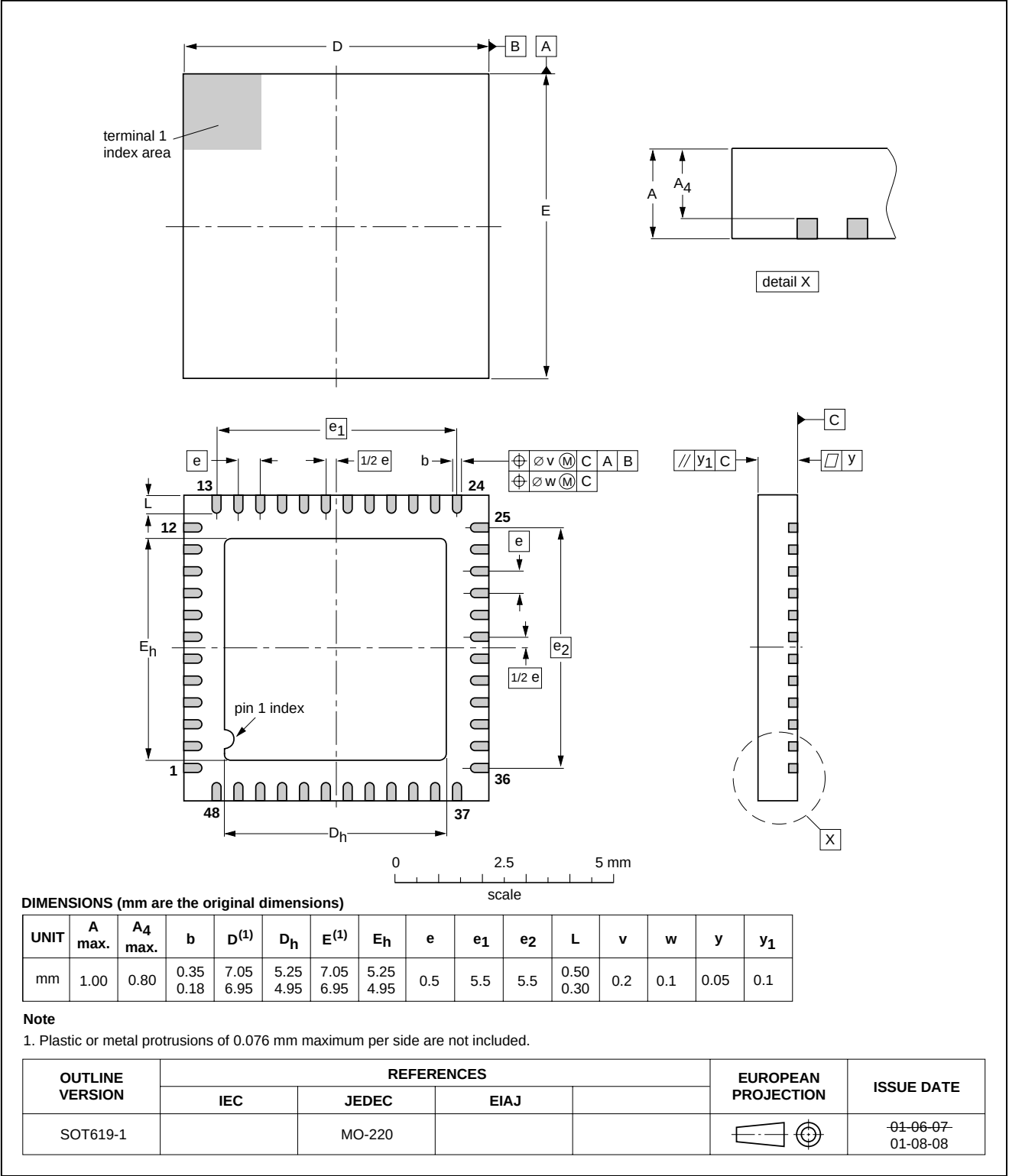


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HVQFN48: plastic, heatsink very thin quad flat package; no leads;
48 terminals; body 7 x 7 x 0.85 mm

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable

Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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