200MHz 通用时钟缓冲器、符合外设组件互连扩展 (PCI-X) 标准

查询样品: CDCV304-EP

特性

- 通用且 **PCI-X 1:4** 时钟缓冲器
- 运行频率
  - **0 MHz** 至 **200 MHz** 通用
- 低输出偏斜： **<100 ps**
- 分配一个时钟输入至一组四个输出
- 当输出使能引脚 **(OE)** 为低电平时，驱动输出的输出使能控制为低电平
- 由 **3.3-V** 或者 **2.5-V** 单电源供电运行
- 符合 **PCI-X** 标准
- **8**-引脚薄型小尺寸 **(TSSOP)** 封装

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装/测试场所
- 一个制造场所
- 可在 **–40°C/105°C** 的温度范围内工作(1)
- 产品生命周期有所延长
- 拓展的产品变更通知
- 产品可追溯性

TSSOP
PW PACKAGE
(TOP VIEW)



(1) 可定制工作温度范围

说明

CDCV304 是一款高性能、低偏斜、通用 PCI-X 兼容型时钟缓冲器。 它分配一个输入时钟信号 (CLKIN) 至输出时钟 (1Y[0:3])。 它专为与 PCI-X 应用一起使用而设计。 CDCV304 运行在 3.3 V 和 2.5 V 电源电压上，因此此器件与 3.3-V PCI-X 规范兼容。

CDCV304 额定运行温度介于 –40°C 至 105°C 之间。

功能框图

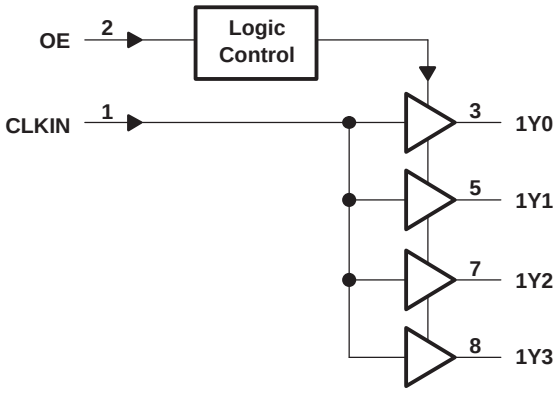


表 1. 功能表

输入		输出
CLKIN	**OE**	**1Y[0:3]**
L	L	L
H	L	L
L	H	L
H	H	H

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 2. ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 105°C	TSSOP - PW	CDCV304TPWREP	C304T	V62/12618-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1Y[0:3]	3, 5, 7, 8	O	Buffered output clocks
CLKIN	1	I	Input reference frequency
GND	4	Power	Ground
OE	2	I	Output enable control
V_{DD}	6	Power	Supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	UNIT
Supply voltage range, V_{DD}	–0.5 V to 4.3 V
Input voltage range, V_I (2) (3)	–0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (2) (3)	–0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I> V_{DD})	±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD})	±50 mA
Storage temperature range T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.

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THERMAL INFORMATION

THERMAL METRIC[1]		CDCV304 PW 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	175.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	61.8	
θ_{JB}	Junction-to-board thermal resistance[4]	104.3	
ψ_{JT}	Junction-to-top characterization parameter[5]	7.7	
ψ_{JB}	Junction-to-board characterization parameter[6]	102.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3		3.6	V
Low-level input voltage, V_{IL}				0.3 x V_{DD}	V
High-level input voltage, V_{IH}		0.7 x V_{DD}			V
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 2.5 V			–12	mA
	V_{DD} = 3.3 V			–24	
Low-level output current, I_{OL}	V_{DD} = 2.5 V			12	mA
	V_{DD} = 3.3 V			24	
Operating free-air temperature, T_A		–40		105	°C

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Clock frequency		0		200	MHz

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –1 mA	V_{DD} – 0.3			V
		V_{DD} = 2.3 V,	I_{OH} = –8 mA	1.78			
		V_{DD} = 3 V,	I_{OH} = –24 mA	1.90			
		V_{DD} = 3 V,	I_{OH} = –12 mA	2.30			
V_{OL}	Low-level output voltage	V_{DD} = 2.3 V,	I_{OL} = 8 mA			0.51	V
		V_{DD} = min to max,	I_{OL} = 1 mA			0.20	
		V_{DD} = 3 V,	I_{OL} = 24 mA			0.84	
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.60	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–45			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–55		
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 2 V	54			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		70		
I_I	Input current	V_I = V_O or V_{DD}				±5	µA
I_{DD}	Dynamic current, see	f = 67 MHz,	V_{DD} = 2.7 V			28	mA
		f = 67 MHz,	V_{DD} = 3.6 V			37	
C_I	Input capacitance	V_{DD} = 3.3 V,	V_I = 0 V or V_{DD}		3		pF
C_O	Output capacitance	V_{DD} = 3.3 V,	V_I = 0 V or V_{DD}		3.2		pF

(1) All typical values are with respect to nominal V_{DD} and T_A = 25°C.

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SWITCHING CHARACTERISTICS

V_{DD} = 2.5 V ± 10%, C_L= 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Low-to-high propagation delay	See Figure 1 and Figure 2	2	2.9	4.5	ns
t_{PHL}	High-to-low propagation delay		2	3	4.5	
$t_{sk(o)}$	Output skew(2)	See Figure 3		50	150	ps
t_r	Output rise slew rate(3)		1	2.2	4	V/ns
t_f	Output fall slew rate(3)		1	2.2	4	V/ns

(1) All typical values are with respect to nominal V_{DD}.
(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs and T_A = -40°C to 85°C.
(3) This symbol is according to PCI-X terminology.

SWITCHING CHARACTERISTICS

V_{DD} = 3.3 V ± 10%, C_L= 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Low-to-high propagation delay	See Figure 1 and Figure 2	1.8	2.4	3.8	ns
t_{PHL}	High-to-low propagation delay		1.8	2.5	3.8	
$t_{sk(o)}$	Output skew(2)			50	100	ps
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f_{out} = 30.72 MHz		63		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		56		
$t_{sk(p)}$	Pulse skew	$V_{IH} = V_{DD}$, V_{IL} = 0 V		180		ps
$t_{sk(pr)}$	Process skew			0.2		ns
$t_{sk(pp)}$	Part-to-part skew			0.25		ns
t_{high}	Clock high time, see Figure 4	66 MHz	6			ns
		140 MHz	2.2			
t_{low}	Clock low time, see Figure 4	66 MHz	6			ns
		140 MHz	3			
t_r	Output rise slew rate(3)		1	2.7	4	V/ns
t_f	Output fall slew rate(3)		1	2.7	4	V/ns

(1) All typical values are with respect to nominal V_{DD}.
(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs and and T_A = -40°C to 85°C.
(3) This symbol is according to PCI-X terminology.

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PARAMETER MEASUREMENT INFORMATION

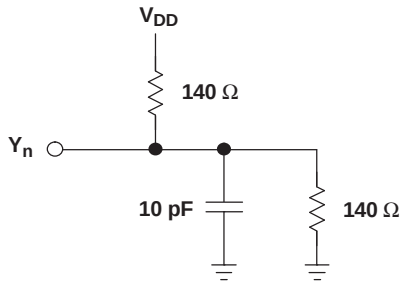


Figure 1. Test Load Circuit

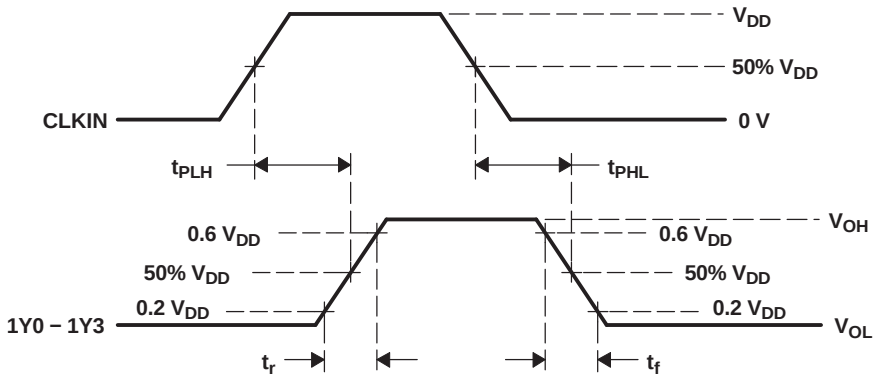


Figure 2. Voltage Waveforms Propagation Delay (t_{pd}) Measurements

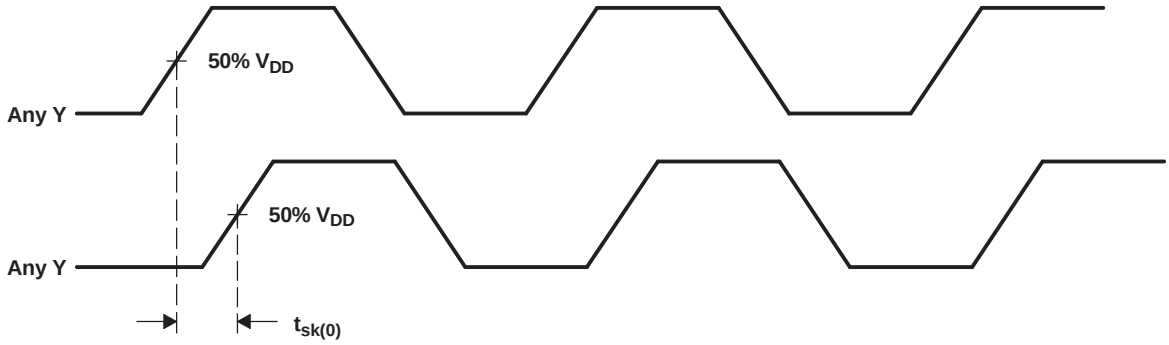
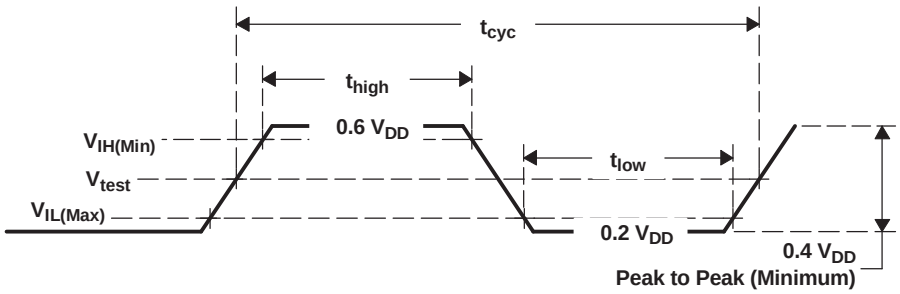


Figure 3. Output Skew

PARAMETER	VALUE	UNIT
$V_{IH(Min)}$	0.5 V_{DD}	V
$V_{IL(Max)}$	0.35 V_{DD}	V
V_{test}	0.4 V_{DD}	V



A. All parameters in Figure 4 are according to PCI-X 1.0 specifications.

Figure 4. Clock Waveform

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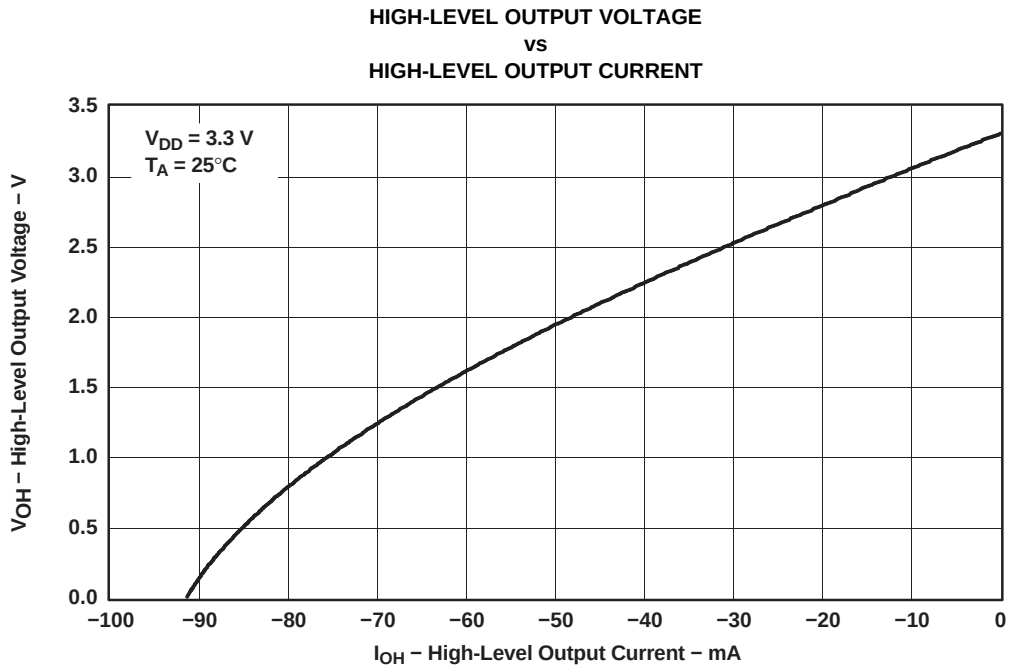


Figure 5.

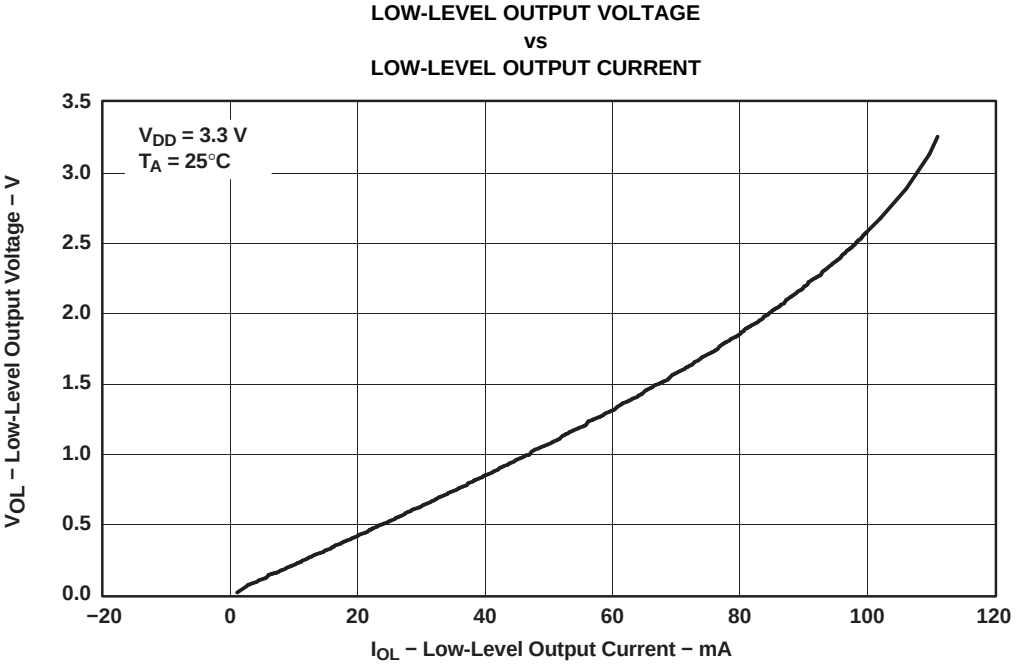


Figure 6.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCV304TPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	C304T	Samples
V62/12618-01XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	C304T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

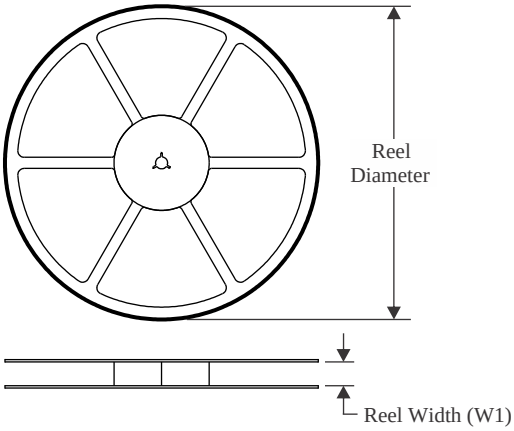
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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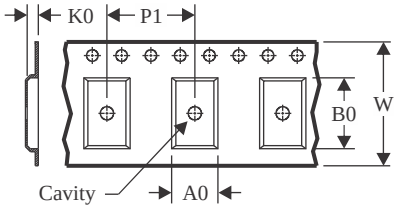
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

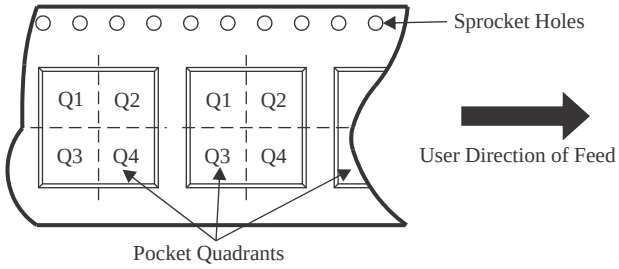


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

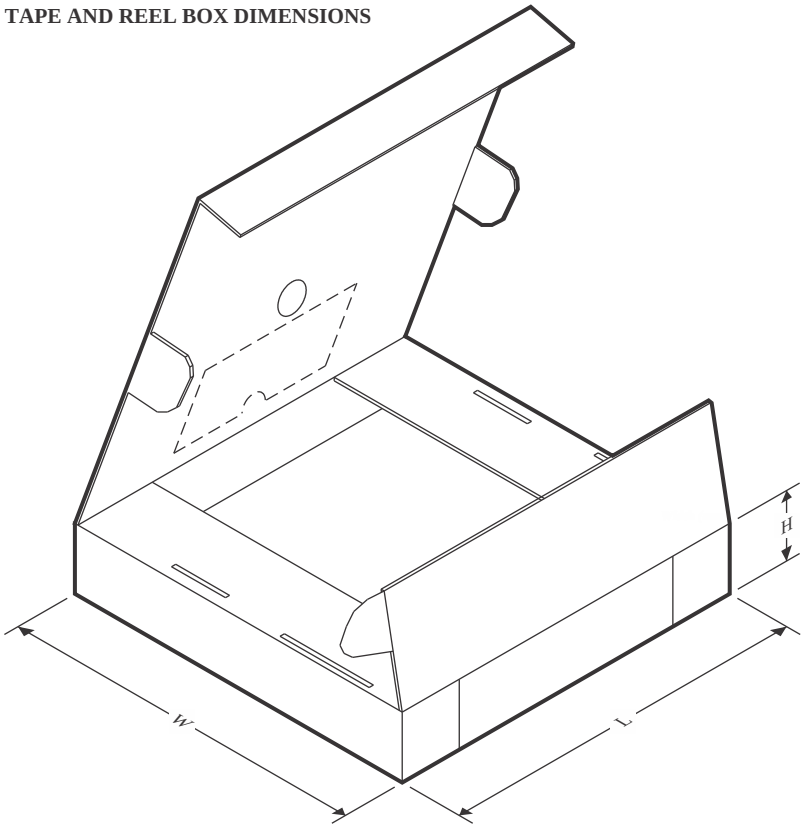
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCV304TPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

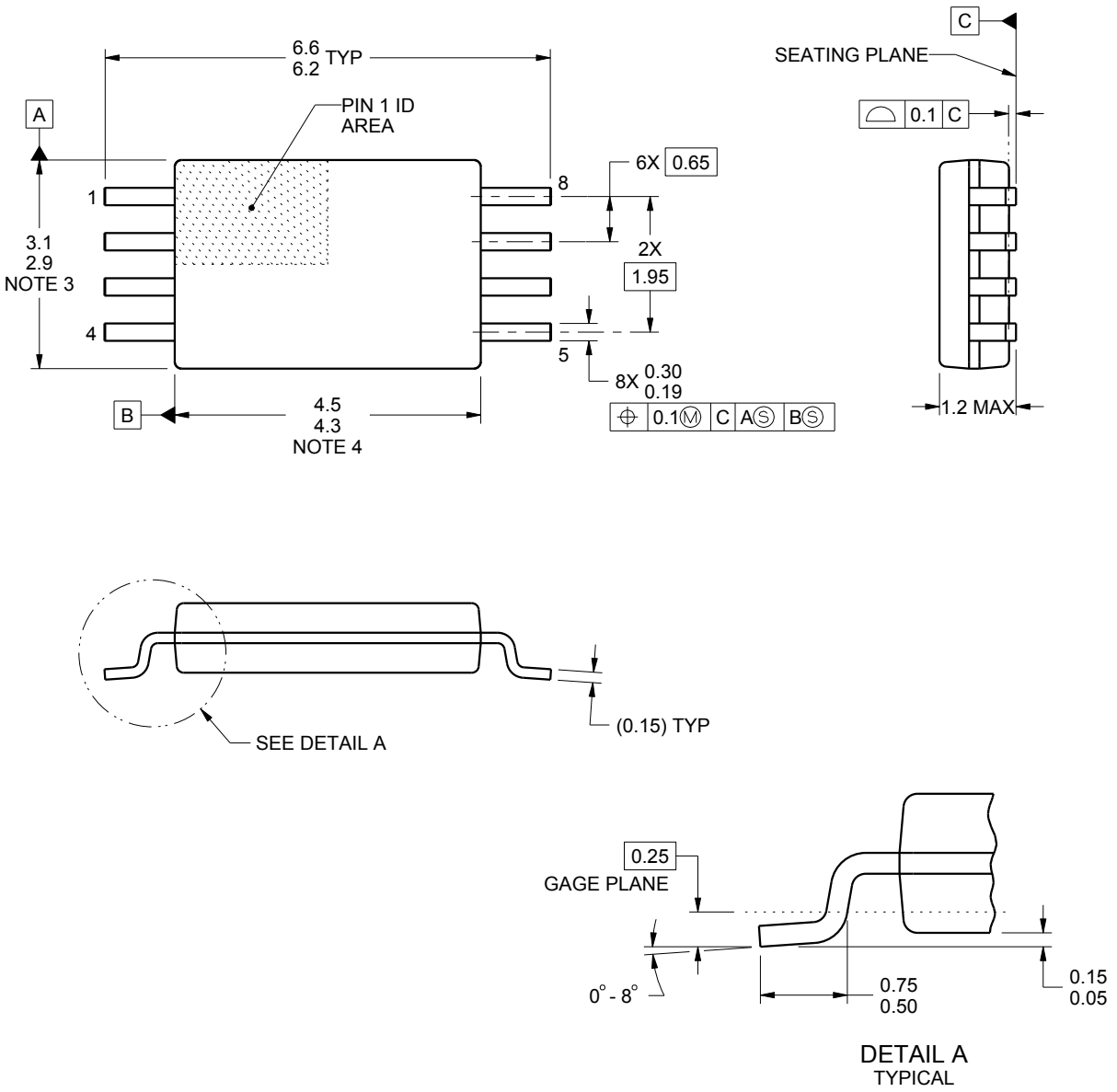
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCV304TPWREP	TSSOP	PW	8	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0008A

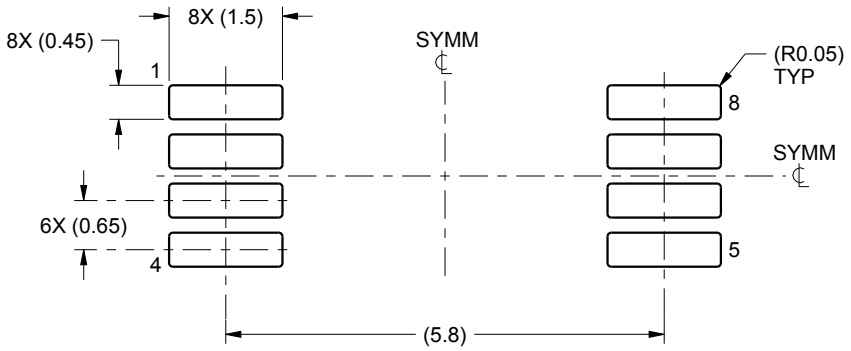
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

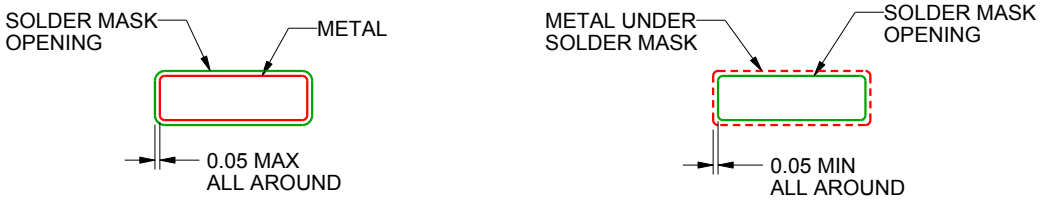


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

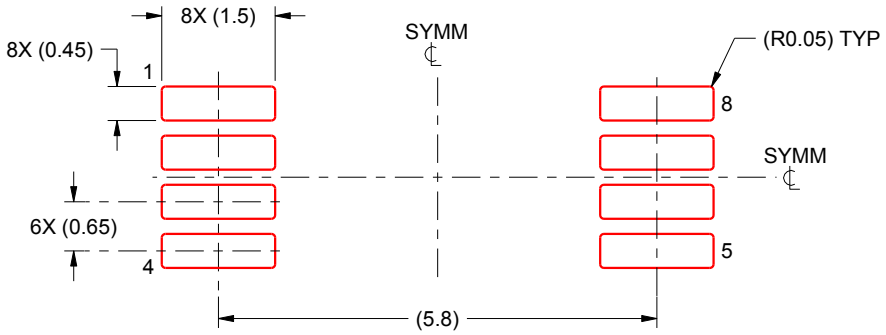


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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