MX878

8-Channel, 60V Relay/Load Driver
Open Drain Output, 3 Wire Interface

Features:

- 8 Outputs Rated at 60V, 200mA
- Open Drain Pull-Down Driver Configuration
- 6V to 60V Driver Supply Range
- 2.7V to 5.5V Logic Supply Range
- 3 Wire Serial Interface plus Chip Select
- Captures Serial & Parallel Input Data
- Outputs can be paralleled
- 28 Lead QFN Package

Applications:

- White Goods
- ATE
- Industrial Equipment
- Automotive Relay Control

General Description

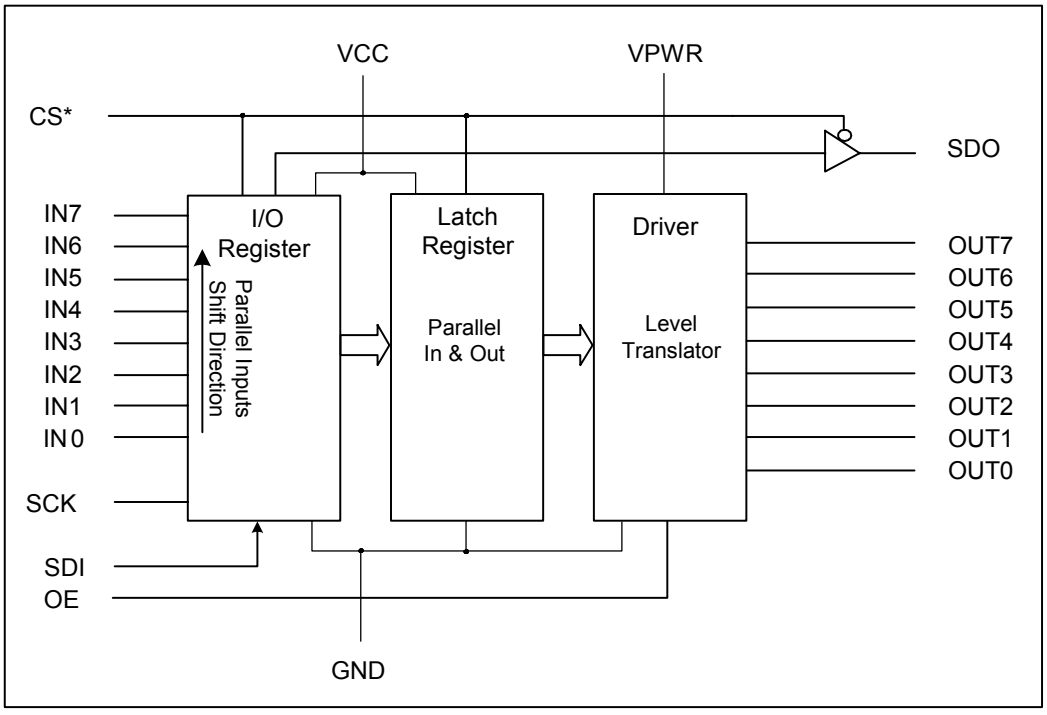
The MX878 is an 8 channel high voltage switch with 8-bit parallel or serial input control. The MX878 connects directly to a microprocessor through a standard 3 wire serial interface. The open drain pull-down output configuration can drive up to 60 volts at 200mA. Outputs can be paralleled for increased drive current up to a device total of 1000mA sink.

The MX878 is designed to operate over a temperature range of -40°C to +85°C, and is available in a QFN-28 Package.

Ordering Information

Part No.	Description	Qty
087800-00	QFN-28	73
087841-00	QFN-28 Tape & Reel	2500

Functional Block Diagram



Absolute Maximum Ratings (Voltages with respect to GND=0V)

Parameter	Symbol	Min	Max	Unit
VPWR Supply Voltage	VPWR		62	V
Logic Supply Voltage	VCC		6	V
Input Pin Voltage	V_{IN}		6	V
Continuous Output Current	I_{OUT}(O_{UT}0-7)		250	mA
Storage Temperature	T_{STG}	-55	150	C^o
Operating Ambient Temp	T_A	-40	85	C^o
Operating Junction Temp	T_J		150	C^o
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	110 Typical		C^o/W

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

ESD Warning

ESD (electrostatic discharge) sensitive device. Although the MX878 features proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DC Electrical Characteristics

VCC=5.0V, VPWR=42V, T_A=25°C, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Logic Supply Voltage		2.7		5.5	V
Logic Supply Current	fSCK = 5 MHz		50		µA
Quiescent Logic Supply Current	fSCK = 0			1	µA
VPWR Voltage		6		60	V
GND Current	Total of all outputs			1000	mA
Quiescent VPWR Current	VPWR = 42V, No load		0.75		mA
High Level Input Voltage	IN0-7, SCK, SDI, OE, CS*	VCC-0.5			V
Low Level Input Voltage				0.5	V
Input Leakage Current				1	µA
SDO Tri-State Leakage Current	CS* = Logic High			1	µA
Out0-7 Current	Any one output, sink			200	mA
Out0-7 ON Resistance	VPWR = 42V		4.5		Ω
Out0-7 Tri-State Leakage Current	OE = Logic Low			1	µA

Notes: To avoid unwanted output during VPWR application and system initialization, keep OE at a logic low until CS* has completed one cycle.

Thermal Resistance is measured in still air with the device soldered to a 6 square inch board without a ground plane. Applications may require derating of the specified maximum currents to avoid exceeding the maximum operation junction temperature.

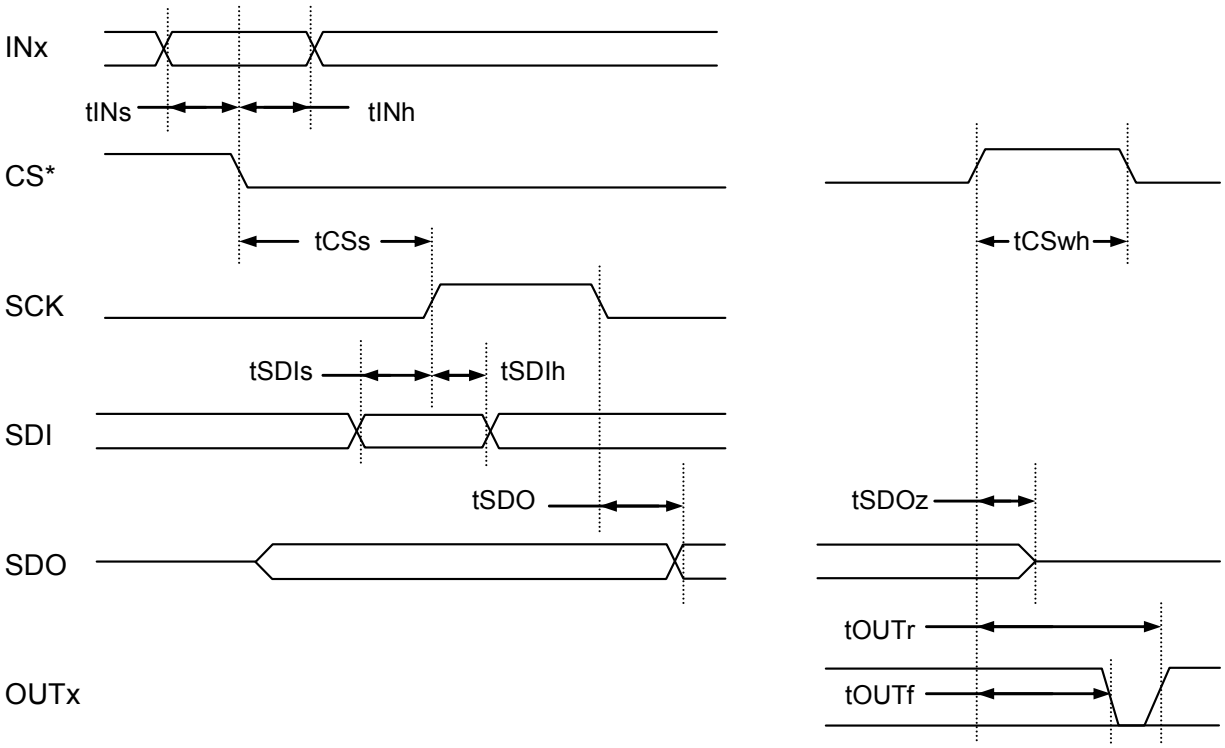
AC Electrical Characteristics

VCC=5.0V, VPWR=42V, TA=25°C, unless otherwise specified.

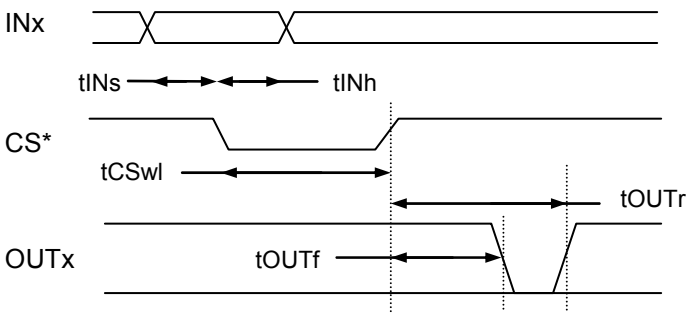
Parameter	Symbol	Condition	Min	Typ	Max	Unit
SCK Period [1]			100		DC	nS
SCK High Time [1]			40			nS
SCK Low Time [1]			40			nS
CS* High Time [1]	tCSwh		50			nS
CS* Falling to SCK Rising [1]	tCSs	Setup Time	150			nS
CS* Low Time [1]	tCSwl	SCK Low, (parallel input mode)	150			nS
INx to CS Falling (SETUP TIME) [1]	tINs		15			nS
INx to CS Falling (HOLD TIME) [1]	tINh		30			
SDI to SCK Rising (SETUP TIME) [1]	tSDIs		20			nS
SDI to SCK Rising (HOLD TIME) [1]	tSDIh		25			
SCK Falling to SDO Data Valid	tSDO			10		nS
CS* Rising to SDO High Z	tSDOz			12		nS
CS* Rising to OUTx Falling	tOUTf	To 50%, C(OUTx) = 1000pF		570		nS
OUTx Fall Time		From 10% to 90%, C(OUTx) = 1000pF		75		nS
OE Rising to OUTx Rising		To 90%		580		nS
OE Rising to OUTx Falling		To 90%		390		nS
OE Falling to OUTx High Z		To 10%, OUTx High		130		nS
		To 10%, OUTx Low		90		nS

Note 1: Guaranteed by design.

Serial Timing



Parallel Timing



Pin Description

Pin No.	Pin Name	Description
4	VPWR	High Voltage Supply (6V to 60V)
2, 5	-	No Connect
6	VCC	Logic Supply (2.7V to 5.5V)
7	SDO	Serial Data Output
8	IN7	Parallel Input
9	IN6	Parallel Input
10	IN5	Parallel Input
11	IN4	Parallel Input
12	IN3	Parallel Input
13	IN2	Parallel Input
14	IN1	Parallel Input
15	IN0	Parallel Input
16	SCK	Serial Clock
18	SDI	Serial Data Input
19	CS*	Chip Select (Active Low)
20	OE	Output Enable
3, 17, 21	GND	Ground
22	OUT0	Parallel Output
23	OUT1	Parallel Output
24	OUT2	Parallel Output
25	OUT3	Parallel Output
26	OUT4	Parallel Output
27	OUT5	Parallel Output
28	OUT6	Parallel Output
1	OUT7	Parallel Output

Functional Description

The MX878 is an 8 channel high voltage driver with 8-bit input control. The MX878 interfaces to a microprocessor through a standard 3 wire serial interface and an active low chip select, or can be used in a parallel-in, parallel-out configuration.

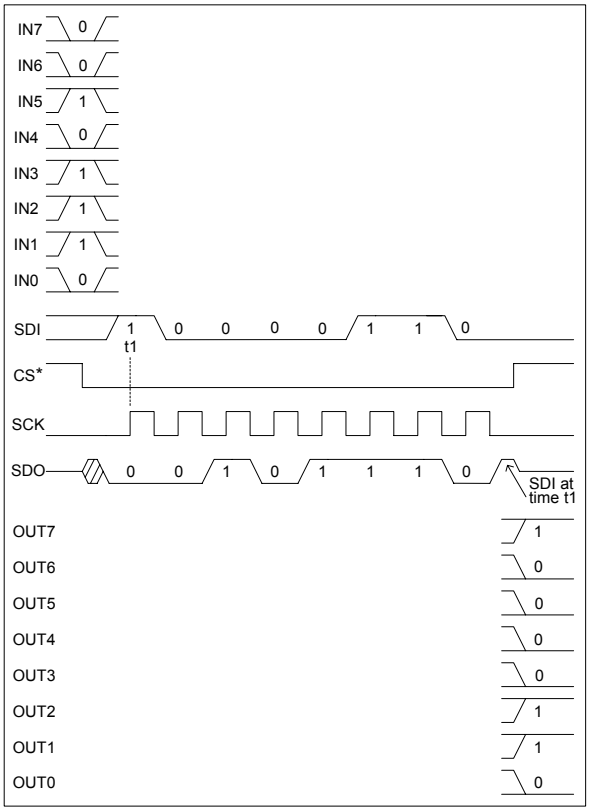
Parallel data is transferred to the I/O register of the MX878 through the parallel input pins, IN0 through IN7 on the falling edge of the chip select pin, CS*. When CS* is in a logic low state, serial data can be transferred to the I/O register through the serial input pin, SDI, and from the I/O register through the serial output pin, SDO. Parallel or serial input data is transferred from the I/O register to the latch and high voltage output drivers, OUT0 through OUT7, on the positive edge of CS*. This data remains latched until the next positive edge of CS*.

The 8-bit I/O shift register is clocked by the serial clock pin, SCK. Serial data presented at the SDI pin is transferred to the shift register on the positive edge of SCK. Data shifts out of the register through the SDO pin on the negative edge of SCK. SDI and SCK are ignored, and SDO transitions to a high impedance condition when CS* is at a logic high state.

Serial data is received by the MX878 through the SDI pin. This data is accepted on the rising edge of SCK. A specific output is programmed to a logic high state if SDI is at a logic high state during the rising edge of SCK. Conversely, a specific output is programmed to a logic low state if SDI is at a logic low state during the rising edge of SCK. Outputs transition to their programmed states on the positive edge of CS* if the output enable pin, OE is in a logic high state.

The MSB input data (IN7) is presented at the serial output pin, SDO on the falling edge of CS*. Input data from IN6 through IN0 is sequentially presented at SDO on negative SCK transitions if CS* remains in a logic low state. If CS* is at a logic low state beyond 8 cycles of SCK, SDI data that has propagated through the I/O register will then be presented at SDO. The SDO pin transitions to a high impedance state when CS* is in a logic level high state, thus allowing multiple serial peripherals to share the microprocessor data pin.

Serial Data Transfer Example

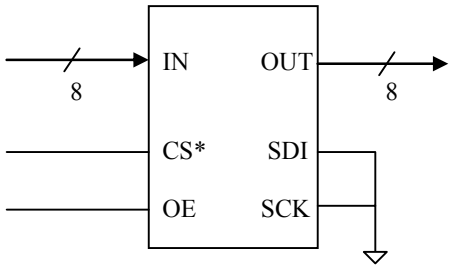


Devices may be serially cascaded by connecting SDO to SDI of the next device. Pins SCK and CS* are common to all devices in serial cascade. For n-cascaded devices the CS* should remain low for 8n cycles of SCK.

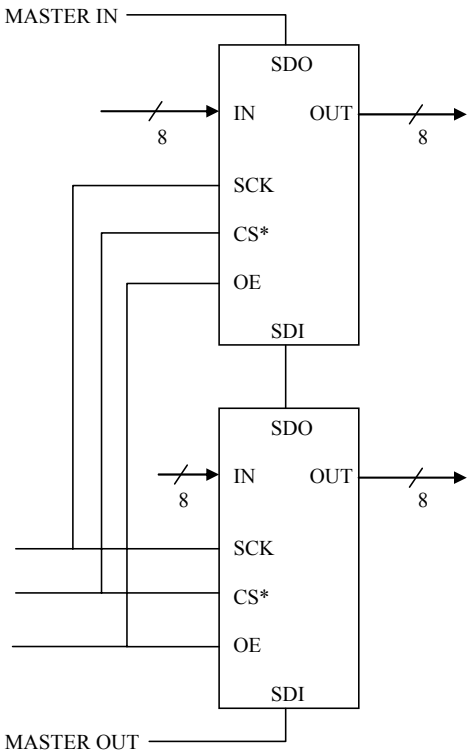
An output enable pin, OE enables the driver outputs OUT0 through OUT7 when logic high. A logic low level on OE forces the OUT0 through OUT7 outputs to a high impedance state.

The MX878 can also operate as a parallel-in, parallel-out level shifter and driver. SCK must remain at a logic low state when operating in this mode. Parallel input data presented to IN0 through IN7 is captured on the falling edge of CS*. This data is transferred to OUT0 through OUT7 on the rising edge of CS*, and remains latched until the next rising edge of CS*.

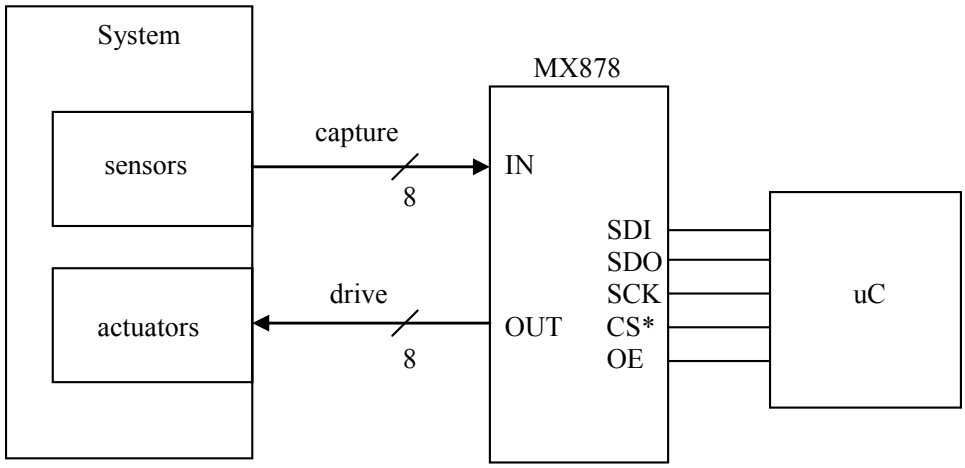
Parallel-in / Parallel-out Application



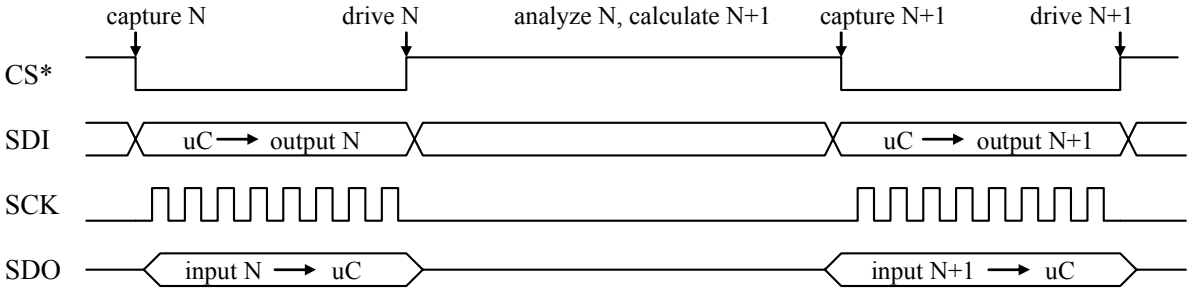
Serial Cascade Application



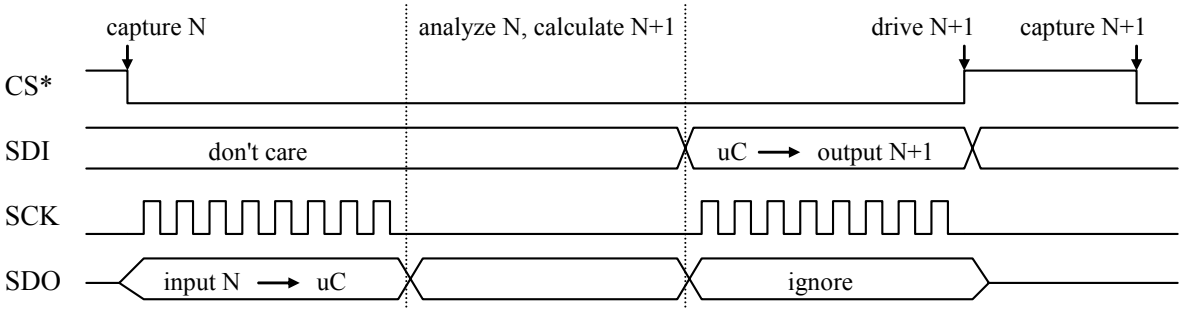
Control System Application



Type 1 timing:

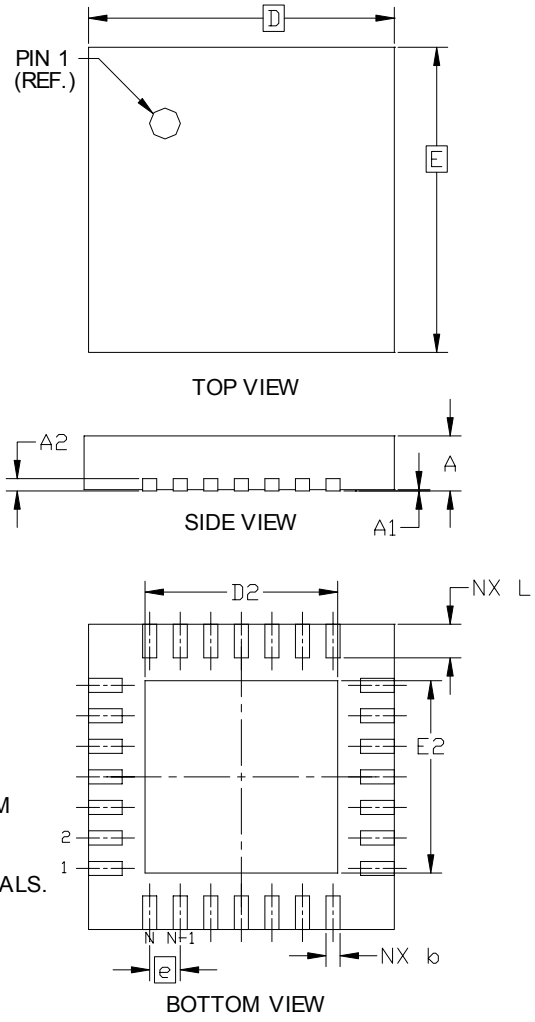


Type 2 timing:



28 LEAD 5MM X 5MM X 0.90MM QFN

DIMENSIONS				
DIM.	INCH		MM.	
	MIN.	MAX.	MIN.	MAX.
A	.031	.039	.80	1.0
A1	0	.002	0	.05
A2	.008 REF.		,200 REF.	
b	.007	.012	.18	.30
D	.197 BSC		5.00 BSC	
D2	.118	.128	3.00	3.25
E	.197 BSC		5.00 BSC	
E2	.118	.128	3.00	3.25
e	.0197 BSC		.500 BSC	
L	.0177	.0256	.45	.65
N	28		28	



3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MO-220 VARIATION VHHD-1.
2. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
1. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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