16-Channel, 1 MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP

Data Sheet **AD7490**

FEATURES

Fast throughput rate: 1 MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low power at maximum throughput rates
5.4 mW maximum at 870 kSPS with 3 V supplies
12.5 mW maximum at 1 MSPS with 5 V supplies
16 (single-ended) inputs with sequencer
Wide input bandwidth
69.5 dB SNR at 50 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface, SPI/QSPI™/MICROWIRE™/ DSP compatible
Full shutdown mode: 0.5 µA maximum
28-lead TSSOP and 32-lead LFCSP packages

FUNCTIONAL BLOCK DIAGRAM

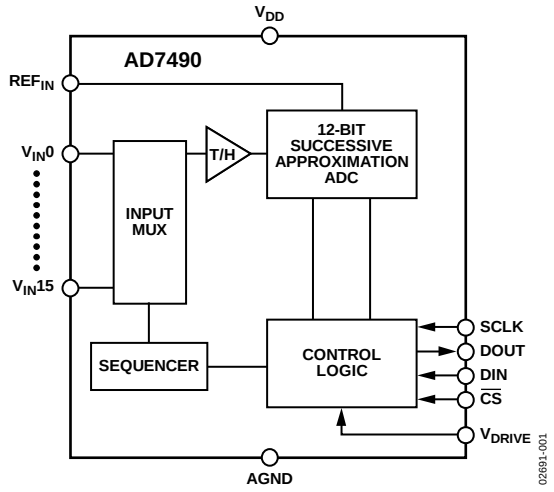


Figure 1.

GENERAL DESCRIPTION

The AD7490 is a 12-bit high speed, low power, 16-channel, successive approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 1 MSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7490 uses advanced design techniques to achieve very low power dissipation at high throughput rates. For maximum throughput rates, the AD7490 consumes just 1.8 mA with 3 V supplies, and 2.5 mA with 5 V supplies.

By setting the relevant bits in the control register, the analog input range for the part can be selected to be a 0 V to REF_{IN} input or a 0 V to 2 × REF_{IN} input, with either straight binary or twos complement output coding. The AD7490 features 16 single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially. The conversion time is determined by the SCLK frequency because this is also used as the master clock to control the conversion.

The AD7490 is available in a 32-lead LFCSP and a 28-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. The AD7490 offers up to 1 MSPS throughput rates. At maximum throughput with 3 V supplies, the AD7490 dissipates just 5.4 mW of power.
2. A sequence of channels can be selected, through which the AD7490 cycles and converts.
3. The AD7490 operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of V_{DD}.
4. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The part also features various shutdown modes to maximize power efficiency at lower throughput rates. Power consumption is 0.5 µA, maximum, when in full shutdown.
5. The part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

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COMPARABLE PARTS

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EVALUATION KITS

- AD7490 Evaluation Board

DOCUMENTATION

Application Notes

- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-931: Understanding PulSAR ADC Support Circuitry

Data Sheet

- AD7490-DSCC: Military Data Sheet
- AD7490-EP: Enhanced Product Data Sheet
- AD7490: 16-Channel, 1MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP Data Sheet

Technical Books

- The Data Conversion Handbook, 2005

User Guides

- UG-446: Evaluating the AD7490 Successive Approximation ADC

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7490 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- AD7490 Evaluation Software
- BeMicro FPGA Project for AD7490 with Nios driver

REFERENCE MATERIALS

Product Selection Guide

- SAR ADC & Driver Quick-Match Guide

Technical Articles

- MS-1779: Nine Often Overlooked ADC Specifications
- MS-2210: Designing Power Supplies for High Speed ADC

Tutorials

- MT-001: Taking the Mystery out of the Infamous Formula, "SNR=6.02N + 1.76dB", and Why You Should Care
- MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design
- MT-031: Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"

DESIGN RESOURCES

- AD7490 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7490 EngineerZone Discussions.

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REVISION HISTORY

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1/02—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK}[1] = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range (B Version): −40°C to +85°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz				
Signal-to-(Noise + Distortion) (SINAD)[2]	V_{DD} = 5 V	69	70.5		dB
	V_{DD} = 3 V	68	69.5		dB
Signal-to-Noise Ratio (SNR)[2]		69.5			dB
Total Harmonic Distortion (THD)[2]	V_{DD} = 5 V		−84	−74	dB
	V_{DD} = 3 V		−77	−71	dB
Peak Harmonic or Spurious Noise (SFDR)[2]	V_{DD} = 5 V		−86	−75	dB
	V_{DD} = 3 V		−80	−73	dB
Intermodulation Distortion (IMD)[2]	fa = 40.1 kHz, fb = 41.5 kHz				
Second-Order Terms			−85		dB
Third-Order Terms			−85		dB
Aperture Delay			10		ns
Aperture Jitter			50		ps
Channel-to-Channel Isolation[2]	f_{IN} = 400 kHz		−82		dB
Full Power Bandwidth	3 dB		8.2		MHz
	0.1 dB		1.6		MHz
DC ACCURACY[2]					
Resolution		12			Bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed no missed codes to 12 bits			−0.95/+1.5	LSB
0 V to REF_{IN} Input Range	Straight binary output coding				
Offset Error			±0.6	±8	LSB
Offset Error Match				±0.5	LSB
Gain Error				±2	LSB
Gain Error Match				±0.6	LSB
0 V to 2 × REF_{IN} Input Range	−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding offset				
Positive Gain Error				±2	LSB
Positive Gain Error Match				±0.5	LSB
Zero Code Error			±0.6	±8	LSB
Zero Code Error Match				±0.5	LSB
Negative Gain Error				±1	LSB
Negative Gain Error Match				±0.5	LSB
ANALOG INPUT					
Input Voltage Range	RANGE bit set to 1	0		REF_{IN}	V
	RANGE bit set to 0, V_{DD} = 4.75 V to 5.25 V for 0 V to 2 × REF_{IN}	0		2 × REF_{IN}	V
DC Leakage Current				±1	µA
Input Capacitance			20		pF
REFERENCE INPUT					
REF_{IN} Input Voltage	±1% specified performance		2.5		V
DC Leakage Current				±1	µA
REF_{IN} Input Impedance	f_{SAMPLE} = 1 MSPS		36		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input High Voltage, V_{INH}		$0.7 \times V_{DRIVE}$			V
Input Low Voltage, V_{INL}				$0.3 \times V_{DRIVE}$	V
Input Current, I_{IN}	V_{IN} = 0 V or V_{DRIVE}		±0.01	±1	µA
Input Capacitance, C_{IN}+[3]				10	pF
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V	V_{DRIVE} − 0.2			V
Output Low Voltage, V_{OL}	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current	WEAK/$\overline{TRI}$ bit set to 0			±10	µA
Floating State Output Capacitance[3]	WEAK/$\overline{TRI}$ bit set to 0			10	pF
Output Coding	Coding bit set to 1		Straight (Natural) Binary		
	Coding bit set to 0		Twos Complement		
CONVERSION RATE					
Conversion Time	16 SCLK cycles, SCLK = 20 MHz			800	ns
Track-and-Hold Acquisition Time[2]	Sine wave input			300	ns
	Full-scale step input			300	ns
Throughput Rate	V_{DD} = 5 V (see the Serial Interface section)			1	MSPS
POWER REQUIREMENTS					
V_{DD}		2.7		5.25	V
V_{DRIVE}		2.7		5.25	V
I_{DD}[4]	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode (Static)	V_{DD} = 2.7 V to 5.25 V, SCLK on or off		600		µA
Normal Mode (Operational)	V_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz			2.5	mA
(f_S = Maximum Throughput)	V_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz			1.8	mA
Auto Standby Mode	f_{SAMPLE} = 500 kSPS		1.55		mA
	Static			100	µA
Auto Shutdown Mode	f_{SAMPLE} = 250 kSPS		960		µA
	Static			0.5	µA
Full Shutdown Mode	SCLK on or off		0.02	0.5	µA
Power Dissipation[4]					
Normal Mode (Operational)	V_{DD} = 5 V, f_{SCLK} = 20 MHz			12.5	mW
	V_{DD} = 3 V, f_{SCLK} = 20 MHz			5.4	mW
Auto Standby Mode (Static)	V_{DD} = 5 V			460	µW
	V_{DD} = 3 V			276	µW
Auto Shutdown Mode (Static)	V_{DD} = 5 V			2.5	µW
	V_{DD} = 3 V			1.5	µW
Full Shutdown Mode	V_{DD} = 5 V			2.5	µW
	V_{DD} = 3 V			1.5	µW

[1] Specifications apply for f_{SCLK} up to 20 MHz. However, for serial interfacing requirements, see the Timing Specifications section.
[2] See the Terminology section.
[3] Guaranteed by characterization.
[4] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, $V_{DRIVE} \leq V_{DD}$, REF_{IN} = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2. Timing Specifications[1]

	Limit at T_{MIN}, T_{MAX}			
Parameter	**V_{DD} = 3 V**	**V_{DD} = 5 V**	**Unit**	**Description**
f_{SCLK}[2]	10	10	kHz min	
	16	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_2	12	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	20	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_3b[4]	30	20	ns max	Delay from $\overline{CS}$ to DOUT valid
t_4[3]	60	40	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	15	15	ns min	SCLK to DOUT valid hold time
t_8[5]	15/50	15/50	ns min/max	SCLK falling edge to DOUT high impedance
t_9	20	20	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	20	ns min	16th SCLK falling edge to $\overline{CS}$ high
t_{12}	1	1	µs max	Power-up time from full power-down/auto shutdown/auto standby modes

[1] Guaranteed by characterization. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V (see Figure 2). The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

[2] The mark/space ratio for the SCLK input is 40/60 to 60/40. The maximum SCLK frequency is 16 MHz with V_{DD} = 3 V to give a throughput of 870 kSPS. Care must be taken when interfacing to account for data access time, t_4, and the setup time required for the user's processor. These two times determine the maximum SCLK frequency with which the user's system can operate (see the Serial Interface section).

[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 0.7 V_{DRIVE}.

[4] t_3b represents a worst-case figure for having ADD3 available on the DOUT line, that is, if the AD7490 goes back into three-state at the end of a conversion and some other device takes control of the bus between conversions, the user has to wait a maximum time of t_3b before having ADD3 valid on the DOUT line. If the DOUT line is weakly driven to ADD3 between conversions, the user typically has to wait 17 ns at 3 V and 12 ns at 5 V after the $\overline{CS}$ falling edge before seeing ADD3 valid on DOUT.

[5] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

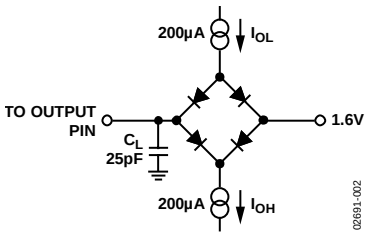


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Ranges	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP, TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	108.2°C/W (LFCSP)
	97.9°C/W (TSSOP)
θ_{JC} Thermal Impedance	32.71°C/W (LFCSP)
	14°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

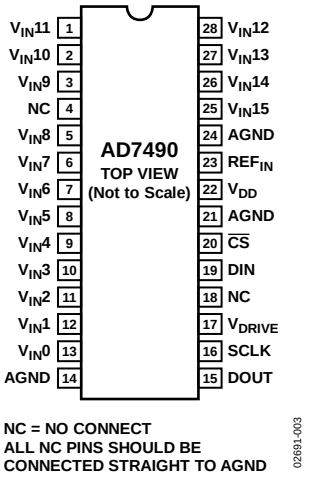


Figure 3. 28-Lead TSSOP Pin Configuration

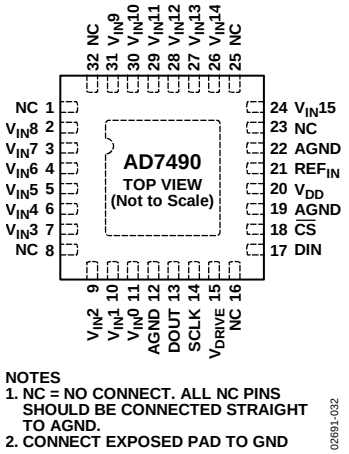


Figure 4. 32-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
20	18	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7490 and also frames the serial data transfer.
23	21	REF_{IN}	Reference Input for the AD7490. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
22	20	V_{DD}	Power Supply Input. The V_{DD} range for the AD7490 is from 2.7 V to 5.25 V. For the 0 V to 2 × REF_{IN} range, V_{DD} should be from 4.75 V to 5.25 V.
14, 21, 24	12, 19, 22	AGND	Analog Ground. Ground reference point for all circuitry on the AD7490. All analog/digital input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
13 to 5, 3 to 1, 28 to 25	11 to 9, 7 to 2, 31 to 26, 24	$V_{IN}0$ to $V_{IN}15$	Analog Input 0 through Analog Input 15. Sixteen single-ended analog input channels that are multiplexed into the on chip track-and-hold. The analog input channel to be converted is selected by using the address bits ADD3 through ADD0 of the control register. The address bits, in conjunction with the SEQ and SHADOW bits, allow the sequence register to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or 0 V to 2 × REF_{IN} as selected via the RANGE bit in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
19	17	DIN	Data In. Logic input. Data to be written to the control register of the AD7490 is provided on this input and is clocked into the register on the falling edge of SCLK (see the Control Register section).
15	13	DOUT	Data Out. Logic output. The conversion result from the AD7490 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided by MSB first. The output coding can be selected as straight binary or twos complement via the CODING bit in the control register.
16	14	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of the AD7490.
17	15	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the AD7490 operates.
N/A	EP	EPAD	Exposed Pad. Connect exposed pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5 shows a typical FFT plot for the AD7490 at 1 MSPS sample rate and 50 kHz input frequency.

Figure 7 shows the power supply rejection ratio vs. supply ripple frequency for the AD7490. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S.

$$PSRR(\text{dB}) = 10 \times \log\left(\frac{Pf}{Pf_s}\right)$$

where:
Pf is equal to the power at frequency f in ADC output.
Pf_S is equal to power at frequency f_S coupled onto the ADC V_{DD} supply input.

Here, a 200 mV p-p sine wave is coupled onto the V_{DD} supply. 10 nF decoupling was used on the supply, and a 1 µF decoupling capacitor was used on the REF_{IN} pin.

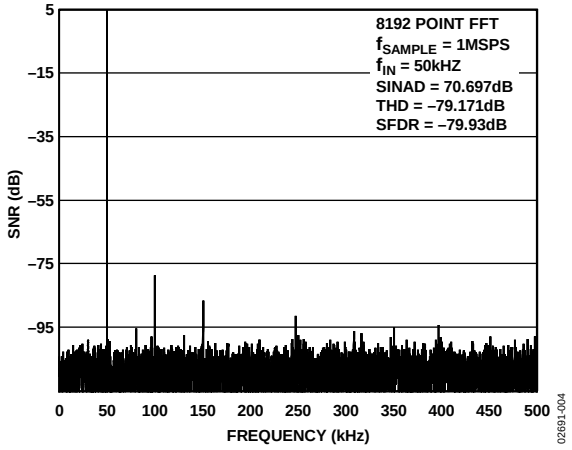


Figure 5. Dynamic Performance at 1 MSPS

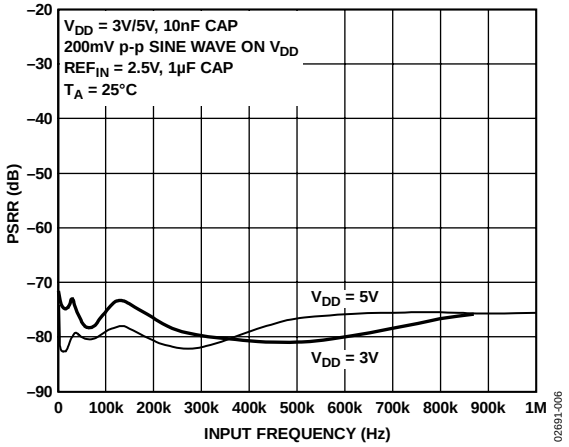


Figure 7. PSRR vs. Supply Ripple Frequency

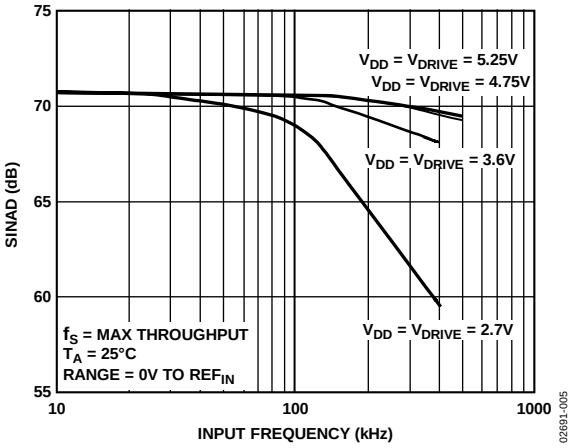


Figure 6. SINAD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS

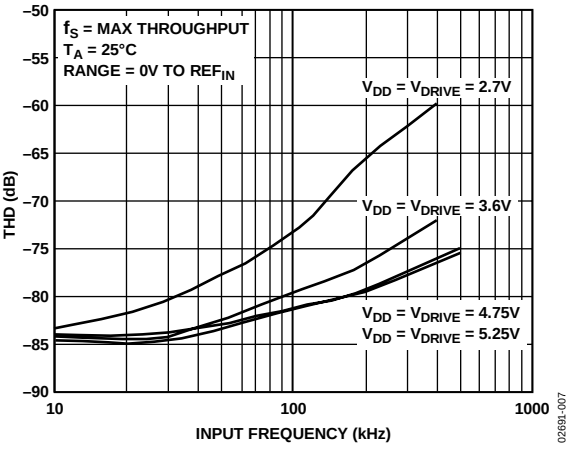


Figure 8. THD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS

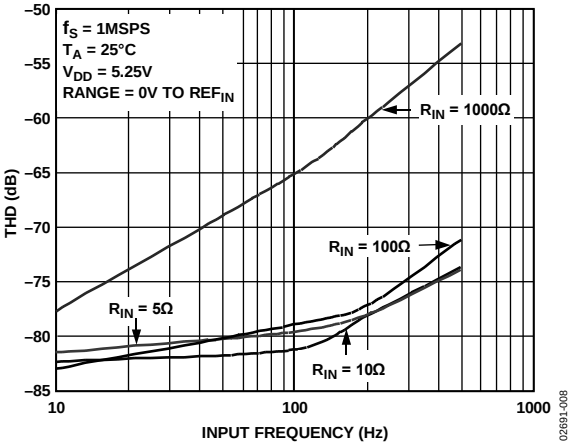


Figure 9. THD vs. Analog Input Frequency for Various Analog Source Impedances

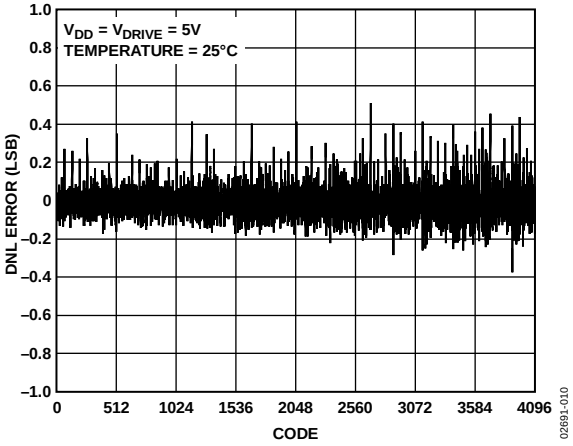


Figure 11. Typical DNL

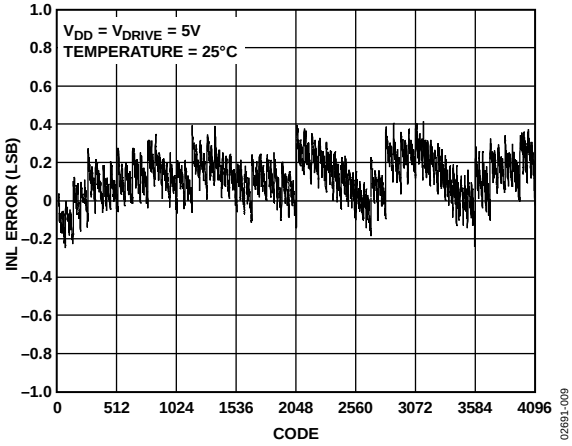


Figure 10. Typical INL

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Zero Code Error
This applies when using the twos complement output coding option, in particular to the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the midscale transition (all 0s to all 1s) from the ideal V_{IN} voltage, that is, REF_{IN} − 1 LSB.

Zero Code Error Match
This is the difference in zero code error between any two channels.

Positive Gain Error
This applies when using the twos complement output coding option, in particular the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the last code transition (011 … 110) to (011 … 111) from the ideal (that is, +REF_{IN} − 1 LSB) after the zero code error has been adjusted out.

Positive Gain Error Match
This is the difference in positive gain error between any two channels.

Negative Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the first code transition (100 … 000) to (100 … 001) from the ideal (that is, −REF_{IN} + 1 LSB) after the zero code error has been adjusted out.

Negative Gain Error Match
This is the difference in negative gain error between any two channels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all 15 nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. This specification is the worst case across all 16 channels for the AD7490.

PSR (Power Supply Rejection)
Variations in power supply affect the full scale transition, but not the converter linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value. (see the Typical Performance Characteristics section).

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track on the 14th SCLK falling edge. Track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-(Noise + Distortion)}\ (\text{dB}) = 6.02N + 1.76$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7490, it is defined as

$$THD(\text{dB}) = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7490 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, and the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

INTERNAL REGISTER STRUCTURE

CONTROL REGISTER

The control register on the AD7490 is a 12-bit, write-only register. Data is loaded from the DIN pin of the AD7490 on the falling edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7490 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after the $\overline{CS}$ falling edge) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 5.

Table 5. Control Register

MSB											LSB
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRITE	SEQ	ADD3	ADD2	ADD1	ADD0	PM1	PM0	SHADOW	WEAK/$\overline{TRI}$	RANGE	CODING

Table 6. Control Register Bit Functions

Bit	Name	Description
11	WRITE	The value written to this bit of the control register determines whether the following 11 bits are loaded to the control register or not. If this bit is a 1, the following 11 bits are written to the control register; if it is a 0, the remaining 11 bits are not loaded to the control register, and it remains unchanged.
10	SEQ	The SEQ bit in the control register is used in conjunction with the SHADOW bit to control the use of the sequencer function and access the Shadow register (see Table 9).
9 to 6	ADD3 to ADD0	These four address bits are loaded at the end of the present conversion sequence and select which analog input channel is to be converted on in the next serial transfer, or they may select the final channel in a consecutive sequence, as described in Table 9. The selected input channel is decoded as shown in Table 7. The next channel to be converted on is selected by the mux on the 14th SCLK falling edge. The address bits corresponding to the conversion result are also output on DOUT prior to the 12 bits of data (see the Serial Interface section).
5, 4	PM1, PM0	Power management bits. These two bits decode the mode of operation of the AD7490, as shown in Table 8.
3	SHADOW	The SHADOW bit in the control register is used in conjunction with the SEQ bit to control the use of the sequencer function and access the Shadow register (see Table 9).
2	WEAK/$\overline{TRI}$	This bit selects the state of the DOUT line at the end of the current serial transfer. If it is set to 1, the DOUT line is weakly driven to the ADD3 channel address bit of the ensuing conversion. If this bit is set to 0, DOUT returns to three-state at the end of the serial transfer. See the Control Register section for more details.
1	RANGE	This bit selects the analog input range to be used on the AD7490. If it is set to 0, the analog input range extends from 0 V to 2 × REF_{IN}. If it is set to 1, the analog input range extends from 0 V to REF_{IN} (for the next conversion). For 0 V to 2 × REF_{IN}, V_{DD} = 4.75 V to 5.25 V.
0	CODING	This bit selects the type of output coding used by the AD7490 for the conversion result. If this bit is set to 0, the output coding for the part is twos complement. If this bit is set to 1, the output coding from the part is straight binary (for the next conversion).

Table 7. Channel Selection

ADD3	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	$V_{IN}0$
0	0	0	1	$V_{IN}1$
0	0	1	0	$V_{IN}2$
0	0	1	1	$V_{IN}3$
0	1	0	0	$V_{IN}4$
0	1	0	1	$V_{IN}5$
0	1	1	0	$V_{IN}6$
0	1	1	1	$V_{IN}7$
1	0	0	0	$V_{IN}8$
1	0	0	1	$V_{IN}9$
1	0	1	0	$V_{IN}10$
1	0	1	1	$V_{IN}11$
1	1	0	0	$V_{IN}12$
1	1	0	1	$V_{IN}13$
1	1	1	0	$V_{IN}14$
1	1	1	1	$V_{IN}15$

Table 8. Power Mode Selection

PM1	PM0	Mode
1	1	Normal operation. In this mode, the AD7490 remains in full power mode, regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the AD7490.
1	0	Full shutdown. In this mode, the AD7490 is in full shutdown mode, with all circuitry on the AD7490 powering down. The AD7490 retains the information in the control register while in full shutdown. The part remains in full shutdown until these bits are changed in the control register.
0	1	Auto shutdown. In this mode, the AD7490 automatically enters shutdown mode at the end of each conversion when the control register is updated. Wake-up time from shutdown is 1 µs, and the user should ensure that 1 µs has elapsed before attempting to perform a valid conversion on the part in this mode.
0	0	Auto standby. In this standby mode, portions of the AD7490 are powered down, but the on-chip bias generator remains powered up. This mode is similar to auto shutdown and allows the part to power up within one dummy cycle, that is, 1 µs with a 20 MHz SCLK.

Sequencer Operation

The configuration of the SEQ and SHADOW bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table 9 outlines the four modes of operation of the sequencer.

Table 9. Sequence Selection

SEQ	SHADOW	Sequence Type
0	0	This configuration means the sequence function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits ADD0 through ADD3 in each prior write operation. This mode of operation reflects the normal operation of a multichannel ADC, without the sequencer function being used, where each write to the AD7490 selects the next channel for conversion (see Figure 12).
0	1	This configuration selects the Shadow register for programming. After the write to the control register, the following write operation loads the contents of the Shadow register. This programs the sequence of channels to be converted on continuously with each successive valid $\overline{CS}$ falling edge (see Shadow register, Table 10 and Figure 13). The channels selected need not be consecutive.
1	0	If the SEQ and SHADOW bits are set in this way, the sequence function is not interrupted upon completion of the write operation. This allows other bits in the control register to be altered while in a sequence without terminating the cycle.
1	1	This configuration is used in conjunction with the ADD3 to ADD0 channel address bits to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel, as determined by the channel address bits in the control register (see Figure 14).

SHADOW REGISTER

The Shadow register on the AD7490 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7490 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that a conversion result is read from the part. This requires 16 serial falling edges for the data transfer. The information is clocked into the Shadow register, provided the SEQ and SHADOW bits are set to 0, 1, respectively, in the previous write to the control register. MSB denotes the first bit in the data stream. Each bit represents an analog input from Channel 0 through Channel 15. A sequence of channels can be selected through which the AD7490 cycles with each consecutive $\overline{CS}$ falling edge after the write to the Shadow register. To select a sequence of channels, the associated channel bit must be set for each analog input. The AD7490 continuously cycles through the selected channels in ascending order, beginning with the lowest channel, until a write operation occurs (that is, the WRITE bit is set to 1), with the SEQ and SHADOW bits configured in any way except 1, 0 (see Table 9). The bit functions are outlined in Table 10.

Figure 12 reflects the normal operation of a multichannel ADC, where each serial transfer selects the next channel for conversion. In this mode of operation, the sequencer function is not used.

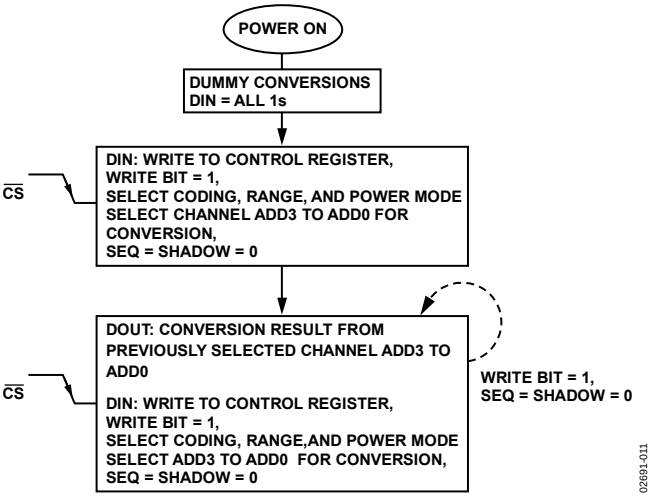


Figure 12. SEQ Bit = 0, SHADOW Bit = 0 Flowchart

Figure 13 shows how to program the AD7490 to continuously convert on a particular sequence of channels using the Shadow register. To exit this mode of operation and revert back to the normal mode of operation of a multichannel ADC (as outlined in Figure 12), ensure that WRITE = 1 and SEQ = SHADOW = 0 on the next serial transfer.

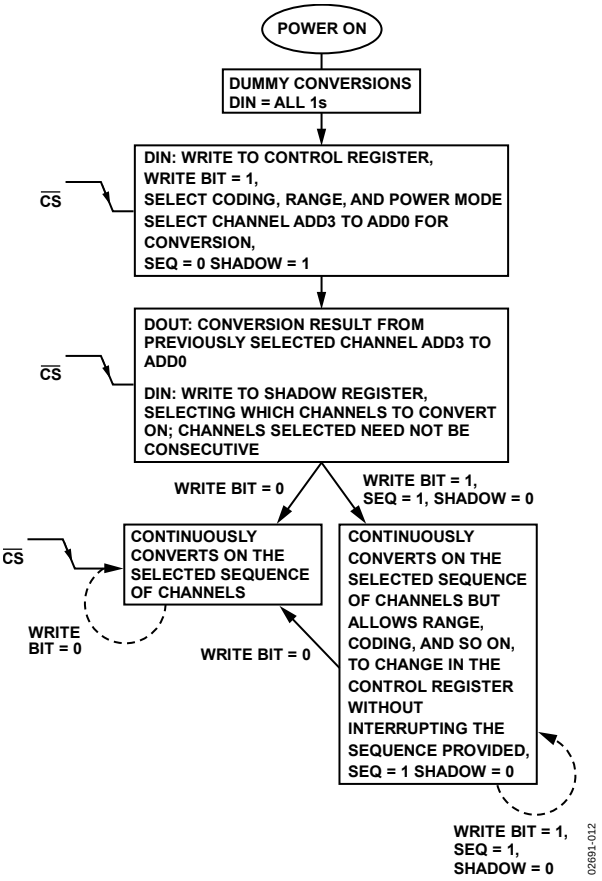


Figure 13. SEQ Bit = 0, SHADOW Bit = 1 Flowchart

Table 10. Shadow Register

MSB															LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$	$V_{IN}8$	$V_{IN}9$	$V_{IN}10$	$V_{IN}11$	$V_{IN}12$	$V_{IN}13$	$V_{IN}14$	$V_{IN}15$

Figure 14 shows how a sequence of consecutive channels can be converted on without having to program the Shadow register or write to the part on each serial transfer. Again, to exit this mode of operation and revert back to the normal mode of operation of a multichannel ADC (as outlined in Figure 12), ensure that the WRITE = 1 and SEQ = SHADOW = 0 on the next serial transfer.

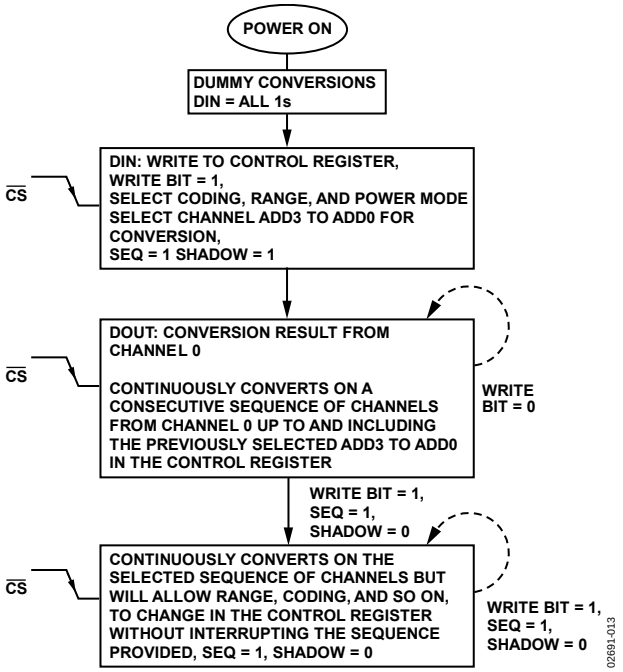


Figure 14. SEQ Bit = 1, SHADOW Bit = 1 Flowchart

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7490 is a fast, 16-channel, 12-bit, single-supply, analog-to-digital converter. The parts can be operated from a 2.7 V to 5.25 V supply. When operated from a 5 V supply and provided with a 20 MHz clock, the AD7490 is capable of throughput rates of up to 1 MSPS.

The AD7490 provides the user with an on-chip, track-and-hold ADC and a serial interface housed in either a 28-lead TSSOP or 32-lead LFCSP package. The AD7490 has 16 single-ended input channels with a channel sequencer, allowing the user to select a sequence of channels through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD74790 is 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, depending on the status of Bit 1 in the control register. For the 0 V to 2 × REF_{IN} range, the part must be operated from a 4.75 V to 5.25 V supply.

The AD7490 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits in the control register.

CONVERTER OPERATION

The AD7490 is a 12-bit successive approximation ADC based around a capacitive DAC. The AD7490 can convert analog input signals in the range 0 V to REF_{IN} or 0 V to 2 × REF_{IN}. Figure 15 and Figure 16 show simplified schematics of the ADC. The ADC comprises control logic, SAR, and a capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 15 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition, and the sampling capacitor acquires the signal on the selected V_{IN} channel.

When the ADC starts a conversion (see Figure 16), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 18 shows the ADC transfer function.

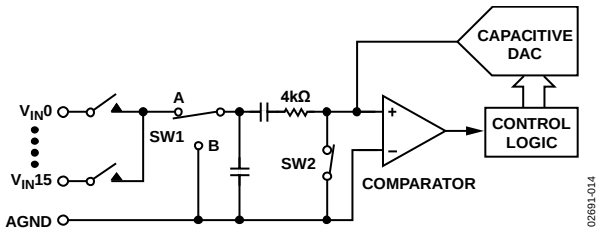


Figure 15. ADC Acquisition Phase

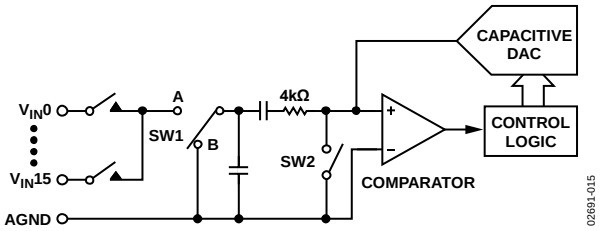


Figure 16. ADC Conversion Phase

Analog Input

Figure 17 shows an equivalent circuit of the analog input structure of the AD7490. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This causes these diodes to become forward biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1 in Figure 17 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a track-and-hold switch and includes the on resistance of the input multiplexer. The total resistance is typically about 400 Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF.

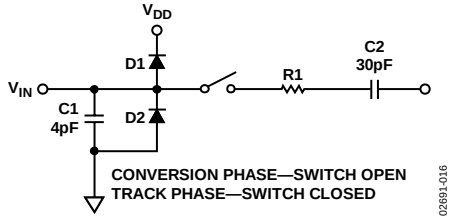


Figure 17. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases, and performance degrades (see Figure 9).

ADC TRANSFER FUNCTION

The output coding of the AD7490 is either straight binary or twos complement depending on the status of the LSB (CODING bit) in the control register. The designed code transitions occur midway between successive LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is equal to $REF_{IN}/4096$. The ideal transfer characteristic for the AD7490 when straight binary coding is selected is shown in Figure 18.

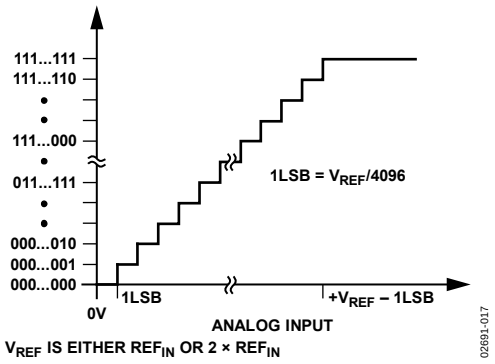


Figure 18. Straight Binary Transfer Characteristic

Handling Bipolar Input Signals

Figure 20 shows how useful the combination of the $2 \times REF_{IN}$ input range and the twos complement output coding scheme is for handling bipolar input signals. If the bipolar input signal is biased about REF_{IN} and twos complement output coding is selected, REF_{IN} becomes the zero code point, $-REF_{IN}$ is negative full scale, and $+REF_{IN}$ becomes positive full scale, with a dynamic range of $2 \times REF_{IN}$.

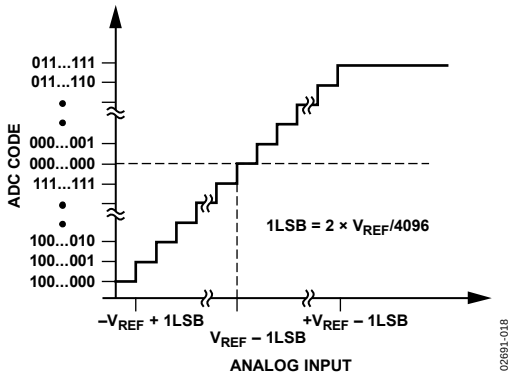


Figure 19. Twos Complement Transfer Characteristic with $REF_{IN} \pm REF_{IN}$ Input Range

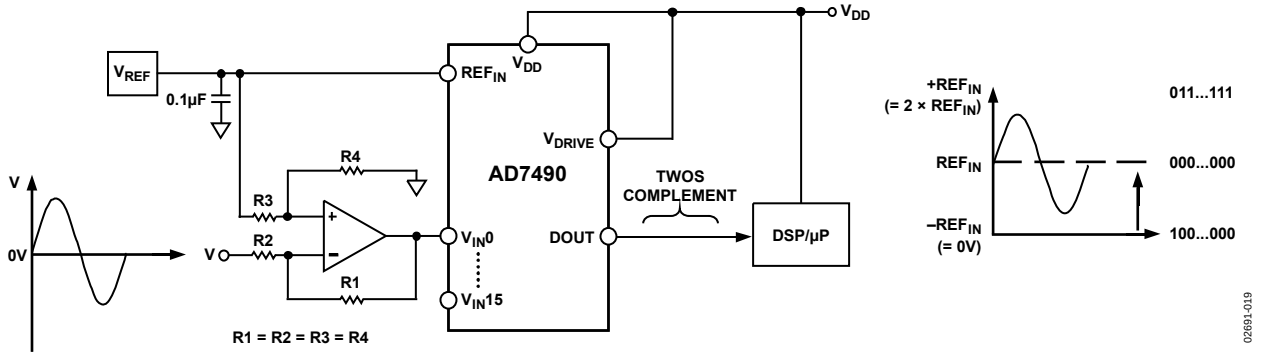


Figure 20. Handling Bipolar Signals

TYPICAL CONNECTION DIAGRAM

Figure 21 shows a typical connection diagram for the AD7490. In this setup, the AGND pin is connected to the analog ground plane of the system. In Figure 21, REF_{IN} is connected to a decoupled 2.5 V supply from a reference source, the AD780, to provide an analog input range of 0 V to 2.5 V (if the RANGE bit is 1) or 0 V to 5 V (if the RANGE bit is 0). Although the AD7490 is connected to a V_{DD} of 5 V, the serial interface is connected to a 3 V microprocessor. The V_{DRIVE} pin of the AD7490 is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see the Digital Input section). The conversion result is output in a 16-bit word. This 16-bit data stream consists of four address bits, indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data. For applications where power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance (see the Modes of Operation section).

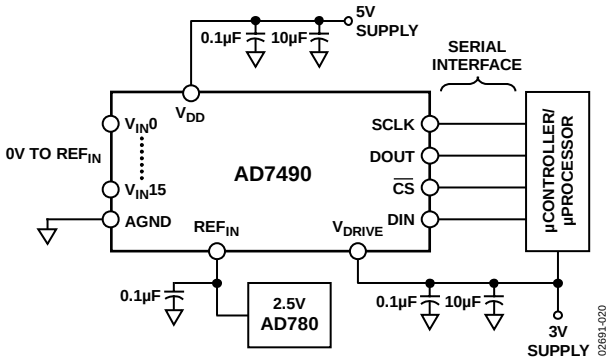


Figure 21. Typical Connection Diagram

Analog Input Channels

Any one of 16 analog input channels can be selected for conversion by programming the multiplexer with the ADD3 to ADD0 address bits in the control register. The channel configurations are shown in Table 7. The AD7490 can also be configured to automatically cycle through a number of channels, as selected. The sequencer feature is accessed via the SEQ and SHADOW bits in the control register (see Table 9). The AD7490 can be programmed to continuously convert on a selection of channels in ascending order. The sequence of analog input channels to be converted on is selected through programming the relevant bits in the Shadow register (see Table 10). The next serial transfer then acts on the sequence programmed by executing a conversion on the lowest channel in the selection.

The next serial transfer results in a conversion on the next highest channel in the sequence, and so on. It is not necessary to write to the control register once a sequencer operation has been initiated. The WRITE bit must be set to 0 or the DIN line tied low to ensure the control register is not accidentally overwritten or the sequence operation interrupted. If the control register is written to at any time during the sequence, it must be ensured that the SEQ and SHADOW bits are set to 1, 0 to avoid interrupting the automatic conversion sequence. This pattern continues until such time as the AD7490 is written to and the SEQ and SHADOW bits are configured with any bit combination except 1, 0. On completion of the sequence, the AD7490 sequencer returns to the first selected channel in the Shadow register and commences the sequence again, if uninterrupted.

Rather than selecting a particular sequence of channels, a number of consecutive channels beginning with Channel 0 can also be programmed via the control register alone without needing to write to the Shadow register. This is possible if the SEQ and SHADOW bits are set to 1, 1. The ADD3 through ADD0 channel address bits then determine the final channel in the consecutive sequence. The next conversion is on Channel 0, then Channel 1, and so on until the channel selected via the ADD3 through ADD0 address bits is reached. The cycle begins again on the next serial transfer, provided the WRITE bit is set to low; or, if high, that the SEQ and SHADOW bits are set to 1, 0, then the ADC continues its preprogrammed automatic sequence uninterrupted. Regardless of which channel selection method is used, the 16-bit word output from the AD7490 during each conversion always contains the channel address that the conversion result corresponds to, followed by the 12-bit conversion result (see the Serial Interface section).

Digital Input

The digital inputs applied to the AD7490 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog inputs.

Another advantage of SCLK, DIN, and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$, DIN, or SCLK is applied before V_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

V_{DRIVE}

The AD7490 also has the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7490 is operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply. The AD7490 has better dynamic performance with a V_{DD} of 5 V, while still being able to interface to 3 V processors. Care should be taken to ensure that V_{DRIVE} does not exceed V_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

Reference Section

An external reference source should be used to supply the 2.5 V reference to the AD7490. Errors in the reference source result in gain errors in the AD7490 transfer function and add to the specified full-scale errors of the part. A capacitor of at least 0.1 μF should be placed on the REF_{IN} pin. Suitable reference sources for the AD7490 include the AD780, REF192, AD1582, ADR03, ADR381, ADR391, and ADR421.

If 2.5 V is applied to the REF_{IN} pin, the analog input range can either be 0 V to 2.5 V or 0 V to 5 V, depending on the RANGE bit in the control register.

MODES OF OPERATION

The AD7490 has a number of different modes of operation. These modes are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The mode of operation of the AD7490 is controlled by the power management bits, PM1 and PM0, in the control register, as detailed in Table 7. When power supplies are first applied to the AD7490, care should be taken to ensure that the part is placed in the required mode of operation (see the Powering Up the AD7490 section).

Normal Mode (PM1 = PM0 = 1)

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times with the AD7490 remaining fully powered at all times. Figure 22 shows the general diagram of the operation of the AD7490 in this mode.

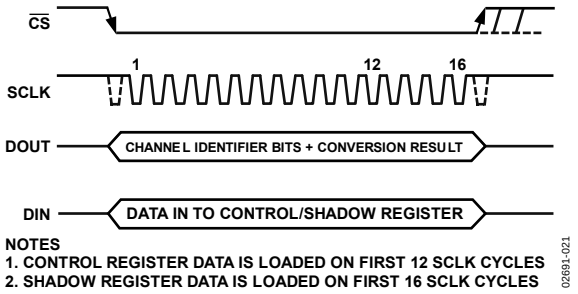


Figure 22. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$, and the track-and-hold enters hold mode, as described in the Serial Interface section. The data presented to the AD7490 on the DIN line during the first 12 clock cycles of the data transfer is loaded

to the control register (provided the WRITE bit is 1). If data is to be written to the Shadow register (SEQ = 0, SHADOW = 1 on previous write), data presented on the DIN line during the first 16 SCLK cycles is loaded into the Shadow register. The part remains fully powered up in normal mode at the end of the conversion as long as PM1 and PM0 are set to 1 in the write transfer during that conversion. To ensure continued operation in normal mode, PM1 and PM0 are both loaded with 1 on every data transfer. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The track-and-hold goes back into track on the 14th SCLK falling edge. $\overline{CS}$ may then idle high until the next conversion or may idle low until sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (DOUT has returned to three-state WEAK/$\overline{TRI}$ bit = 0), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Full Shutdown (PM1 = 1, PM0 = 0)

In this mode, all internal circuitry on the AD7490 is powered down. The part retains information in the control register during full shutdown. The AD7490 remains in full shutdown until the power management bits in the control register, PM1 and PM0, are changed.

If a write to the control register occurs while the part is in full shutdown, with the power management bits changed to PM0 = PM1 = 1 (normal mode), the part begins to power up on the $\overline{CS}$ rising edge. The track-and-hold that was in hold while the part was in full shutdown returns to track on the 14th SCLK falling edge.

To ensure that the part is fully powered up, $t_{POWER\ UP}$ (t_{12}) should elapse before the next $\overline{CS}$ falling edge. Figure 23 shows the general diagram for this mode.

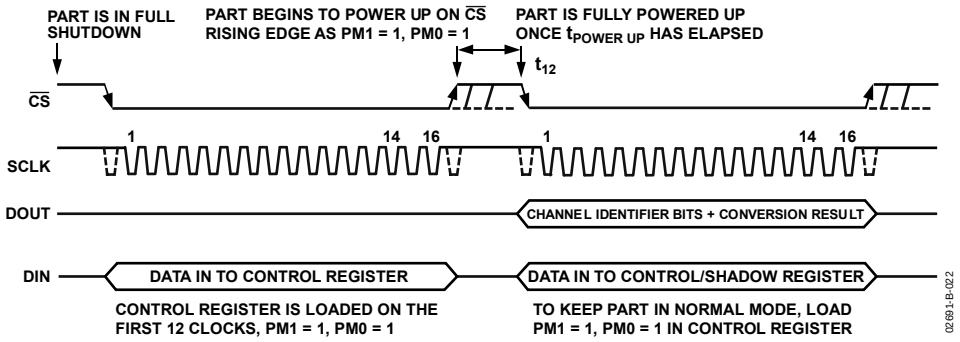


Figure 23. Full Shutdown Mode Operation

Auto Shutdown (PM1 = 0, PM0 = 1)

In this mode, the AD7490 automatically enters shutdown at the end of each conversion when the control register is updated. When the part is in shutdown, the track-and-hold is in hold mode. Figure 24 shows the general diagram of the operation of the AD7490 in this mode.

In shutdown mode, all internal circuitry on the AD7490 is powered down. The part retains information in the control register during shutdown. The AD7490 remains in shutdown until the next $\overline{CS}$ falling edge it receives. On this $\overline{CS}$ falling edge, the track-and-hold that was on hold while the part was in shutdown mode returns to track-and-hold. Wake-up time from auto shutdown is 1 µs, and the user should ensure that 1 µs elapses before attempting a valid conversion. When running the AD7490 with a 20 MHz clock, one dummy cycle of 16 × SCLK should be sufficient to ensure the part is fully powered up. During this dummy cycle, the contents of the control register should remain unchanged; therefore, the WRITE bit should be 0 on the DIN line. This dummy cycle effectively halves the throughput rate of the part, with every other conversion result being valid. In this mode, the power consumption of the part is greatly reduced with the part entering shutdown at the end of each conversion. When the control register is programmed to move into auto shutdown, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

Auto Standby (PM1 = PM0 = 0)

In this mode, the AD7490 automatically enters standby mode at the end of each conversion when the control register is updated. Figure 25 shows the general diagram of the operation of the AD7490 in this mode. When the part is in standby, portions of the AD7490 are powered-down, but the on-chip bias generator remains powered up. The part retains information in the control register during standby. The AD7490 remains in standby until it receives the next $\overline{CS}$ falling edge. On this $\overline{CS}$ falling edge, the track-and-hold that was on hold while the part was in standby returns to track. Wake-up time from standby is 1 µs; the user should ensure that 1 µs elapses before attempting a valid conversion on the part in this mode. When running the AD7490 with a 20 MHz clock, one dummy cycle of 16 × SCLK should be sufficient to ensure the part is fully powered up. During this dummy cycle, the contents of the control register should remain unchanged; therefore, the WRITE bit should be set to 0 on the DIN line. This dummy cycle effectively halves the throughput rate of the part with every other conversion result being valid. In this mode, the power consumption of the part is greatly reduced with the part entering standby at the end of each conversion. When the control register is programmed to move into auto standby, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

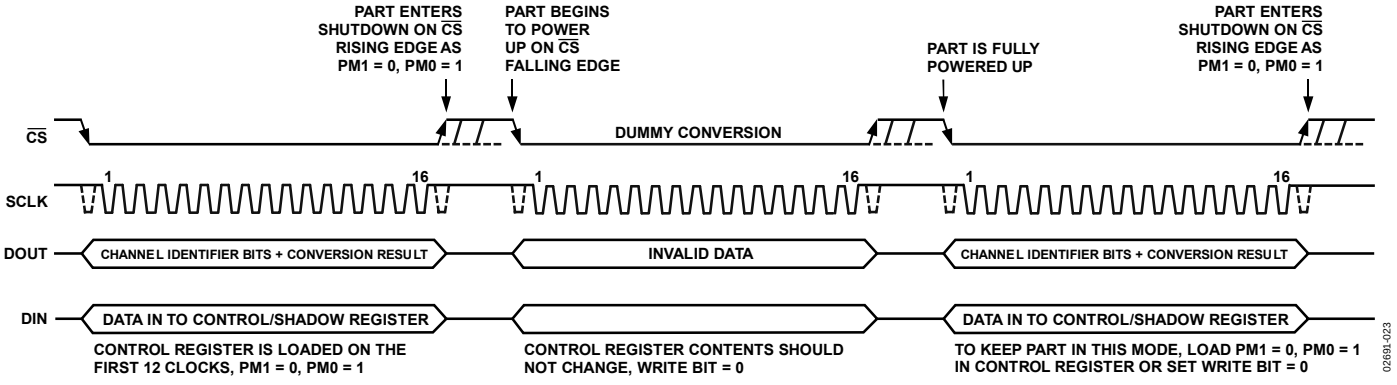


Figure 24. Auto Shutdown Mode Operation

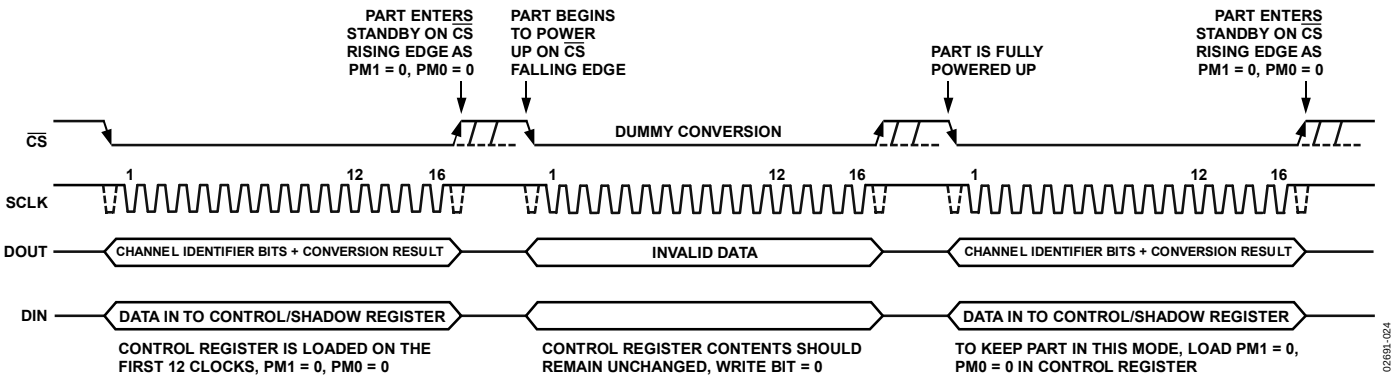


Figure 25. Auto Standby Mode Operation

Powering Up the AD7490

When supplies are first applied to the AD7490, the ADC may power up in any of the operating modes of the part. To ensure that the part is placed into the required operating mode, the user should perform a dummy cycle operation, as outlined in Figure 26.

The three dummy conversion operations outlined in Figure 26 must be performed to place the part into either of the auto modes. The first two conversions of this dummy cycle operation are performed with the DIN line tied high, and for the third conversion of the dummy cycle operation, the user should write the desired control register configuration to the AD7490 to place the part into the required auto mode. On the third $\overline{CS}$ rising edge after the supplies are applied, the control register contains the correct information and valid data results from the next conversion.

Therefore, to ensure the part is placed into the correct operating mode when supplies are first applied to the AD7490, the user must first issue two serial write operations with the DIN line tied high. On the third conversion cycle, the user can then write to the control register to place the part into any of the operating modes. The user should not write to the Shadow register until the fourth conversion cycle after the supplies are applied to the ADC to guarantee that the control register contains the correct data.

If the user wishes to place the part into either normal mode or full shutdown mode, the second dummy cycle with DIN tied high can be omitted from the three dummy conversion operation outlined in Figure 26.

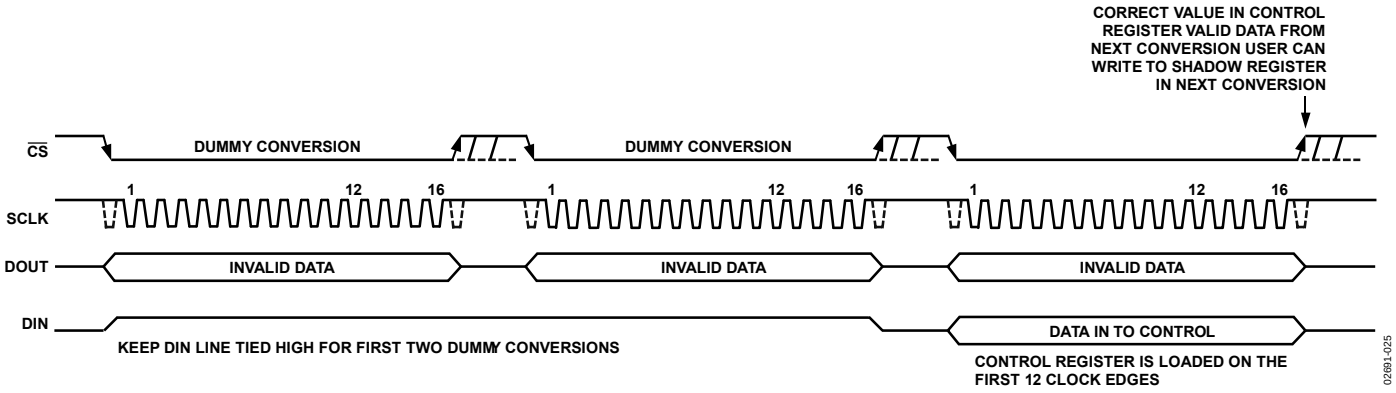


Figure 26. Placing into the Required Operating Mode After Supplies Are Applied

SERIAL INTERFACE

Figure 27 shows the detailed timing diagram for serial interfacing to the AD7490. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7490 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled at this point. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold goes back into track on the 14th SCLK falling edge, as shown in Figure 27 at point B, except when the write is to the Shadow register, in which case the track-and-hold does not return to track until the rising edge of $\overline{CS}$, that is, Point C in Figure 28. On the 16th SCLK falling edge, the DOUT line goes back into three-state (assuming the WEAK/$\overline{TRI}$ bit is set to 0). Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7490. The 12 bits of conversion data are preceded by the four channel address bits, ADD3 to ADD0, identifying which channel the conversion result corresponds to. $\overline{CS}$ going low allows the ADD3 address bit to be read in by the microprocessor or DSP. The remaining address bits and data bits are then clocked out by subsequent SCLK falling edges, beginning with the second address bit, ADD2. Thus, the first SCLK falling edge on the serial clock has the ADD3 address bit provided and also clocks out address bit ADD2. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

Writing information to the control register takes place on the first 12 falling edges of SCLK in a data transfer, assuming the MSB, that is, the WRITE bit, has been set to 1. If the control register is programmed to use the Shadow register, writing information to the Shadow register takes place on all 16 SCLK falling edges in the next serial transfer (see Figure 28). The Shadow register is updated upon the rising edge of $\overline{CS}$, and the track-and-hold begins to track the first channel selected in the sequence.

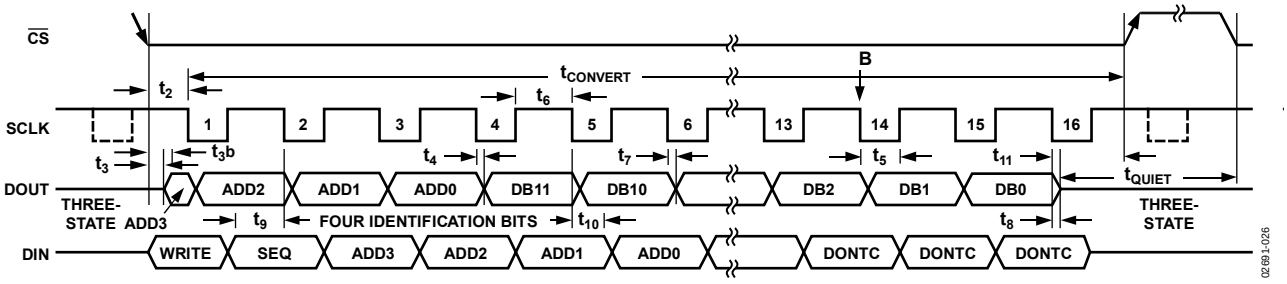


Figure 27. Serial Interface Timing Diagram

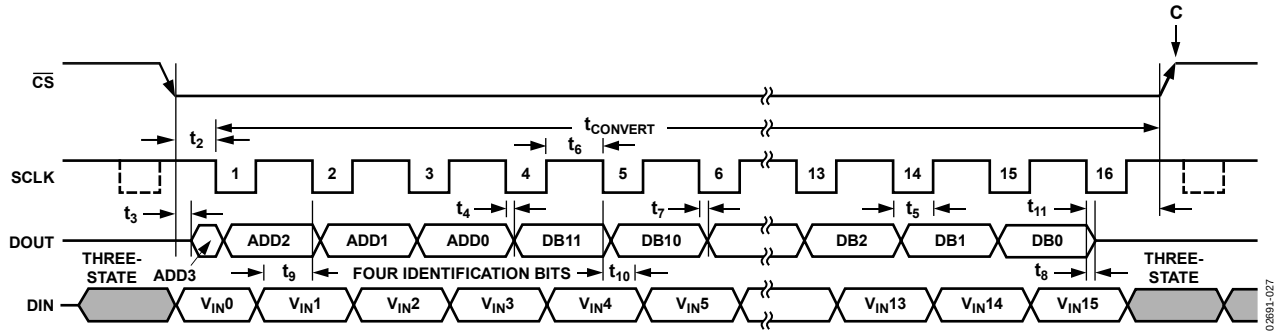


Figure 28. Writing to Shadow Register Timing Diagram

If the WEAK/$\overline{\text{TRI}}$ bit in the control register is set to 1, instead of returning to true three-state on the 16th SCLK falling edge, the DOUT line is pulled weakly to the logic level corresponding to ADD3 of the next serial transfer. This is done to ensure that the MSB of the next serial transfer is set up in time for the first SCLK falling edge after the $\overline{\text{CS}}$ falling edge. If the WEAK/$\overline{\text{TRI}}$ bit is set to 0 and the DOUT line has been in true three-state between conversions, the ADD3 address bit may not be set up in time for the DSP/microcontroller to clock it in successfully, depending on the particular DSP or microcontroller interfacing to the AD7490. In this case, ADD3 would only be driven from the falling edge of $\overline{\text{CS}}$ and must then be clocked in by the DSP on the following falling edge of SCLK. However, if the WEAK/$\overline{\text{TRI}}$ bit is set to 1, although DOUT is driven with the ADD3 address bit since the last conversion, it is nevertheless so weakly driven that another device may still take control of the bus. It does not lead to a bus contention (for example, a 10 kΩ pull-up or pull-down resistor is sufficient to overdrive the logic level of ADD3 between conversions), and all 16 channels may be identified. If this does happen and another device takes control of the bus, it is not guaranteed that DOUT will be fully driven to ADD3 again in time for the read operation when control of the bus is taken back.

This is especially useful if using an automatic sequence mode to identify to which channel each result corresponds. If only the first eight channels are in use, Address Bit ADD3 does not need to be decoded, and whether it is successfully clocked in as a 1 or 0 does not matter as long as it is still counted by the DSP/microcontroller as the MSB of the 16-bit serial transfer.

POWER vs. THROUGHPUT RATE

By operating the AD7490 in auto shutdown or auto standby mode, the average power consumption of the ADC decreases at lower throughput rates. Figure 29 shows that as the throughput rate is reduced, the part remains in shutdown state longer and the average power consumption drops accordingly over time.

For example, if the AD7490 is operated in a continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 20 MHz (V_{DD} = 5 V), with PM1 = 0 and PM0 = 1 (that is, the device is in auto shutdown mode), the power consumption is calculated as shown in Equation 1.

The maximum power dissipation during normal operation is 12.5 mW (V_{DD} = 5 V). If the power-up time from auto shutdown is one dummy cycle, that is, 1 µs, and the remaining conversion time is another cycle, that is, 1 µs, then the AD7490 can be said to dissipate 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in shutdown mode. The AD7490 can be said to dissipate 2.5 µW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is

$$\frac{2}{10} \times 12.5\ \text{mW} + \frac{8}{10} \times 2.5\ \mu\text{W} = 2.502\ \text{mW} \quad (1)$$

When operating the AD7490 in auto standby mode (PM1 = PM0 = 0 at 5 V, 100 kSPS), the AD7490 power dissipation is calculated as shown in Equation 2.

The maximum power dissipation is 12.5 mW at 5 V during normal operation. Again the power-up time from auto standby is one dummy cycle, 1 µs, and the remaining conversion time is another dummy cycle, 1 µs. The AD7490 dissipates 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in standby mode, dissipating 460 µW for 8 µs. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each conversion cycle is

$$\frac{2}{10} \times 12.5\ \text{mW} + \frac{8}{10} \times 460\ \mu\text{W} = 2.868\ \text{mW} \quad (2)$$

Figure 29 shows the power vs. throughput rate when using both the auto shutdown mode and auto standby mode with 5 V supplies. At the lower throughput rates, power consumption for the auto shutdown mode is lower than that for the auto standby mode, with the AD7490 dissipating less power when in shutdown compared to standby. As the throughput rate is increased, however, the part spends less time in power-down states; hence, the difference in power dissipated is negligible between modes. For 3 V supplies, the power consumption of the AD7490 decreases. Similar power calculations can be done at 3 V.

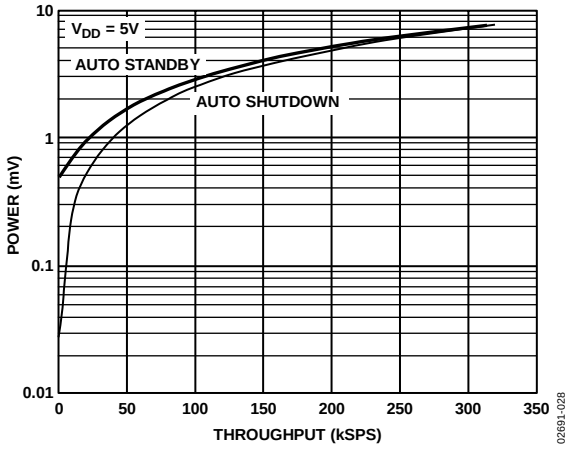


Figure 29. Power vs. Throughput Rate in Auto Shutdown and Auto Standby Mode

MICROPROCESSOR INTERFACING

The serial interface on the AD7490 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7490 with some of the more common microcontroller and DSP serial interface protocols.

AD7490 to TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7490. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7490 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX0 (TX serial clock on Serial Port 0) and FSX0 (TX frame sync from Serial Port 0). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The connection diagram is shown in Figure 30. Note that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provide equidistant sampling. The V_{DRIVE} pin of the AD7490 takes the same supply voltage as that of the TMS320C541. This allows the ADC to operate at a higher voltage than the serial interface, that is, TMS320C541, if necessary.

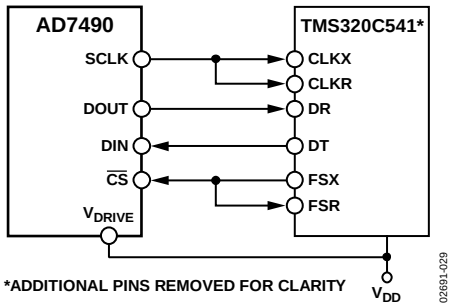


Figure 30. Interfacing to the TMS320C541

AD7490 to ADSP-21xx

The ADSP-21xx family of DSPs is interfaced directly to the AD7490 without any glue logic required. The V_{DRIVE} pin of the AD7490 takes the same supply voltage as that of the ADSP-218x.This allows the ADC to operate at a higher voltage than the serial interface, that is, ADSP-218x, if necessary.

The SPORT0 control register should be set up as follows:

- TFSW = RFSW = 1, alternate framing
- INVRFS = INVTFS = 1, active low frame signal
- DTYPE = 00, right justify data
- SLEN = 1111, 16-bit data-words
- ISCLK = 1, internal serial clock
- TFSR = RFSR = 1, frame every word
- IRFS = 0
- ITFS = 1

The connection diagram is shown in Figure 31. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode, and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and, as with all signal processing applications, equidistant sampling is necessary. In this example, however, the timer interrupt is used to control the sampling rate of the ADC, and under certain conditions, equidistant sampling may not be achieved.

The timer register, for example, is loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and, thus, the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, if the ADSP-2189 with a 20 MHz crystal has an overall master clock frequency of 40 MHz, then the master cycle time is 25 ns. If the SCLKDIV register is loaded with a value of 3, an SCLK of 5 MHz is obtained, and eight master clock periods elapse for every 1 SCLK period. Depending on the throughput rate selected, if the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and subsequently between transmit instructions. This situation results in nonequidistant sampling because the transmit instruction occurs on a SCLK edge. If the number of SCLKs between interrupts is a figure of N, equidistant sampling is implemented by the DSP.

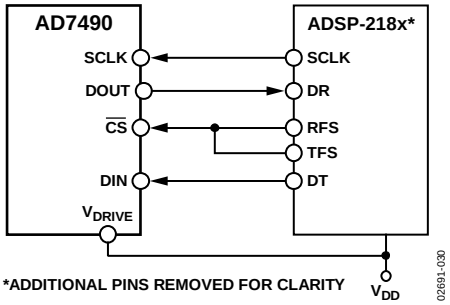


Figure 31. Interfacing to the ADSP-218x

AD7490 to DSP563xx

The connection diagram in Figure 32 shows how the AD7490 can be connected to the ESSI (synchronous serial interface) of the DSP563xx family of DSPs from Motorola. Each ESSI (two on board) is operated in synchronous mode (the SYN bit in CRB = 1) with internally generated word length frame sync for both Tx and Rx (FSL1 = 0 and FSL0 = 0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB.

Set the word length to 16 by setting WL1 = 1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so the frame sync is negative. Note that for signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx provide equidistant sampling.

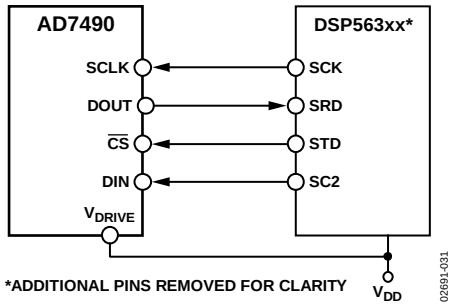


Figure 32. Interfacing to the DSP563xx

In the example shown in Figure 32, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output, SCKD = 1. The AD7490 V_{DRIVE} pin takes the same supply voltage as that of the DSP563xx. This allows the ADC to operate at a higher voltage than the serial interface, that is, DSP563xx, if necessary.

APPLICATION HINTS

Grounding and Layout

The AD7490 has very good immunity to noise on the power supplies shown in the PSRR vs. Supply Ripple Frequency plot, Figure 7. Care should still be taken, however, with regard to grounding and layout.

The printed circuit board that houses the AD7490 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. All three AGND pins of the AD7490 should be sunk in the AGND plane. Digital and analog ground planes should be joined at only one place. If the AD7490 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7490.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7490 to avoid noise coupling. The power supply lines to the AD7490 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

PCB Design Guidelines for Chip Scale Package

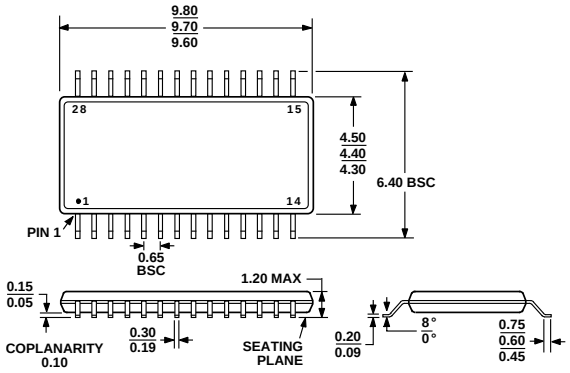
The lands on the chip scale package (CP-32) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided. Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

Evaluating the AD7490 Performance

The recommended layout for the AD7490 is outlined in the evaluation board for the AD7490. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CONTROL BRD2. The EVAL-CONTROL BRD2 can be used in conjunction with the AD7490 evaluation board, as well as many other Analog Devices, Inc., evaluation boards ending in the CB designator, to demonstrate and evaluate the ac and dc performance of the AD7490.

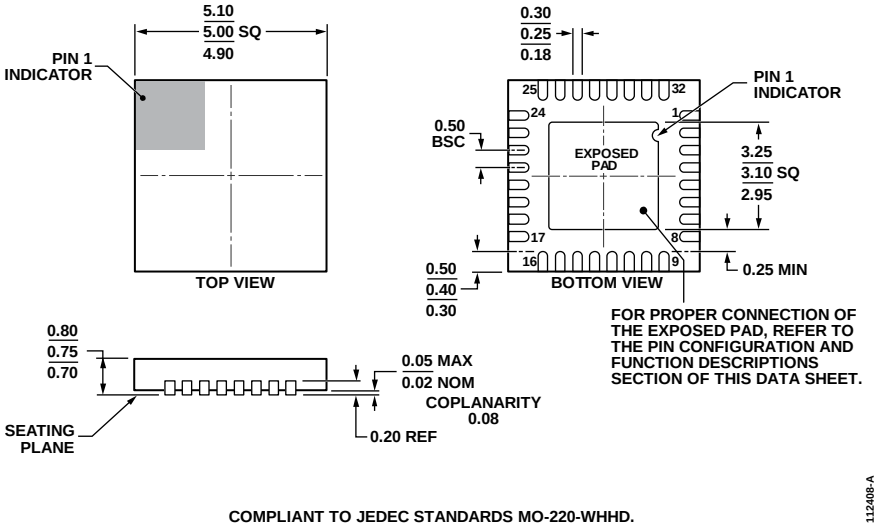
The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7490. The software and documentation are on a CD shipped with the evaluation board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 33. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 34. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Integral Linearity Error (LSB)	Package Description	Package Option
AD7490BCPZ	−40°C to +85°C	±1	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD7490BCPZ-REEL7	−40°C to +85°C	±1	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD7490BRU	−40°C to +85°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD7490BRU-REEL7	−40°C to +85°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD7490BRUZ	−40°C to +85°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD7490BRUZ-REEL	−40°C to +85°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD7490BRUZ-REEL7	−40°C to +85°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
EVAL-AD7490SDZ			Evaluation Board	
EVAL-SDP-CB1Z			Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7490CBZ can be used as a standalone evaluation board or in conjunction with the evaluation controller board for evaluation/demonstration purposes.
[3] The EVAL-CONTROL BRD2 is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in a CB designator. To order a complete evaluation kit, you need to order the particular ADC evaluation board (for example, EVAL-AD7490CBZ), the EVAL-CONTROL-BRD2, and a 12 V ac transformer. See the relevant evaluation board data sheet for more information.

NOTES

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