July 09, 2008

IRS2530D(S)

DIM8™ DIMMING BALLAST CONTROL IC

IC Features

- Dimming ballast control plus half-bridge driver
- Closed-loop lamp current dimming control
- Internal non-ZVS protection
- Internal crest factor protection
- Programmable preheat time
- Fixed dead-time (2.0μs typ.)
- Lamp insert auto-restart
- Internal bootstrap MOSFET
- Internal 15.6V zener clamp diode on Vcc
- Micropower startup (250μA)
- Latch immunity and ESD protection

Ballast System Features

- Single chip dimming solution
- Simple lamp current dimming control method
- Single lamp current sensing resistor required
- No half-bridge current-sensing resistor required
- No external protection circuits required (fully internal)
- Flash-free lamp start at all dimming levels
- Large reduction in component count
- Easy to use for fast design cycle time
- Increased manufacturability and reliability

Product Summary

Topology	Half-Bridge
V_{OFFSET}	600 V
V_{OUT}	V_{CC}
I_{O+} & I_{O-} (typical)	180mA & 260mA
Deadtime (typical)	2.0μs

Package Types



PDIP8

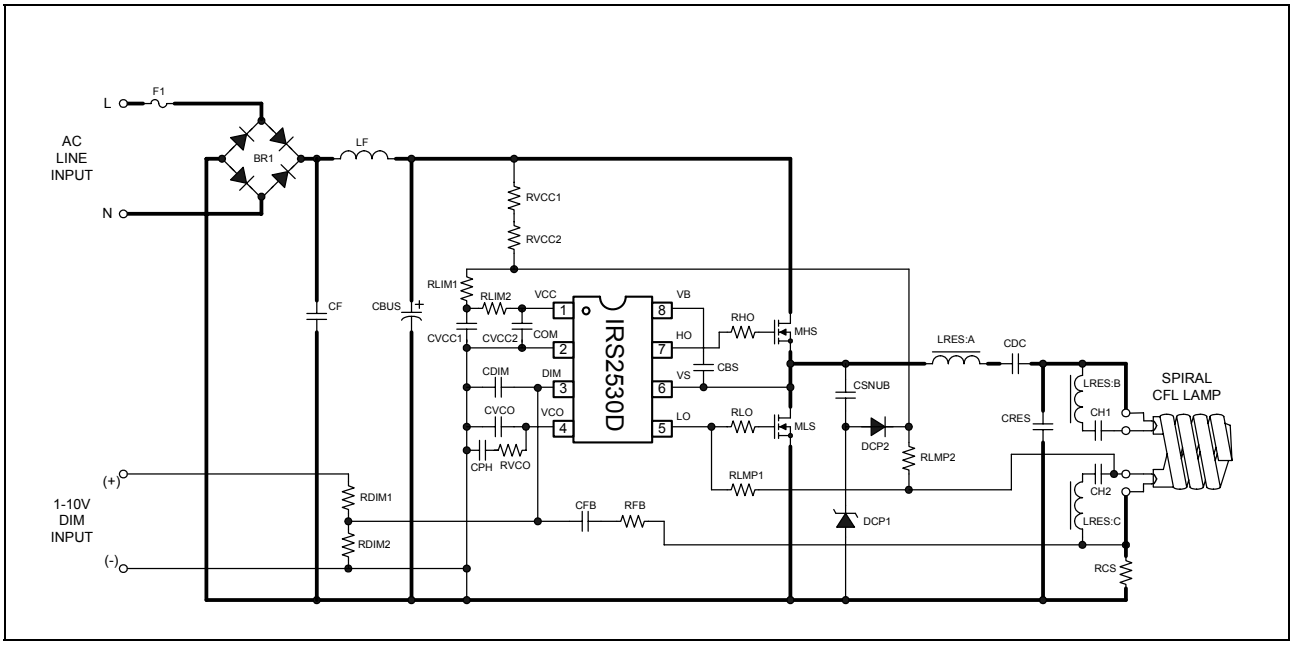


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Typical applications

- Linear dimming ballast (down to 10%)
- 3-way dimming ballast
- Multi-level switch dimming ballast

Typical Connection Diagram



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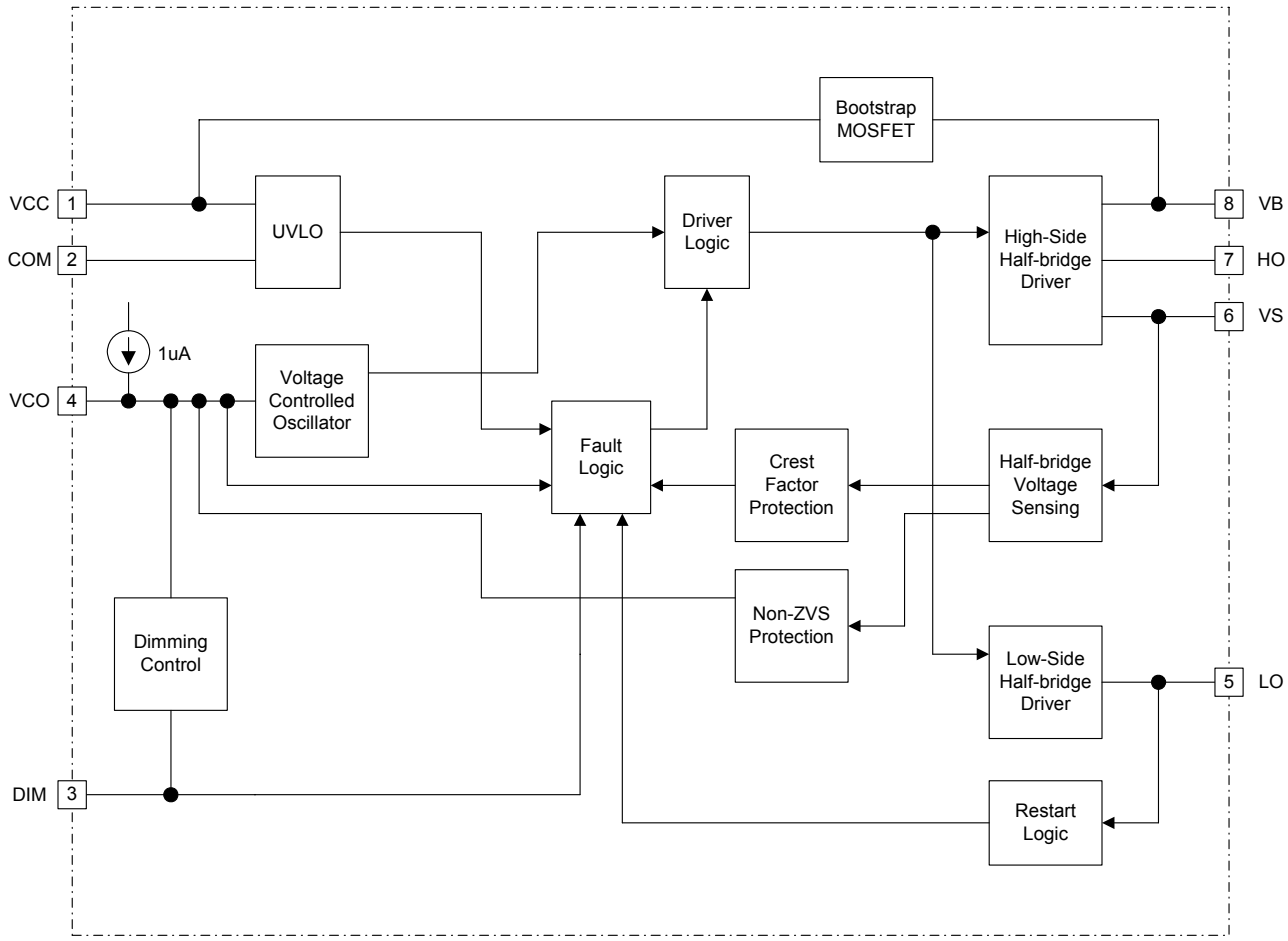
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Description

This IC takes full advantage of IR's patented ballast and high-voltage technologies to realize a simple, high-performance dimming ballast solution. A single high-voltage pin senses the half-bridge current and voltage to perform necessary ballast protection functions. The DC dim input voltage reference and the AC lamp current feedback have been coupled together allowing a single pin to be used for dimming. Combining these high-voltage control algorithms together with a simple dimming method in a single 8-pin IC results in a large reduction in component count, an increase in manufacturability and reliability, a reduced design cycle time, while maintaining high dimming ballast system performance

Block Diagram



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Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8	MSL2††† (per IPC/JEDEC J-STD-020C)
		PDIP8	Not applicable (non-surface mount package style)
ESD	**Machine Model**	Class C (per JEDEC standard EIA/JESD22-A115)	
	Human Body Model	Class 3A (per EIA/JEDEC standard JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78A)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-Side Floating Supply Voltage	-0.3	625	V
V_S	High-Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	Low-Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{VCO}	VCO Input Voltage††	-0.3	6	
V_{DIM}	DIM Input Voltage	-0.3	V_{CC} + 0.3	
I_{CC}	Supply Current†	---	20	mA
I_{OMAX}	Maximum allowable current at LO, HO and PFC due to external power transistor Miller effect.	-500	500	
dV_S/dt	Allowable VS Pin Voltage Slew Rate	-50	50	V/ns
P_D	Maximum Power Dissipation @ $T_A \leq +25^oC$, 8-Pin DIP	---	1.0	W
P_D	Maximum Power Dissipation @ $T_A \leq +25^oC$, 8-Pin SOIC	---	0.625	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin DIP	---	85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin SOIC	---	128	
T_J	Junction Temperature	-55	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	---	300	

† This IC contains a zener clamp structure between the chip VCC and COM which has a nominal breakdown voltage of 15.6V. This supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

†† This IC contains a zener clamp structure between the chip VCO and COM which has a nominal breakdown voltage of 7.25V. This pin should not be driven by a DC, low impedance power source greater than the V_{VCOMAX} specified in the Electrical Characteristics section.

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Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High-Side Floating Supply Voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady State High-Side Floating Supply Offset Voltage	-3.0†††	600	V
V_{CC}	Supply Voltage	V_{CCUV+} + 0.1V	V_{CLAMP}	V
I_{CC}	Supply Current	---	5	mA
V_{VCO}	VCO Pin Voltage	0	6	V
T_J	Junction Temperature	-40	125	ºC

††† Care should be taken to avoid output switching conditions where the V_S node decreases below COM by more than 5V.

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Electrical Characteristics

VCC=VBS=14V, VS=0V, CVCC=CBS=0.1μF, CVCO=CDIM=10nF, CLO=CHO=1nF, and TA = 25°C unless otherwise specified. The output voltage and current (VO and IO) parameters are referenced to COM and are applicable to the respective HO and LO output leads.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CLAMP}	V_{CC} Zener Clamp Voltage	14.6	15.6	16.6	V	I_{CC} = 10mA
V_{CCUV+}	Rising V_{CC} UVLO+ Threshold	11.5	12.5	13.5		
V_{CCUV-}	Falling V_{CC} UVLO- Threshold	9.5	10.5	11.5		
V_{CCUVHY}	V_{CC} Undervoltage Lockout Hysteresis	1.5	2.0	3.0		
I_{QCCUV}	Micropower Startup V_{CC} Supply Current	---	250	---	μA	V_{CC} = 8V
I_{CCDIM}	DIM Mode V_{CC} Supply Current	---	4.5	---	mA	MODE = DIM
I_{QCCFLT}	Fault Mode V_{CC} Supply Current	---	375	---	μA	MODE = FAULT
V_{VCOMAX}	VCO Pin Zener Clamp Voltage	---	7.25	---	V	MODE = DIM
Floating Supply Characteristics						
I_{BS}	V_{BS} Supply Current	---	2	3	mA	MODE = DIM
I_{QBSUV}	UVLO Mode VBS Quiescent Current	---	---	50	μA	VBS = 7V
V_{BSUV+}	Rising V_{BS} Supply Undervoltage Threshold	8.0	9.0	10.0	V	
V_{BSUV-}	Falling V_{BS} Supply Undervoltage Threshold	7.0	8.0	9.0		
I_{LK}	Offset Supply Leakage Current	---	---	50	μA	V_B = V_S = 600V
Ballast Control Characteristics						
f_{MIN}	Minimum Output Frequency	32.0	34.2	36.4	kHz	VCO = 6V
f_{MAX}	Maximum Output Frequency	---	115	---		VCO = 0V
d	Duty Cycle	---	50	---	%	
DT	Output Deadtime (HO or LO)	---	2.0	---	μs	MODE = ALL
I_{VCO}	VCO Pin Charging Current	---	1	---	μA	MODE = PH/IGN
V_{LOSD+}	LO Pin Shutdown Threshold	---	8.75	---	V	MODE = FAULT
V_{LOSD-}	LO Pin Re-start Threshold	---	8.5	---		MODE = FAULT
V_{ZVSTH}	VS Non-ZVS Detection Threshold	---	4.5	---	V	MODE = DIM, LO = HIGH
$V_{VCOFLT+}$	VCO Fault Rising Threshold	---	4.0	---		MODE = PH/IGN
CSCF	Crest factor peak-to-average fault factor	---	5.5	---	N/A	MODE = DIM VS offset = 0.5V

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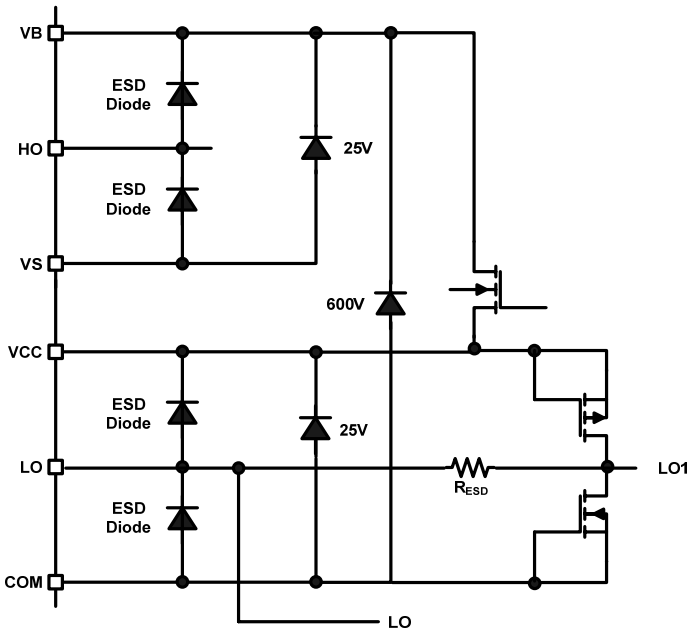
Electrical Characteristics

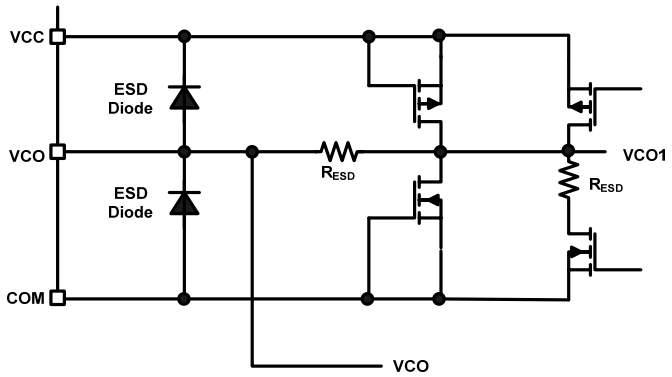
VCC=VBS=14V, VS=0V, CVCC=CBS=0.1µF, CVCO=CDIM=10nF, CLO=CHO=1nF, and TA = 25°C unless otherwise specified. The output voltage and current (VO and IO) parameters are referenced to COM and are applicable to the respective HO and LO output leads.

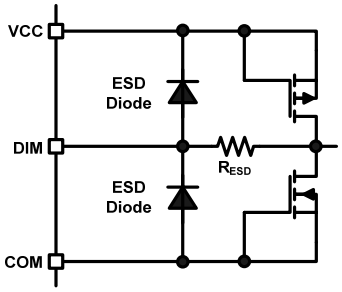
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Dimming Control Characteristics						
V_{DIMREG}	DIM Regulation Threshold	---	0.0	---	V	MODE = DIM
Gate Driver Output Characteristics (HO and LO)						
V_{OH}	High-Level Output Voltage	---	VCC	---		I_O = 0A
V_{OL}	Low-Level Output Voltage	---	COM	---		I_O = 0A
V_{OL_UV}	UV-Mode Output Voltage	---	COM	---		I_O = 0A, $V_{CC} \leq V_{CCUV-}$
t_r	Output Rise Time	---	120	220	ns	
t_f	Output Fall Time	---	50	80		
t_{SD}	Shutdown Propagation Delay	---	350	---		
I_{O+}	Output source current	---	180	---	mA	
I_{O-}	Output sink current	---	260	---		
Bootstrap FET Characteristics						
VB_ON	VB when the bootstrap FET is on	---	13.3	---	V	
IB_CAP	VB source current when FET is on	30	55	---	mA	CBS = 0.1µF
IB_10V	VB source current when FET is on	8	12	---		VB = 10V

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I/O Pin Equivalent Circuit Diagrams





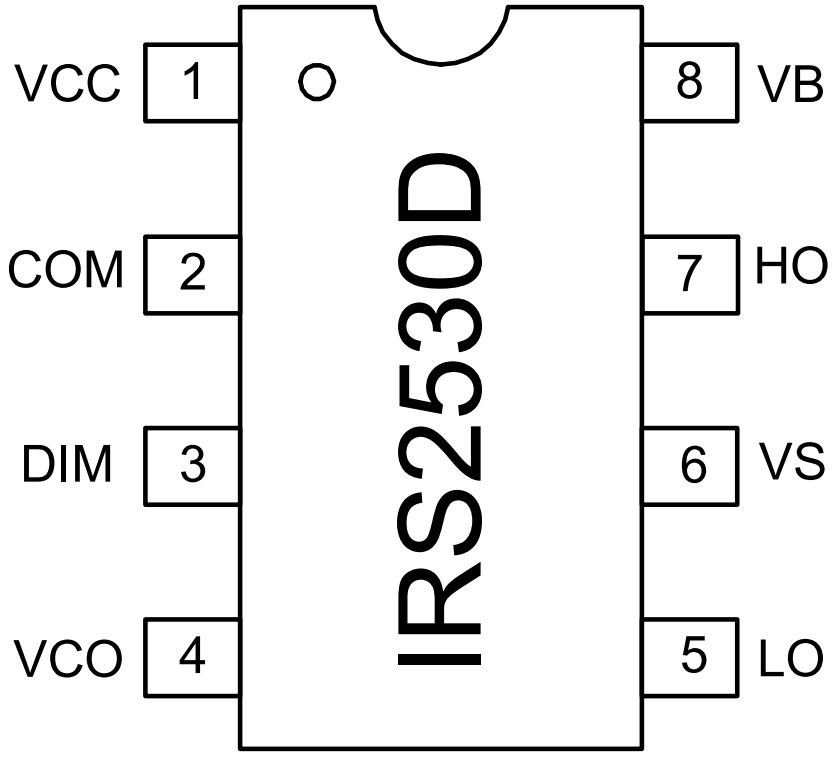


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Lead Definitions

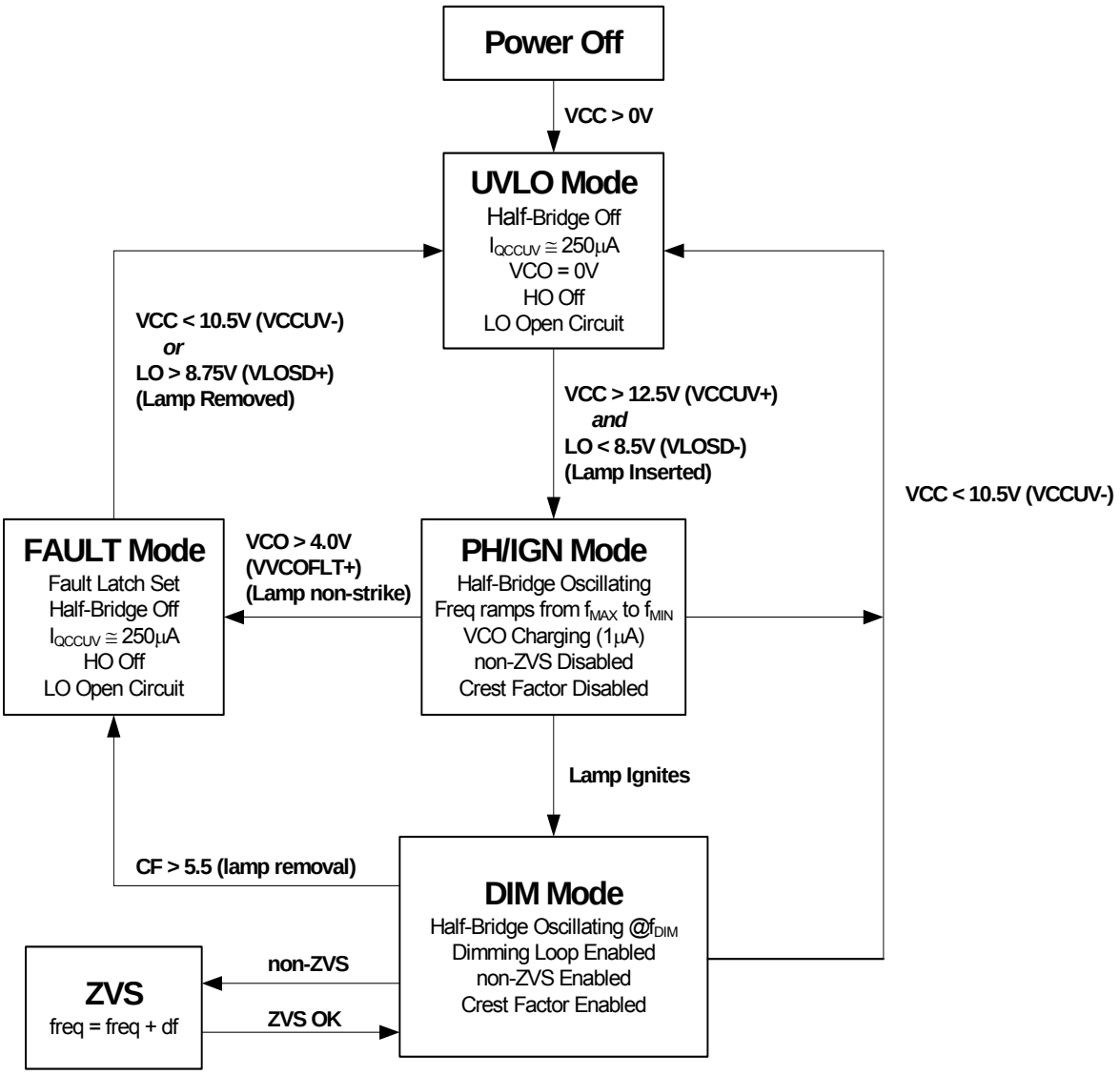
Pin #	Symbol	Description
1	VCC	Logic and internal gate drive supply voltage
2	COM	IC power and signal ground
3	DIM	Dimming DC reference and AC lamp current feedback input
4	VCO	Voltage-controlled oscillator (VCO) input
5	LO	Half-bridge low-side gate driver output
6	VS	High voltage floating supply return and half-bridge sensing input
7	HO	High-side gate driver output
8	VB	High-side gate driver floating supply

Lead Assignments



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State Diagram



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Application Information and Additional Details

Information regarding the following topics is included as subsections within this section of the datasheet:

- UVLO Mode and IC Supply Circuitry
- Preheat/Ignition (PH/IGN) Mode
- Dim Mode
- Non Zero-Voltage Switching (ZVS) Protection
- Crest Factor Over-current Protection
- Fault Mode and Lamp Reset
- Component Selection
- PCB Layout Guidelines

UVLO Mode and IC Supply Circuitry

The Under-Voltage Lock-Out Mode (UVLO) is defined as the state the IC is in when V_{CC} is below the turn-on threshold of the IC, V_{CCUV+} (12.5 V, typical), and LO is above the shutdown threshold, V_{LOSD+} (8.75 V, typical). The UVLO circuit is designed to maintain an ultra-low supply current I_{QCCUV} (<250 µA), and to guarantee that the IC is fully functional before the high- and low-side output gate drivers are activated. The VCC capacitor, CVCC, is charged up from the DC bus voltage through supply resistors RVCC1 and RVCC2 (Figure 1). The values of these resistors are chosen such that VCC reaches the UVLO+ turn-on threshold voltage at the desired DC bus voltage level. Once the capacitor voltage on VCC reaches the start-up threshold, V_{CCUV+}, the IC turns on and the HO and LO gate drive outputs start oscillating. The capacitor CVCC should be large enough to hold the voltage at VCC above the V_{CCUV-} threshold until the external auxiliary supply can take over and supply the required voltage and current to the IC.

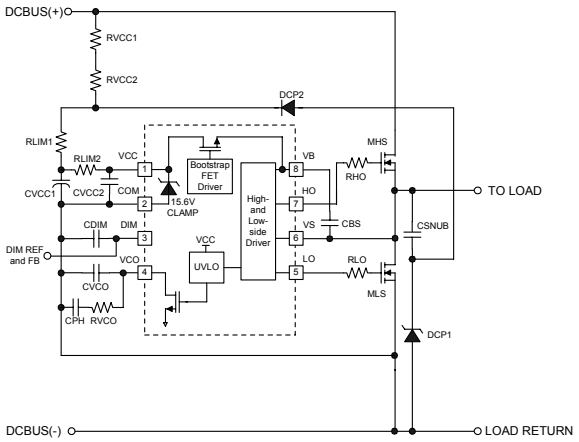


Figure 1, UVLO and supply circuitry.

An external charge pump circuit consisting of capacitor CSNUB and diodes DCP1 and DCP2, comprises the auxiliary supply voltage for the low-side circuitry (Figure 1). To limit high peak currents that can flow from the external charge pump to VCC, a zener diode (18 V, typical) should be used for the lower charge pump diode, DCP1. Also, two low-ohmic resistors (RLIM1 and RLIM2, 10 Ω each, typical) should be used together with CVCC1 and CVCC2 to further limit and filter fast current spikes to minimize resulting voltage spikes that can occur at VCC. An internal bootstrap MOSFET between VCC and VB and external supply capacitor, CBS, determine the supply voltage for the high-side driver circuitry (Figure 1). The bootstrap MOSFET is turned on when LO is 'high' and charges CBS from VCC each cycle to maintain the VB-to-VS voltage above the V_{BSUV-} threshold (8 V, typical). The value of CBS should be chosen such that the VB-to-VS voltage and ripple stays above V_{BSUV-} at all times. When VCC exceeds V_{CCUV+} for the first time, LO will first oscillate for several cycles

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until the VB-to-VS voltage exceeds the high-side UVLO rising threshold, V_{BSUV+} (9 V, typical), and the high-side driver is enabled. The capacitor CVCC should be large enough such that VCC does not reach UVLO- before HO is enabled and the charge pump supply takes over.

External gate drive resistors, RHO and RLO, are also recommended as standard design practice to limit high peak currents that can flow into or out of the HO and LO gate drive outputs.

During UVLO Mode, the high-side gate driver output, HO, is 'low' and the VCO pin is pulled down internally to COM. The low-side gate driver output, LO, is open circuit and is used as a shutdown/reset input function for automatically restarting the IC when a lamp has been removed and re-inserted. The IC includes an internal shutdown threshold, V_{LOSD+} (8.75 V, typical), and re-start logic circuit at the LO pin that is only active during UVLO mode. If VCC is above V_{CCUV+}, but the lamp is removed, the external pull-up network (RLMP1 and RLMP2) will pull LO above V_{LOSD+} and the IC will remain in UVLO mode. When the lamp is re-inserted, the lower filament of the lamp will pull LO down below V_{LOSD-} (8.5 V, typical) and the IC will exit UVLO Mode and enter Preheat/Ignition Mode.

Preheat/Ignition (PH/IGN) Mode

When VCC exceeds V_{CCUV+} and the LO pin is below V_{LOSD-}, the IC enters Preheat/Ignition Mode. An internal current source, I_{VCO} (1 µA, typical), (Figure 2) charges the external capacitor on pin VCO causing the voltage on pin VCO to start ramping up linearly. An additional quick-start current, I_{VCOQS} (50 µA, typical), is also connected to the VCO pin and charges the VCO pin initially to 0.85 V. The quick-start current charges the VCO voltage up quickly to the internal 1 to 5 V range of the internal VCO. When the VCO voltage exceeds 0.85 V the quick-start current is then disconnected internally and the VCO voltage continues to charge up with the normal frequency sweep current source, I_{VCO} (1 µA, typical) (Figure 3).

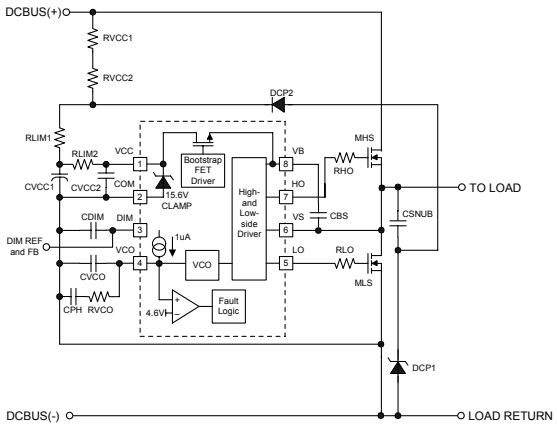


Figure 2, Preheat/Ignition Mode circuitry.

The frequency ramps down from the maximum frequency towards the resonance frequency of the high-Q ballast output stage. The lamp filaments are preheated as the lamp voltage and load current increase. The voltage on pin VCO continues to increase and the frequency keeps decreasing until the lamp ignites. If the lamp ignites successfully, the IC will then enter DIM Mode (Figure 3).

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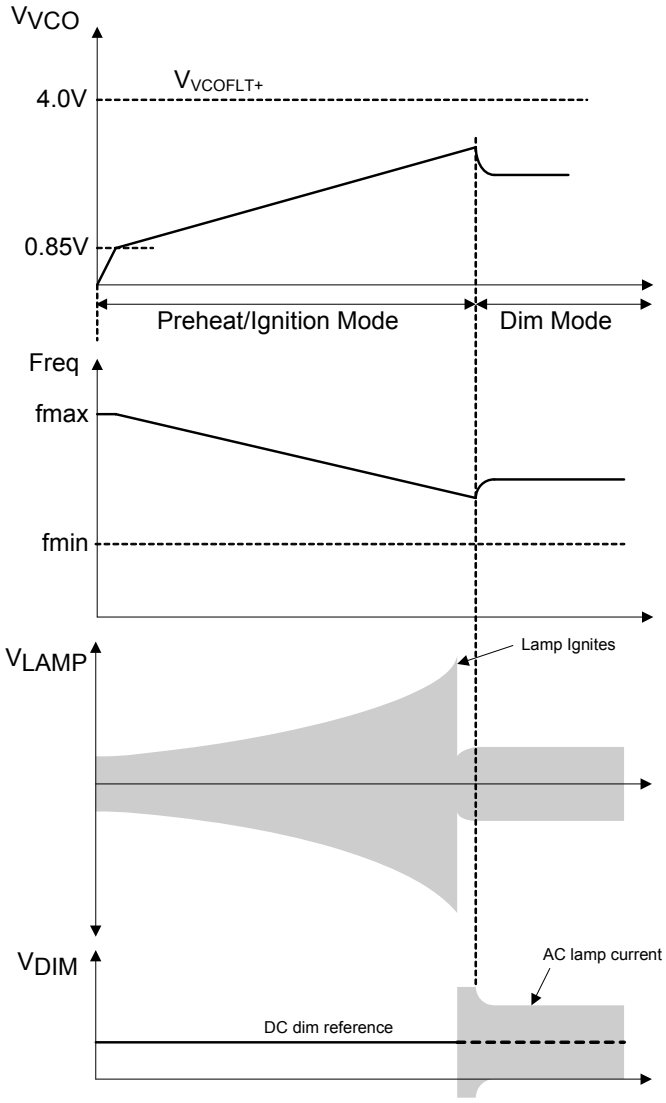


Figure 3, Preheat/Ignition/Dim Mode timing diagram.

The resonant output stage transitions to a series-L, parallel-RC circuit with the Q-value and operating point determined by the user dim level (Figure 4). If the lamp does not ignite, the voltage on pin VCO continues to increase and the frequency continues to decrease until the VCO voltage exceeds $V_{VCOFLT+}$ (4.0V, typical) and the IC enters Fault Mode and shuts down. The minimum frequency should be set below the high-Q resonance frequency of the ballast output stage to ensure that the frequency ramps through resonance for lamp ignition (Figure 4). The desired preheat time can be set by adjusting the slope of the VCO ramp with the external capacitor, CPH.

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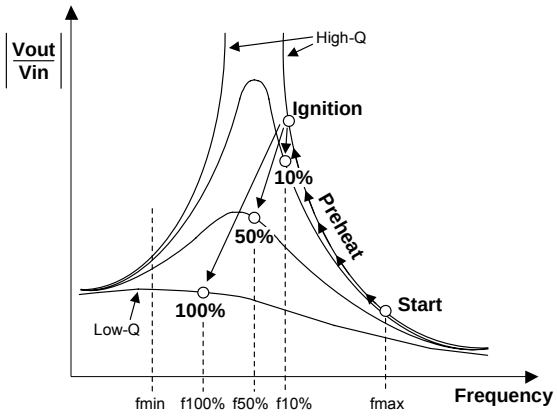


Figure 4, Resonant tank Bode plot with lamp dimming operating points.

Dim Mode

When the lamp ignites, the ballast output stage becomes a series-L, parallel-RC circuit and the AC lamp current flows through the current sensing resistor, RCS. The resulting AC voltage across resistor RCS is coupled to the DIM pin through feedback resistor, RFB (1 kΩ, typical), and feedback capacitor, CFB (0.1 µF, typical). The DIM pin voltage is a combination of the DC offset voltage provided by the user dim setting and the AC voltage that is capacitively coupled through capacitor CFB from the lamp current sensing resistor to the DIM pin. The IC enters Dim Mode when the lamp ignites and the dimming control loop becomes active. The DC+AC voltage at the DIM pin is regulated by the control loop such that the valley of the AC voltage always stays at COM. By offsetting the AC voltage with a DC reference and holding the valley of the AC voltage at COM, the amplitude of the AC voltage, and therefore the AC lamp current, is accurately controlled. When the DC reference voltage at the DIM pin is decreased for dimming, the valleys of the AC voltage are pushed below COM. The dimming control circuit increases the frequency to decrease the AC lamp current until the AC valleys at the DIM pin are at COM again. When the DC reference is increased to increase the brightness level, the valleys of the AC voltage increase above COM. The dimming control circuit decreases the frequency to increase the AC lamp current until the AC valleys at the DIM pin are at COM again. In this way, the dimming control circuit keeps the AC lamp current peak-to-peak amplitude regulated to the desired value at all DC dim level settings. Capacitor CVCO programs the speed of the dimming loop and is typically set to a low value (2.2 nF, typical) for cycle-by-cycle lamp current control. An additional compensation network is formed by RVCO (1.5 kΩ, typical) and CPH to prevent the VCO voltage from changing too much from one cycle to the next for maintaining smooth and stable dimming. A capacitor, CDIM (10 nF, typical) is also necessary from the DIM pin to COM for filtering high-frequency switching noise.
During Dim Mode, the VS-sensing circuit and non-ZVS and crest factor protection circuits are also enabled (see State Diagram, Page 11).

Non Zero-Voltage Switching (ZVS) Protection

During Dim Mode, if the voltage at the VS pin has not slewed entirely to COM during the dead-time such that there is voltage between the drain and source of the external low-side half-bridge MOSFET when LO turns-on, then the system is operating too close to, or, on the capacitive side of resonance. The result is non-ZVS capacitive-mode switching that causes high peak currents to flow in the half-bridge MOSFETs that can damage or destroy them (Figure 5). This can typically occur during a decrease of the DC bus during an AC mains interrupt or brown-out condition, lamp variations over time, driving an incorrect lamp type, or component and temperature variations. To protect against this, an internal high-voltage MOSFET is turned on at each turn-off of HO and the VS-sensing circuit measures the VS voltage at each rising edge of LO. If the VS voltage is greater than V_{ZVSTH} (4.5 V, typical), the non-ZVS control circuit will increase the frequency until ZVS is reached again. Increasing the frequency due to non-ZVS during a brown-out also ensures that

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that the ignition/preheat ramp will be reset to re-ignite the lamp reliably in case the DC bus decreases too far and the lamp extinguishes.

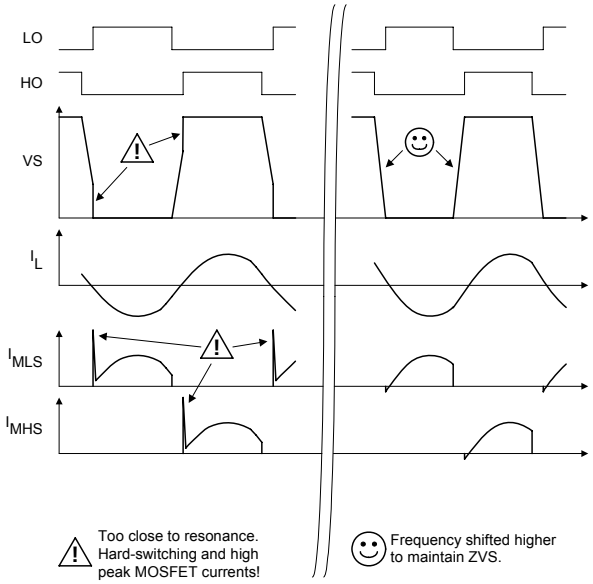


Figure 5, Non-ZVS protection timing diagram.

Crest Factor Over-current Protection

The IRS2530D uses the VS-sensing circuitry to also measure the low-side half-bridge MOSFET current for detecting an over-current fault. By using the R_{DSon} of the external low-side MOSFET for current sensing, the IC eliminates the need for an external current sensing resistor. To cancel changes in the R_{DSon} value due to temperature and MOSFET variations, the IC performs a crest factor measurement that detects when the peak current exceeds the average current by a factor of 5.5 (CSCF). Measuring the crest factor is ideal for detecting when the inductor saturates due to excessive current that occurs in the resonant tank when the frequency is too close to resonance. During Dim Mode, the crest factor over-current protection is used to detect if the filaments fail, the lamp is removed, or the lamp becomes deactivated. During each of these fault conditions, the output stage will transition to a series-LC configuration. The resonant inductor, LRES, and resonant capacitor, CRES, remain connected together to form a complete circuit due to the voltage-mode heating configuration to the lamp (see Typical Application Diagram, Page 1). The frequency will move towards resonance until the inductor saturates. The crest factor protection circuit will then detect the saturation and the IC will enter Fault Mode and shut down.

Fault Mode and Lamp Reset

During Fault Mode the internal fault latch is set, HO is off, LO is open circuit, and the IC consumes an ultra-low micro-power current (see State Diagram, Page 11). The IC can be reset with a lamp exchange (as detected by the LO pin) or a recycling of VCC below and back above the UVLO thresholds. During Fault Mode, the LO pin is open circuit and is used as an input pin for resetting the IC. If the lamp is removed, the external pull-up network at the lower lamp filament, RLMP1 and RLMP2 (see Typical Application Diagram, Page 1), will pull LO above V_{LOSD+} (8.75V, typical) and the IC will exit Fault Mode and enter UVLO mode. When the lamp is re-inserted, the lower filament of the lamp will pull LO down below V_{LOSD-} (8.5V, typical) and the IC will exit UVLO Mode and enter Preheat/Ignition Mode and restart the lamp.

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Component Selection

Proper design of the circuit schematic (see Typical Application Diagram, Page 1) and component selection is important for achieving proper ballast functionality and preventing problems. The following design procedure should be followed for determining the various programming and filtering component values:

1) Capacitor CPH programs the desired preheat/ignition time. CPH is charged up by an internal 1 µA current source at the VCO pin. The value of CPH is determined by:

$$C_{PH} = \frac{I_{VCO} \cdot t_{PH/IGN}}{V_{VCOFLT}} = \frac{1\mu A \cdot t_{PH/IGN}}{4V}$$

2) Capacitor CVCO programs the speed of the dimming feedback loop. To ensure smooth and stable dimming, CVCO should be small enough such that the dimming loop reacts to lamp current changes each switching cycle. The value of CVCO is typically fixed for most lamp types and is given as:

$$C_{VCO} = 2.2nF$$

3) Resistor RVCO and capacitor CPH provide additional compensation of the dimming loop to prevent the VCO voltage from changing too much over a given switching cycle. The value of RVCO is typically fixed for most lamp types and is given as:

$$R_{VCO} = 1.5k\Omega$$

4) Resistor RCS measures the lamp current for dimming. RCS should be kept small to minimize power losses but the peak voltage across RCS at the lowest lamp current dimming level should be above a minimum level to avoid noise problems. Using the minimum rms lamp current during dimming, a minimum allowable peak voltage level across RCS of 100 mV, and an additional factor of 5 (signal attenuation due to RFB and CDIM), the value of RCS is determined by:

$$R_{CS} = \frac{100mV}{I_{LAMP_RMS_MIN} \cdot \sqrt{2}} \times 5$$

Using the maximum rms lamp current, the power loss in resistor RCS is then determined by:

$$P_{LOSS_RCS} = (I_{LAMP_RMS_MAX})^2 \times R_{CS}$$

5) The additional feedback components include RFB for current limiting and noise filtering, CFB for DC blocking, and CDIM for noise filtering. The value of these components are typically fixed for most lamp types and are given as:

$$R_{FB} = 1k\Omega$$

$$C_{FB} = 0.1\mu F$$

$$C_{DIM} = 10nF$$

6) Capacitors CVCC2 and CBS are the low-side and high-side supply capacitors for maintaining their respective supply voltages and providing high-frequency noise filtering. These capacitors are typically fixed and are given as:

$$C_{VCC2} = C_{BS} = 0.1\mu F$$

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Component Selection (continued)

7) Resistors RVCC1 and RVCC2 provide the micro-power supply current to VCC and therefore determine the AC line input voltage where the ballast first turns on. The value of these resistors is determined by:

$$R_{VCC1} + R_{VCC2} = \frac{VAC_{ON} \cdot \sqrt{2} - VCCUV^{+}}{250uA}$$

8) The additional supply components include capacitor CVCC1 for holding up VCC until the charge pump takes over, charge pump capacitor CSNUB for providing VCC supply current, charge pump diodes DCP1 and DCP2, and limiting resistors RLIM1 and RLIM2 for preventing high currents from flowing into VCC. These components are typically fixed for most design and are given as:

$$C_{VCC1} = 1\mu F$$

$$C_{SNUB} = 1nF / 1KV$$

$$D_{CP1} = 18V / 500mW$$

$$D_{CP2} = 1N4148$$

$$R_{LIM1} = R_{LIM2} = 10\Omega$$

9) Resistors RLMP1 and RLMP2 provide the necessary pull-up signal to the LO pin for detecting the removal and insertion of the lower lamp filament. Both of these resistor should be high-ohmic to minimize current flow from VCC and to minimize current flow from the low-side filament to the LO pin. These resistor values are typically fixed and are given as:

$$R_{LMP1} = 470K\Omega$$

$$R_{LMP2} = 1M\Omega$$

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PCB Layout Guidelines

Proper care should be taken when laying out a PCB board to minimize noise effects due to high-frequency switching and to ensure proper functionality of the IRS2530D.

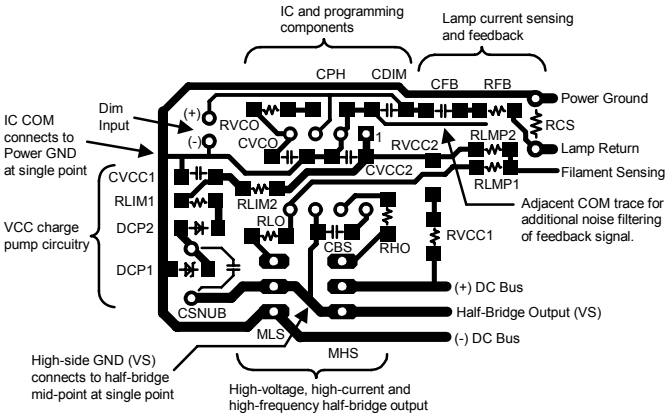


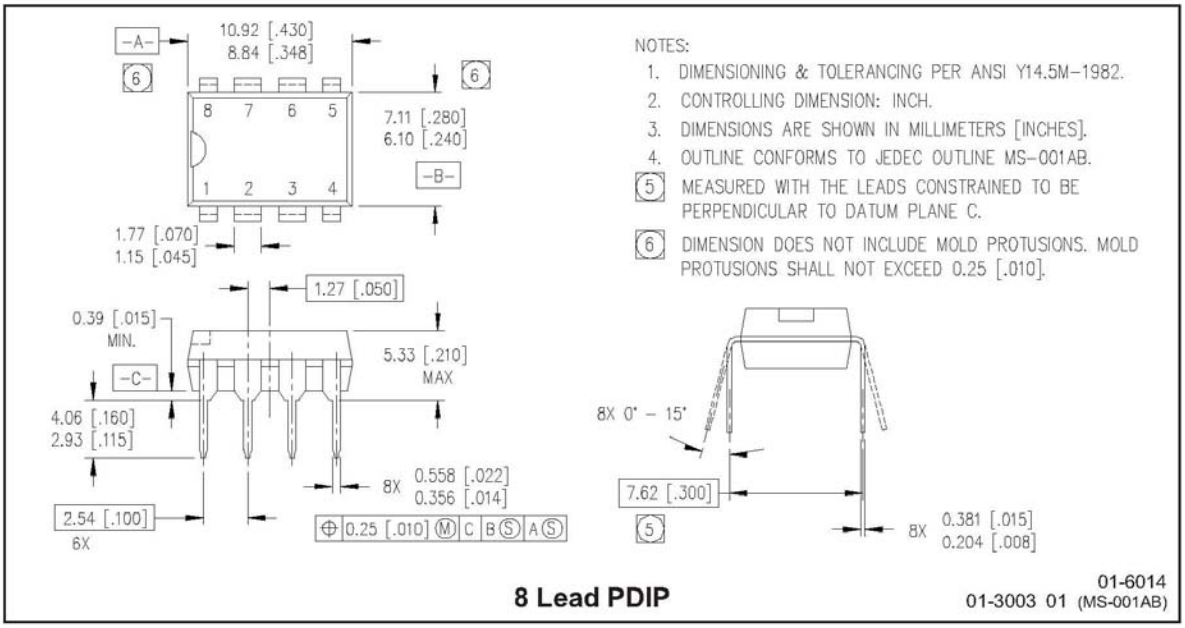
Figure 9, Typical through-hole and SMD single-layer PCB layout for Application Diagram, Page 1 (bottom copper layer shown from top view).

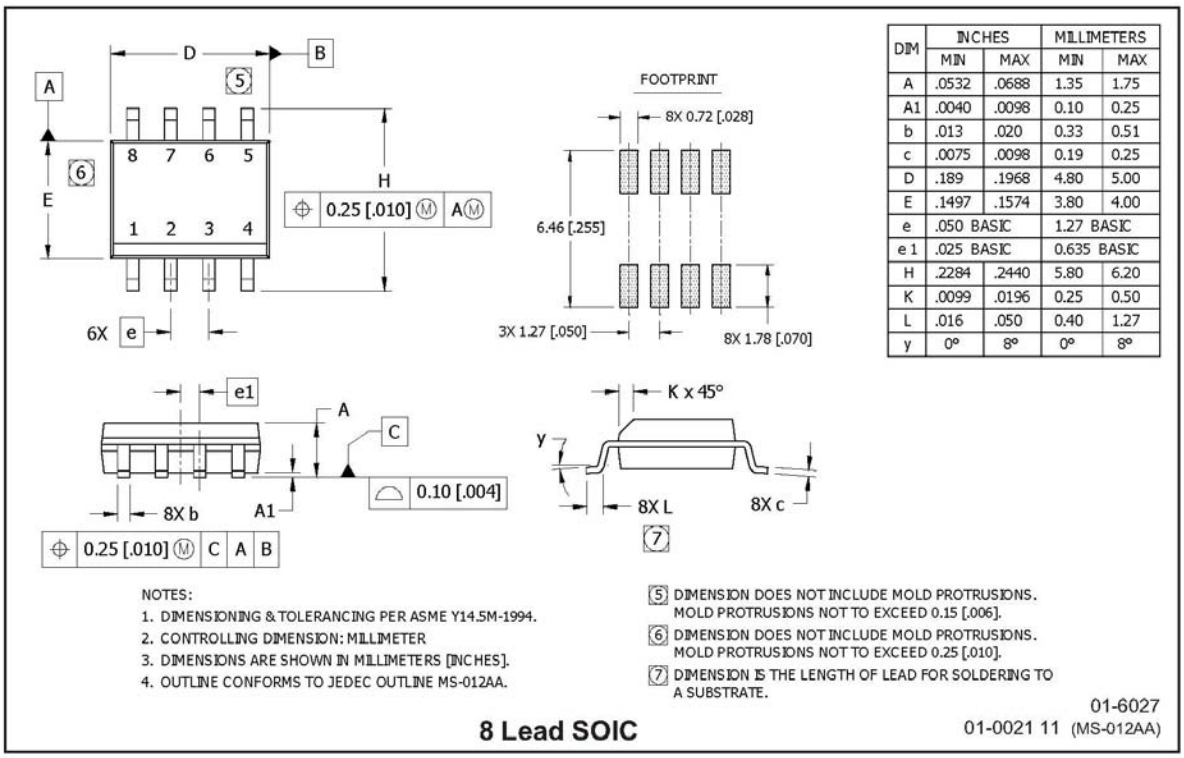
The programming components for the IC should be connected to the IC COM pin and then connected to power ground at a single point (Figure 9). The lamp current sensing feedback components (RFB, CFB) should be kept as far away as possible from the high-voltage/high-frequency half-bridge components to prevent switching noise from distorting the lamp current feedback signal. Adjacent ground traces to the feedback signals can also help reduce switching noise. In general, the following guidelines should be followed during PCB board layout:

1) Place all IC supply capacitors (CVCC2, CBS) and as close as possible to their respective supply and return pins (CVCC, CBS).
2) Place all IC programming and filter components as close as possible between their respective pins and COM (CVCO, RVCO, CPH, CDIM, CFB, RFB).
3) Connect IC COM to power GND at one connection only. Do not route power GND through the programming components or IC COM!
4) Connect high-side gate-drive ground (VS) to half-bridge mid-point at one connection only. Do not route high-side power ground through the VS components or VS pin.
5) Connect the anode of charge pump diode DCP1 to power ground. Do not connect to IC COM.
6) Use gate resistors (RLO, RHO) between all gate driver outputs and the gate of their respective power MOSFETs.
7) Use zener diode (18 V, typical) for lower charge pump diode (DCP1) and limiting resistors and capacitors (RLIM1, CVCC1, RLIM2, CVCC2) to filter high current spikes that can cause large voltage spikes to occur on VCC.

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Package Details

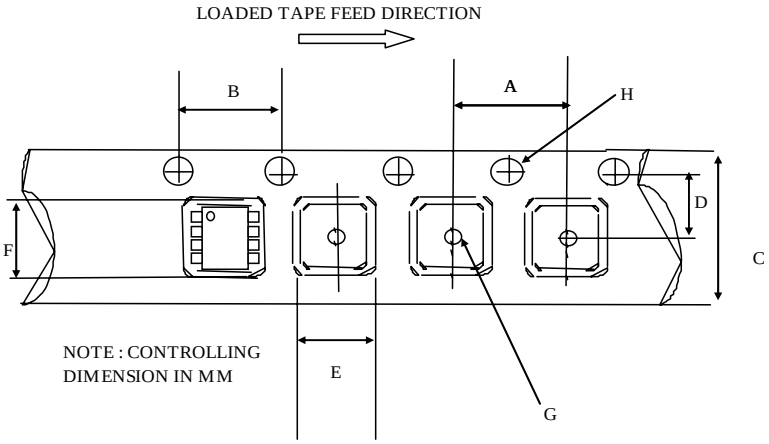




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

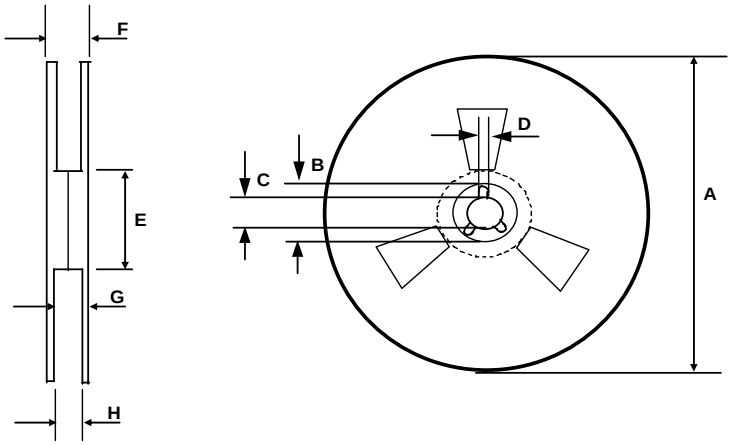
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Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

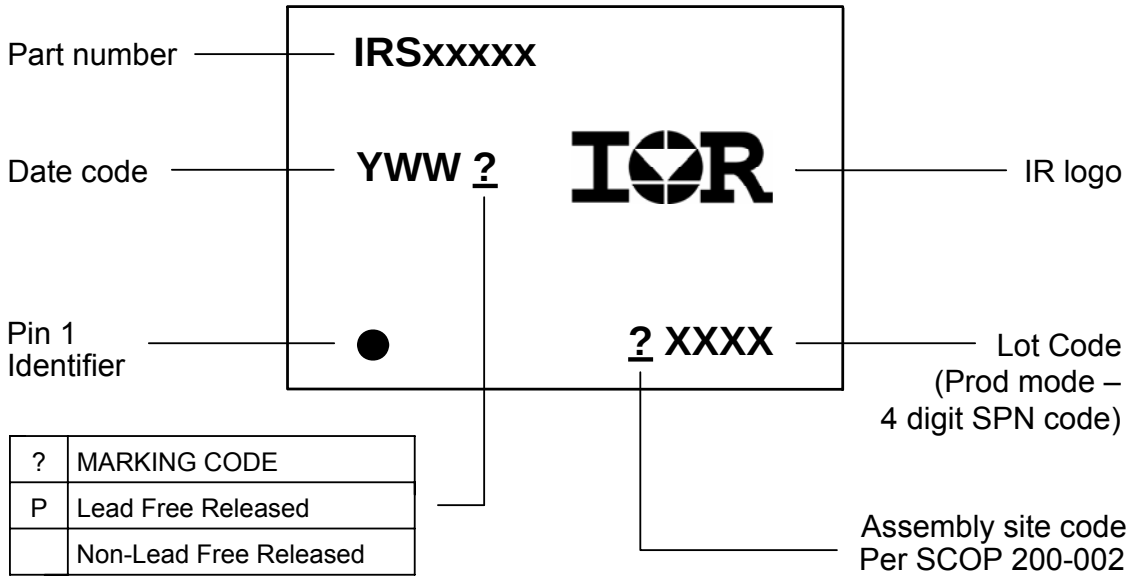


REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

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Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

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Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2530D	PDIP8	Tube/Bulk	50	IRS2530DPBF
	SOIC8N	Tube/Bulk	95	IRS2530DSPBF
		Tape and Reel	2500	IRS2530DSTRPBF

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