μPD4464
8,192 x 8-BIT STATIC CMOS RAM

Description

The μPD4464 is a high-speed 8,192-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Full CMOS storage cells with six transistors make the μPD4464 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is included for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 volts.

The μPD4464 is available in standard 28-pin plastic DIP or miniflat packaging.

Features

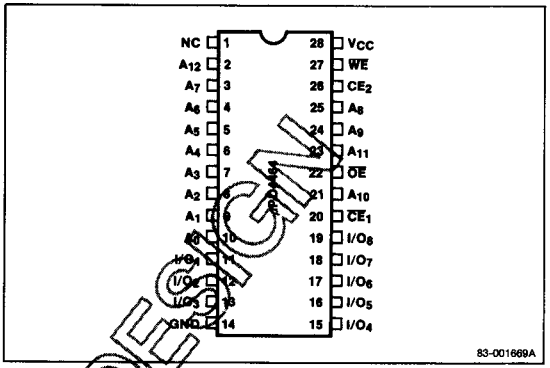
- ☐ Operating temperature range: −40 to 85 °C
- ☐ Single +5-volt power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O using three-state output
- ☐ One output enable pin and two chip enable pins for easy application
- ☐ Data retention voltage: 2 V minimum
- ☐ Standard 28-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Active Current (max)	Standby Current (max)	Package
μPD4464C-12	120 ns	40 mA	10 μA	28-pin plastic DIP
C-15	150 ns	40 mA		
C-20	200 ns	35 mA		
μPD4464C-12L	120 ns	40 mA	1 μA (at $T_A = 60$ °C)	28-pin plastic DIP
C-15L	150 ns	40 mA		
C-20L	200 ns	35 mA		
μPD4464G-12	120 ns	40 mA	10 μA	28-pin plastic miniflat
G-15	150 ns	40 mA		
G-20	200 ns	35 mA		
μPD4464G-12L	120 ns	40 mA	1 μA (at $T_A = 60$ °C)	28-pin plastic miniflat
G-15L	150 ns	40 mA		
G-20L	200 ns	35 mA		

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0–A_{12}	Address inputs
I/O_1–I/O_8	Data inputs/outputs
$\overline{CE}_1$	Chip enable (active low)
CE_2	Chip enable (active high)
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Power supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, V_{OUT} (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	−40 to 85 °C
Storage temperature, T_{STG}	−55 to 125 °C
Power dissipation, P_D	1.0 W

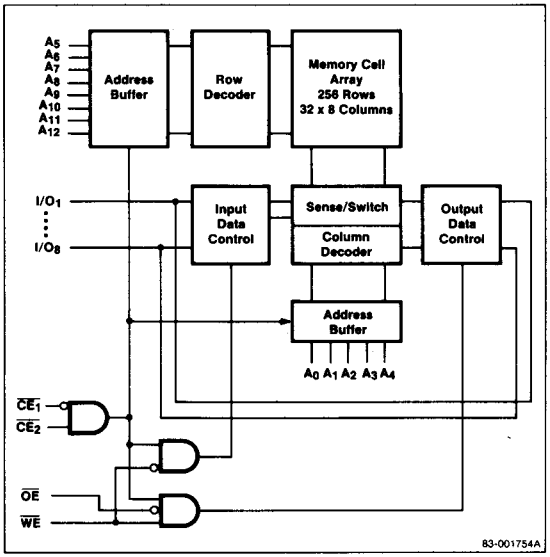
Notes:

(1) −3.0 V minimum (pulse width = 50 ns maximum)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

NOT FOR NEW DESIGN

Block Diagram



Recommended DC Operating Conditions

$T_A = -40$ to 85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC}+0.5$	V

Notes:

(1) −3.0 V minimum (pulse width = 50 ns maximum)

Capacitance

$T_A = 25°C$; f = 1.0 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
I/O capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

DC Characteristics

$T_A = -40$ to 85°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0$ V to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0$ V to V_{CC}; $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			40 (Note 1)	mA	$\overline{CE} = V_{IL}$; $CE_2 = V_{IH}$; $I_{I/O} = 0$ (min cycle)
	I_{CCA2}		5	10	mA	$\overline{CE} = V_{IL}$; $CE_2 = V_{IH}$; $I_{I/O} = 0$ (dc current)
Standby supply current	I_{CCS1}		0.004	10 (Note 2)	μA	$\overline{CE} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V
	I_{CCS2}		0.004	10 (Note 2)	μA	$CE_2 \leq 0.2$ V
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2.1$ mA
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA

Notes:

(1) μPD4464-20/-20L: 35 mA max

(2) μPD4464-12L/-15L/-20L: 1.0 μA max (−40 to 60°C)
0.2 μA max (−40 to 25°C)

Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D_{OUT} disabled	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care

AC Characteristics

$T_A = -40$ to 85°C; $V_{CC} = +5.0$ V ±10%

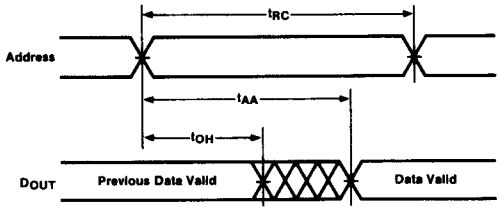
Parameter	Symbol	Limits μPD4464-12 Min	Limits μPD4464-12 Max	Limits μPD4464-15 Min	Limits μPD4464-15 Max	Limits μPD4464-20 Min	Limits μPD4464-20 Max	Unit	Test Conditions (Note 1)
Read Cycle									
Read cycle time	t_{RC}	120		150		200		ns	
Address access time	t_{AA}		120		150		200	ns	
$\overline{CE}_1$ access time	t_{CO1}		120		150		200	ns	
CE_2 access time	t_{CO2}		120		150		200	ns	
Output enable to output valid	t_{OE}		60		75		100	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
Chip enable ($\overline{CE}_1$) to output in low-Z	t_{LZ1}	10		10		100		ns	
Chip enable (CE_2) to output in low-Z	t_{LZ2}	10		10		10		ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	
Chip enable ($\overline{CE}_1$) to output in high-Z	t_{HZ1}		40		75		100	ns	
Chip enable (CE_2) to output in high-Z	t_{HZ2}		40		75		100	ns	
Output enable to output in high-Z	t_{OHZ}		40		60		80	ns	
Write Cycle									
Write cycle time	t_{WC}	120		150		200		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	85		130		180		ns	
Chip enable (CE_2) to end of write	t_{CW_2}	85		130		180		ns	
Address valid to end of write	t_{AW}	85		130		180		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	70		100		140		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	50		70		80		ns	
Data hold time	t_{DH}	5		5		5		ns	
Write enable to output in high-Z	t_{WHZ}		40		75		100	ns	
Output active from end of write	t_{OW}	5		10		10		ns	

Notes:

(1) Input pulse levels = 0.8 V to 2.4 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; output load = 1 TTL gate and $C_L = 100$ pF.

Timing Waveforms

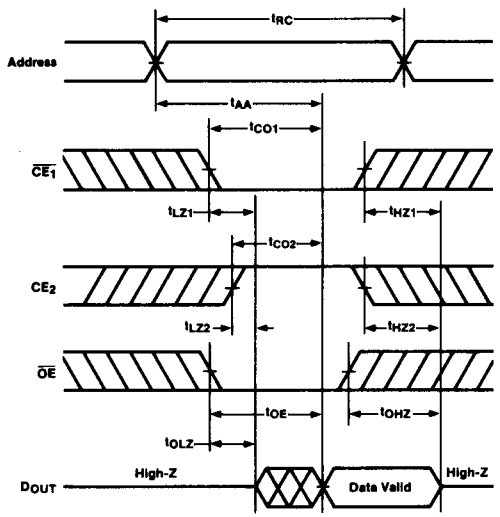
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The device is continuously selected; $\overline{CE_1} = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

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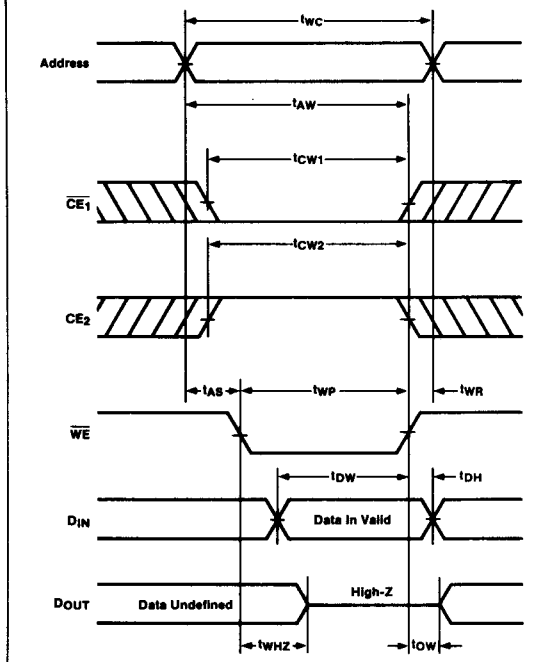
Read Cycle No. 2 (Chip Enable Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The address inputs are valid prior to or coincident with the $\overline{CE_1}$ transition low and the CE_2 transition high.

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Write Cycle No. 1 ($\overline{WE}$-Controlled)

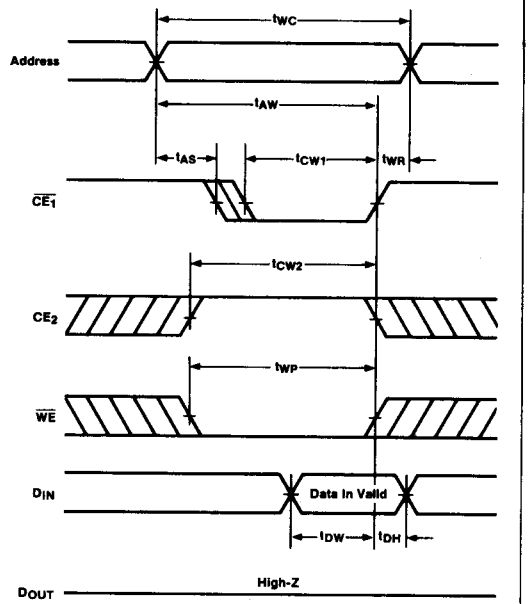


Note:
[1] A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE_1}$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.
[3] If $\overline{OE}$ is high the I/O pins remain in a high impedance state.

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Timing Waveforms (cont)

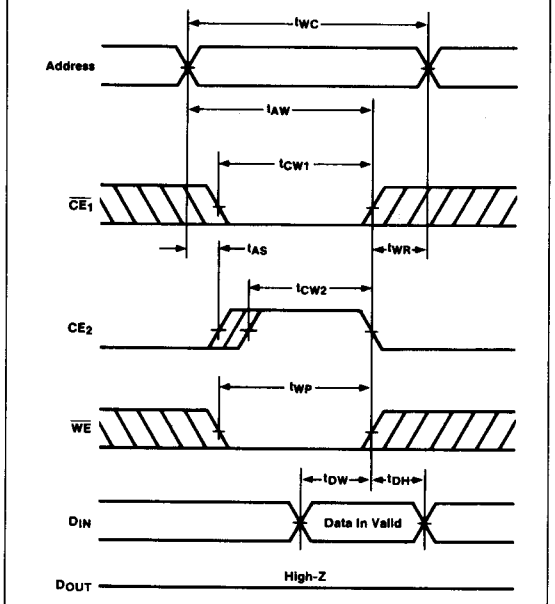
Write Cycle No. 2 ($\overline{CE}_1$-Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

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Write Cycle No. 3 (CE_2-Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

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Low V_{CC} Data Retention Characteristics

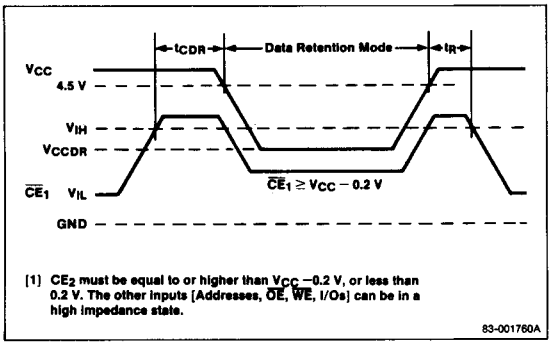
$T_A = -40$ to 85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V
	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		0.003	10 (Note 1)	μA	$V_{CC} = 3.0$ V; $\overline{CE}_1 \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V
	I_{CCDR2}		0.003	10 (Note 1)	μA	$V_{CC} = 3.0$ V; $CE_2 \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) μPD4464-12L/-15L/-20L: 1.0 μA max (−40 to 60°C)
0.2 μA max (−40 to 25°C)

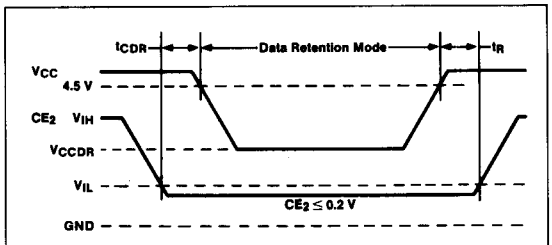
Data Retention ($\overline{CE}_1$-Controlled)



[1] CE_2 must be equal to or higher than V_{CC} −0.2 V, or less than 0.2 V. The other inputs [Addresses, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high impedance state.

83-001760A

Data Retention (CE_2-Controlled)



Note:

(1) The other inputs (Addresses, $\overline{CE}_1$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

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