

0.5A HIGH-SPEED MOSFET DRIVERS

FEATURES

- Latch-Up Protected: Will Withstand 500mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected4kV
- High Peak Output Current 0.5A
- Wide Operating Range 4.5V to 16V
- High Capacitive Load Drive Capability 500pF in 25nsec
- Short Delay Time 35nsec Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Delay Times
- Low Supply Current
 - With Logic “1” Input 500μA
 - With Logic “0” Input 150μA
- Low Output Impedance 16Ω
- Pinout Same as TC1411/12/13

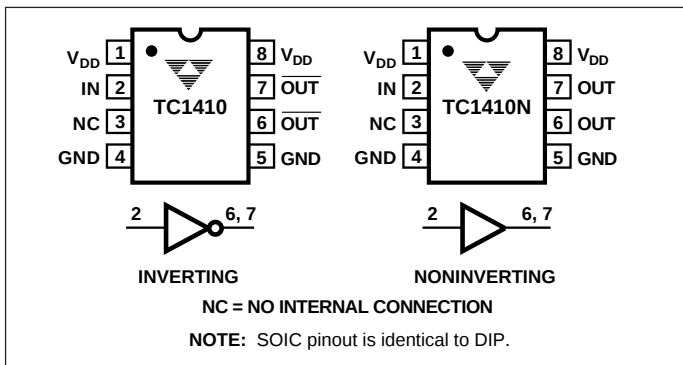
GENERAL DESCRIPTION

The TC1410/1410N are 0.5V CMOS buffer/drivers . They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1410/1410N can easily switch 500pF gate capacitance in 25nsec with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater accuracy.

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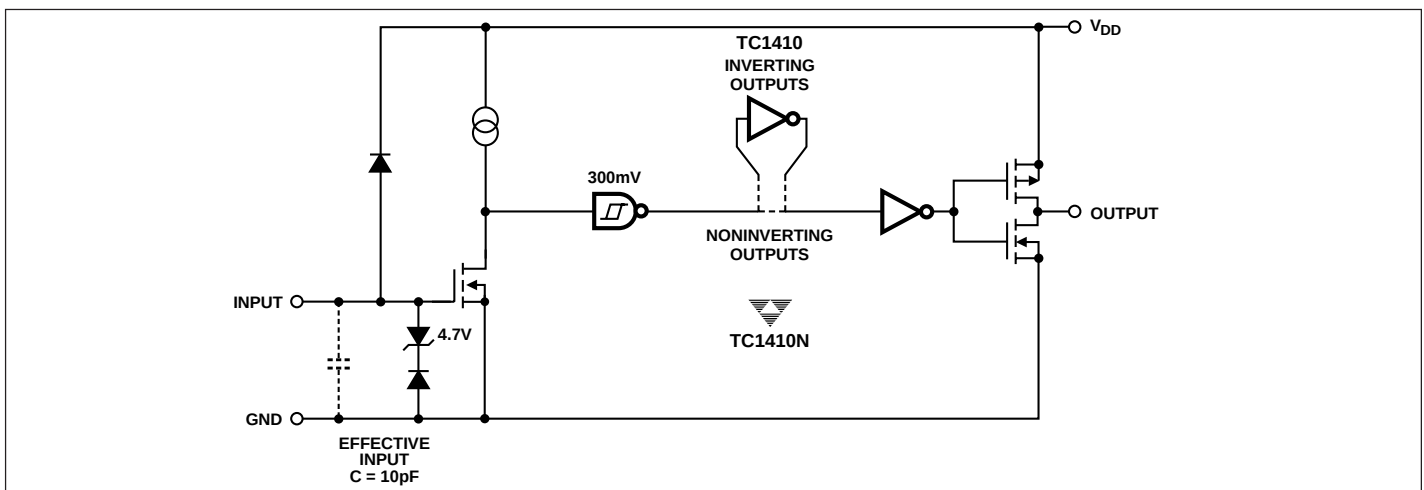
PIN CONFIGURATIONS



ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1410COA	8-Pin SOIC	0°C to +70°C
TC1410CPA	8-Pin Plastic DIP	0°C to +70°C
TC1410EOA	8-Pin SOIC	– 40°C to +85°C
TC1410EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC1410NCOA	8-Pin SOIC	0°C to +70°C
TC1410NCPA	8-Pin Plastic DIP	0°C to +70°C
TC1410NEOA	8-Pin SOIC	– 40°C to +85°C
TC1410NEPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC1410 TC1410N

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	+20V
Input Voltage, IN A or IN B. ($V_{DD} + 0.3V$) to (GND – 5.0V)	
Maximum Chip Temperature	+150°C
Storage Temperature Range	– 65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Package Thermal Resistance	
CerDIP $R_{\theta J-A}$	150°C/W
CerDIP $R_{\theta J-C}$	50°C/W
PDIP $R_{\theta J-A}$	125°C/W
PDIP $R_{\theta J-C}$	42°C/W
SOIC $R_{\theta J-A}$	155°C/W
SOIC $R_{\theta J-C}$	45°C/W

Operating Temperature Range

C Version	0°C to +70°C
E Version	– 40°C to +85°C

Power Dissipation ($T_A \leq 70^\circ\text{C}$)

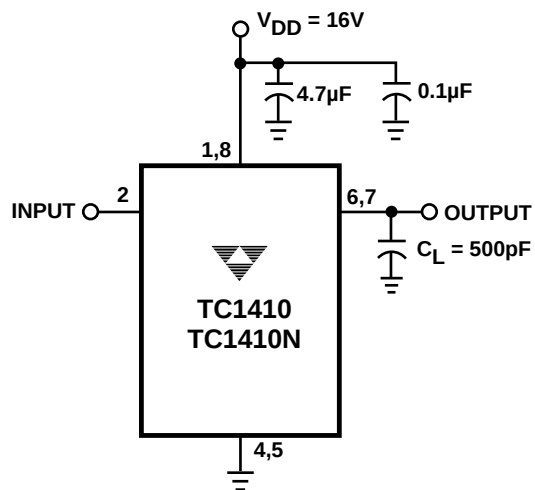
Plastic DIP	730mW
CerDIP	800mW
SOIC	470mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

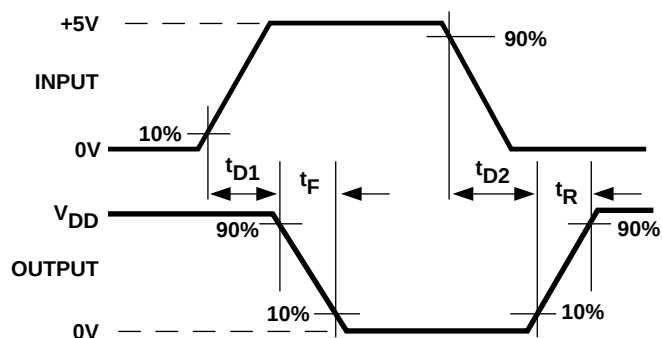
ELECTRICAL CHARACTERISTICS: Over operating temperature range with $4.5V \leq V_{DD} \leq 16V$, unless otherwise specified. Typical values are measured at $T_A = 25^\circ\text{C}$; $V_{DD} = 16V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.0	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \leq V_{IN} \leq V_{DD}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $T_A = 25^\circ\text{C}$	– 1 – 10	—	1 10	μA
Output						
V_{OH}	High Output Voltage	DC Test $V_{DD} - 0.025$	—	—	V	
V_{OL}	Low Output Voltage	DC Test	—	—	0.025	V
R_O	Output Resistance	$V_{DD} = 16V$, $I_O = 10\text{mA}$ $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— — —	16 20 20	22 28 28	Ω
I_{PK}	Peak Output Current	$V_{DD} = 16V$	—	0.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle $\leq 2\%$ $t \leq 300 \mu\text{sec}$ $V_{DD} = 16V$	0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1 $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— — —	25 27 29	35 40 40	nsec
t_F	Fall Time	Figure 1 $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— — —	25 27 29	35 40 40	nsec
t_{D1}	Delay Time	Figure 1 $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— — —	30 33 35	40 45 45	nsec
t_{D2}	Delay Time	Figure 1 $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— — —	30 33 35	40 45 45	nsec
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ $V_{IN} = 0V$ $V_{DD} = 16V$	— —	0.5 0.1	1.0 0.15	mA

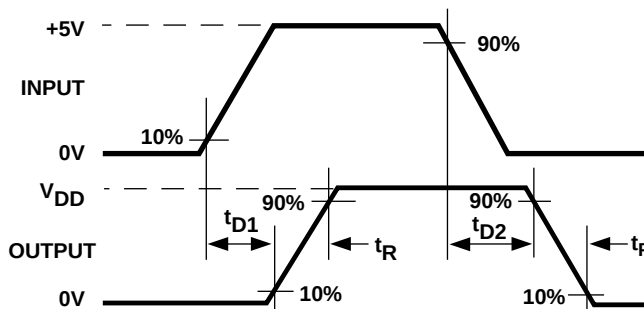
NOTE: 1. Switching times are guaranteed by design.



INPUT: 100 kHz, square wave,
 $t_{RISE} = t_{FALL} \leq 10ns$

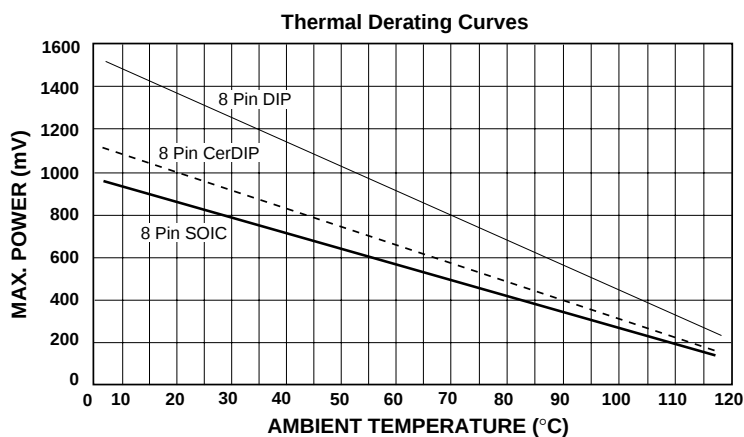


Inverting Driver
TC1410



Noninverting Driver
TC1410N

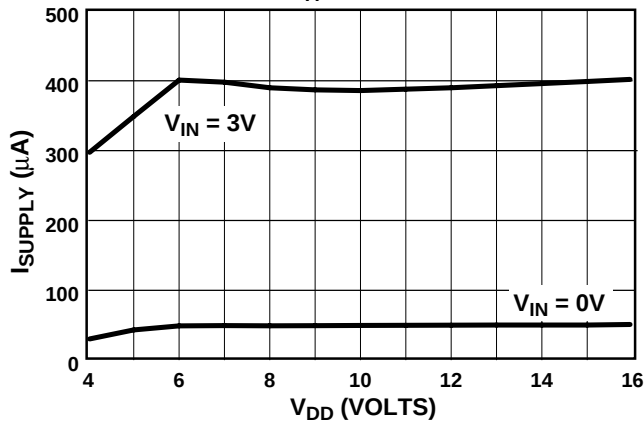
Figure 1. Switching Time Test Circuit



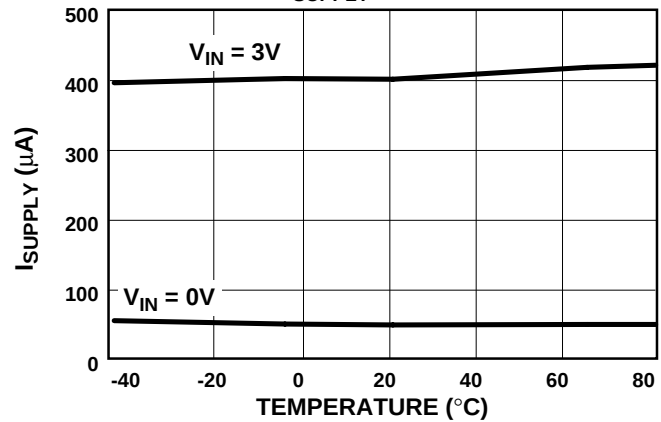
TC1410 TC1410N

TYPICAL CHARACTERISTICS

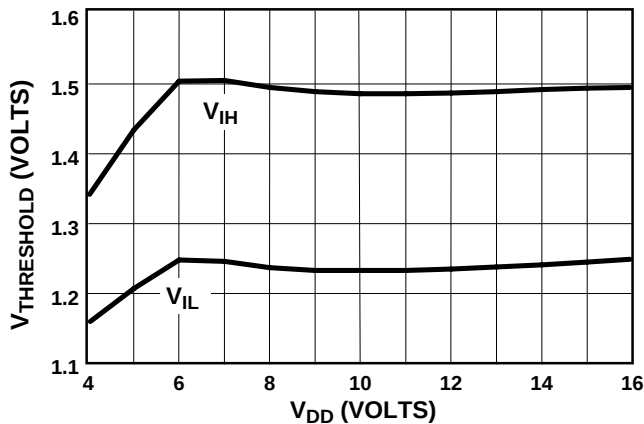
Quiescent Supply Current
vs. Supply Voltage
 $T_A = 25^\circ\text{C}$



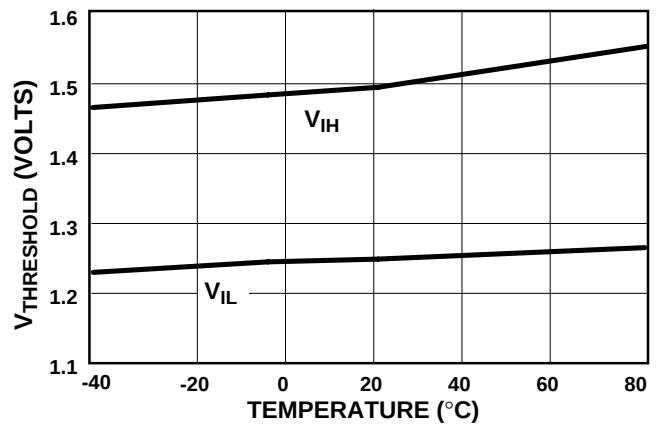
Quiescent Supply Current
vs. Temperature
 $V_{\text{SUPPLY}} = 16\text{V}$



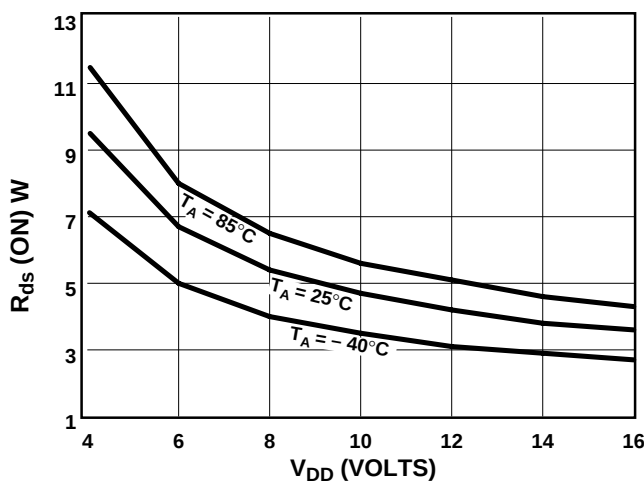
Input Threshold
vs. Supply Voltage
 $T_A = 25^\circ\text{C}$



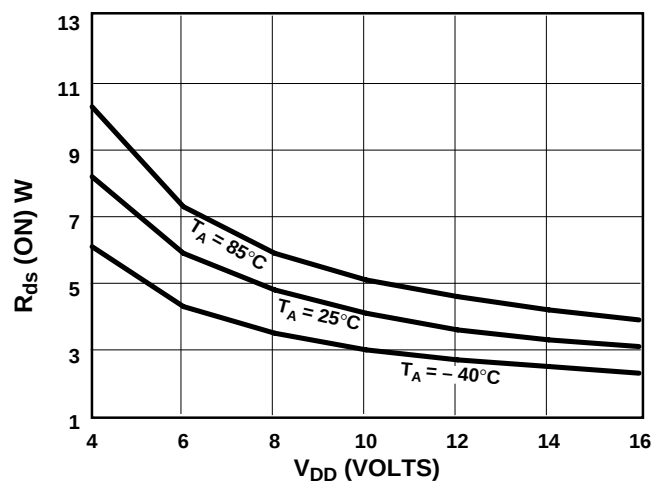
Input Threshold
vs. Temperature
 $V_{\text{SUPPLY}} = 16\text{V}$



High-State Output Resistance

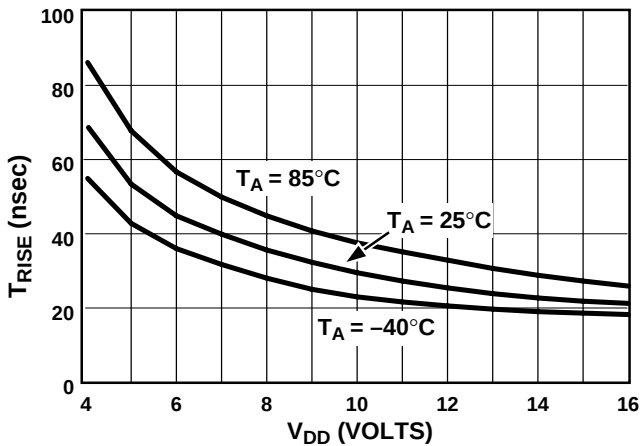


Low-State Output Resistance

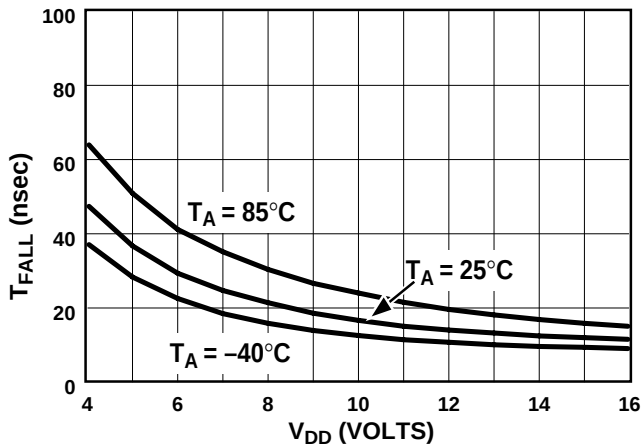


TYPICAL CHARACTERISTICS (Cont.)

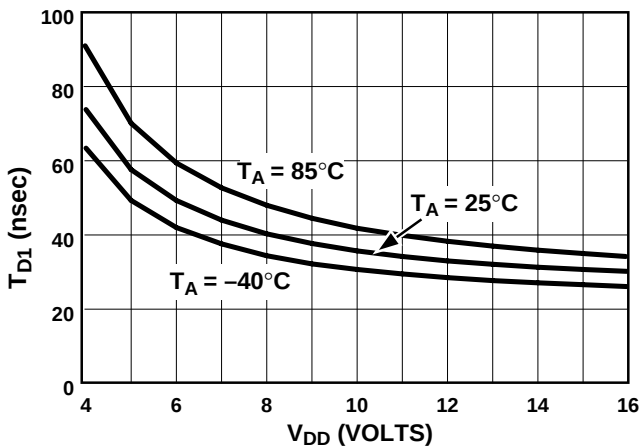
Rise Time vs. Supply Voltage
 $C_{LOAD} = 500pF$



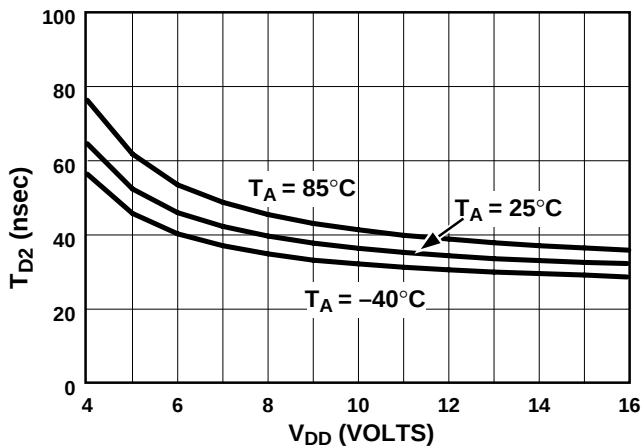
Fall Time vs. Supply Voltage
 $C_{LOAD} = 500pF$



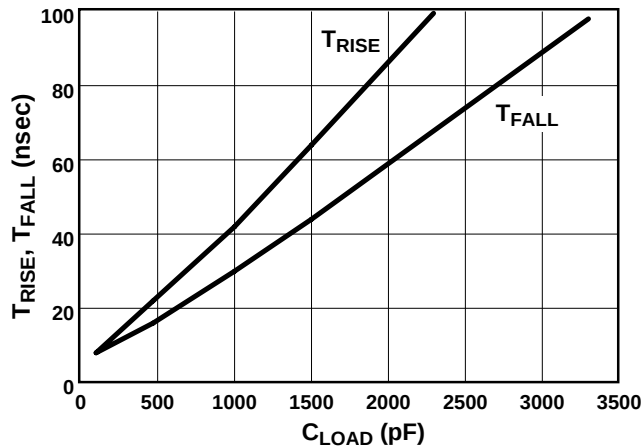
T_{D1} Propagation Delay vs. Supply Voltage
 $C_{LOAD} = 500pF$



T_{D2} Propagation Delay vs. Supply Voltage
 $C_{LOAD} = 500pF$



Rise and Fall Times vs. Capacitive Load
 $T_A = 25^\circ C, V_{DD} = 16V$



Propagation Delays vs. Capacitive Load
 $T_A = 25^\circ C, V_{DD} = 16V$

