



### GENERAL DESCRIPTION



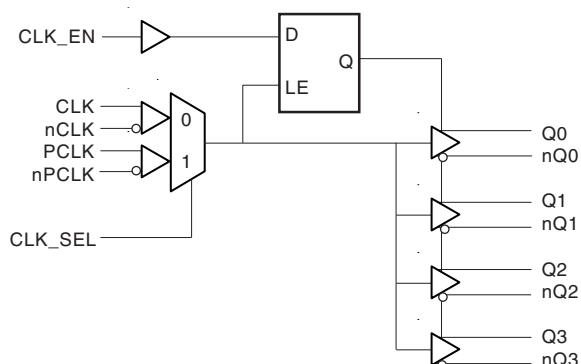
The ICS8523I is a low skew, high performance 1-to-4 Differential-to-HSTL fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8523I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8523I ideal for those applications demanding well defined performance and repeatability.

### FEATURES

- 4 differential HSTL compatible outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, HSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to HSTL levels with resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.6ns (maximum)
- 3.3V core, 1.8V output operating supply
- Lead-Free package available
- -40°C to 85°C ambient operating temperature

### BLOCK DIAGRAM



### PIN ASSIGNMENT

|         |    |    |      |
|---------|----|----|------|
| GND     | 1  | 20 | Q0   |
| CLK_EN  | 2  | 19 | nQ0  |
| CLK_SEL | 3  | 18 | VDDO |
| CLK     | 4  | 17 | Q1   |
| nCLK    | 5  | 16 | nQ1  |
| PCLK    | 6  | 15 | Q2   |
| nPCLK   | 7  | 14 | nQ2  |
| nc      | 8  | 13 | VDDO |
| nc      | 9  | 12 | Q3   |
| VDD     | 10 | 11 | nQ3  |

**ICS8523I**  
**20-Lead TSSOP**  
6.5mm x 4.4mm x 0.92mm body package  
**G Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

| Number | Name             | Type   |          | Description                                                                                                                                                                |
|--------|------------------|--------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1      | GND              | Power  |          | Power supply ground.                                                                                                                                                       |
| 2      | CLK_EN           | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 3      | CLK_SEL          | Input  | Pulldown | Clock select input. When HIGH, selects differential PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTTL interface levels.                              |
| 4      | CLK              | Input  | Pulldown | Non-inverting differential clock input.                                                                                                                                    |
| 5      | nCLK             | Input  | Pullup   | Inverting differential clock input.                                                                                                                                        |
| 6      | PCLK             | Input  | Pulldown | Non-inverting differential LVPECL clock input.                                                                                                                             |
| 7      | nPCLK            | Input  | Pullup   | Inverting differential LVPECL clock input.                                                                                                                                 |
| 8, 9   | nc               | Unused |          | No connect.                                                                                                                                                                |
| 10     | V <sub>DD</sub>  | Power  |          | Core supply pin.                                                                                                                                                           |
| 11, 12 | nQ3, Q3          | Output |          | Differential output pair. HSTL interface levels.                                                                                                                           |
| 13, 18 | V <sub>DDO</sub> | Power  |          | Output supply pins.                                                                                                                                                        |
| 14, 15 | nQ2, Q2          | Output |          | Differential output pair. HSTL interface levels.                                                                                                                           |
| 16, 17 | nQ1, Q1          | Output |          | Differential output pair. HSTL interface levels.                                                                                                                           |
| 19, 20 | nQ0, Q0          | Output |          | Differential output pair. HSTL interface levels.                                                                                                                           |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | KΩ    |



**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Inputs |         |                 | Outputs       |                |
|--------|---------|-----------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0:Q3         | nQ0:nQ3        |
| 0      | 0       | CLK, nCLK       | Disabled; LOW | Disabled; HIGH |
| 0      | 1       | PCLK, nPCLK     | Disabled; LOW | Disabled; HIGH |
| 1      | 0       | CLK, nCLK       | Enabled       | Enabled        |
| 1      | 1       | PCLK, nPCLK     | Enabled       | Enabled        |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

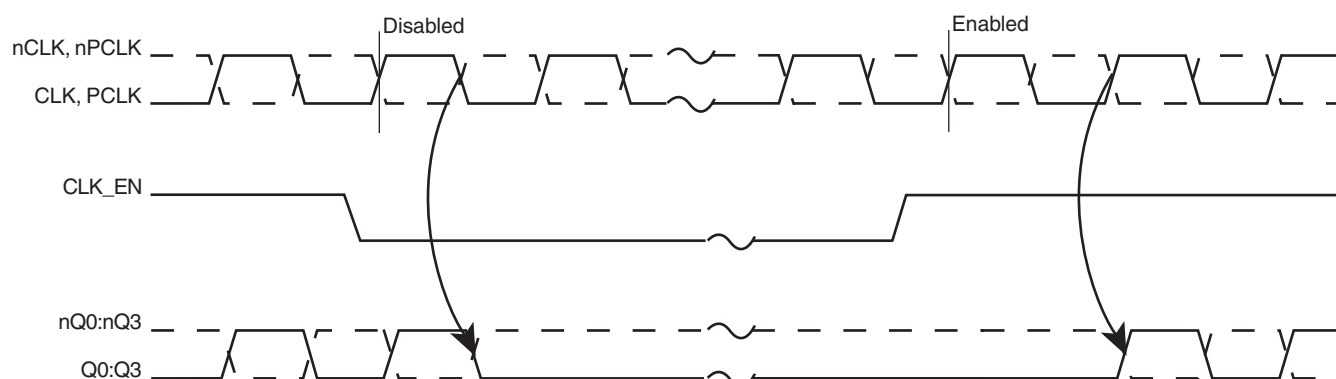


**FIGURE 1. CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs         |                | Outputs |         | Input to Output Mode         | Polarity      |
|----------------|----------------|---------|---------|------------------------------|---------------|
| CLK or PCLK    | nCLK or nPCLK  | Q0:Q3   | nQ0:nQ3 |                              |               |
| 0              | 0              | LOW     | HIGH    | Differential to Differential | Non Inverting |
| 1              | 1              | HIGH    | LOW     | Differential to Differential | Non Inverting |
| 0              | Biased; NOTE 1 | LOW     | HIGH    | Single Ended to Differential | Non Inverting |
| 1              | Biased; NOTE 1 | HIGH    | LOW     | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0              | HIGH    | LOW     | Single Ended to Differential | Inverting     |
| Biased; NOTE 1 | 1              | LOW     | HIGH    | Single Ended to Differential | Inverting     |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".



#### ABSOLUTE MAXIMUM RATINGS

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Power Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Power Supply Voltage |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current        |                 |         |         | 55      | mA    |

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter          | Test Conditions | Minimum                           | Typical | Maximum        | Units   |
|----------|--------------------|-----------------|-----------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage | CLK_EN, CLK_SEL | 2                                 |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  | CLK_EN, CLK_SEL | -0.3                              |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | CLK_EN          | $V_{DD} = V_{IN} = 3.465V$        |         | 5              | $\mu A$ |
|          |                    | CLK_SEL         | $V_{DD} = V_{IN} = 3.465V$        |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK_EN          | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |                | $\mu A$ |
|          |                    | CLK_SEL         | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5      |                | $\mu A$ |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                               | Test Conditions | Minimum                           | Typical | Maximum         | Units   |
|-----------|-----------------------------------------|-----------------|-----------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                      | nCLK            | $V_{DD} = V_{IN} = 3.465V$        |         | 5               | $\mu A$ |
|           |                                         | CLK             | $V_{DD} = V_{IN} = 3.465V$        |         | 150             | $\mu A$ |
| $I_{IL}$  | Input Low Current                       | nCLK            | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |                 | $\mu A$ |
|           |                                         | CLK             | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5      |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage              |                 | 0.15                              |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1, 2 |                 | 0.5                               |         | $V_{DD} - 0.85$ | V       |

NOTE 1: For single ended applications the maximum input voltage for CLK and nCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                            | Test Conditions | Minimum                           | Typical | Maximum  | Units   |
|-----------|--------------------------------------|-----------------|-----------------------------------|---------|----------|---------|
| $I_{IH}$  | Input High Current                   | PCLK            | $V_{DD} = V_{IN} = 3.465V$        |         | 150      | $\mu A$ |
|           |                                      | nPCLK           | $V_{DD} = V_{IN} = 3.465V$        |         | 5        | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | PCLK            | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5      |          | $\mu A$ |
|           |                                      | nPCLK           | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |          | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.3                               |         | 1        | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | 1.5                               |         | $V_{DD}$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications the maximum input voltage for PCLK and nPCLK is  $V_{DD} + 0.3V$ .

**TABLE 4D. HSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol      | Parameter                            | Test Conditions | Minimum                                  | Typical | Maximum                                  | Units |
|-------------|--------------------------------------|-----------------|------------------------------------------|---------|------------------------------------------|-------|
| $V_{OH}$    | Output High Voltage;<br>NOTE 1       |                 | 0.9                                      |         | 1.4                                      | V     |
| $V_{OL}$    | Output Low Voltage;<br>NOTE 1        |                 | 0                                        |         | 0.4                                      | V     |
| $V_{OX}$    | Output Crossover Voltage             |                 | $40\% \times (V_{OH} - V_{OL}) + V_{OL}$ |         | $60\% \times (V_{OH} - V_{OL}) + V_{OL}$ | V     |
| $V_{SWING}$ | Peak-to-Peak<br>Output Voltage Swing |                 | 0.6                                      |         | 1.3                                      | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to ground.

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol       | Parameter                    | Test Conditions    | Minimum | Typical | Maximum | Units |
|--------------|------------------------------|--------------------|---------|---------|---------|-------|
| $f_{MAX}$    | Output Frequency             |                    |         |         | 650     | MHz   |
| $t_{PD}$     | Propagation Delay; NOTE 1    | $f \leq 650MHz$    | 1.0     |         | 1.6     | ns    |
| $t_{sk(o)}$  | Output Skew; NOTE 2, 4       |                    |         |         | 50      | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 |                    |         |         | 250     | ps    |
| $t_R$        | Output Rise Time             | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| $t_F$        | Output Fall Time             | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| odc          | Output Duty Cycle            |                    | 45      |         | 55      | %     |

All parameters measured at 500MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

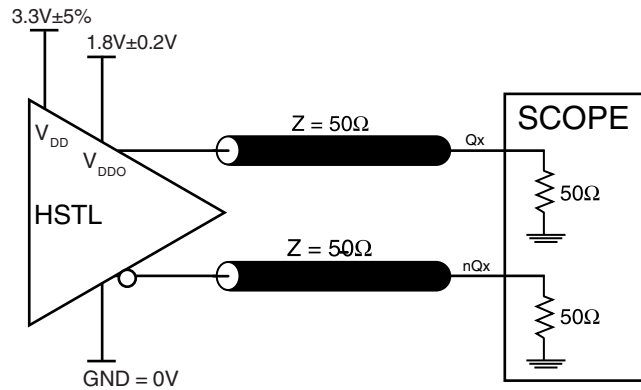
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

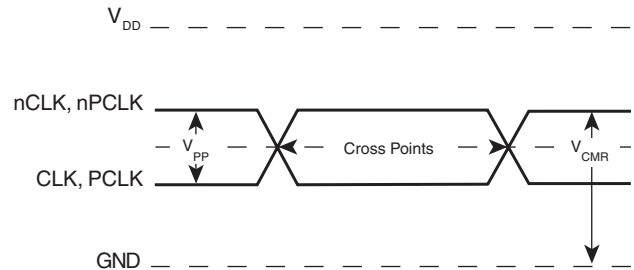
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



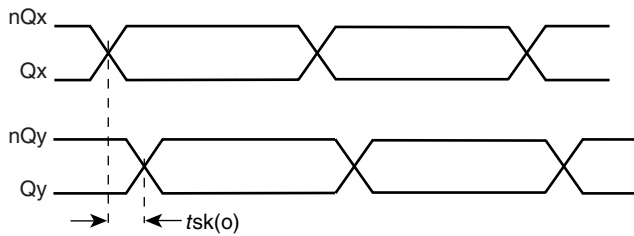
## PARAMETER MEASUREMENT INFORMATION



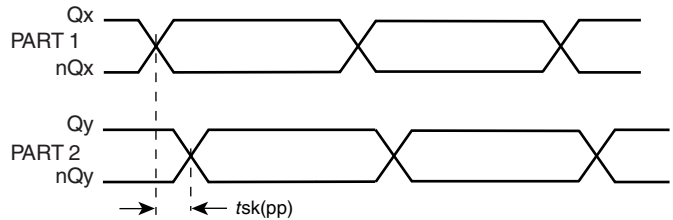
**3.3V/1.8V Output Load AC Test Circuit**



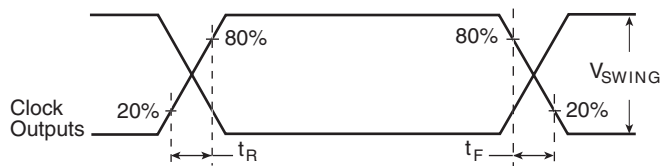
**DIFFERENTIAL INPUT LEVEL**



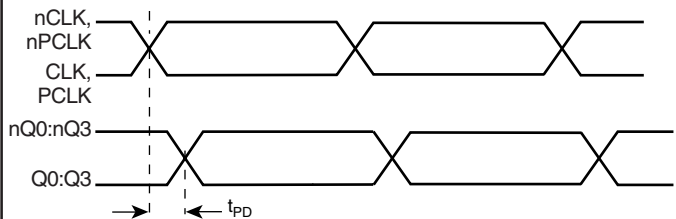
**OUTPUT SKEW**



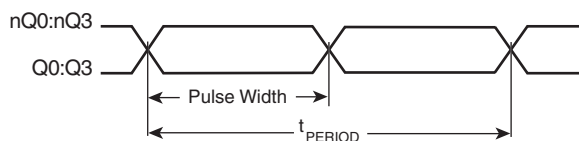
**PART-TO-PART SKEW**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



**odc &  $t_{PERIOD}$**

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

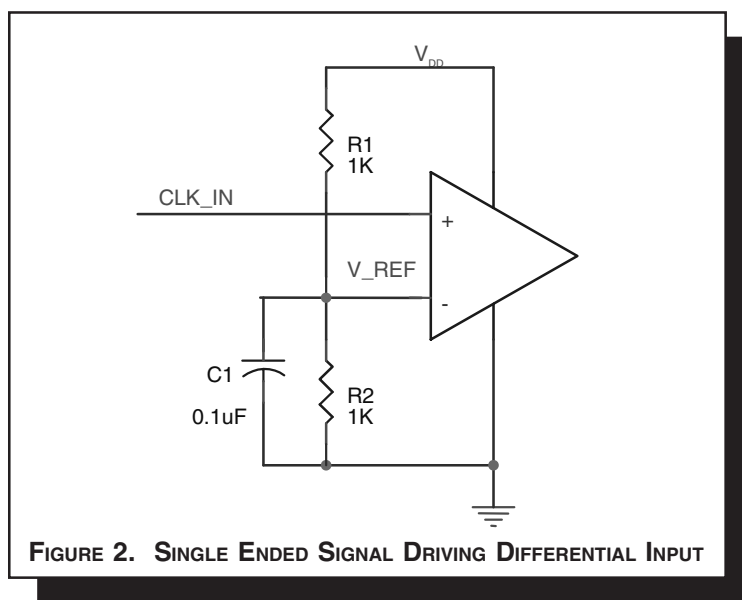


## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin.

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .





### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSSL and other differential signals. Both  $V_{\text{SWING}}$  and  $V_{\text{OH}}$  must meet the  $V_{\text{PP}}$  and  $V_{\text{CMR}}$  input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

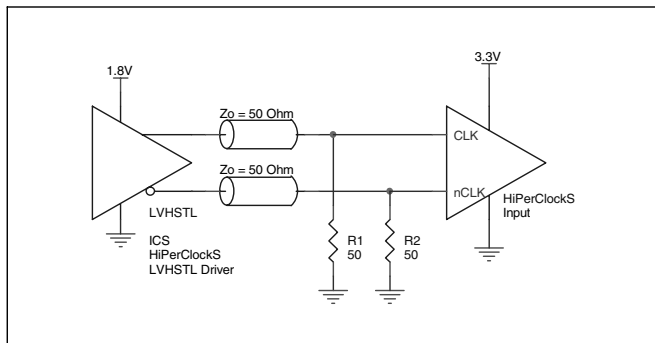


**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS HSTL DRIVER**

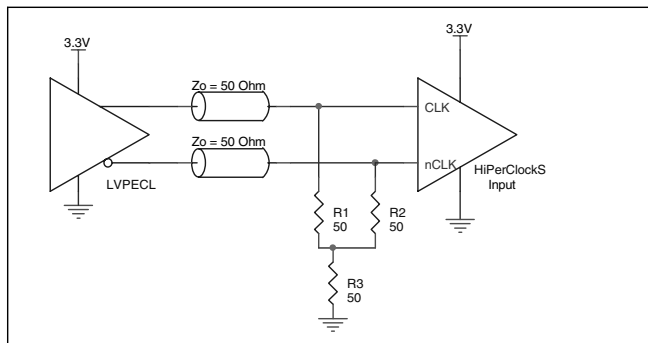


**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

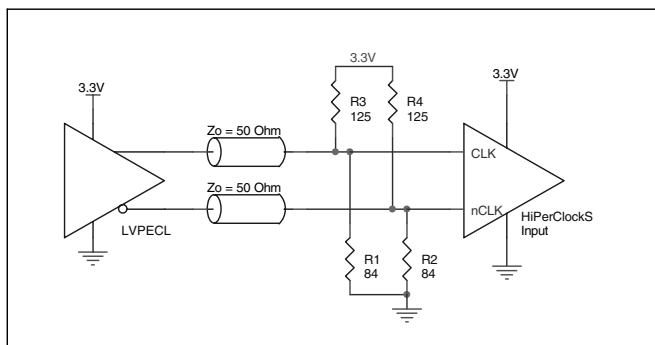


**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

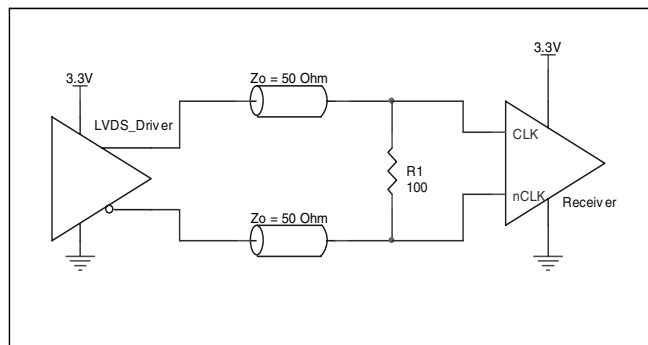


**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

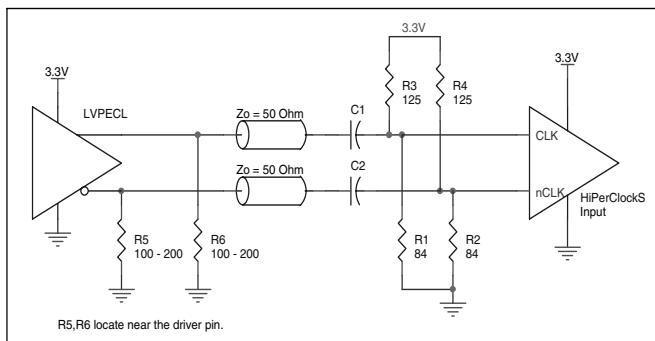


**FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**



### LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{\text{SWING}}$  and  $V_{\text{OH}}$  must meet the  $V_{\text{PP}}$  and  $V_{\text{CMR}}$  input requirements. Figures 4A to 4F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

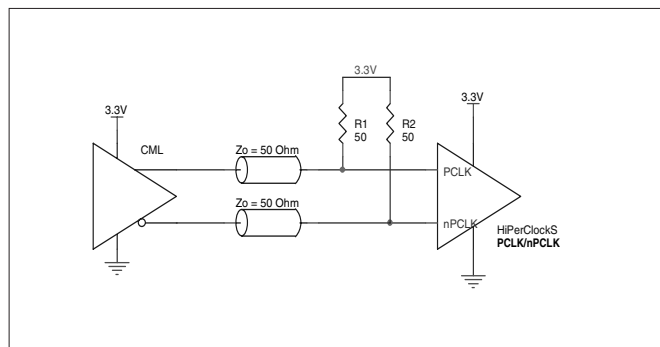


**FIGURE 4A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**

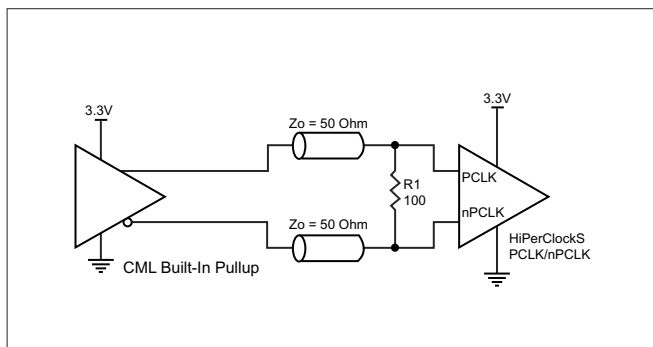


**FIGURE 4B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**

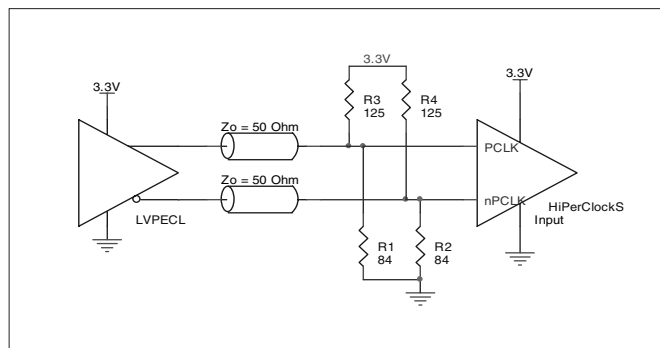


**FIGURE 4C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**

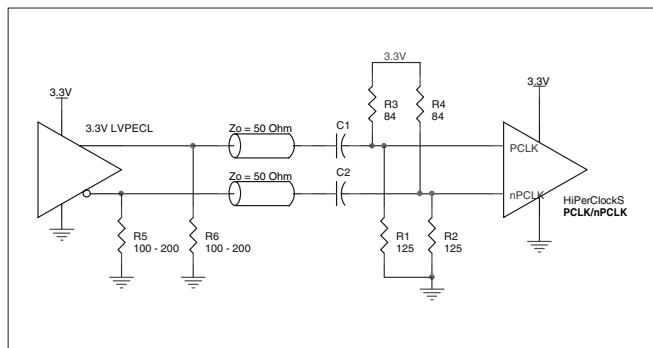


**FIGURE 4D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**

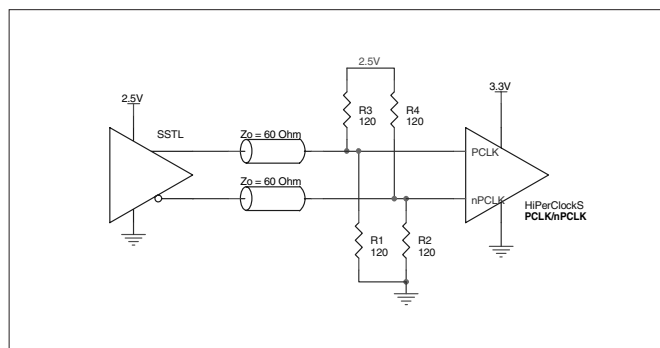


**FIGURE 4E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**

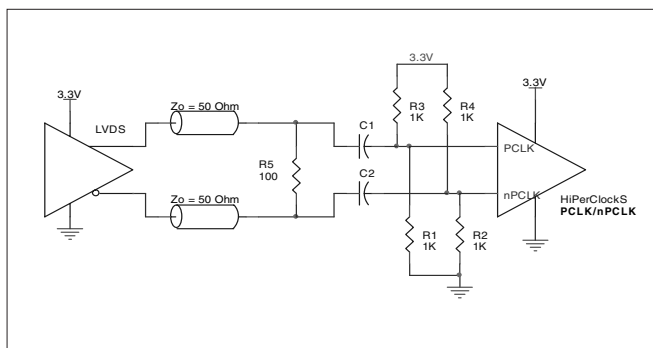
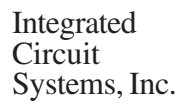


**FIGURE 4F. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**



10



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8523I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8523I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 55mA = 190.6mW$
- Power (outputs)<sub>MAX</sub> = **32.6mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 32.6mW = 130.4mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.6mW + 130.4mW = 321mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.321W * 66.6^\circ C/W = 106.4^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

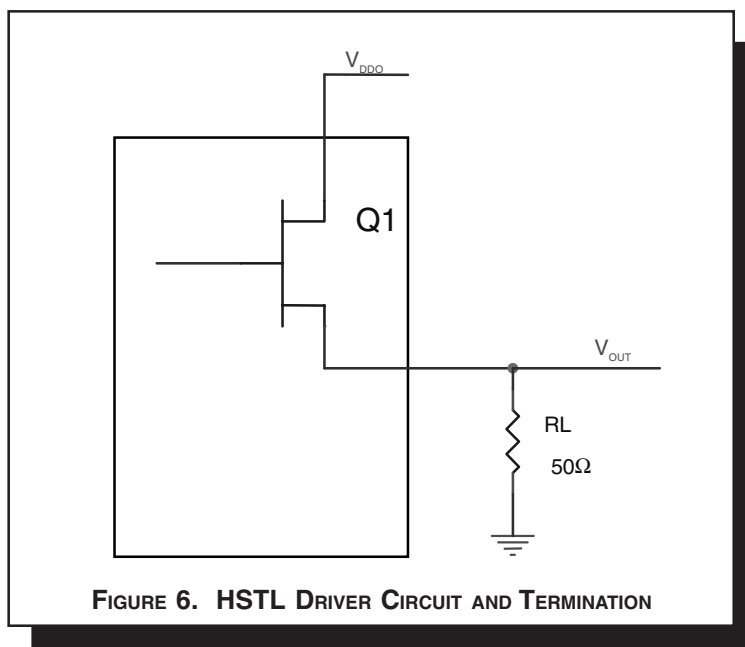
| <b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>                                                |           |            |            |
|---------------------------------------------------------------------------------------------------------------------|-----------|------------|------------|
|                                                                                                                     | <b>0</b>  | <b>200</b> | <b>500</b> |
| Single-Layer PCB, JEDEC Standard Test Boards                                                                        | 114.5°C/W | 98.0°C/W   | 88.0°C/W   |
| Multi-Layer PCB, JEDEC Standard Test Boards                                                                         | 73.2°C/W  | 66.6°C/W   | 63.5°C/W   |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |           |            |            |



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 6*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MIN} / R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$$

$$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd\_H = (0.9V/50\Omega) * (2V - 0.9V) = \mathbf{19.8mW}$$

$$Pd\_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{32.6mW}$$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |          |          |
|----------------------------------------------------|-----------|----------|----------|
|                                                    | 0         | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 73.2°C/W  | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8523I is: 472



**PACKAGE OUTLINE - G SUFFIX FOR 20 LEADP TSSOP**

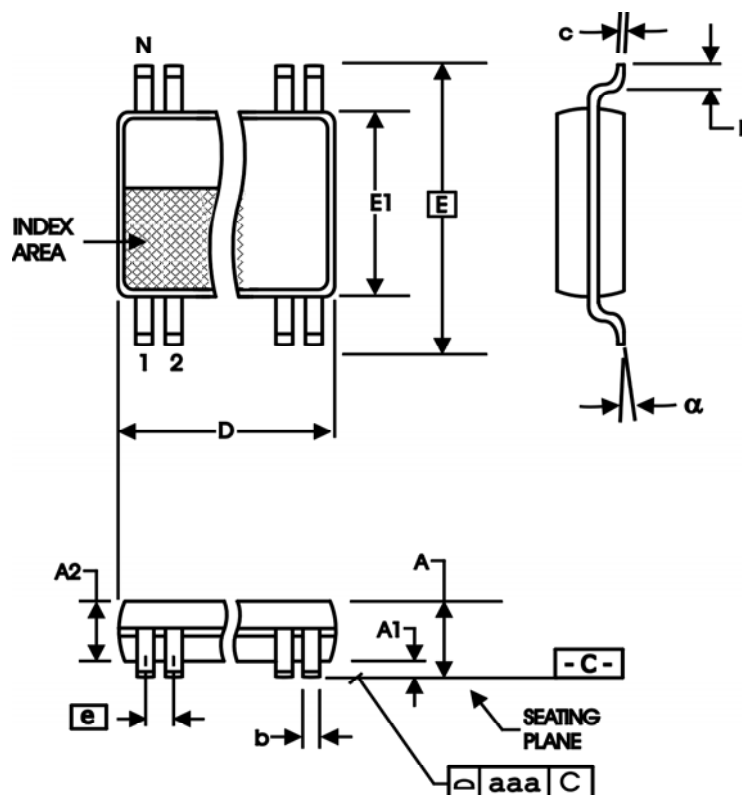


**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL   | Millimeters |         |
|----------|-------------|---------|
|          | Minimum     | Maximum |
| N        | 20          |         |
| A        | --          | 1.20    |
| A1       | 0.05        | 0.15    |
| A2       | 0.80        | 1.05    |
| b        | 0.19        | 0.30    |
| c        | 0.09        | 0.20    |
| D        | 6.40        | 6.60    |
| E        | 6.40 BASIC  |         |
| E1       | 4.30        | 4.50    |
| e        | 0.65 BASIC  |         |
| L        | 0.45        | 0.75    |
| $\alpha$ | 0°          | 8°      |
| aaa      | --          | 0.10    |

Reference Document: JEDEC Publication 95, MS-153



Integrated  
Circuit  
Systems, Inc.

# ICS8523I

## LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-HSTL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking      | Package                                    | Count       | Temperature   |
|-------------------|--------------|--------------------------------------------|-------------|---------------|
| ICS8523BGI        | ICS8523BGI   | 20 lead TSSOP                              | 72 per tube | -40°C to 85°C |
| ICS8523BGIT       | ICS8523BGI   | 20 lead TSSOP on Tape and Reel             | 2500        | -40°C to 85°C |
| ICS8523BGILF      | ICS8523BGILF | 20 lead "Lead-Free" TSSOP                  | 72 per tube | -40°C to 85°C |
| ICS8523BGILFT     | ICS8523BGILF | 20 lead "Lead-Free" TSSOP on Tape and Reel | 2500        | -40°C to 85°C |

The aforementioned trademark, HiPerClockS™ is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.



Integrated  
Circuit  
Systems, Inc.

# ICS8523I

## LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-HSTL FANOUT BUFFER

### REVISION HISTORY SHEET

| Rev | Table | Page    | Description of Change                                                                                                                                                                           | Date     |
|-----|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| B   | T5    | 5       | AC Characteristics table. $t_{PD}$ row, changed Min. from 1.2ns to 1.0ns.                                                                                                                       | 1/11/02  |
| B   |       | 1       | Revised Features section, Bullet 1,6 - took out 1.8V                                                                                                                                            | 5/6/02   |
| B   |       | 8 - 10  | In the Application Information section, added Schematic Examples                                                                                                                                | 10/28/02 |
| C   | T2    | 2       | Pin Characteristics Table - changed $C_{IN}$ 4pF max. to 4pF typical.                                                                                                                           | 6/23/03  |
|     |       | 4       | Absolute Maximum Ratings - changed Output rating.                                                                                                                                               |          |
|     | T4D   | 5       | HSTL DC Characteristics Table - changed $V_{OH}$ 1V min. to 0.9V min.                                                                                                                           |          |
|     |       | 11 - 12 | Power Considerations - changed Total Power Dissipation to reflect $V_{OH}$ change.<br>Calculations changed due to new Total Power Dissipation.<br>Changed LVHSTL to HSTL throughout data sheet. |          |
| C   |       | 1       | Added Lead-Free bullet to Features section.                                                                                                                                                     | 9/16/04  |
|     |       | 9       | Updated LVPECL Clock Input Interface section.                                                                                                                                                   |          |
|     | T9    | 15      | Added Lead-Free Part Number to Ordering Information Table.                                                                                                                                      |          |