# 3.3V, PCI Express® 3.0 2-Lane, (4-Channel), Differential Mux/Demux with Bypass

## Features

- 8 Differential Channel SPST switch with Mux/DeMux option
- PCIe® 3.0 performance
- Bi-directional operation
- Low Bit-to-Bit Skew: 10ps (between ± signals)
- Low Crosstalk: -50dB @ 4.0GHz (8Gbps)
- Low Off Isolation: -21dB @4GHz
- Low Insertion Loss: -1.8dB @ 4.0GHz (8Gbps)
- Return Loss: -15dB @4GHz
- $V_{DD}$ Operating Range: 3.3V ±10%
- ESD Tolerance: 2kV HBM
- Packaging (Pb-free & Green): 42-contact, TQFN (ZH42)

## Description

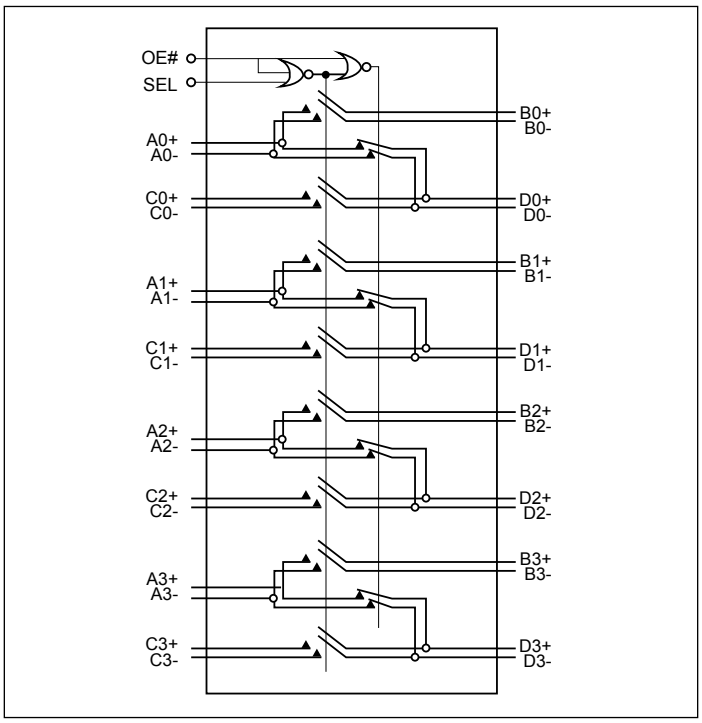
Pericom semiconductor's PI3PCIE3422 is an 8 to 4 channel differential multiplexer/demultiplexer featuring 8-channel pass-through. It supports two full PCIe® lanes at 8.0Gbps PCIe® 3.0 performance.

With the select control input low Port A connects to Port B, and Port C connects to port D for an 8-channel differential pass-though. When the select control input is high Port A connects to Port D, and Port B and Port C are in a high-impedance state. The mux/demux function is between Port A and Ports B or D as determined by the select input control.

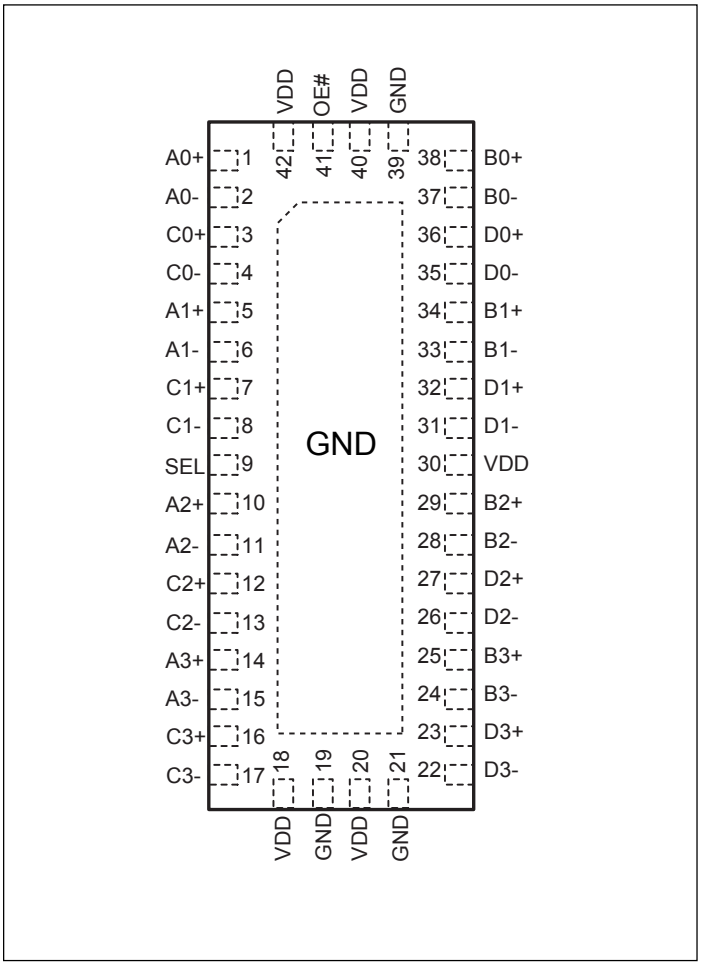
## Truth Table

| Function | SEL | OE# |
|---|---|---|
| Ax = Bx<br>Cx = Dx | L | 0 |
| Ax = Dx<br>B = C = Hi-Z | H | 0 |
| Ax, Bx, Cx, Dx = Hi-Z (disconnected) | x | 1 |

## Block Diagram




## Pin Diagram (Top-side view)



## Pin Description

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1<br>2 | A0+<br>A0– | I/O | Signal I/O, Channel 0, Port A |
| 5<br>6 | A1+<br>A1– | I/O | Signal I/O, Channel 1, Port A |
| 10<br>11 | A2+<br>A2– | I/O | Signal I/O, Channel 2, Port A |
| 14<br>15 | A3+<br>A3– | I/O | Signal I/O, Channel 3, Port A |
| 38<br>37 | B0+<br>B0– | I/O | Signal I/O, Channel 0, Port B |
| 34<br>33 | B1+<br>B1– | I/O | Signal I/O, Channel 1, Port B |
| 29<br>28 | B2+<br>B2– | I/O | Signal I/O, Channel 2, Port B |
| 25<br>24 | B3+<br>B3– | I/O | Signal I/O, Channel 3, Port B |
| 3<br>4 | C0+<br>C0– | I/O | Signal I/O, Channel 0, Port C |
| 7<br>8 | C1+<br>C1– | I/O | Signal I/O, Channel 1, Port C |
| 12<br>13 | C2+<br>C2– | I/O | Signal I/O, Channel 2, Port C |
| 16<br>17 | C3+<br>C3– | I/O | Signal I/O, Channel 3, Port C |
| 36<br>35 | D0+<br>D0– | I/O | Signal I/O, Channel 0, Port D |
| 32<br>31 | D1+<br>D1– | I/O | Signal I/O, Channel 1, Port D |
| 27<br>26 | D2+<br>D2– | I/O | Signal I/O, Channel 2, Port D |
| 23<br>22 | D3+<br>D3– | I/O | Signal I/O, Channel 3, Port D |
| 41 | OE# | I | Output Enable, active low. When OE# = 0 the device I/O is enabled. When OE#=1, all I/O are high impedance |
| 9 | SEL | I | Operation mode Select<br>(when SEL=0: A→B, C→D, when SEL=1: A→D, B + C = Hi-Z) |
| 18, 20, 30, 40, 42 | $V_{DD}$ | Pwr | 3.3V ±10% Positive Supply Voltage |
| 19, 21, 39, Center Pad | GND | Pwr | Power ground |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Supply Voltage to Ground Potential | –0.5V to +4.6V |
| Channel DC Input Voltage | –0.5V to 1.5V |
| DC Output Current | 120mA |
| Power Dissipation | 0.5W |
| SEL DC Input Voltage | –0.5V to 4.6V |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Electrical Characteristics** Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | 3.3V Power Supply | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | Total current from $V_{DD}$ 3.3V supply | SEL and OE# at OV or $V_{DD}$ | | 0.15 | 1 | mA |
| $T_{CASE}$ | Case temperature range for operation within spec. | | -40 | | 85 | Celsius |

## DC Electrical Characteristics for Switching over Operating Range

| Parameters | Description | Test Conditions(1) | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ - SEL | Input HIGH Voltage, SEL input | Guaranteed HIGH level | 2 | | 3.6 | V |
| $V_{IL}$ - SEL | Input LOW Voltage, SEL input | Guaranteed LOW level | 0 | | 0.8 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$ = Max., $V_{IN}$ = –18mA | | –0.7 | –1.2 | |
| $I_{IH}$ | Input HIGH Current for OE# and SEL | $V_{DD}$ = Max., $V_{IN}$ = $V_{DD}$ | -10 | | 10 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{DD}$ = Max., $V_{IN}$ = 1.5V | -10 | | +10 | |
| $I_{IL}$ | Input LOW Current | $V_{DD}$ = Max., $V_{IN}$ = GND | -10 | | +10 | |
| $R_{ON}$ | On Channel Resistance | $V_{DD}$ = Min., $V_{IN}$ = 1.3V, $I_{IN}$ = 40mA | | 8 | 15 | Ohm |
| $C_{ON}$ | On Channel Capacitance | $V_{DD}$ = 3.3V, $V_{IN}$ = 0 | | 2.5 | | pF |
| $I_{OZ}$ | Output Current | $V_{DD}$ = Max., $V_{IN}$ = 0V to 1.5V | -10 | | +10 | µA |

**Note:**

**1. Typical values are at VDD = 3.3V, TA = 25°C ambient and maximum loading.**

## Switching Characteristics

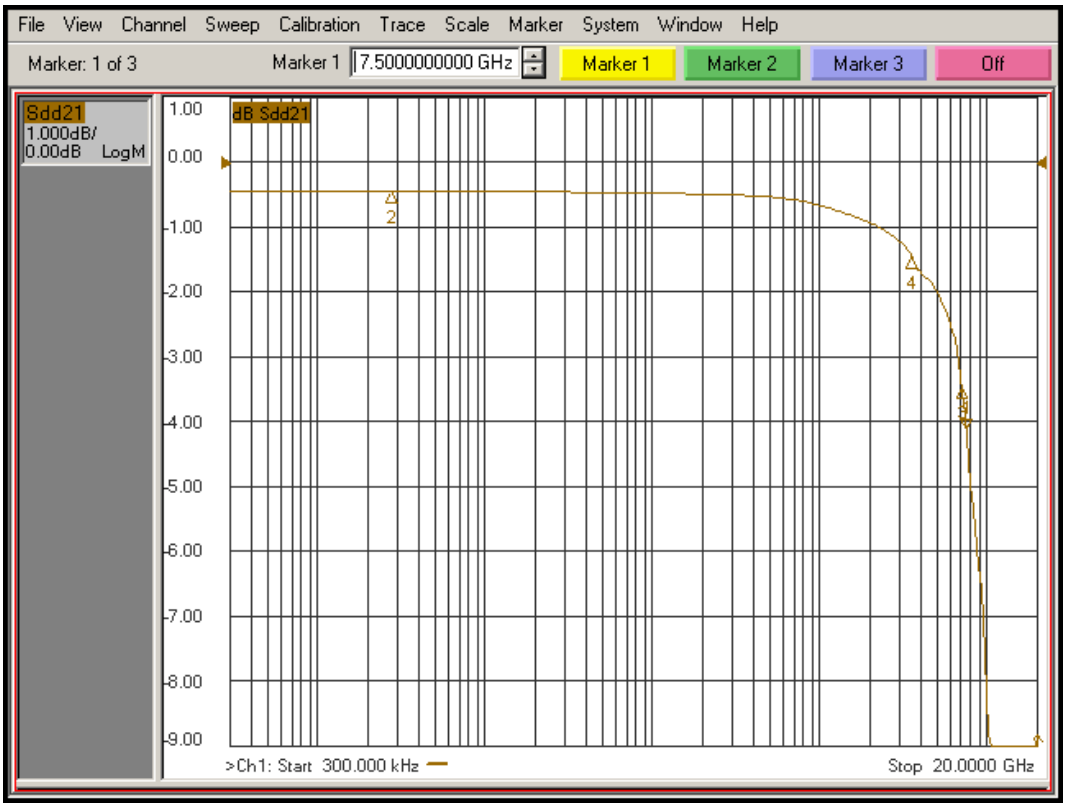
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PZH}$, $t_{PZL}$ | Line Enable Time - SEL to $A_N$, $B_N$, $C_N$, $D_N$ | | 0.5 | 15 | 25 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Line Disable Time - SEL to $A_N$, $B_N$, $C_N$, $D_N$ | | 0.5 | 5 | 25 | |
| $t_{b-b}$ | Bit-to-bit skew within the same differential pair | | | 4 | 10 | ps |
| $t_{ch-ch}$ | Channel-to-channel skew | | | | 20 | |

## Dynamic Electrical Characteristics

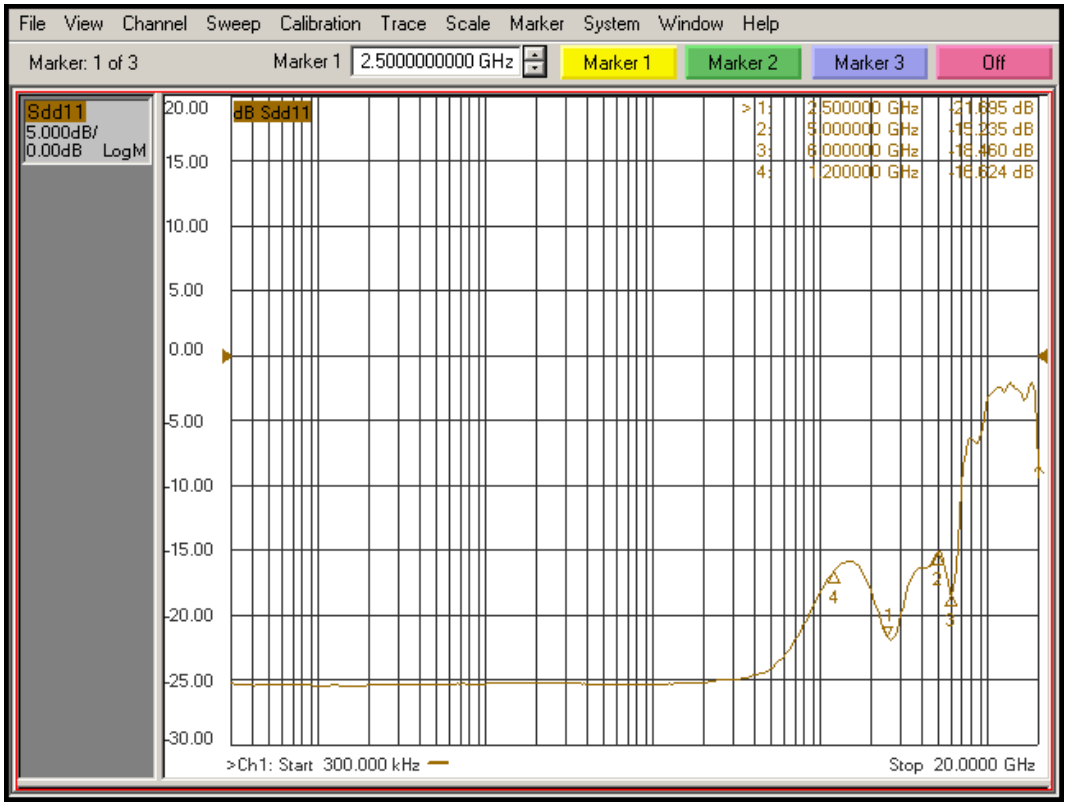
| Parameter | Description | Test Conditions | Min. | Typ.(1) | Max. | Units |
|---|---|---|---|---|---|---|
| BW | Bandwidth -3dB | | | 7 | | GHz |
| DDIL | Differential Insertion Loss ($V_{IN}$ = -10dBm, DC = 0V) | f=1.25GHz<br>f=2.5GHz<br>f=4.0GHz<br>f=5.0GHz<br>f=8.0GHz | | -0.9<br>-1.2<br>-1.7<br>-2.0<br>-5.0 | -1.0<br>-1.3<br>-1.8<br>-2.1<br>-5.1 | dB |
| $DDIL_{OFF}$ | Differential Off Isolation | f= 4.0GHz | | -19 | | dB |
| DDRL | Differential Return Loss | f= 0 to 1.25GHz<br>f= 1.25 to 2.5GHz<br>f= 2.5 to 4.0GHz | | -16<br>-15<br>-15 | -15<br>-14<br>-14 | dB |
| DDNEXT | Near End Crosstalk | f= 0 to 2.8GHz<br>f= 2.8 to 5.0GHz<br>f= 5.0 to 8.0GHz | | -52<br>-50<br>-48 | | dB |

**Notes:**

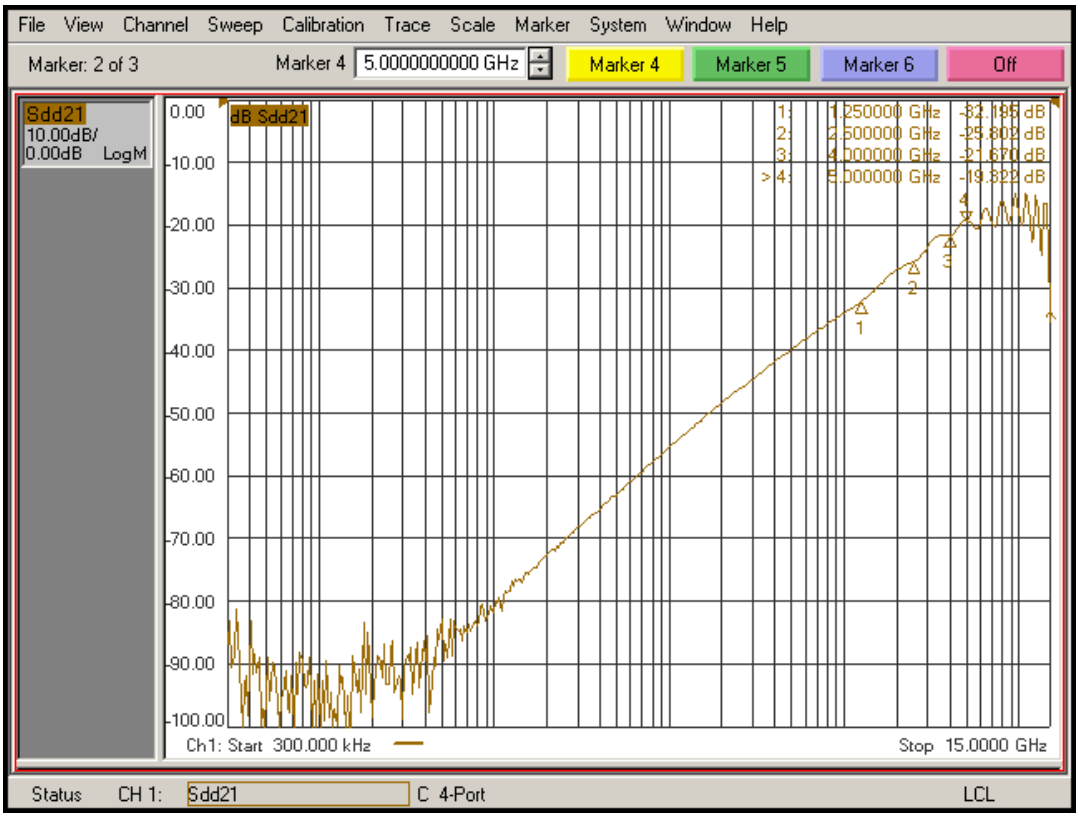
**1. Guaranteed by design. Typical values are at $V_{DD}$ = 3.3V , $T_A$ = 25°C ambient and maximum loading.**



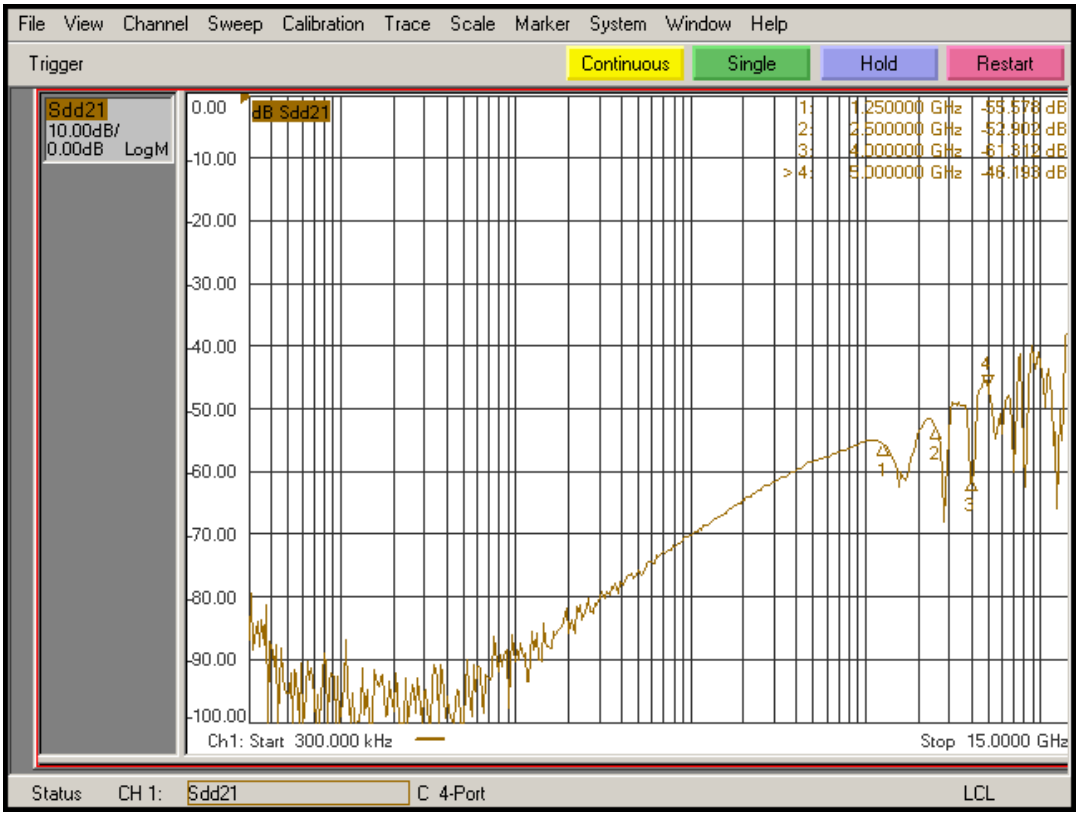

**Differential Insertion Loss**



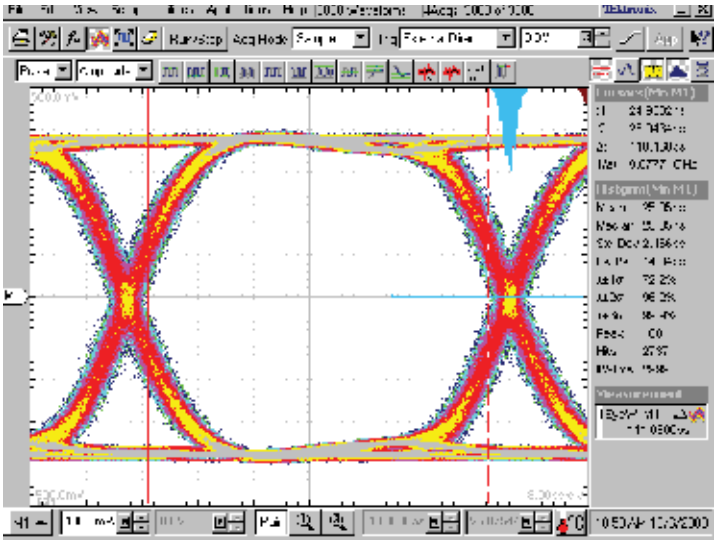

**Differential Return Loss**



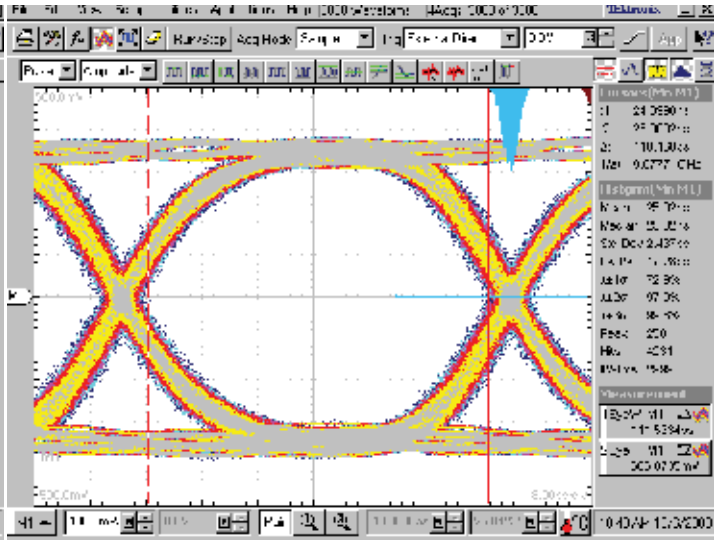

**Differential Off Isolation**



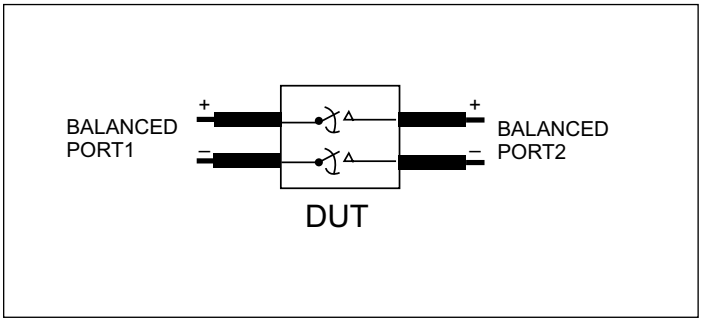

**Differential Crosstalk**



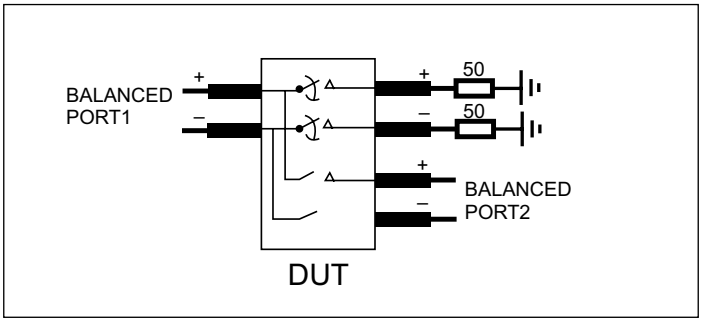
8.0 Gbps RX signal eye without PI3PCIE3422



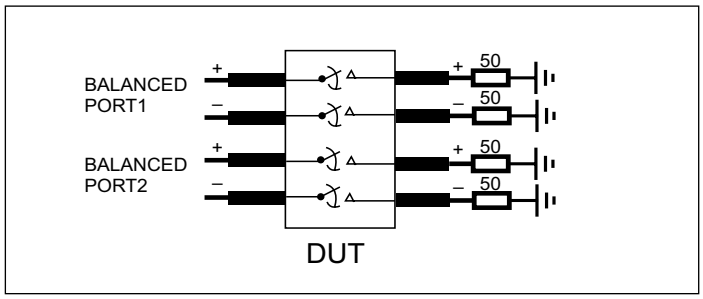
8.0 Gbps RX signal eye with PI3PCIE3422




Differential Insertion Loss and Return Test Circuit

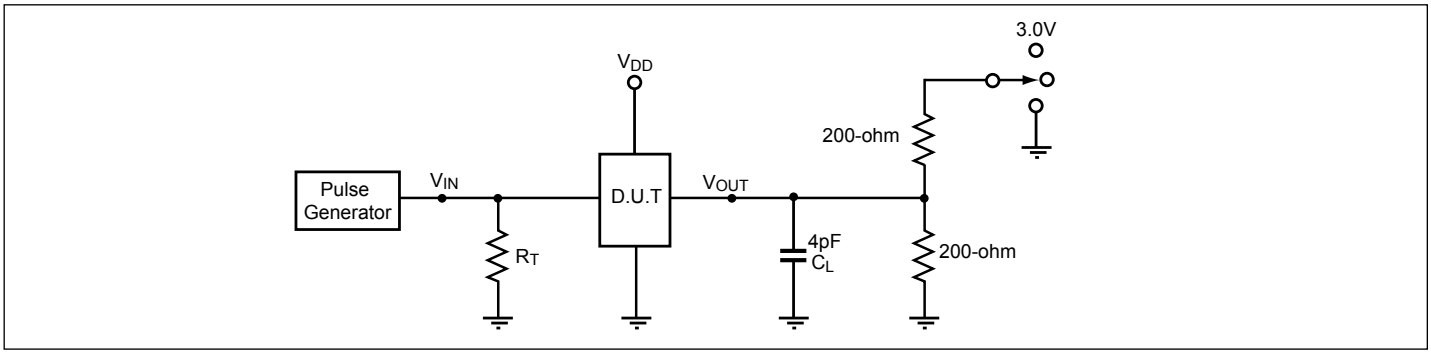



Differential Off Isolation Test Circuit




Differential Near End Xtalk Test Circuit

## Test Circuit for Electrical Characteristics(1-5)



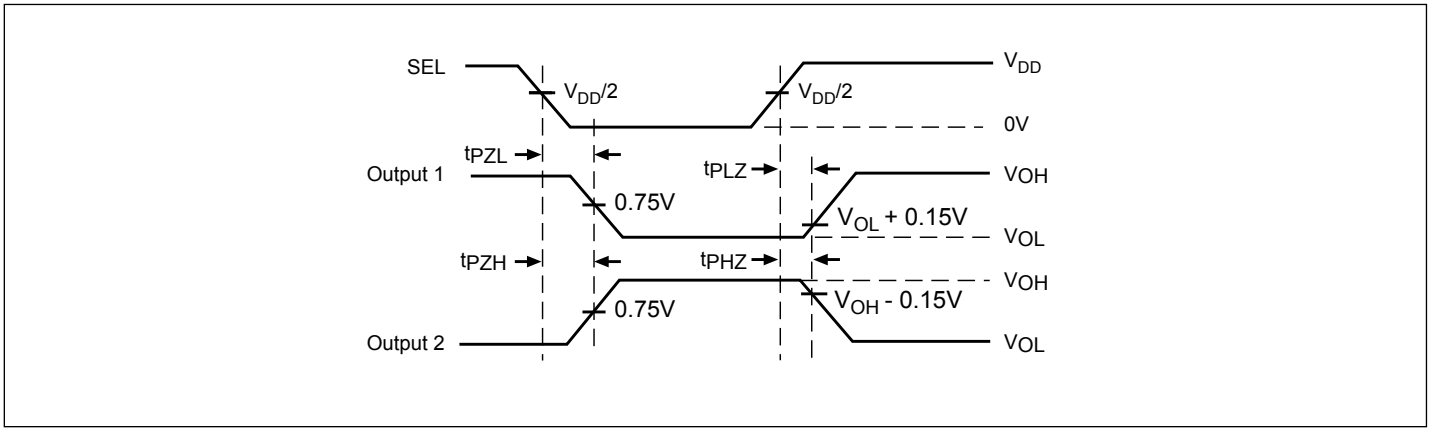

**Notes:**

1. **$C_L$ = Load capacitance: includes jig and probe capacitance.**
2. **$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator**
3. **Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.**
4. **All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.**
5. **The outputs are measured one at a time with one transition per measurement.**

## Switch Positions

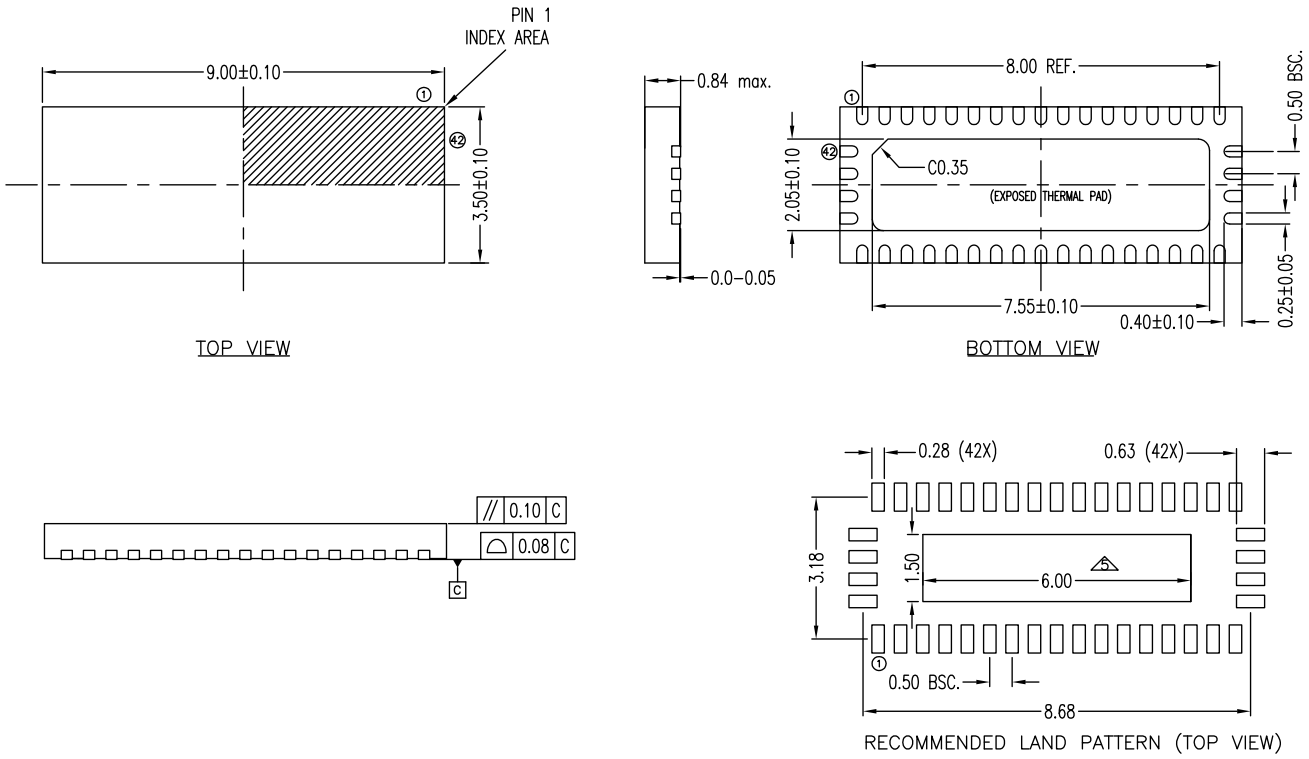
| Test | Switch |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | 3.0V |
| $t_{PHZ}$, $t_{PZH}$ | GND |
| Prop Delay | Open |

## Switching Waveforms




**Voltage Waveforms Enable and Disable Times**

## Packaging Information




**Notes:**
1. All dimensions are in millimeters. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220.
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

| | |
|---|---|
| PERICOM Enabling Serial Connectivity | DATE: 11/14/12 |
| DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN) | |
| PACKAGE CODE: ZH42 | |
| DOCUMENT CONTROL #: PD-2035 | REVISION:D |

12-0529

**Note:**

**For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php**

## Ordering Information

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI3PCIE3422ZHE | ZH | Pb-free & Green, 42-contact TQFN |

**Notes:**

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **"E" denotes Pb-free and Green**
- **Adding an "X" at the end of the ordering code denotes tape and reel packaging**