60V Common Mode, Fixed Gain, Bidirectional Precision Current Sensing Amplifier

Check for Samples: LMP8602, LMP8602Q, LMP8603, LMP8603Q

FEATURES

- **Unless Otherwise Noted, Typical Values at T_A = 25°C, V_S = 5.0V, Gain = 50x (LMP8602), Gain = 100x (LMP8603)**
- **TCV_{os} 10µV/°C max**
- **CMRR 90 dB Min**
- **Input Offset Voltage 1 mV Max**
- **CMVR at V_S = 3.3V −4V to 27V**
- **CMVR at V_S = 5.0V −22V to 60V**
- **Operating Ambient Temperature Range −40°C to 125°C**
- **Single Supply Bidirectional Operation**
- **All Min / Max Limits 100% Tested**
- **LMP8602Q and LMP8603Q Available in Automotive AEC-Q100 Grade 1 Qualified Version**

APPLICATIONS

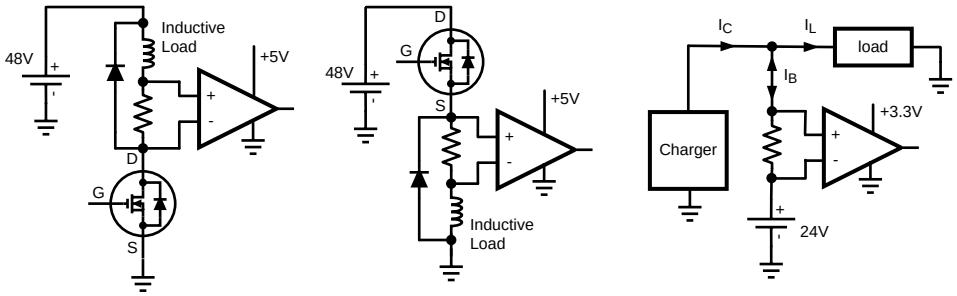
- **High Side and Low Side Driver Configuration Current Sensing**
- **Bidirectional Current Measurement**
- **Current Loop to Voltage Conversion**
- **Automotive Fuel Injection Control**
- **Transmission Control**
- **Power Steering**
- **Battery Management Systems**

DESCRIPTION

The LMP8602 and LMP8603 are fixed gain precision amplifiers. The parts will amplify and filter small differential signals in the presence of high common mode voltages. The input common mode voltage range is –22V to +60V when operating from a single 5V supply. With a 3.3V supply, the input common mode voltage range is from –4V to +27V. The LMP8602 and LMP8603 are members of the Linear Monolithic Precision (LMP®) family and are ideal parts for unidirectional and bidirectional current sensing applications. All parameter values of the parts that are shown in the tables are 100% tested and all bold values are also 100% tested over temperature.

The parts have a precise gain of 50x for the LMP8602 and 100x for the LMP8603, which are adequate in most targeted applications to drive an ADC to its full scale value. The fixed gain is achieved in two separate stages, a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 5x for the LMP8602 and 10x for the LMP8603. The connection between the two stages of the signal path is brought out on two pins to enable the possibility to create an additional filter network around the output buffer amplifier. These pins can also be used for alternative configurations with different gain as described in the applications section.

Typical Applications



DESCRIPTION (CONTINUED)

The mid-rail offset adjustment pin enables the user to use these devices for bidirectional single supply voltage current sensing. The output signal is bidirectional and mid-rail referenced when this pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

The LMP8602 and LMP8603 are available in a 8–Pin SOIC package and in a 8–Pin VSSOP package.

The LMP8602Q and LMP8603Q incorporate enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body	For input pins only	±4000V
		For all other pins	±2000V
	Machine Model		200V
	Charge Device Model		1000V
Supply Voltage (V_S - GND)			6.0V
Continuous Input Voltage (−IN and +IN)(4)			−22V to 60V
Transient (400 ms)			−25V to 65V
Maximum Voltage at A1, A2, OFFSET and OUT Pins			V_S +0.3V and GND -0.3V
Storage Temperature Range			−65°C to 150°C
Junction Temperature(5)			150°C
Mounting Temperature	Infrared or Convection (20 sec)		235°C
	Wave Soldering Lead (10 sec)		260°C

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Human Body Model per MIL-STD-883, Method 3015.7. Machine Model, per JESD22-A115-A. Field-Induced Charge-Device Model, per JESD22-C101-C.

(4) For the VSSOP package, the bare board spacing at the solder pads of the package will be to small for reliable use at higher voltages (V_{CM} >25V) Therefore it is strongly advised to add a conformal coating on the PCB assembled with the LMP8602 and LMP8603.

(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Operating Ratings(1)

Supply Voltage (V_S – GND)		3.0V to 5.5V
Offset Voltage (Pin 7)		0 to V_S
Temperature Range(2)	Packaged devices	−40°C to +125°C
Package Thermal Resistance(2)	8-Pin SOIC (θ_{JA})	190°C/W
	8-Pin VSSOP (θ_{JA})	203°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

3.3V Electrical Characteristics(1)

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3V, GND = 0V, −4V ≤ V_{CM} ≤ 27V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I_S	Supply Current				1	**1.3**	mA
A_V	Total Gain	LMP8602		49.75	50	50.25	V/V
		LMP8603		99.5	100	100.5	
	Gain Drift(4)	−40°C ≤ T_A ≤ 125°C			−2.7	**±20**	ppm/°C
SR	Slew Rate(5)	V_{IN} = ±0.165V		0.4	0.7		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift(6)	−40°C ≤ T_A ≤ 125°C			2	**±10**	µV/°C
e_n	Input Referred Voltage Noise	0.1 Hz − 10 Hz, 6 Sigma			16.4		μV_{P-P}
		Spectral Density, 1 kHz			830		nV/√Hz
PSRR	Power Supply Rejection Ratio	DC, 3.0V ≤ V_S ≤ 3.6V, V_{CM} = V_S/2		**70**	86		dB
	Mid−scale Offset Scaling Accuracy	LMP8602			±0.25	±1	%
			Input Referred			±0.33	mV
		LMP8603			±0.45	±1.5	%
			Input Referred			±0.248	mV
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	−4V ≤ V_{CM} ≤ 27V		**250**	295	**350**	kΩ
R_{DM}	Input Impedance Differential Mode	−4V ≤ V_{CM} ≤ 27V		**500**	590	**700**	kΩ
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			±0.15	±1	mV
DC CMRR	DC Common Mode Rejection Ratio	−2V ≤ V_{CM} ≤ 24V		**86**	96		dB
AC CMRR	AC Common Mode Rejection Ratio(7)	f = 1 kHz		80	94		dB
		f = 10 kHz			85		
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR		**−4**		**27**	V

(1) The electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(7) AC Common Mode Signal is a $5V_{PP}$ sine-wave (0V to 5V) at the given frequency.

3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3V, GND = 0V, −4V ≤ V_{CM} ≤ 27V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
K1	Gain[4]			9.95	10.0	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor			**99**	100	**101**	kΩ
TCR_{F-INT}	Output Impedance Filter Resistor Drift				±5	**±50**	ppm/°C
A1 V_{OUT}	A1 Output Voltage Swing	V_{OL}	R_L = ∞		2	**10**	mV
		V_{OH}		**3.2**	3.25		V
Output Buffer (From A2 (pin 4) to OUT (pin 5)							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		−2 **−2.5**	±0.5	2 **2.5**	mV
K2	Gain[4]	LMP8602		4.975	5	5.025	V/V
		LMP8603		9.95	10	10.05	
I_B	Input Bias Current of A2[8]				−40		fA
						±20	n A
A2 V_{OUT}	A2 Output Voltage Swing[9][10]	V_{OL}, R_L = 100 kΩ	LMP8602		10	**40**	mV
			LMP8603		10	**80**	
		V_{OH}, R_L = 100 kΩ		**3.28**	3.29		V
I_{SC}	Output Short-Circuit Current[11]	Sourcing, V_{IN} = V_S, V_{OUT} = GND		-25	-38	-60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S		30	46	65	

(8) Positive current corresponds to current flowing into the device.
(9) For this test input is driven from A1 stage in uni-directional mode (Offset pin connected to GND).
(10) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(11) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

5V Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)						
I_S	Supply Current			1.1	**1.5**	mA
A_V	Total Gain[4]	LMP8602	49.75	50	50.25	V/V
		LMP8603	99.5	100	100.5	
	Gain Drift	−40°C ≤ T_A ≤ 125°C		−2.8	**±20**	ppm/°C
SR	Slew Rate[5]	V_{IN} = ±0.25V	0.6	0.83		V/µs
BW	Bandwidth		50	60		kHz
V_{OS}	Input Offset Voltage			0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift[6]	−40°C ≤ T_A ≤ 125°C		2	**±10**	µV/°C
e_N	Input Referred Voltage Noise	0.1 Hz − 10 Hz, 6 Sigma		17.5		μV_{P-P}
		Spectral Density, 1 kHz		890		nV/√Hz

(1) The electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
PSRR	Power Supply Rejection Ratio	DC 4.5V ≤ V_S ≤ 5.5V		**70**	90		dB
	Mid−scale Offset Scaling Accuracy	LMP8602			±0.25	±1	%
			Input Referred			±0.50	mV
		LMP8603			±0.45	±1.5	%
			Input Referred			±0.375	mV
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	0V ≤ V_{CM} ≤ 60V		**250**	295	**350**	kΩ
		−20V ≤ V_{CM}< 0V		**165**	193	**250**	kΩ
R_{DM}	Input Impedance Differential Mode	0V ≤ V_{CM} ≤ 60V		**500**	590	**700**	kΩ
		−20V ≤ V_{CM} < 0V		**300**	386	**500**	kΩ
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			±0.15	±1	mV
DC CMRR	DC Common Mode Rejection Ratio	−20V ≤ V_{CM} ≤ 60V		**90**	105		dB
AC CMRR	AC Common Mode Rejection Ratio(7)	f = 1 kHz		80	96		dB
		f = 10 kHz			83		
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR		**−22**		**60**	V
K1	Gain(4)			9.95	10	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor			**99**	100	**101**	kΩ
TCR_{F-INT}	Output Impedance Filter Resistor Drift				±5	**±50**	ppm/°C
A1 V_{OUT}	A1 Ouput Voltage Swing	V_{OL}	R_L = ∞		2	**10**	mV
		V_{OH}		**4.95**	4.985		V
Output Buffer (From A2 (pin 4) to OUT (pin 5)							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		−2 **−2.5**	±0.5	2 **2.5**	mV
K2	Gain(8)	LMP8602		4.975	5	5.025	V/V
		LMP8603		9.95	10	10.05	
I_B	Input Bias Current of A2(9)				−40		fA
						±20	nA
A2 V_{OUT}	A2 Ouput Voltage Swing(10) (11)	V_{OL}, R_L = 100 kΩ	LMP8602		10	**40**	mV
			LMP8603		10	**80**	
		V_{OH}, R_L = 100 kΩ		**4.98**	4.99		V
I_{SC}	Output Short-Circuit Current(12)	Sourcing, V_{IN} = V_S, V_{OUT} = GND		–25	–42	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S		30	48	65	

(7) AC Common Mode Signal is a $5V_{PP}$ sine-wave (0V to 5V) at the given frequency.
(8) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits.
(9) Positive current corresponds to current flowing into the device.
(10) For this test input is driven from A1 stage in uni-directional mode (Offset pin connected to GND).
(11) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(12) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

BLOCK DIAGRAM

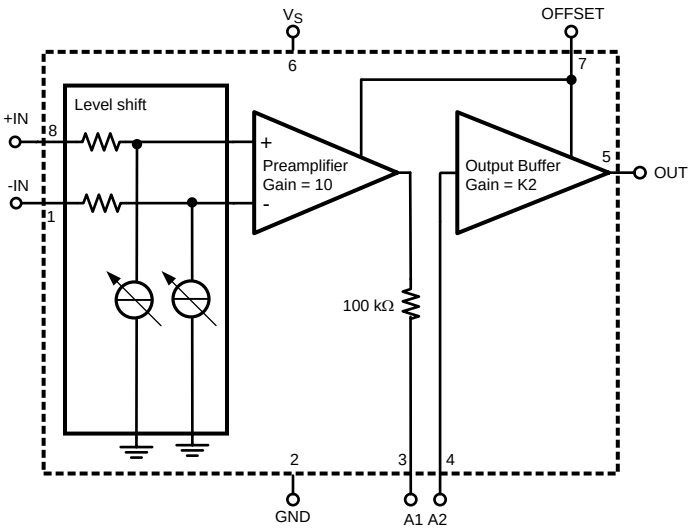


Figure 1. K2 = 5 for LMP8602, K2 = 10 for LMP8603

Connection Diagram

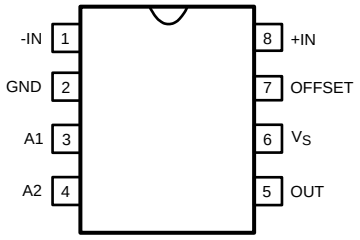


Figure 2. 8-Pin SOIC / VSSOP
Top View

PIN DESCRIPTIONS

	Pin	Name	Description
Power Supply	2	GND	Power Ground
	6	V_S	Positive Supply Voltage
Inputs	1	−IN	Negative Input
	8	+IN	Positive Input
Filter Network	3	A1	Preamplifier output
	4	A2	Input from the external filter network and / or A1
Offset	7	OFFSET	DC Offset for bidirectional signals
Output	5	OUT	Single ended output

Typical Performance Characteristics

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

V_{OS} vs. V_{CM} at V_S = 3.3V

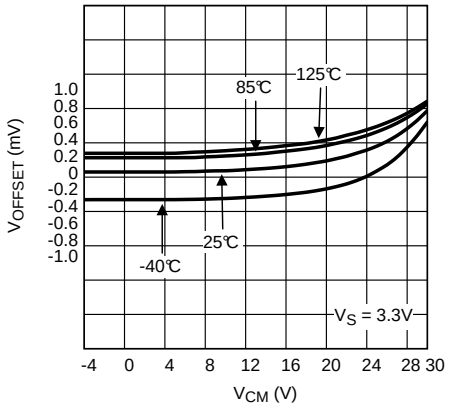


Figure 3.

V_{OS} vs. V_{CM} at V_S = 5V

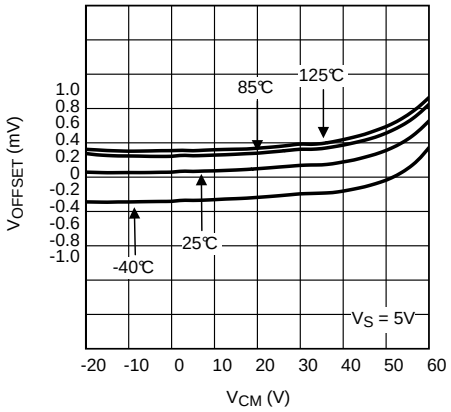


Figure 4.

Input Bias Current Over Temperature (+IN and −IN pins) at V_S = 3.3V

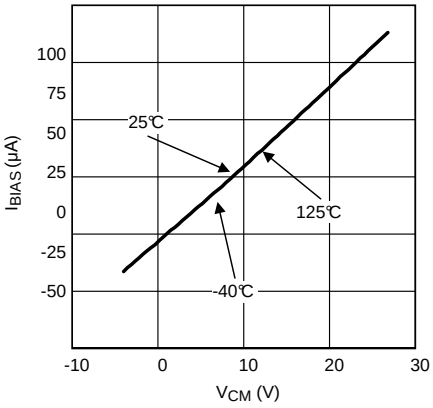


Figure 5.

Input Bias Current Over Temperature (+IN and −IN pins) at V_S = 5V

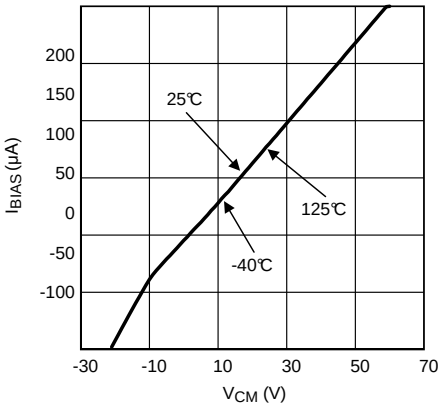


Figure 6.

Input Bias Current Over Temperature (A2 pin) at V_S = 5V

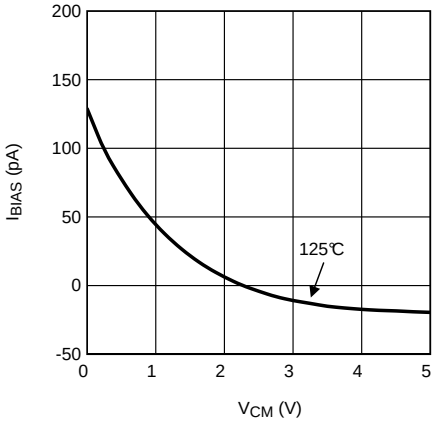


Figure 7.

Input Bias Current Over Temperature (A2 pin) at V_S = 5V

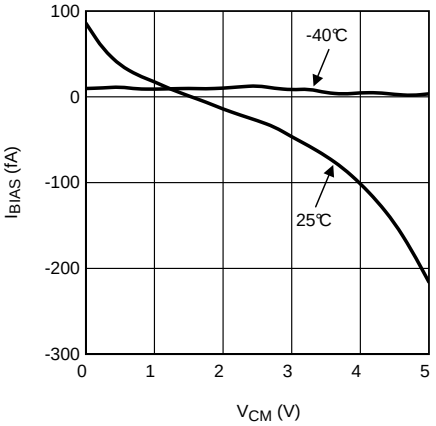


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Input Referred Voltage Noise vs. Frequency

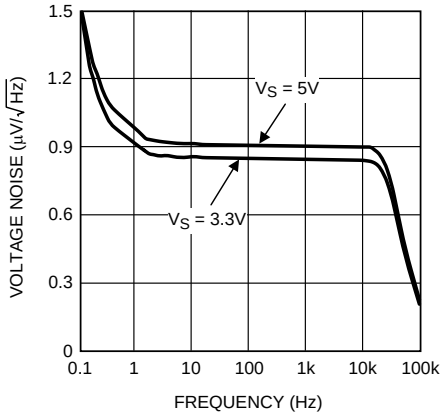


Figure 9.

PSRR vs. Frequency

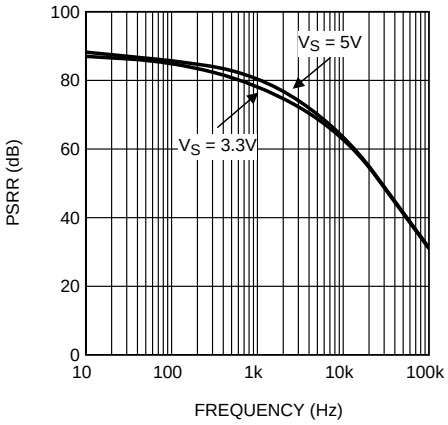


Figure 10.

Gain vs. Frequency LMP8602

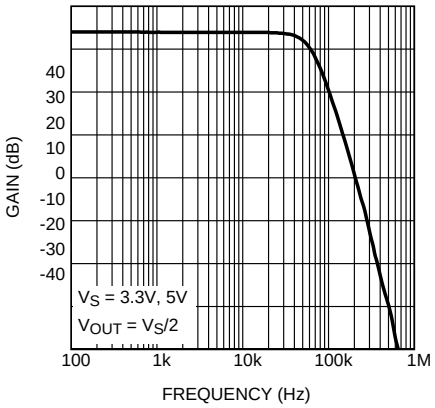


Figure 11.

Gain vs. Frequency LMP8603

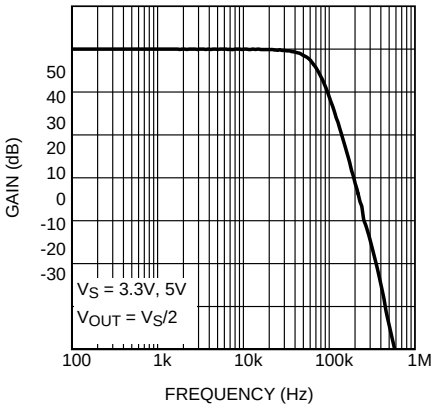


Figure 12.

CMRR vs. Frequency at V_S = 3.3V

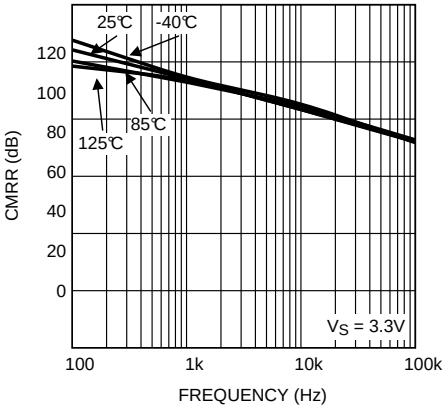


Figure 13.

CMRR vs. Frequency at V_S = 5V

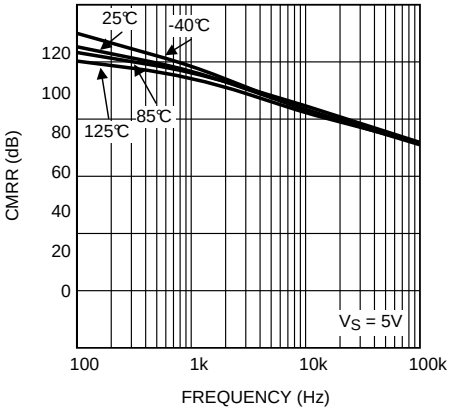


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Step Response at V_S = 3.3V
R_L = 10kΩ LMP8602

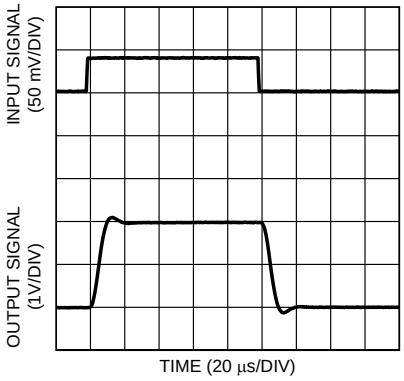


Figure 15.

Step Response at V_S = 5V
R_L = 10kΩ LMP8602

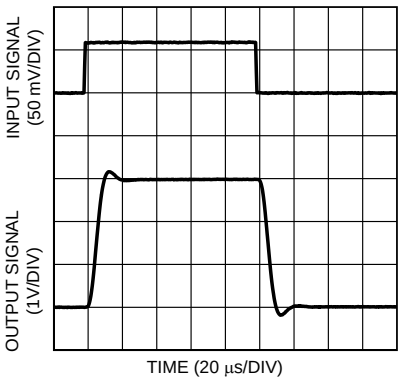


Figure 16.

Settling Time (Falling Edge) at V_S = 3.3V
LMP8602

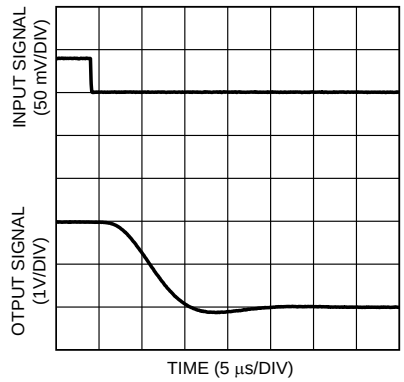


Figure 17.

Settling Time (Falling Edge) at V_S = 5V
LMP8602

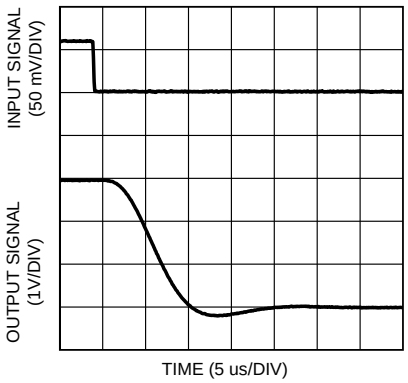


Figure 18.

Settling Time (Rising Edge) at V_S = 3.3V
LMP8602

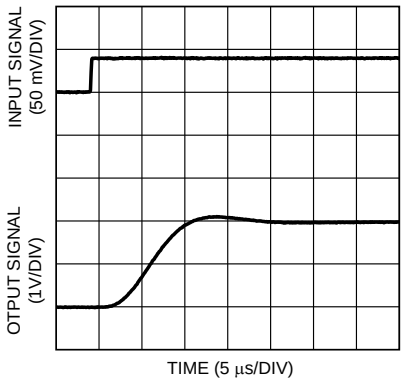


Figure 19.

Settling Time (Rising Edge) at V_S = 5V
LMP8602

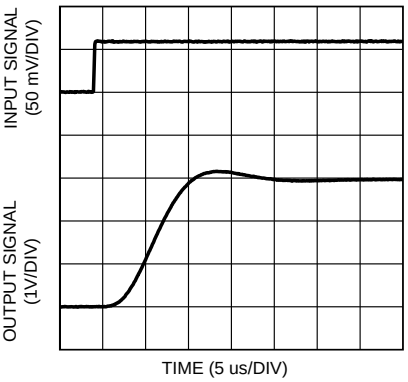


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Step Response at V_S = 3.3V
R_L = 10kΩ LMP8603

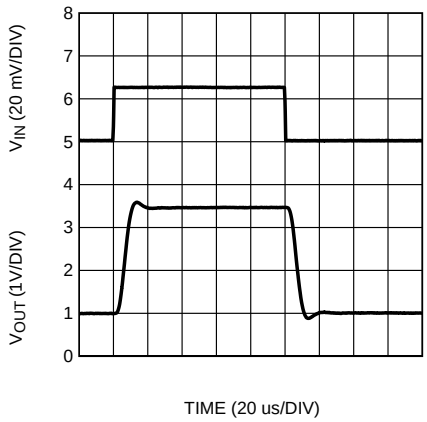


Figure 21.

Step Response at V_S = 5V
R_L = 10kΩ LMP8603

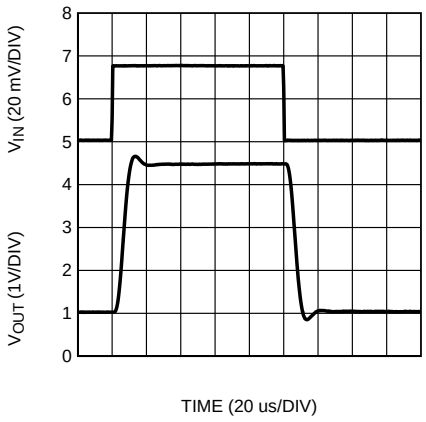


Figure 22.

Settling Time (Falling Edge) at V_S = 3.3V
LMP8603

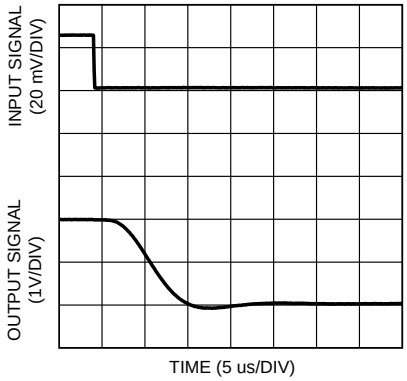


Figure 23.

Settling Time (Falling Edge) at V_S = 5V
LMP8603

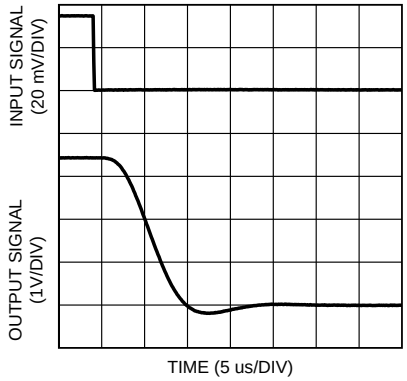


Figure 24.

Settling Time (Rising Edge) at V_S = 3.3V
LMP8603

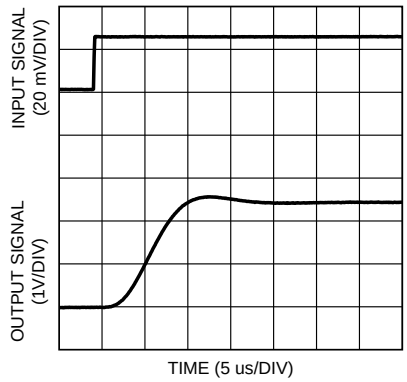


Figure 25.

Settling Time (Rising Edge) at V_S = 5V
LMP8603

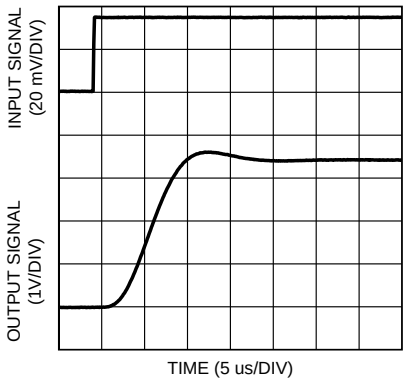


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Positive Swing vs. R_{LOAD} at V_S = 3.3V

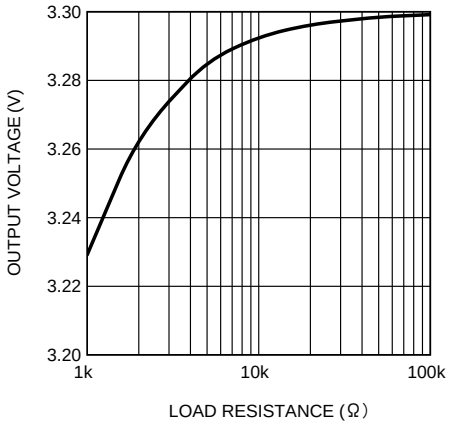


Figure 27.

Positive Swing vs. R_{LOAD} V_S = 5V

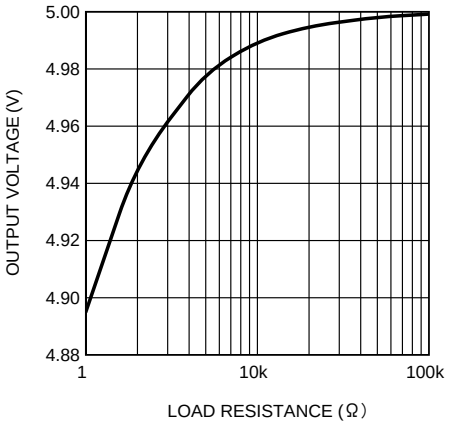


Figure 28.

Negative Swing vs. R_{LOAD} at V_S = 3.3V

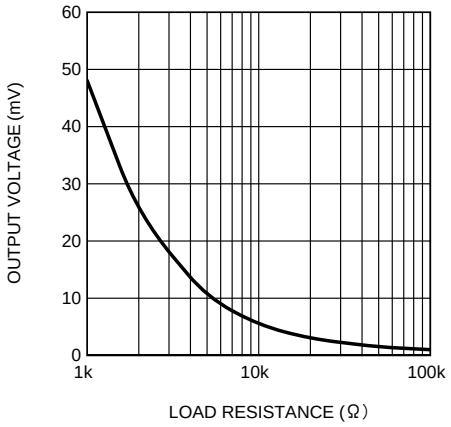


Figure 29.

Negative Swing vs. R_{LOAD} at V_S = 5V

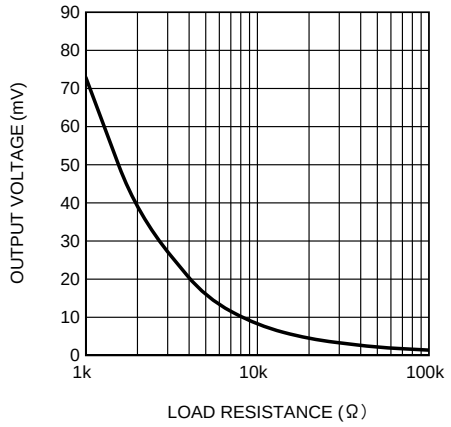


Figure 30.

Gain Drift Distribution LMP8602
5000 parts

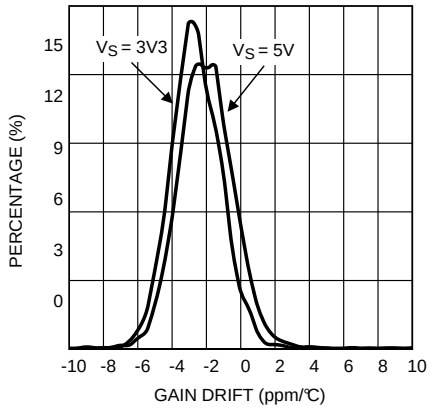


Figure 31.

Gain Drift Distribution LMP8603
5000 parts

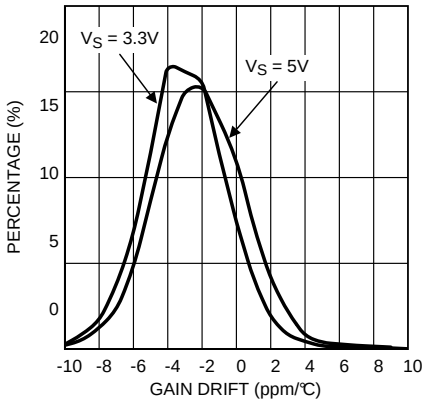


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Gain error Distribution at V_S = 3.3V LMP8602
5000 parts

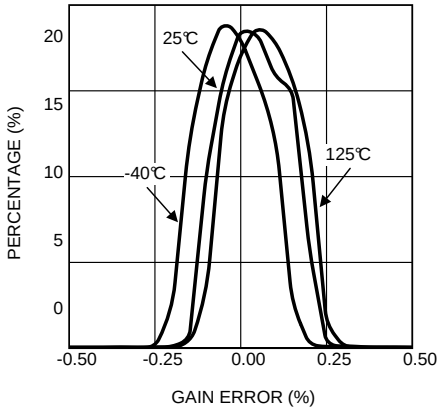


Figure 33.

Gain error Distribution at V_S = 3.3V LMP8603
5000 parts

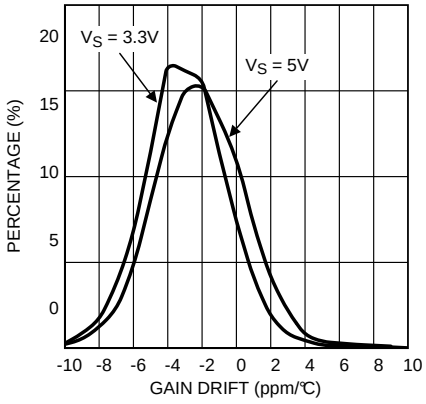


Figure 34.

Gain error Distribution at V_S = 5V LMP8602
5000 parts

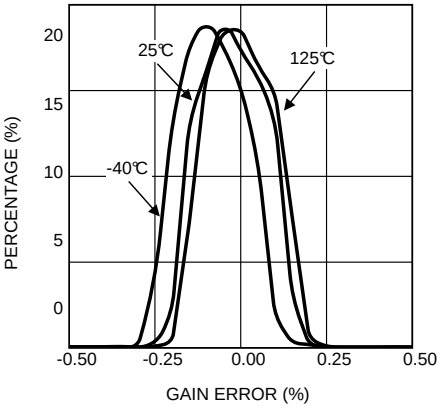


Figure 35.

Gain error Distribution at V_S = 5V LMP8603
5000 parts

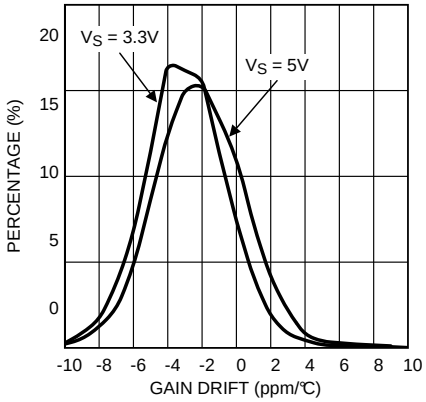


Figure 36.

CMRR Distribution at V_S = 3.3V
5000 parts

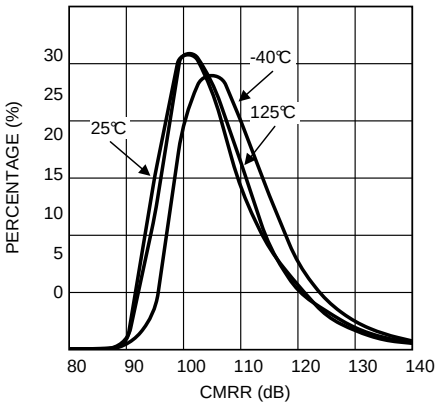


Figure 37.

CMRR Distribution at V_S = 5V
5000 parts

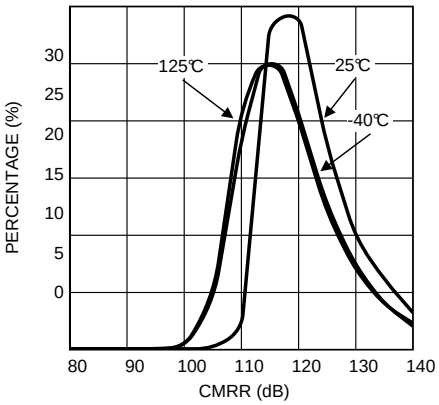


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, −22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

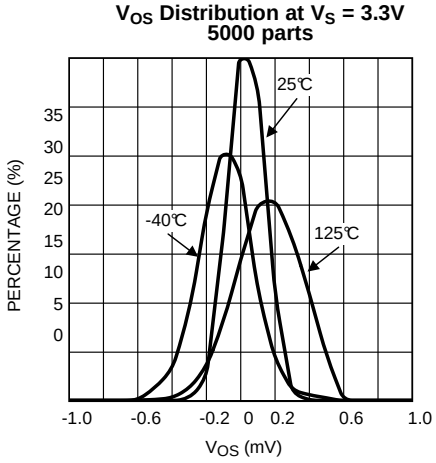


Figure 39.

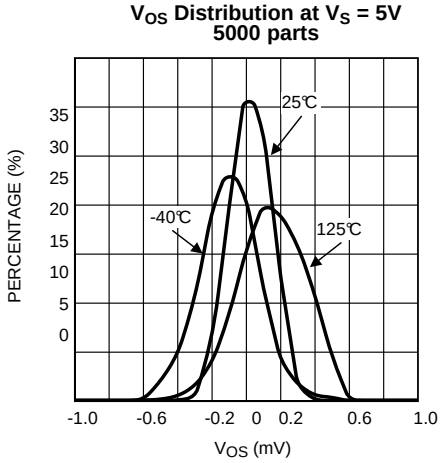


Figure 40.

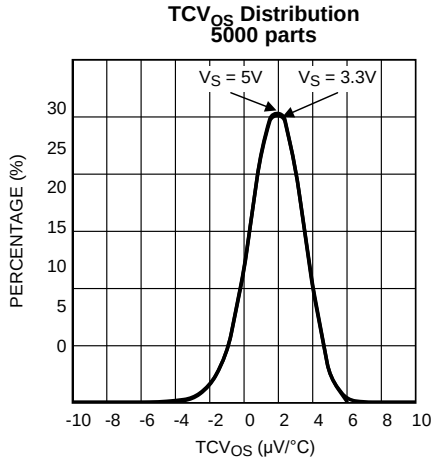


Figure 41.

APPLICATION INFORMATION

GENERAL

The LMP8602 and LMP8603 are fixed gain differential voltage precision amplifiers with a gain of 50x for the LMP8602, and 100x for the LMP8603. The input common mode voltage range is -22V to +60V when operating from a single 5V supply or -4V to +27V input common mode voltage range when operating from a single 3.3V supply. The LMP8602 and LMP8603 are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage the LMP8602 and LMP8603 achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP8602 and LMP8603 will amplify and filter small differential signals in the presence of high common mode voltages.

The LMP8602/LMP8602Q/LMP8603/LMP8603Q use level shift resistors at the inputs. Because of these resistors, the LMP8602/LMP8602Q/LMP8603/LMP8603Q can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

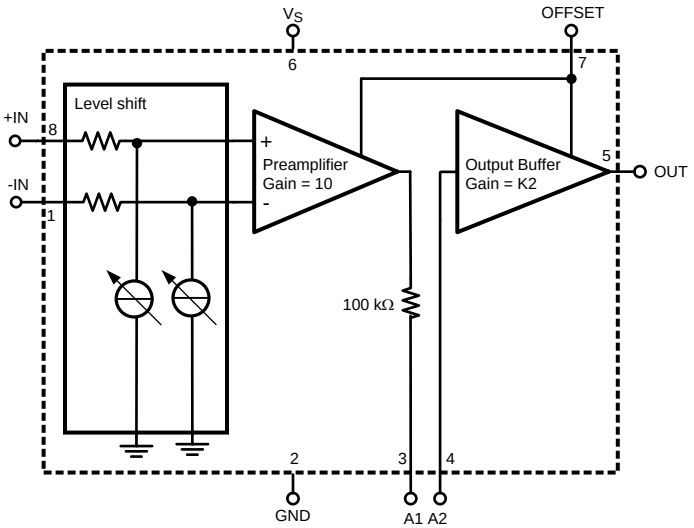
PERFORMANCE GUARANTIES

To guaranty the high performance of the LMP8602/LMP8602Q/LMP8603/LMP8603Q, all minimum and maximum values shown in the parameter tables of this datasheet are 100% tested where all bold limits are also 100% tested over temperature.

THEORY OF OPERATION

The schematic shown in Figure 42 gives a schematic representation of the internal operation of the LMP8602/LMP8603.

The signal on the input pins is typically a small differential voltage across a current sensing shunt resistor. The input signal may appear at a high common mode voltage. The input signals are accessed through two input resistors. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common mode voltage behind these resistors within the supply rails. Subsequently, the signal is gained up by a factor of 10 (K1) and brought out on the A1 pin through a trimmed 100 kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as will be explained in subsequent sections. The signal on the A2 pin is further amplified by a factor (K2) which equals a factor of 5 for the LMP8602 and a factor of 10 for the LMP8603. The output signal of the final gain stage is provided on the OUT pin. The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing as will be explained below.



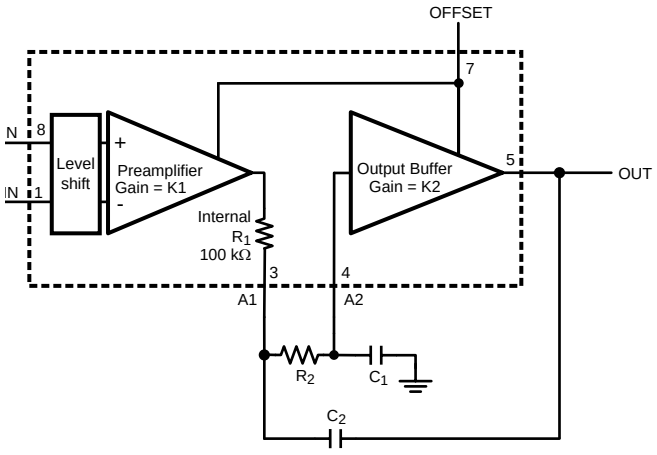
K2 = 5 for LMP8602, K2 = 10 for LMP8603

Figure 42. Theory of Operation

ADDITIONAL SECOND ORDER LOW PASS FILTER

The LMP8602/LMP8602Q/LMP8603/LMP8603Q has a third order Butterworth low-pass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage of the part. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first order low pass filter with a time constant determined by the 100 kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second order Sallen-Key low pass filter as shown in Figure 43 by adding external components R_2, C_1 and C_2. Together with the internal 100 kΩ resistor R_1, this circuit creates a second order low-pass filter characteristic.



K1 = 10, K2 = 5 for LMP8602, K2 = 10 for LMP8603

Figure 43. Second Order Low Pass Filter

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier can be written as:

$$H(s) = \frac{K_1 * K_2 \frac{1}{R_1R_2C_1C_2}}{s^2 + s * \left[\frac{1}{R_1C_2} + \frac{1}{R_2C_2} + \frac{(1 - K_2)}{R_2C_1}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (1)$$

where

- K_1 equals the gain of the preamplifier
- K_2 that of the buffer amplifier

The above equation can be written in the normalized frequency response for a 2nd order low pass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\frac{(j\omega)^2}{\omega_o^2} + \frac{j\omega}{Q\omega_o} + 1} \quad (2)$$

The Cutt-off frequency ω_o in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (3)$$

And the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + (1 - K_2) * R_1C_2} \quad (4)$$

For any filter gain K > 1x, the design procedure can be very simple if the two capacitors are chosen to in a certain ratio.

$$C_2 = \frac{C_1}{K_2 - 1} \tag{5}$$

Inserting this in the above equation for Q results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{R_1 C_1 + R_2 C_1 - \frac{(K_2 - 1) R_1 C_1}{K_2 - 1}} \tag{6}$$

Which results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{C_1 R_2} = \frac{\sqrt{\frac{R_1 R_2}{K_2 - 1}}}{R_2} \tag{7}$$

In this case, given the predetermined value of R1 = 100 kΩ (the internal resistor), the quality factor is set solely by the value of the resistor R_2.

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with the following equation:

$$R_2 = \frac{R_1}{(K - 1) Q^2} \tag{8}$$

For the gain of 5 for the LMP8602 this results in:

$$R_2 = \frac{R_1}{4Q^2} \tag{9}$$

For the gain of 10 for the LMP8603 this is:

$$R_2 = \frac{R_1}{9Q^2} \tag{10}$$

For instance, the value of Q can be set to $0.5\sqrt{2}$ to create a Butterworth response, to $1/\sqrt{3}$ to create a Bessel response, or a 0.5 to create a critically damped response. Once the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C_1 = \frac{(K_2 - 1) Q}{R_1 \omega_0} \tag{11}$$

Which for the gain = 5 will give:

$$C1 = \frac{4Q}{R_1 \omega_0} \tag{12}$$

and for the gain = 10:

$$C_1 = \frac{9Q}{R_1 \omega_0} \tag{13}$$

For C_2 the value is calculated with:

$$C_2 = \frac{C_1}{K_2 - 1} \tag{14}$$

Or for a gain = 5:

$$C_2 = \frac{C_1}{4} \tag{15}$$

and for a gain = 10:

$$C_2 = \frac{C_1}{9} \tag{16}$$

Note that the frequency response achieved using this procedure will only be accurate if the cut-off frequency of the second order filter is much smaller than the intrinsic 60 kHz low-pass filter. In other words, to have the frequency response of the LMP8602/LMP8602Q/LMP8603/LMP8603Q circuit chosen such that the internal poles do not affect the external second order filter.

For a desired Q = 0.707 and a cut off frequency = 3 kHz, this will result for the LMP8602 in rounded values for R2 = 51 kΩ, C1 = 1.5 nF and C2 = 3.9 nF

And for the LMP8603 this will result in rounded values for R2 = 22 kΩ, C1 = 3.3 nF and C2 = 0.39 nF

GAIN ADJUSTMENT

The gain of the LMP8602 is 50 and the gain of the LMP8603 is 100, however, this gain can be adjusted as the signal path in between the two internal amplifiers is available on the external pins.

Reduce Gain

Figure 44 shows the configuration that can be used to reduce the gain of the LMP8602 and the LMP8603 in unidirectional sensing applications.

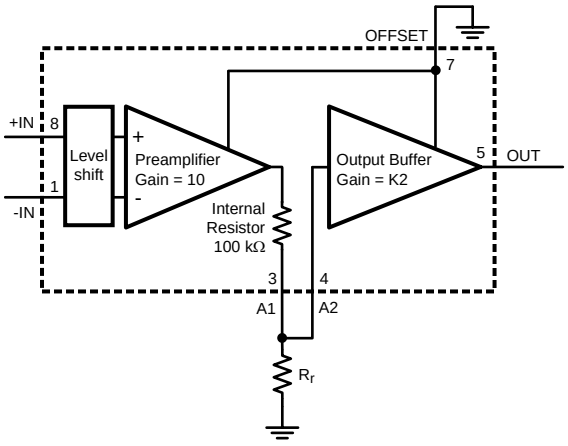


Figure 44. Reduce Gain for Unidirectional Application

R_r creates a resistive divider together with the internal 100 kΩ resistor such that, for the LMP8602, the reduced gain G_r becomes:

$$G_r = \frac{50\ R_r}{R_r + 100\ k\Omega} \tag{17}$$

For the LMP8603:

$$G_r = \frac{100\ R_r}{R_r + 100\ k\Omega} \tag{18}$$

Given a desired value of the reduced gain G_r, using this equation the required value for R_r can be calculated for the LMP8602 with:

$$R_r = 100\ k\Omega\ X\ \frac{G_r}{50 - G_r} \tag{19}$$

and for the LMP8603 with:

$$R_r = 100\ k\Omega\ x\ \frac{G_r}{100 - G_r} \tag{20}$$

Figure 45 shows the configuration that can be used to reduce the gain of the LMP8602 and the LMP8603 in bidirectional sensing applications. The required value for R_r can be calculated with the equations above. The maximum mid-scale offset scaling accuracy of the LMP8602 is ±1% and the maximum mid-scale offset scaling accuracy of the LMP8603 is ±1.5%. The pair of resistors selected have to match much better than 1% and 1.5% to prevent a significant error contribution to the offset voltage.

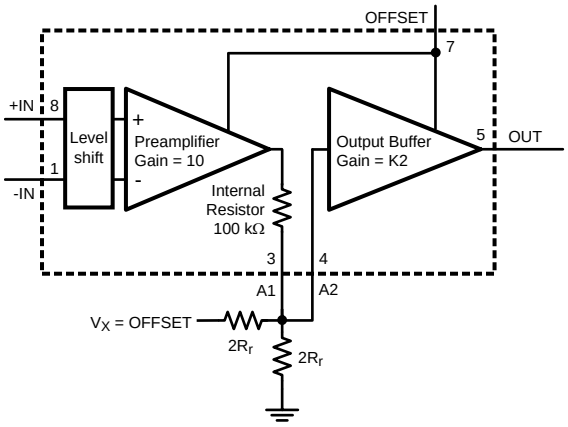


Figure 45. Reduce Gain for Bidirectional Application

Increase Gain

Figure 46 shows the configuration that can be used to increase the gain of the LMP8602/ LMP8602Q/ LMP8603/ LMP8603Q.

R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i for the LMP8602 becomes:

$$G_i = \frac{50\ R_i}{R_i - 400\ k\Omega} \tag{21}$$

and for the LMP8603:

$$G_i = \frac{100\ R_i}{R_i - 900\ k\Omega} \tag{22}$$

From this equation, for a desired value of the gain, the required value of R_i can be calculated for the LMP8602 with:

$$R_i = 400\ k\Omega\ X\ \frac{G_i}{G_i - 50} \tag{23}$$

and for the LMP8603 with:

$$R_i = 900\ k\Omega \times \frac{G_i}{G_i - 100} \tag{24}$$

It should be noted from the equation for the gain G_i that for large gains R_i approaches 100 kΩ x (K_2 - 1). In this case, the denominator in the equation becomes close to zero. In practice, for large gains the denominator will be determined by tolerances in the values of the external resistor R_i and the internal 100 kΩ resistor, and the K_2 gain error. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system will even become unstable. It is recommended to limit the application of this technique to gain increases of a factor 2.5 or smaller.

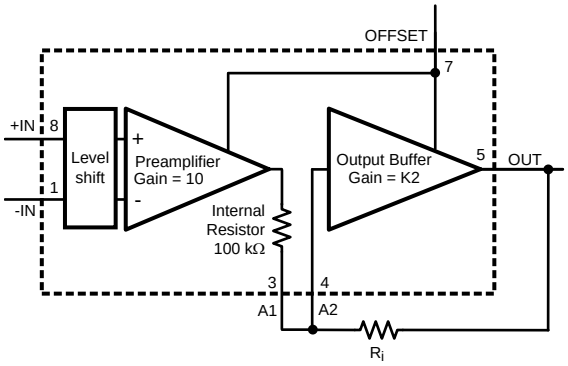


Figure 46. Increase Gain

BIDIRECTIONAL CURRENT SENSING

The signal on the A1 and OUT pins is ground-referenced when the OFFSET pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured. When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. When the offset pin is connected to a voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and V_S/2 by applying twice that voltage from a low impedance source to the OFFSET pin.

With the offset pin connected to the supply pin (V_S) the operation of the amplifier will be fully bidirectional and symmetrical around 0V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S.

Example:

With 5V supply and a gain of 50x for the LMP8602, a differential input signal of +10 mV will result in 3.0V at the output pin. similarly -10 mV at the input will result in 2.0V at the output pin.

With 5V supply and a gain of 100x for the LMP8603, a differential input signal of +10 mV will result in 3.5V at the output pin. similarly -10 mV at the input will result in 1.5V at the output pin. (1)

POWER SUPPLY DECOUPLING

In order to decouple the LMP8602/LMP8602Q/LMP8603/LMP8603Q from AC noise on the power supply, it is recommended to use a 0.1 µF bypass capacitor between the V_S and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 µF bypass capacitor may further reduce the supply noise.

(1) The OFFSET pin has to be driven from a very low-impedance source (<10Ω). This is because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (e.g. a resistive divider between the supply rails) accuracy will decrease.

LAYOUT CONSIDERATIONS

The two input signals of the LMP8602/LMP8602Q/LMP8603/LMP8603Q are differential signals and should be handled as a differential pair. For optimum performance these signals should be closely together and of equal length. Keep all impedances in both traces equal and do not allow any other signal or ground in between the traces of this signals.

The connection between the preamplifier and the output buffer amplifier is a high impedance signal due to the 100 kΩ series resistor at the output of the preamplifier. Keep the traces at this point as short as possible and away from interfering signals.

The LMP8602/LMP8602Q/LMP8603/LMP8603Q is available in a 8–Pin SOIC package and in a 8–Pin VSSOP package. For the VSSOP package, the bare board spacing at the solder pads of the package will be too small for reliable use at higher voltages (V_{CM} > 25V) In this situation it is strongly advised to add a conformal coating on the PCB assembled with the LMP8602/LMP8602Q/LMP8603/LMP8603Q in VSSOP package.

DRIVING SWITCHED CAPACITIVE LOADS

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP8602/LMP8602Q/LMP8603/ LMP8603Q is driving such ADCs the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 47 where the output is connected to a capacitor that is driven by a rail to rail square wave.

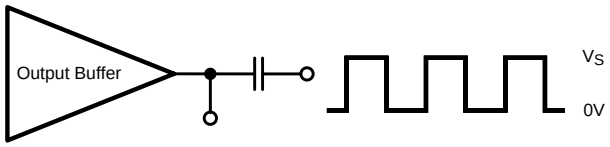


Figure 47. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP8602/LMP8602Q/LMP8603/ LMP8603Q output. The resulting V_{OUT} disturbance signals are shown in Figure 48 and Figure 49.

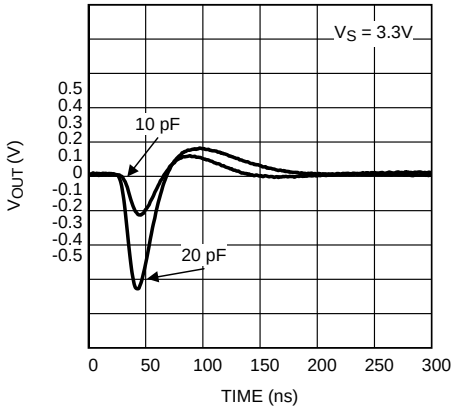


Figure 48. Capacitive Load Response at 3.3V

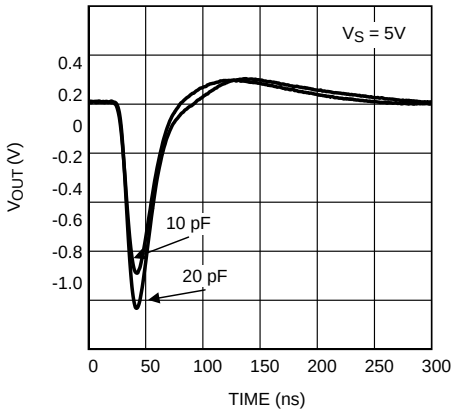


Figure 49. Capacitive Load Response at 5.0V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, an additional RC filter can be placed in between the LMP8602/LMP8602Q/LMP8603/LMP8603Q and the ADC as illustrated in Figure 50.

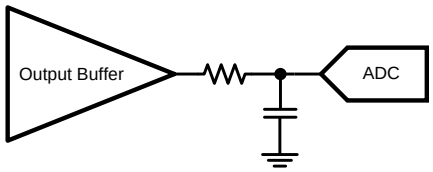


Figure 50. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample and hold capacitor at the input of the ADC and the RC time constant of the external filter should be such that the speed of the system is not affected.

LOW SIDE CURRENT SENSING APPLICATION WITH LARGE COMMON MODE TRANSIENTS

Figure 51 illustrates a low side current sensing application with a low side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common mode voltage range of the LMP8602/LMP8603 and because of the high AC common mode rejection ratio, the LMP8602/LMP8603 is very well suited for this application.

For this application the following example can be used for the calculation of the output signal:

When using a sense resistor, R_{SENSE}, of 0.01 Ω and a current of 1A, then the output voltage at the input pins of the LMP8602 is: $R_{SENSE} * I_{LOAD}$ = 0.01 Ω * 1A = 0.01V

With the gain of 50 for the LMP8602 this will give an output of 0.5V. Or in other words, V_{OUT} = 0.5V/A.

For the LMP8603 the calculation is similar, but with a gain of 100, giving an output of 1 V/A.

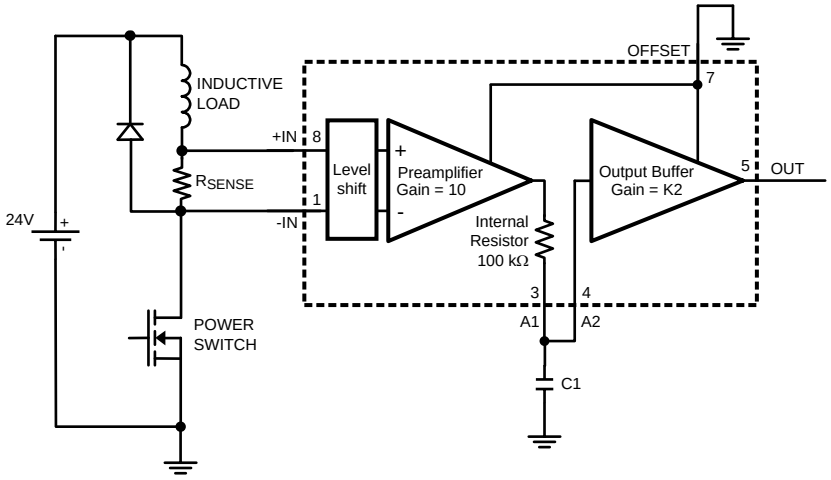


Figure 51. Low Side Current Sensing Application with Large Common Mode Transients

HIGH SIDE CURRENT SENSING APPLICATION WITH NEGATIVE COMMON MODE TRANSIENTS

Figure 52 illustrates the application of the LMP8602/LMP8603 in a high side sensing application. This application is similar to the low side sensing discussed above, except in this application the common mode voltage on the shunt drops below ground when the driver is switched off. Because the common mode voltage range of the LMP8602/LMP8603 extends below the negative rail, the LMP8602/LMP8603 is also very well suited for this application.

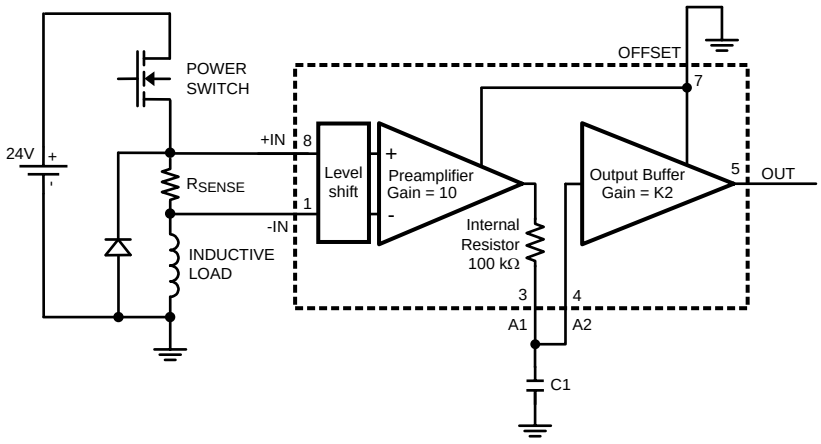


Figure 52. High Side Current Sensing Application with Negative Common Mode Transients

BATTERY CURRENT MONITOR APPLICATION

This application example shows how the LMP8602/LMP8603 can be used to monitor the current flowing in and out a battery pack. The fact that the LMP8602/LMP8603 can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher then the charging current, the output voltage of the LMP8602/LMP8603 will be above the "half offset voltage" for a net current flowing out of the battery. When the charging current is higher then the load current the output will be below this "half offset voltage".

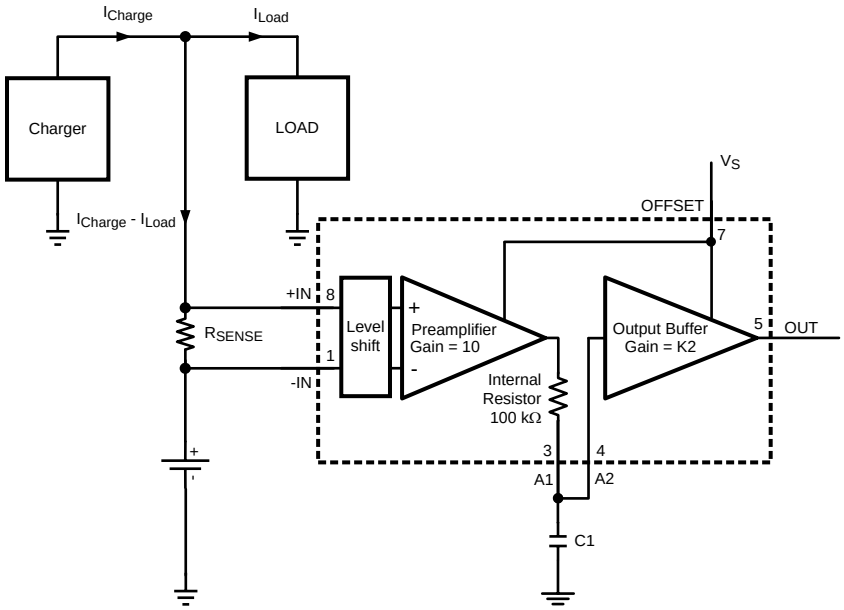
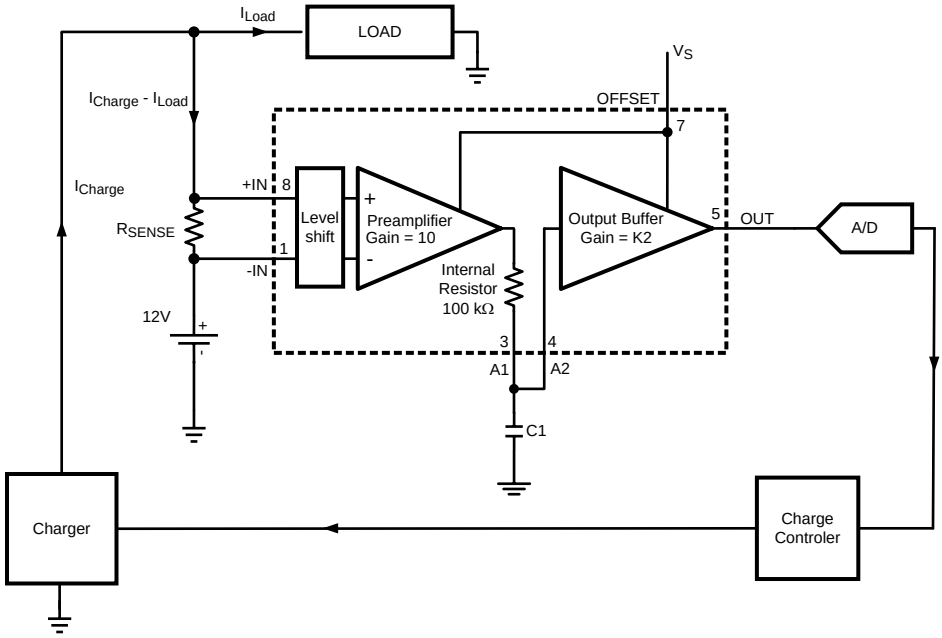


Figure 53. Battery Current Monitor Application

ADVANCED BATTERY CHARGER APPLICATION

The above circuit can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 54. The output signal of the LMP8602/LMP8602Q/LMP8603/LMP8603Q is digitized with the A/D converter and used as an input for the charge controller. The charge controller can be used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery.



K2 = 5 for LMP8602
K2 = 10 for LMP8603

Figure 54. Advanced Battery Charger Application

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP8602MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8602MA	Samples
LMP8602MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8602MA	Samples
LMP8602MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8602QMA	Samples
LMP8602QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8602QMA	Samples
LMP8602QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8602QMME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8602QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8603MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8603MA	Samples
LMP8603MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8603MA	Samples
LMP8603MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8603QMA	Samples
LMP8603QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8603QMA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP8603QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples
LMP8603QMME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples
LMP8603QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LMP8602, LMP8602-Q1, LMP8603, LMP8603-Q1 :

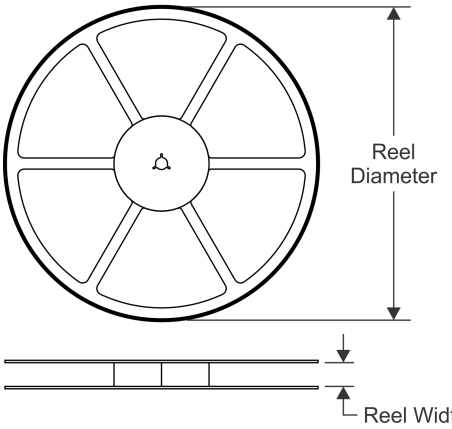
- Catalog: LMP8602, LMP8603
- Automotive: LMP8602-Q1, LMP8603-Q1

NOTE: Qualified Version Definitions:

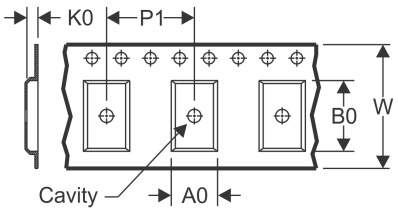
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

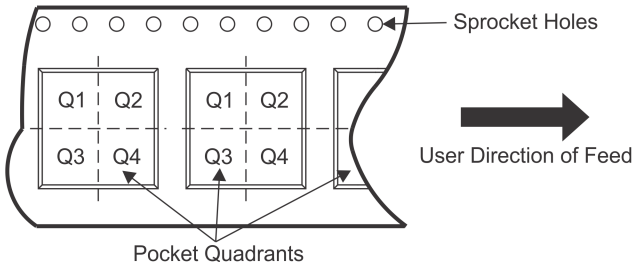


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

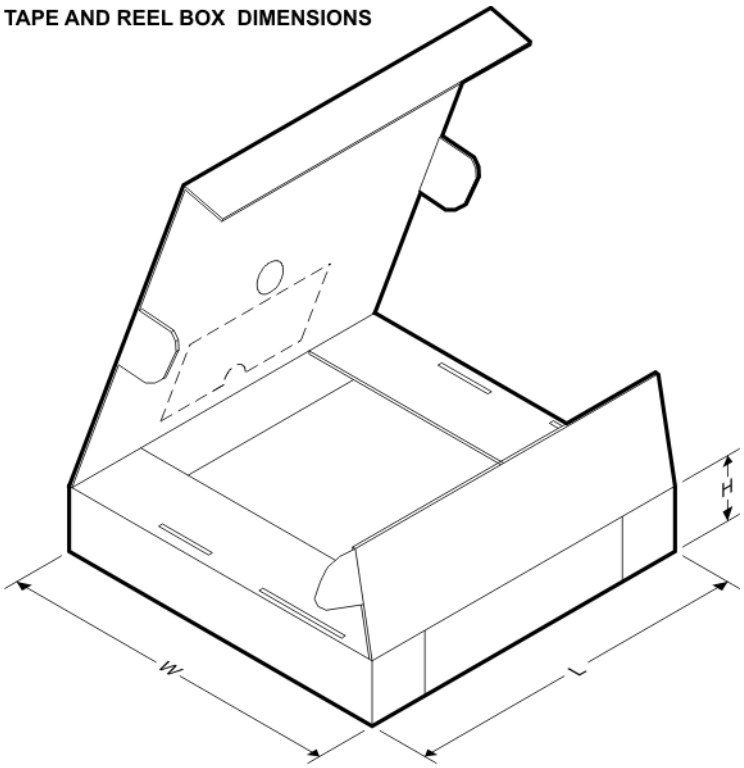
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8602MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8602MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8602QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8603MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8603QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603QMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

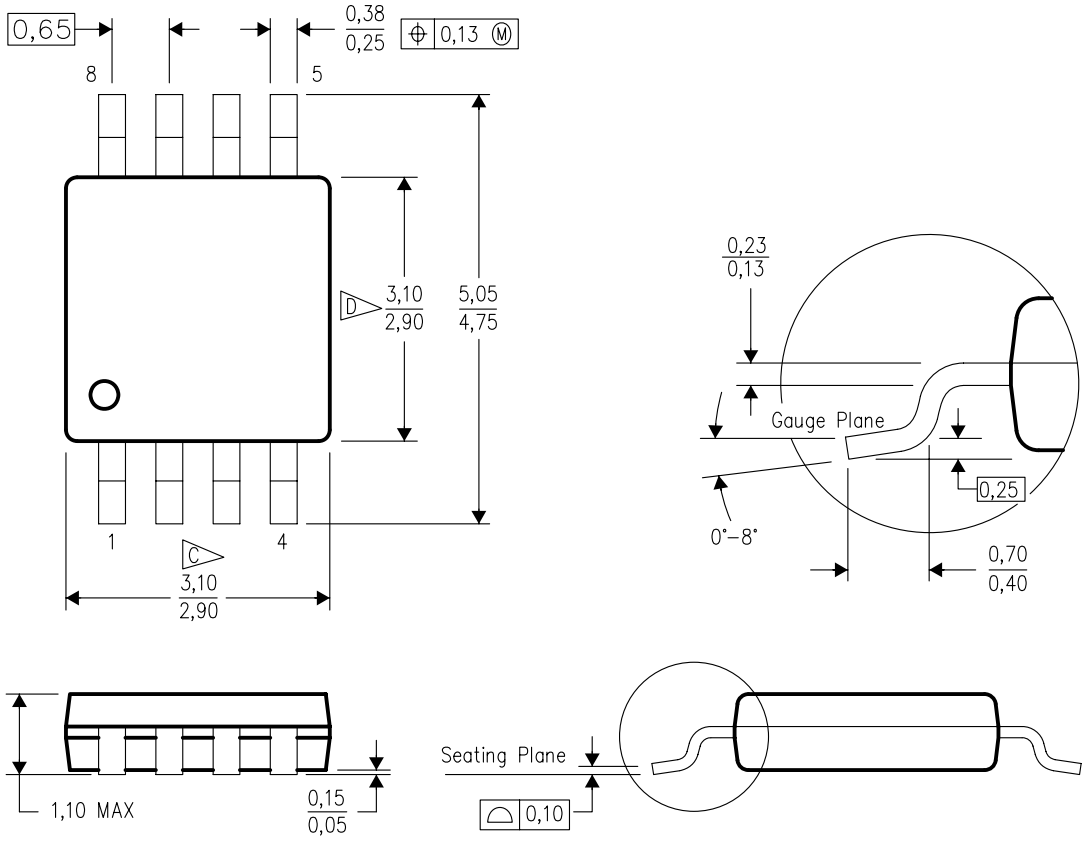
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8602MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8602MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8602MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8602MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8602QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8602QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8602QMME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8602QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8603MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8603MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8603MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8603MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8603QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8603QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8603QMME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8603QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

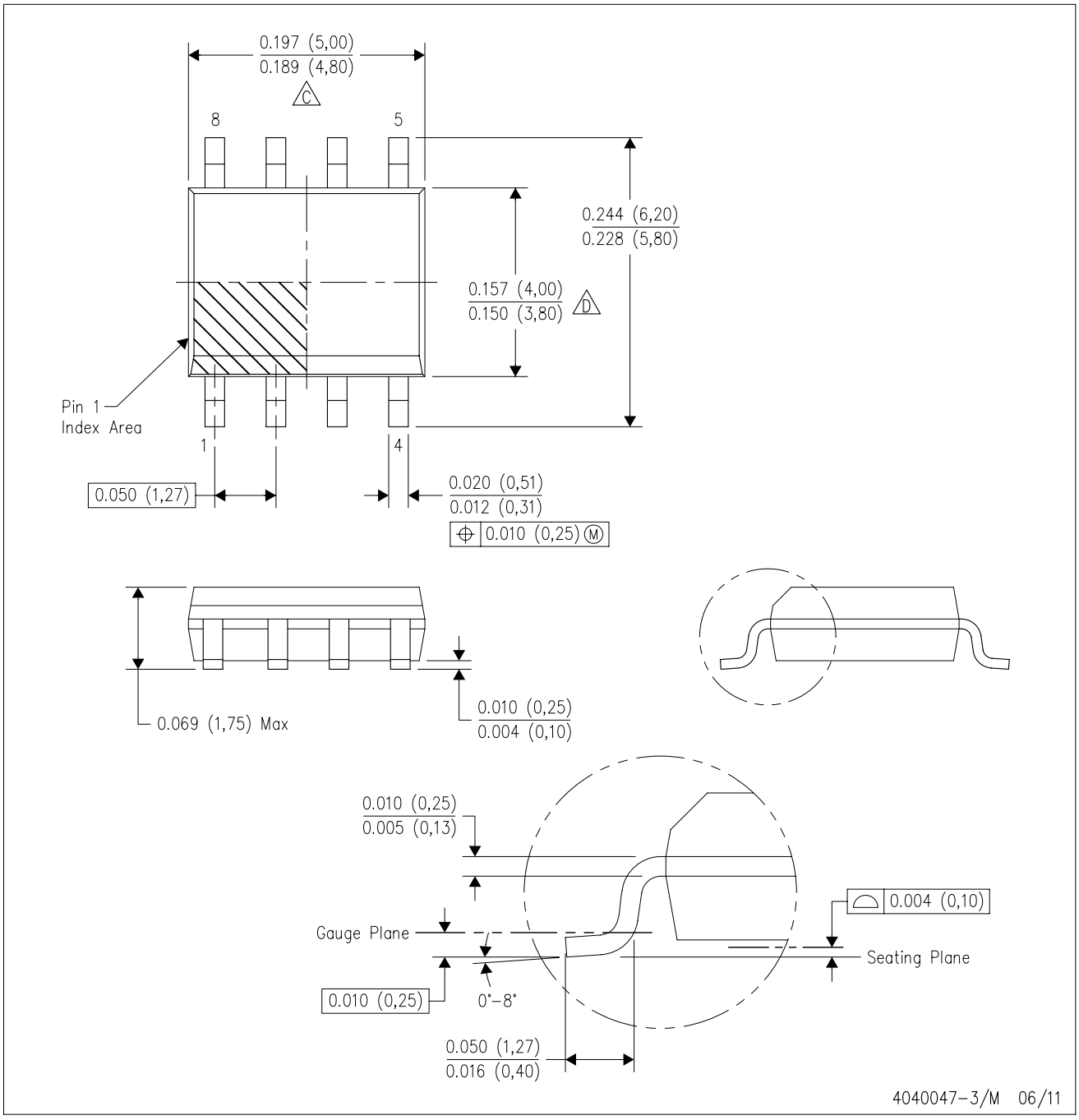
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265