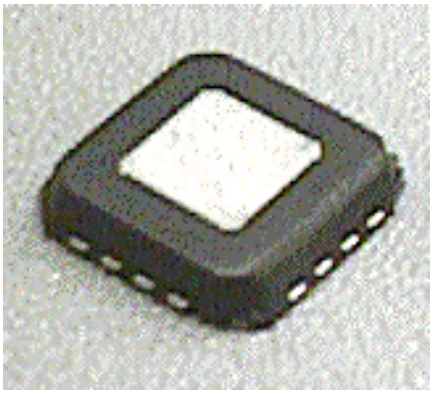
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB31356AFL

1.8GHz,600MHz DUAL-PLL FREQUENCY SYNTHESIZER

The TB31356AFL is a PLL synthesizer used for application of the digital mobile communication and similar other applications. The device features two independently-controllable, built-in PLLs.



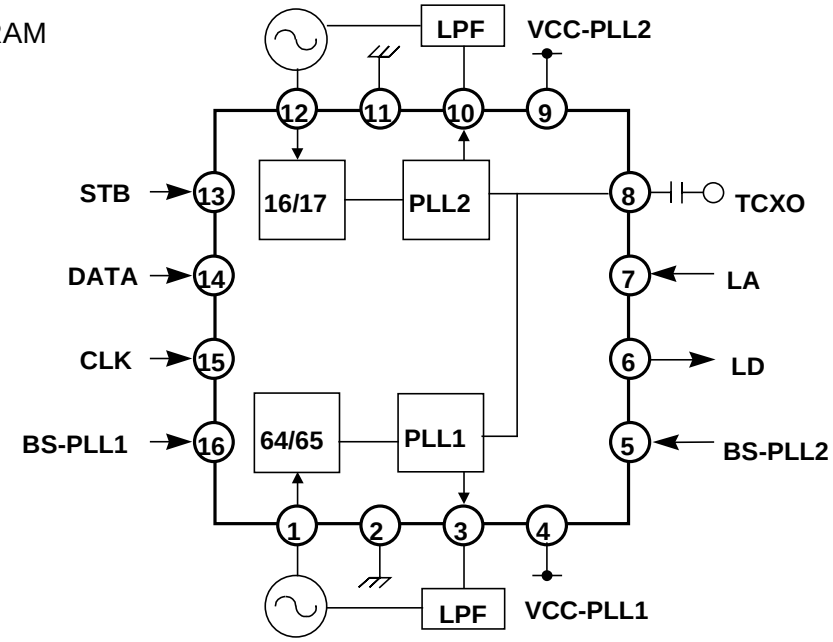
QON16-P-0404-0.65

Weight : 0.04g (Typ.)

FEATURES

- Operating frequency PLL1 : 700 to 1800MHz
  PLL2 : 40 to 600MHz
- Current consumption Total : 3.7mA(PLL1+PLL2+XIN) (Typ.)
  PLL1 : 2.7mA (PLL1+XIN) (Typ.)
  PLL2 : 1.1mA (PLL2+XIN) (Typ.)
  (XIN=0.1mA Typ.)
- Operating voltage : 2.4 to 3.3V
- Independent battery save supported
- Compact leadless package : QON16pin(0.65mm pitch)

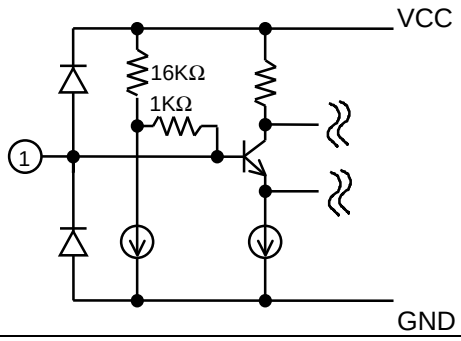
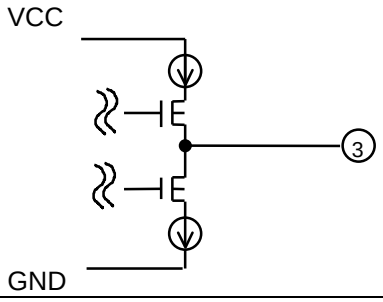
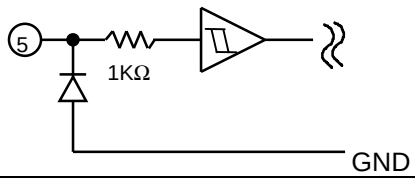
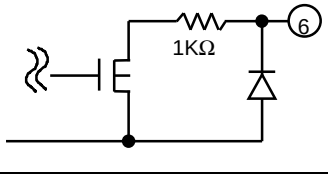
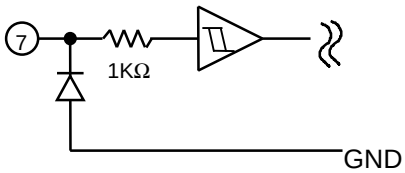
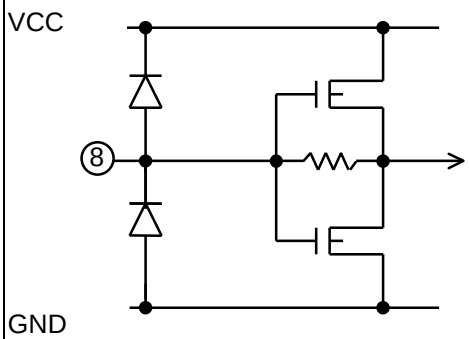
BLOCK DIAGRAM

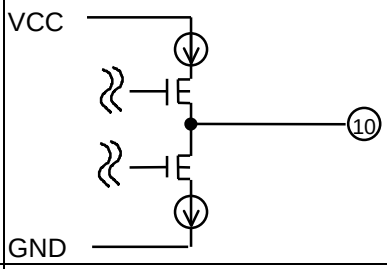
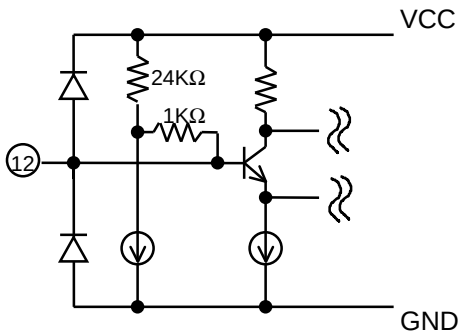
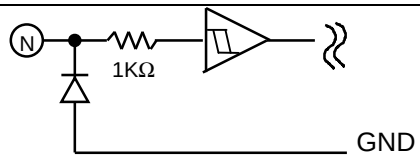


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PIN FUNCTION (The value of resistor and capacitor are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	FIN1	PLL1 prescaler input pin. Inputs frequency from VCO.	
2	GND	Ground pin.	-
3	CP1	Charge pump output pin for PLL1. Constant current output.	
4	VCC-PLL1	Power supply pin (PLL1).	-
5	BS-PLL2	PLL2 battery saving pin.	
6	LD	Lock detection output pin. Open drain output. PLL to be detected can be switched by serial data.	
7	LA	PLL2 setting frequency switch pin.	
8	XIN	Reference oscillator input pin.	
9	VCC-PLL2	Power supply pin (PLL2).	-

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
10	CP2	Charge pump output pin for PLL2. Constant current output.	
11	GND	Ground pin.	-
12	FIN2	PLL2 prescaler input pin. Inputs Frequency from VCO.	
13	STB	Strobe input pin.	 N=13,14,15,16
14	DATA	Data input pin.	
15	CLK	Clock input pin.	
16	BS-PLL1	PLL1 battery saving pin.	

DESCRIPTION OF FUNCTION AND OPERATION

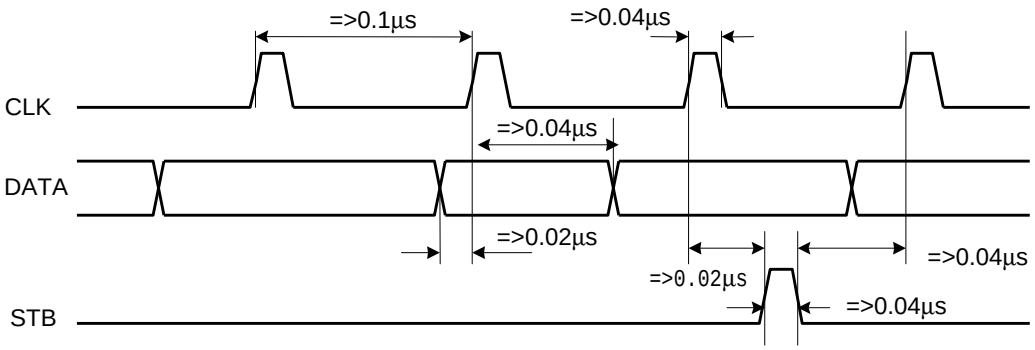
(1) Serial data control

TB31356AFL operates according to serial data program. Serial data is input from the clock (CLK), data (DATA), and strobe (STB) pin.

(2) Entry of serial data

- At the rising edge of each clock pulse, data is sent to the internal shift register from the LSB sequentially. When all the data is sent, set the strobe pin to high. At this rising edge, data is stored in latches depending on the control contents. At the same time as data is stored, control starts.
- The CLK, DATA, and STB pin contain the schmitt trigger circuit to prevent the data errors by noise, etc.
- At power on, send the option control data before any other divider data.

(3) Serial data input timing



(4) Serial data groups and group code

- The IC has control divided into five groups so that they may be controlled independent of one another. Each group is identified by three-bit group code attached at the data end.

Bit before preceding one	Preceding bit	Last bit	Control contents
0	0	0	PLL1 programmable divider (FIN1) data
0	1	0	PLL2 programmable divider (FIN2) data
0	0	1	PLL1 reference divider (XIN) data
0	1	1	PLL2 reference divider (XIN) data
1	0	0	Option Control

(5) PLL1 divider data

- Consist of a 6-bit swallow counter (programmable counter), a 12-bit programmable counter, and a 1/64, 1/65 two modulus prescaler.
- By sending any data to the swallow counter and programmable counter, number of division can be set from 4032 to 262143.

LSB

A0	A1	A2	A3	A4	A5	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	SB1	SB2	SBX	0	0	0
Swallow counter : A						Programmable counter : N												Battery saving			Group code		

Number of divisions = 64N+A (4032 =< Number of divisions =< 262143)
$A=A0+A1*2^{1}.....+A5*2^{5}$ A : Value of A counter
$N=D0+D1*2^{1}+.....+D11*2^{11}$ N : Value of N counter

(6) PLL2 divider data

- Consist of a 4-bit swallow counter (programmable counter), a 11-bit programmable counter, and a 1/16, 1/17 two modulus prescaler.
- By sending any data to the swallow counter and programmable counter, number of division can be set from 240 to 32767.

LSB

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	LA	SB1	SB2	SBX	0	1	0
Swallow counter : A				Programmable counter : N												Battery saving			Group code		

Number of divisions = 16N+A (240 =< Number of divisions =< 32767)
$A=A0+A1*2^{1}.....+A3*2^{3}$ A : Value of A counter
$N=D0+D1*2^{1}+.....+D10*2^{10}$ N : Value of N counter

(7) PLL1 reference divider data

- Consist of a 12-bit reference counter (programmable counter).
- By sending any data to the reference counter, number of division can be set from 4 to 4095

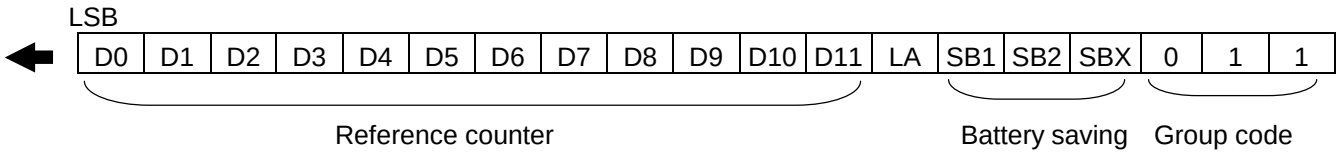
LSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	SB1	SB2	SBX	0	0	1
Reference counter												Battery saving			Group code		

$D=D0+D1*2^{1}+.....D11*2^{11}$
4 =< Number of divisions =< 4095

(8) PLL2 reference divider data

- Consist of a 12-bit reference counter (programmable counter).
- By sending any data to the reference counter, number of division can be set from 4 to 4095.



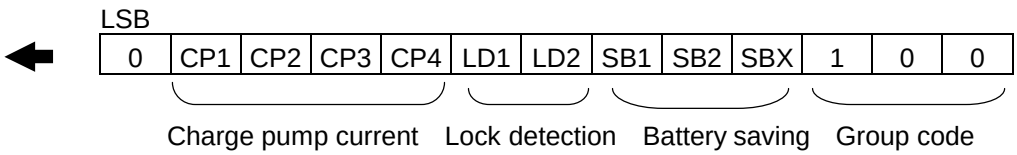
$D=D0+D1*2^{1}+.....D11*2^{11}$

4 =< Number of divisions =< 4095

•PLL2 divider data

LA External Pin	Resistor
L	LA = ”0”
H	LA = ”1”

(9) Option Control



- Charge pump output current

This IC uses a constant current output type charge pump circuit. Output current is varied by serial data “CP1” and “CP2”.

CP1	CP3	PLL1 Charge Pump Output Current
0	0	4mA
0	1	2mA
1	0	1mA
1	1	0.5mA

CP2	CP4	PLL2 Charge Pump Output Current
0	0	4mA
0	1	2mA
1	0	1mA
1	1	0.5mA

l Lock detection

A signal indicating whether the PLL has phase-locked to the desired frequency is presented to the LD pin. The PLL to be detected in this way can be selected by setting two bits, LD1 and LD2, as shown in the table below.

LD1	LD2	Detected PLL
0	0	Not detected (fixed low)
0	1	PLL2
1	0	PLL1
1	1	Only when both PLL1 and PLL2 are detected

Locked in phase = open, Unlocked = low, Power-down mode = open

l Power-down mode

The PLL1, PLL2, and crystal oscillator circuit can be switched between operating and power-down modes by using three bits—SB1, SB2, and SBX. The table below shows how operation is controlled by using these bits and external battery save pins.

External Pin		Serial Data			Operation State		
BS1	BS2	SB1	SB2	SBX	PLL1	PLL2	Buffer
L	L	*	*	*	OFF	OFF	OFF
L	H	*	*	*	OFF	ON	ON
H	L	*	*	*	ON	OFF	ON
H	H	0	0	0	OFF	OFF	OFF
H	H	0	0	1	OFF	OFF	ON
H	H	0	1	*	OFF	ON	ON
H	H	1	0	*	ON	OFF	ON
H	H	1	1	*	ON	ON	ON

Notes1 : ON : operating, OFF : power-down (not operating), * : don't care

Notes2 : Switching between operating and battery saving (power down) mode by using serial data is renewed at the rising edge of strobe signal.

Notes3 : Switching between operating and battery saving (power down) mode by using external pin (BS-PLL1,BS-PLL2) is controlled real-time.

Notes4 : Immediately after power on, need a initial setting by serial data before operation state "ON".

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	VCC-PLL1 , VCC-PLL2	3.6	V
Power Dissipation	PD	240	mW
Input Voltage	CLK , DATA , STB , LA , BS-PLL1 , BS-PLL2	3.6	V
Storage Temperature	Tstg	–55 to +150	°C

Note: The maximum ratings cannot be exceeded even for an instant. Ple ase make sure the device is operated under conditions not exceeding the parameters shown here.

OPERATING RANGES

CHARACTERISTIC	SYMBOL	TEST CIR-CI UT	TEST CONDITION	RANGE	UNIT
Operating Voltage	Vopr	-	Ta=25°C	2.4 to 3.3	V
Operating Temperature	Topr	-		–30 to +85	°C
Operating Frequency	fopr	-	FIN1	700 to 1800	MHz
			FIN2	40 to 600	MHz
			FXIN	5 to 30	MHz
			FCLK	1k to 10M	Hz
Input Operating Voltage	VINopr	-	VIN1	92 to 107	dBμV
			VIN2	92 to 107	dBμV
			VXIN	97 to 113	dBμV
Power Supply Voltage at Stand-by 1	ICCQ1	-	VCC-PLL1 , VCC-PLL2 , BS1="L" , BS2="L"	0 to 10	μA
Low Level Input Voltage	VL(SW)	-	BS State BS-PLL1 , BS-PLL2 , LA, CLK , DATA , STB	–0.2 to VCC*0.2	V
High Level Input Voltage	VH(SW)	-	Active State BS-PLL1 , BS-PLL2 , LA, CLK , DATA , STB	VCC*0.8 to 3.3	V

Note 1: The allowable operating ranges stipulate conditions under which the device's basic functions can operate normally, although accompanied by fluctuations in its electrical characteristics.

Note 2: The unit "dBμV" denotes the level at load-end. (0 dBm = 107 dBμV @50Ω)

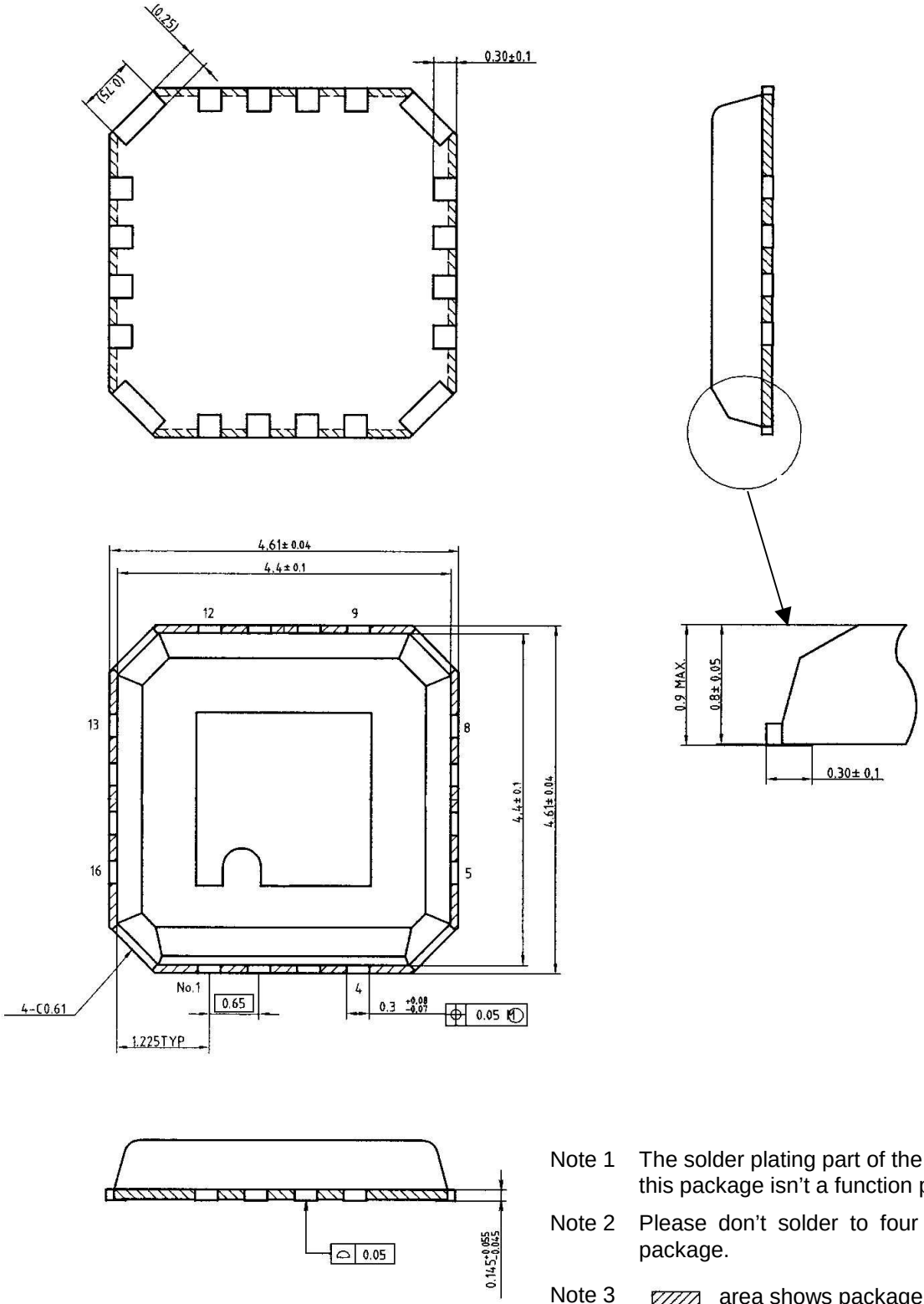
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, FIN1=1619MHz, FIN2=130MHz, XIN=14.4MHz, VCC-PLL1=3.0V, VCC-PLL2=3.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CIUT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Current Consumption 1 at No Signal	Icco1		All Operating (PLL1+PLL2+XIN) VCC-PLL1 , VCC-PLL2 BS1="H" , BS2="H" , SB1="1" , SB2="1"	-	3.7	4.8	mA
Current Consumption 2 at No Signal	Icco2		PLL1 Operating (PLL1+XIN) VCC-PLL1 , VCC-PLL2 BS1="H" , BS2="L"	-	2.7	3.5	mA
Current Consumption 3 at No Signal	Icco3		PLL2 Operating (PLL2+XIN) VCC-PLL1 , VCC-PLL2 BS1="L" , BS2="H"	-	1.1	1.4	mA
Current Consumption 4 at No Signal	Icco4		XIN Operating VCC-PLL1 , VCC-PLL2 BS1="H" , BS2="H" , SB1="0",SB2="0",SB="1"	-	0.10	0.13	mA
PLL1 Charge Pump Output Current 1	ICP1		Vcp1=1/2VCC CP1="0" , CP3="0"	2.8	4.0	5.2	mA
PLL1 Charge Pump Output Current 2	ICP2		Vcp1=1/2VCC CP1="0" , CP3="1"	1.4	2.0	2.6	mA
PLL1 Charge Pump Output Current 3	ICP3		Vcp1=1/2VCC CP1="1" , CP3="0"	0.7	1.0	1.3	mA
PLL1 Charge Pump Output Current 4	ICP4		Vcp1=1/2VCC CP1="1" , CP3="1"	0.35	0.5	0.65	mA
PLL2 Charge Pump Output Current 5	ICP5		Vcp2=1/2VCC CP2="0" , CP4="0"	2.8	4.0	5.2	mA
PLL2 Charge Pump Output Current 6	ICP6		Vcp2=1/2VCC CP2="0" , CP4="1"	1.4	2.0	2.6	mA
PLL2 Charge Pump Output Current 7	ICP7		Vcp2=1/2VCC CP2="1" , CP4="0"	0.7	1.0	1.3	mA
PLL2 Charge Pump Output Current 8	ICP8		Vcp2=1/2VCC CP2="1" , CP4="1"	0.35	0.5	0.65	mA
Charge Pump Off Leak Current	ICP(OFF)		PLL1 , PLL2 , Vcp=1/2VCC	–0.1	0	0.1	μA
LD Output Off Leak Current	ILD		VLD=3.3V	–1	0	1	μA
LD Output On Resistance	RLD(ON)		VLD=0.4V	-	1100	-	Ω

OUTLINE DRAWING

QON16-P-0404-0.65 Unit : mm



Note 1 The solder plating part of the four corners of this package isn't a function pins.

Note 2 Please don't solder to four corners of this package.

Note 3 area shows package thorn.