6/5/4/3/2/1-Phase Synchronous-Rectified Buck Controller for Next Generation GPU Core Power

General Description

The uP1637 is an 6/5/4/3/2/1-phase PWM controller specifically designed to provide high-precision output voltage system for next generation GPUs. The uP1637 works with tables which programed by I2C. The controller also includes programmable output voltage and active voltage positioning functions to adjust the output voltage as a function of the load current, so it is optimally positioned for a load current transient.

The uP1637 adopts continuous DCR current sensing for load line programming and channel current balance. The uP1637 also provides accurate and reliable over current protection, over voltage protection and a delayed power good output. The uP1637 includes an I2C interface, allowing the controller to communicate with other devices. Signals sent over the I2C bus can command the uP1637 to adjust output voltage, switching frequency and operating phase number in different load current state.

The uP1637 is available in VQFN5x5-40L package.

Ordering Information

Order Number	Package	Top Marking
uP1637PQGJ	VQFN5x5- 40L	uP1637P

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

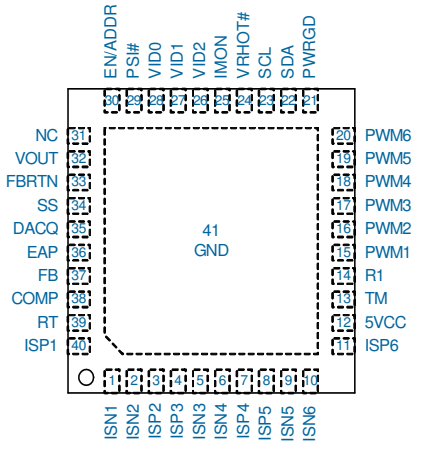
Applications

- GPU Core Power Supplies

Features

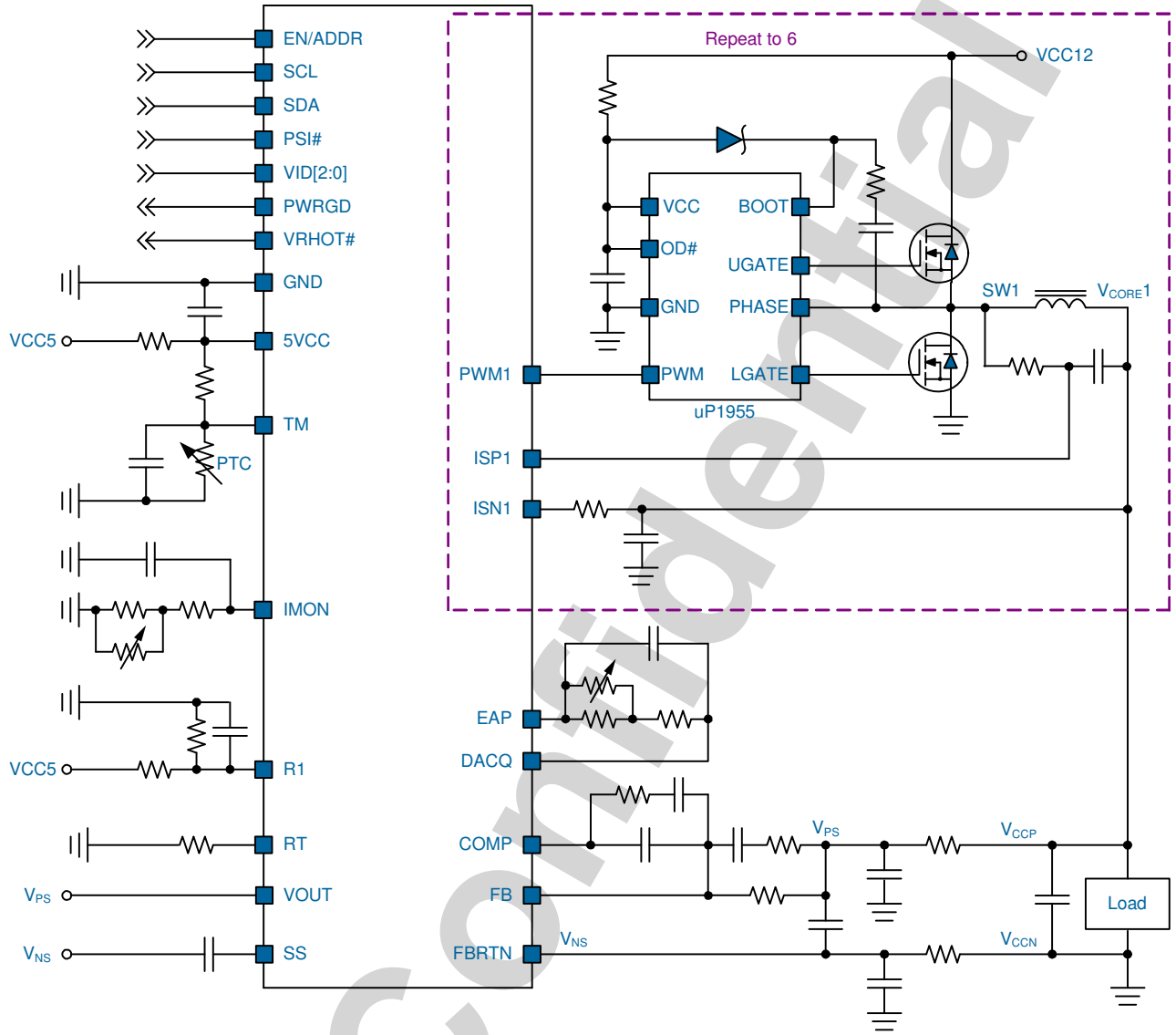
- Selectable 6/5/4/3/2/1-Phase Operation by Hardware Setting
- Precision Core Voltage Regulation
- Differential Remote Voltage Sensing
- Continuous Inductor DCR Current Sensing
- I2C Interface
  - Voltage Adjustment
  - Switching Frequency Adjustment
  - Operating Phase Number Adjustment
- High Accuracy Reference Voltage
  - 0.5% Accuracy
  - Selectable Initial Voltage
  - I2C Programmable Output Voltage
- Over-Current Protection
- Over/Under-Voltage Protection
- Adjustable Soft-Start
- Programmable Operation Frequency from 100kHz to 1MHz per Phase
- RoHS Compliant and Halogen Free

Pin Configuration



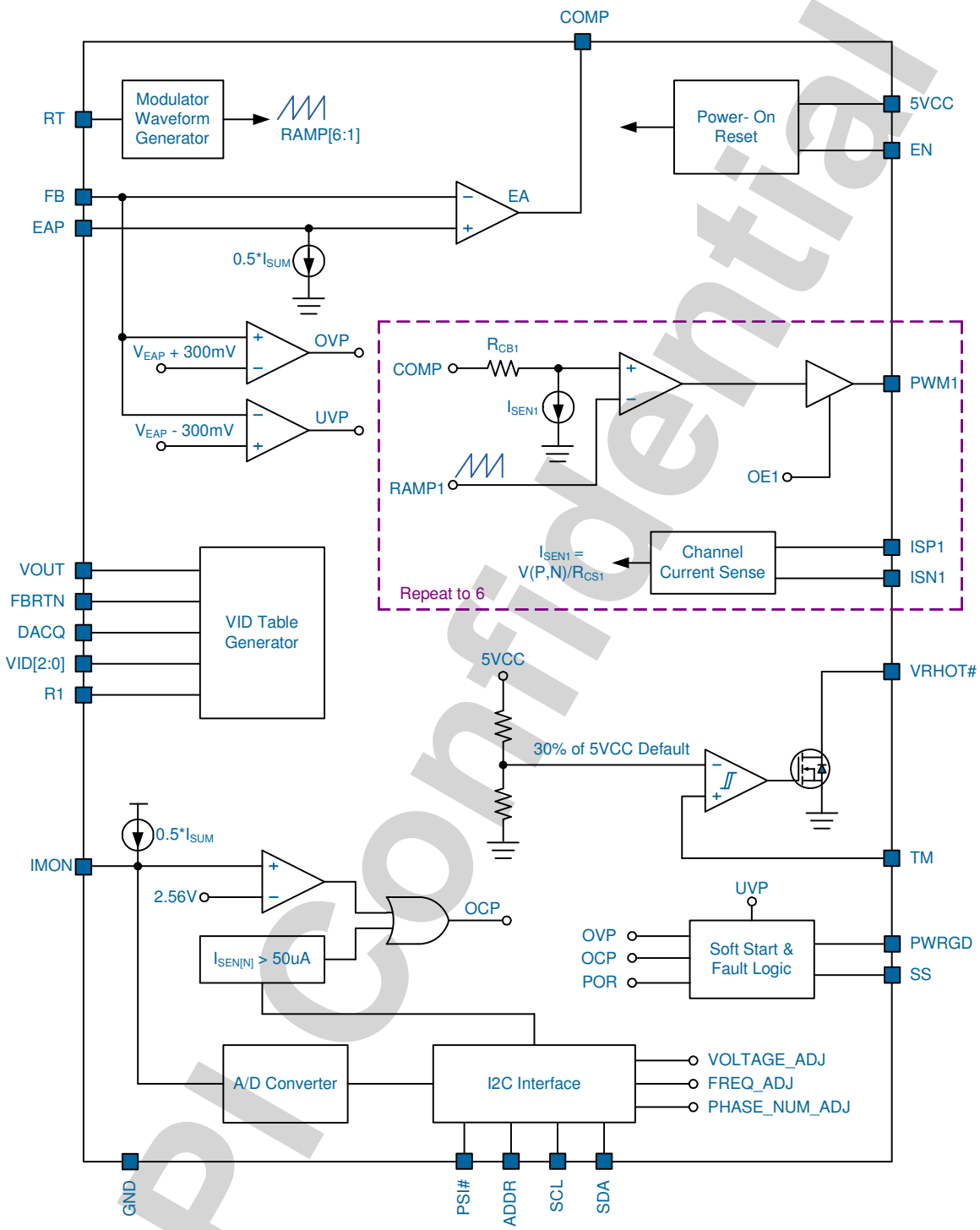
uPI Confidential

Typical Application Circuit



uPI Confidential

Functional Block Diagram



uPI Confidential

Functional Pin Description

No.	Name	Pin Function
1	ISN1	**Inverting Input of the Current Sensing GM Amplifier for Phase 1.** Tie this pin to the midway of VCORE side of channel 1 sensing capacitor. The VCORE side of channel 1 inductor should be placed as close as possible. The resistance between ISN1 to the VCORE side of inductor 1 should be as equal as possible. PCB trace resistance should be taken into consideration.
2	ISN2	**Inverting Input of the Current Sensing GM Amplifier for Phase 2.** Tie this pin to the midway of VCORE side of channel 2 sensing capacitor. The VCORE side of channel 2 inductor should be placed as close as possible. The resistance between ISN2 to the VCORE side of inductor 2 should be as equal as possible. PCB trace resistance should be taken into consideration.
3	ISP2	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 2.** This pin is used for differentially sensing channel 2 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
4	ISP3	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 3.** This pin is used for differentially sensing channel 3 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
5	ISN3	**Inverting Input of the Current Sensing GM Amplifier for Phase 3.** Tie this pin to the midway of VCORE side of channel 3 sensing capacitor. The VCORE side of channel 3 inductor should be placed as close as possible. The resistance between ISN3 to the VCORE side of inductor 3 should be as equal as possible. PCB trace resistance should be taken into consideration.
6	ISN4	**Inverting Input of the Current Sensing GM Amplifier for Phase 4.** Tie this pin to the midway of VCORE side of channel 4 sensing capacitor. The VCORE side of channel 4 inductor should be placed as close as possible. The resistance between ISN4 to the VCORE side of inductor 4 should be as equal as possible. PCB trace resistance should be taken into consideration.
7	ISP4	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 4.** This pin is used for differentially sensing channel 4 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
8	ISP5	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 5.** This pin is used for differentially sensing channel 5 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
9	ISN5	**Inverting Input of the Current Sensing GM Amplifier for Phase 5.** Tie this pin to the midway of VCORE side of channel 5 sensing capacitor. The VCORE side of channel 5 inductor should be placed as close as possible. The resistance between ISN5 to the VCORE side of inductor 5 should be as equal as possible. PCB trace resistance should be taken into consideration.
10	ISN6	**Inverting Input of the Current Sensing GM Amplifier for Phase 6.** Tie this pin to the midway of VCORE side of channel 6 sensing capacitor. The VCORE side of channel 6 inductor should be placed as close as possible. The resistance between ISN6 to the VCORE side of inductor 6 should be as equal as possible. PCB trace resistance should be taken into consideration.
11	ISP6	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 6.** This pin is used for differentially sensing channel 6 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
12	5VCC	**Supply Input for the IC.** Connect this pin to a 5V voltage source with RC filter. Connect this pin to a 5V supply and decouple using a 0.1uF ceramic capacitor.

UPI Confidential

Functional Pin Description

No.	Name	Pin Function
13	TM	**Thermal Monitor.**
14	R1	**Initial Output Voltage Setting.** Connect a voltage divider on this pin to set the VBOOT voltage.
15	PWM1	**PWM Output for Phase 1.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
16	PWM2	**PWM Output for Phase 2.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
17	PWM3	**PWM Output for Phase 3.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
18	PWM4	**PWM Output for Phase 4.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
19	PWM5	**PWM Output for Phase 5.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
20	PWM6	**PWM Output for Phase 6.** Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP1955.
21	PWRGD	**Power Good Indication.** This pin is an open-drain output that indicates the soft start process is complete and no fault happens.
22	SDA	**Data for I2C Interface.** Connect SDA to the bidirectional data line of the I2C bus.
23	SCLK	**Clock for I²C Interface.** Connect SCLK to the clock signal for the I2C bus.
24	VRHOT#	**High Temperature Warning Output.** This pin is set to high impedance when the output voltage is within regulation and pulled low when sensed temperature exceeds over temperature warning level.
25	IMON	**Output Current Indication and Over Current Setting**. Connect a resistor between this pin and GND to set the trigger threshold level for over current protection. This pin also intends for output current indication since its voltage is directly proportional to the output current.
26, 27, 28	VID2/1/0	**Digital Inputs 2/1/0 for Power Play.** See the related sections for detail.

uPI Confidential

Functional Pin Description

No.	Name	Pin Function
29	PSI#	**Power State Indicator Input from GPU.** PSI# is an active low signal. When GPU PSI# goes low, controller will reduce the operating phase number to improve light load efficiency.
30	EN/ADDR	**Chip Enable and Address Selection for I2C Interface.** Pulling this pin lower than 0.4V shuts down the device.The pin also selects which of the two 8-bit slave I2C addresses will be used by the controller. Connecting this pin higher than 2.25V will choose address 8E. Connecting this pin between 1.05V~1.75V will choose address 8C.
31	NC	**Not Connected.**
32	VOUT	**Output Voltage Detection Input.** VOUT is used for voltage regulation. Connect this pin to the VOUT net of VR.
33	FBRTN	**Feedback Return.** VID DAC and error amplifier reference for remote sensing of the output voltage.
34	SS	**Soft Start.** A capacitor connected between SS and FBRTN sets the soft start ramp-up time. Pull this pin to GND will shut down the controller.
35	DACQ	**DAC Output.**
36	EAP	**Non-Inverting Input of the Error Amplifier.** Connect a resistor from this pin to DAC to set the load line slope.
37	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
38	COMP	**Compensation Output.** This pin is the output of the error amplifier
39	RT	**Switching Frequency Programming.** Connect a resistor from this pin to GND to set the switching frequency.
40	ISP1	**Non-inverting Input of the Current Sensing GM Amplifier for Phase 1.** This pin is used for differentially sensing channel 1 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
Exposed Pad		**Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

uPI Confidential

Functional Description

The uP1637 is a 6/5/4/3/2/1-phase, multimode (voltage control, current balance control, loadline control), fixed frequency PWM synchronous-rectified buck controller. The internal VID DAC is designed to interface with the next generation GPUs.

Phase Number of Operation

The uP1637 supports 6/5/4/3/2/1-phase operation. The phase number of operation is set by the status of ISN pins at power on reset. These pins are asserted High if its voltage is higher than (5VCC - 1V). Normally, the uP1637 operates as an 6-phase PWM controller. Connect ISN6 to 5VCC for 5-phase operation; ISN5 to 5VCC for 4-phase operation; ISN4 to 5VCC for 3-phase operation, etc. When operating in 5-phase, PWM6 outputs are set high impedance; in 4-phase, PWM[6:5]; in 3-phase, PWM[6:4], etc. Phase number of operation is decided and latched at each POR rising edge.

Phase Switching Frequency

The phase switching frequency of the uP1637 is set by an external resistor connected between RT pin and GND. The frequency can be calculated as below and follows the graph in Figure 1.

$$F_{SW} = \frac{8.4 \times 10^9}{R_{RT} + 2k\Omega}$$

R_{RT} (kΩ)	F_{SW} (kHz)	R_{RT} (kΩ)	F_{SW} (kHz)
56.52	150	11.73	600
40.92	200	10.52	650
32.01	250	9.47	700
25.9	300	8.81	750
21.7	350	8.28	800
19.07	400	7.71	850
16.45	450	6.92	900
14.66	500	6.46	950
12.99	550	6.15	1000

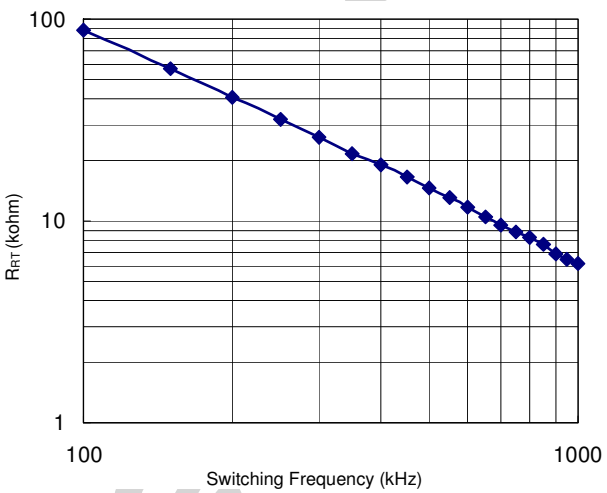


Figure1. R_{RT} vs. Phase Switching Frequency

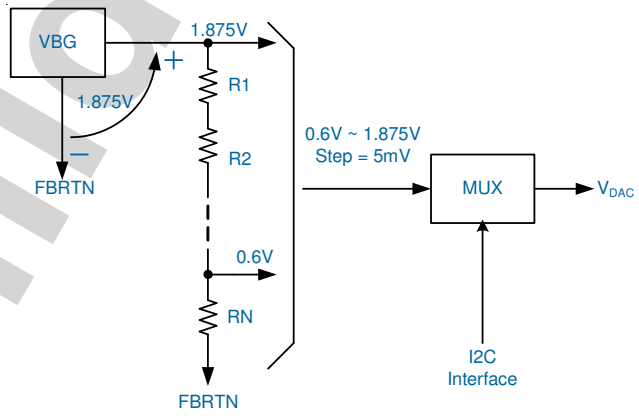


Figure2. V_{DAC} Generator Circuit

The uP1637 builds in a precise bandgap reference circuit as shown in Figure 2. The output voltage of bandgap reference is 1.875V with respective to FBRTN. The uP1637 uses plural resistors to generate precise reference voltages ranging from 0.6V to 1.875V, with 5mV increments. All the voltages connect to a multiplexer (MUX). The multiplexer outputs the selected voltage, V_{DAC} according to the VID inputs and I2C command. Please note that all the voltage values in Figure 2 are referred to FBRTN.

Initial Voltage Setting

The R1 pin is an initial output voltage setting pin as shown in Figure 3.

uPI Confidential

Functional Description

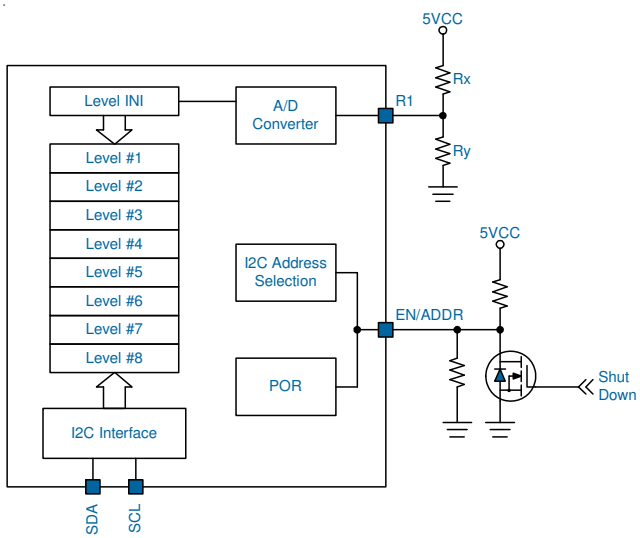


Figure 3. Initial Voltage Setting and Address Selection

The voltage divider at the R1 pin sets the voltage of R1, and the Initial voltage V_INI is decided by the voltage of R1 at $V_{CC}5$ POR rising edge. V_INI is written to Reg0x8B and copied to Reg0xD4/D5/D6/D7/D8/D9/DA/DB. See the related sections for detail.

Chip Enable and Address Selection

Pulling EN/ADDR lower than 0.6V shuts down the device. The pin also selects which of the two 8-bit slave I2C addresses will be used by the controller. Connecting this pin higher than 2.25V will choose address 8E. Connecting this pin between 1.05V~1.75V will choose address 8C.

Power Up Sequence and Power Play

The uP1637 supports selectable initial voltage, parallel VID (PVI), series VID (SVI) and autophase mode. Mode selection is programmed by Reg0xD3[7:6] and Reg0x17[7].

Reg0x17[7]	Reg0xD3[7]	Reg0xD3[6]	Mode
0	0	0	V_INI
0	0	1	PVI
0	1	0	SVI
0	1	1	SVI
1	0	0	Autophase
1	0	1	Autophase
1	1	0	Autophase
1	1	1	Autophase

Figure 4 shows the power up sequence.

The EN/ADDR pin is released and enables the uP1637, programs initial voltage and at the end of T0. There is an extra 400us time delay (T1) before the current source I_{SS} begins charging the C_{SS}. At the end of T1, the uP1637 initiates the soft start cycle. The voltage of DACQ is always ~0.4V lower than SS. 80us after the voltage of DACQ ramping up to the initial voltage V_INI, the uP1637 asserts PWRGD to high.

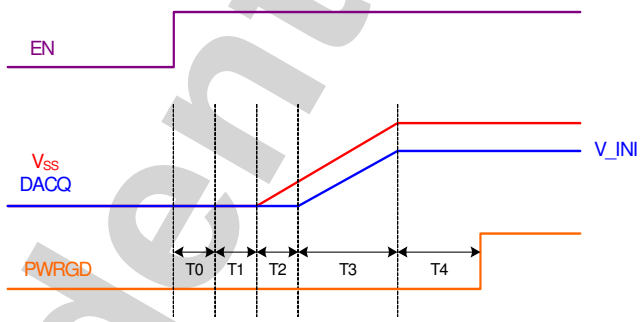


Figure 4. Power Up Sequence

T0 = 300us

T1 = 400us

T2 = 0.4V*C_{SS}/32uA

T3 = V_INI*C_{SS}/32uA

T4 = 80us

Parallel VID

Reg0xD4/D5/D6/D7/D8/D9/DA/DB program the Level #1~#8 voltages for PVI power play that is selected by VID[2:0] as shown in the table below.

VID[2:0]	Level #	Register
[000]	Level #1	D4
[001]	Level #2	D5
[010]	Level #3	D6
[011]	Level #4	D7
[100]	Level #5	D8
[101]	Level #6	D9
[110]	Level #7	DA
[111]	Level #8	DB

UPI Confidential

Functional Description

Output Voltage Differential Sensing

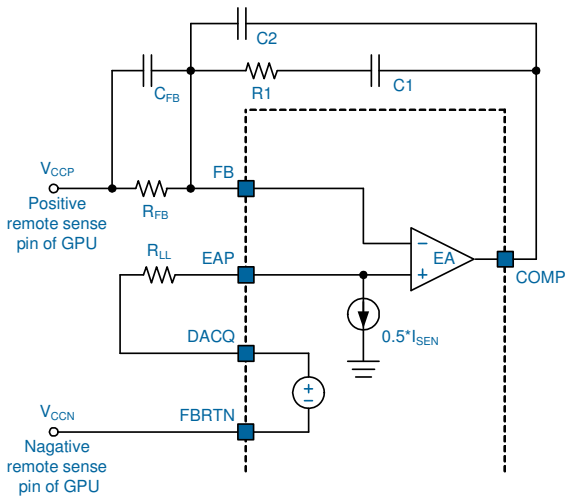


Figure 5. Circuit for V_{OUT} Differential Sensing

The uP1637 uses differential sensing by a high-gain low-offset error amplifier as shown in Figure 5. The GPU voltage is sensed between the FB and FBRTN pins. A resistor R_{FB} connects FB pin and the positive remote sense pin of the GPU V_{CCP}. FBRTN pin connects to the negative remote sense pin of GPU V_{CCN} directly. The error amplifier compares V_{EAP} (= V_{DACQ} - 0.5*I_{SEN} x R_{LL}) with the V_{FB} to regulate the output voltage.

V_INI (0x8B)

This register is the initial voltage V_INI read back.

V_{R1} (% of VCC5)	initial V_{REF} (V)	Reg0x8B
92~100%	0.75	0x1E
82~88%	0.80	0x28
72~78%	0.85	0x32
62~68%	0.90	0x3C
52~58%	0.95	0x46
42~48%	1.00	0x50
32~38%	1.05	0x5A
22~28%	1.10	0x64
12~18%	1.15	0x6E
0~8%	1.20	0x78

CHIPID (Reg0xD0)

This register is the chip ID of the uP1637. The default code is 0x1E.

IMONAD (Reg0xD1)

The voltage V_{IMON} at IMON pin is digitized and stored in register IMONAD[7:0] as:

IMON[7:0] x 10mV < V_{IMON} < IMON[7:0] x 10mV + 10mV

VID Register (Reg0xD2, Reg0xD4 ~ Reg0xDB, Reg0x09 ~ Reg0x10)

Reg0xD2: VID register for SVI.

Reg0xD4: VID register for PVI when VID[2:0] = [000]

Reg0xD5: VID register for PVI when VID[2:0] = [001]

Reg0xD6: VID register for PVI when VID[2:0] = [010]

Reg0xD7: VID register for PVI when VID[2:0] = [011]

Reg0xD8: VID register for PVI when VID[2:0] = [100]

Reg0xD9: VID register for PVI when VID[2:0] = [101]

Reg0xDA: VID register for PVI when VID[2:0] = [110]

Reg0xDB: VID register for PVI when VID[2:0] = [111]

Reg0x09: VID register for autophase mode at load current state 0.

Reg0x0A: VID register for autophase mode at load current state 1.

Reg0x0B: VID register for autophase mode at load current state 2.

Reg0x0C: VID register for autophase mode at load current state 3.

Reg0x0D: VID register for autophase mode at load current state 4.

Reg0x0E: VID register for autophase mode at load current state 5.

Reg0x0F: VID register for autophase mode at load current state 6.

Reg0x10: VID register for autophase mode at load current state 7.

MODE (Reg0xD3[7:6])

MODE[7:6] = [00]: V_INI.

MODE[7:6] = [01]: V_PVI.

MODE[7:6] = [1x]: V_SVI.

OC_CH (Reg0xD3[5:4])

Channel current OCP level adjusting.

OC_CH[5:4] = [00]: Isen = 50uA.

OC_CH[5:4] = [01]: Isen = 60uA.

OC_CH[5:4] = [10]: Isen = 70uA.

OC_CH[5:4] = [11]: Isen = 40uA.

IIC_TM (Reg0xD3[3:0])

VR_HOT and thermal shut down level adjusting.

IIC_TM[3:2] = [00]: VR_HOT# trigger level = 30% of 5VCC

IIC_TM[3:2] = [01]: VR_HOT# trigger level = 40% of 5VCC

uPI Confidential

IIC_TM[3:2] = [10]: VR_HOT# trigger level = 50% of 5VCC

IIC_TM[3:2] = [11]: VR_HOT# trigger level = 60% of 5VCC

IIC_TM[1:0] = [00]: Thermal shut down trigger level = 50% of 5VCC

IIC_TM[1:0] = [01]: Thermal shut down trigger level = 60% of 5VCC

IIC_TM[1:0] = [10]: Thermal shut down trigger level = 70% of 5VCC

IIC_TM[1:0] = [11]: Thermal shut down trigger level = 80% of 5VCC

MISC (Reg0xDC[7:4])

Reg0xDC[7:4] set the watch dog timer.

MISC[7] = 1/0: enable/disable the watch dog timer.

MISC[6]: read only. This bit is set to 1 if time-out happens and is set to 0 if this bit is read.

MISC[5:4] = [00]: Time-out = 400ms.

MISC[5:4] = [01]: Time-out = 800ms.

MISC[5:4] = [10]: Time-out = 1600ms.

MISC[5:4] = [11]: Time-out = 3200ms.

FLAG (Reg0xDD[7:3])

These bits are set to 1 if faults happen.

FLAG[7]: VRHOT# warning.

FLAG[6]: UVP (Under Voltage Protection)

FLAG[5]: OCP (Over Current Protection)

FLAG[4]: TSD (Thermal Shut Down)

FLAG[3]: OVP (Over Voltage Protection)

IICVID (Reg0xDD[2:0])

Read back VID[2:0]

VM Register (Reg0x01 ~ Reg0x07)

VM0~6: Define the 8 load current states (LCS0~7)

LCS0: V(IMON) > VM0[7:0]*10mV, highest load current.

LCS1: VM0[7:0]*10mV > V(IMON) > VM1[7:0]*10mV

LCS2: VM1[7:0]*10mV > V(IMON) > VM2[7:0]*10mV

LCS3: VM2[7:0]*10mV > V(IMON) > VM3[7:0]*10mV

LCS4: VM3[7:0]*10mV > V(IMON) > VM4[7:0]*10mV

LCS5: VM4[7:0]*10mV > V(IMON) > VM5[7:0]*10mV

LCS6: VM5[7:0]*10mV > V(IMON) > VM6[7:0]*10mV

LCS7: VM6[7:0]*10mV > V(IMON), lowest load current.

VM_Hys (Reg0x08[2:0])

Define the V(IMON) hysteresis voltage of entering/exiting LCS.

VM_Hys[2:0] = [000] : 0mV

VM_Hys[2:0] = [001] : 15mV

VM_Hys[2:0] = [010] : 30mV

VM_Hys[2:0] = [011] : 45mV

VM_Hys[2:0] = [100] : 60mV

VM_Hys[2:0] = [101] : 75mV

VM_Hys[2:0] = [110] : 90mV

VM_Hys[2:0] = [111] : 105mV

IICF0 (Reg0x11[7:6]), IICF1 (Reg0x11[5:4]), IICF2 (Reg0x11[3:2]), IICF3 (Reg0x11[1:0]), IICF4 (Reg0x12[7:6]), IICF5 (Reg0x12[5:4]), IICF6 (Reg0x12[3:2]), IICF7 (Reg0x12[1:0])

IICF0~7 define the frequency offset in load current states LCS0~7 respectively.

IICFn[1:0] = [00] => 1.0 x F0

IICFn[1:0] = [01] => 1.2 x F0

IICFn[1:0] = [10] => 1.4 x F0

IICFn[1:0] = [11] => 0.8 x F0

F0 is the frequency set by resister between RT pin and GND.

IICP0 (Reg0x13[7:4]), IICP1 (Reg0x13[3:0]), IICP2 (Reg0x14[7:4]), IICP3 (Reg0x14[3:0]), IICP4 (Reg0x15[7:4]), IICP5 (Reg0x15[3:0]), IICP6 (Reg0x16[7:4]), IICP7 (Reg0x16[3:0])

IICP0~7 define the operating phase number in load current states LCS0~7 respectively.

IICPn[3:0] = [0000] => full-phase set by hardware

IICPn[3:0] = [0001] => 1-phase

IICPn[3:0] = [0010] => 2-phase

IICPn[3:0] = [0011] => 3-phase

IICPn[3:0] = [0100] => 4-phase

IICPn[3:0] = [0101] => 5-phase

IICPn[3:0] = [0110] => 6-phase

IICPn[3:0] = [0111] => 6-phase

IICPn[3:0] = [1xxx] => 6-phase

UPI Confidential

ENABLE (Reg0x17)

ENABLE[7] =1/0: enable/disable AUTOPHASE.

ENABLE[6:5]: Reserved.

ENABLE[4] =1/0: disable/enable DROOP.

ENABLE[3:0]: Reserved.

IMONAD (Reg0x18)

The voltage of IMON pin is digitized and stored in register IMONAD[7:0] as:

IMON[7:0]*10mV < V(IMON) < IMON[7:0]*10mV + 10mV.

PhaseNo (Reg0x19)

PhaseNo[7:4] stores the maximal phase number of operation that is set by ISNn when POR is released. PhaseNo[3:0] stores the present phase number of operation according to load current states.

Channel Current Sensing

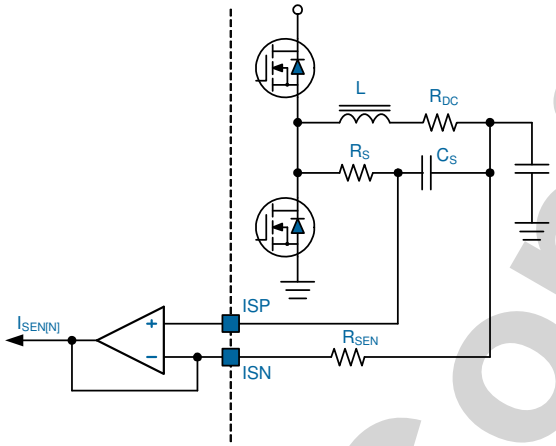


Figure 7. Circuit for Channel Current Sensing

The uP1637 provides low-input-offset current sense amplifier (CSA) to sense the individual inductor current as shown in Figure 7. Output current of CSA ($I_{SEN[N]}$) is used for channel current balance, droop function and over current protection. It is recommended to select larger RC time constant for thermal compensation. That is

R_S x C_S = k x L/R_{DC} , k = 1.2~2.0.

Channel current OCP is set by R_{SEN}. It is recommended to select Rsen ~= 1000 x R_{DC}.

Current Balance

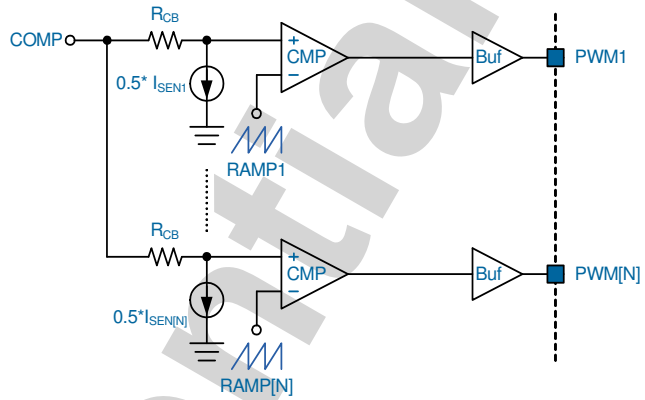


Figure 8. Channel Current Balance

In Figure 8, $I_{SEN[N]}$ is the current signal which is proportional to current flowing through channel N. Larger $I_{SEN[N]}$ will lower the positive input voltage of the corresponding PWM comparator and decrease the PWM duty of the corresponding channel as shown in Figure 8. Eventually, current flowing through each channel will be balanced.

LOADLINE

I_{SEN} in Figure 5 is equal to 0.5*SUM($I_{SEN[N]}$). I_{SEN} flows through R_{LL} and makes V_{EAP} equal to "V_{DACQ}-0.5*I_{SEN}*R_{LL}" In steady state, output voltage is equal to V_{EAP}. Thus, the output voltage decreasing linearly with I_{OUT} is obtained. The loadline is defined as

LL(loadline) = $\Delta V_{OUT}/\Delta I_{OUT}$ = 0.5 * R_{DC} * R_{LL}/R_{SEN}

Over Current Protection (OCP)

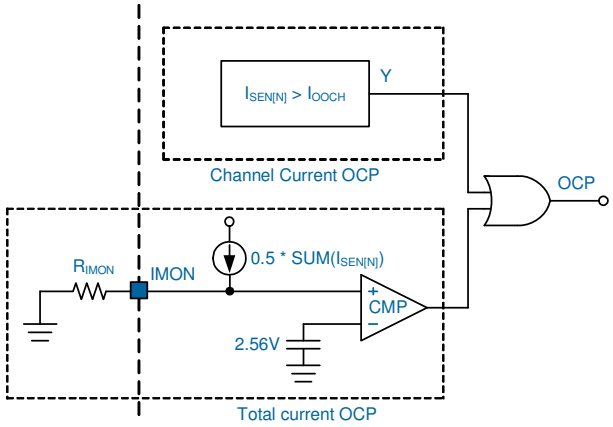


Figure 9. Over Current Protection

The uP1637 provides both channel current OCP and total current OCP as shown in Figure 9.

The total current OCP is activated by monitoring the IMON pin voltage. If V_{IMON} > 2.56V, total current OCP will be

uPI Confidential

triggered. If operating phase number changes, the total current OCP level will be automatically changed in proportion to target operating phase number.

The channel current OCP function provides both current limiting behavior and also latched-off mechanism. The threshold of channel current OCP is set by R_{SEN} resistors as shown in Figure 7. When any particular phase's sensed current fulfills the following criteria:

$I_{SEN[N]} > I_{OCCH}$

where $I_{SEN[N]} = Ich*R_{DC}/R_{SEN}$ and I_{OCCH} = 50uA (default), the particular phase will be forced PWM = low to limit its current. If all operating phases are running under current limiting condition and lasting 80us, the channel current OCP latched-off will be activated.

Both total current OCP and channel current OCP latched-off events trigger the uP1637 to shut down. After OCP shut down, the uP1637 turns off both high-side and low-side MOSFETs of all phases. Only VCC re-POR can release the OCP shut down and re-initiate soft start sequence.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds "V_{EAP} + 300mV", OVP is triggered and latched. uP1637 will try to turn on low side MOSFET and turn off high side MOSFET to protect the GPU. A 20us delay is used in OVP detection circuit to prevent false trigger. Only re-start up can release OVP latch.

Under Voltage Protection (UVP)

The under voltage protection monitors the output voltage via the FB pin. After uP1637 starting up and VOUT ramping up to V_INI, uP1637 initiates UVP function. Once V_{FB} is lower than 160mV or is lower than "V_{EAP} – 300mV", UVP is triggered and latched. uP1637 will try to turn off both low side and high side MOSFET. A 10us delay is used in UVP detection circuit to prevent false trigger. Only re-start up can release UVP latch.

Temperature Monitoring

The VRHOT# is a high temperature warning pin as shown in Figure 10. This pin is an open-drain output pin. When the sensed temperature is over the over temperature warning level, VRHOT# is pulled low. A PTC network is used to monitor the converter temperature. The uP1637 asserts over temperature warning and turns on the internal MOSFET if

$V_{TM} > 0.3*V_{5VCC}$, default value, can be adjusted by I2C.

The uP1637 asserts thermal shutdown and turns off upper/lower MOSFETs if

$V_{TM} > 0.5 * V_{5VCC}$, default value, can be adjusted by I2C.

An NTC network is also OK for temperature monitoring.

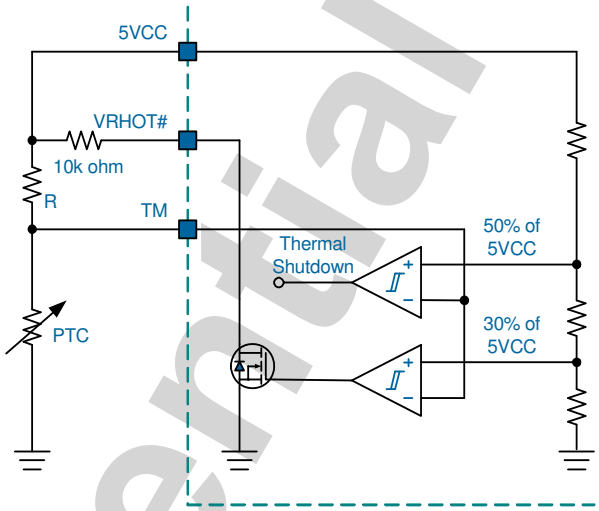


Figure 10. Temperature Monitoring and VRHOT#

Power Saving Mode

The uP1637 accept the PSI signal from GPU to change the operating phase number and improve efficiency over wide range of output current. When $V_{PSI\#} > 2.25V$, the controller operates in full-phase mode, $1.75V > V_{PSI\#} > 0.9V$, the controller operates in 2-phase mode, $V_{PSI\#} < 0.4V$, controller operates with single-phase mode. If the AUTOPHASE function is enabled, operating phase number will be programmed by I2C interface.

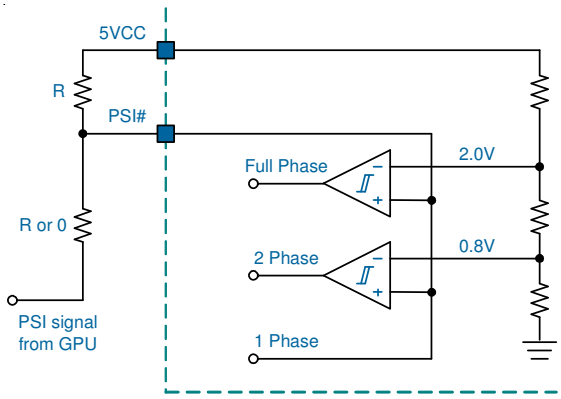
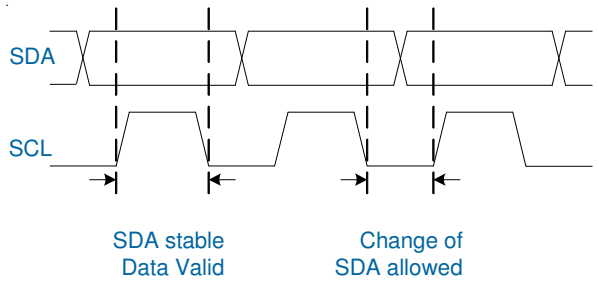


Figure 11. PSI# Function

Data Validity

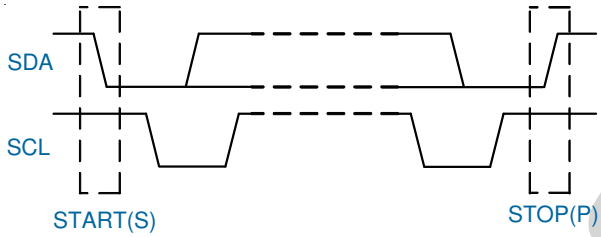
The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to the figure below.

uPI Confidential



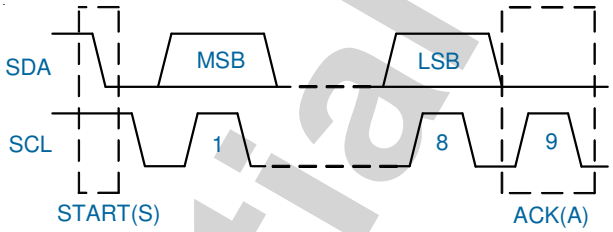
START and STOP Conditions

A START (S) condition is a HIGH to LOW transition of SDA while SCL is HIGH. The STOP (P) condition is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition must be sent before each START condition.



Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address pulls SDA low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Read and Write Protocol

Write to a Single Register

S	slave_addr+W	AS	reg_addr	AS	reg_data	AS	P

Read from a Single Register

S	slave_addr+W	AS	reg_addr	AS	S	slave_addr+R	AS	reg_data	NA	P

S = START, P = STOP, AS = ACK from slave, AM = ACK from master, NA = No ACK

uPI Confidential

Table 1. I2C Registers Summary for PVI and SVI

Reg. Addr.	Type	Name	Default	Description
0x8B	R	V_INI[7:0]	Set by R1	Initial voltage = V_INI[7:0] * 5mV + 600mV
0xD0	R	ChipID[7:0]	1Eh	Chip ID
0xD1	R	IMONAD[7:0]	xxh	V(IMON) = IMON[7:0]*10mV ~ IMON[7:0]*10mV + 10mV
0xD2	R/W	V_SVI[7:0]	Set by R1	V_{REF} for SVI mode = V_SVI[7:0]*5mV + 600mV. Initial value = V_INI[7:0]
0xD3	R/W	MODE[7:6], OC_CH[5:4], TM[3:0]	00h	MODE[7:6]: V_{REF} = V_INI or V_PVI or V_SVI (Priority of 0x17[7] AUTOPHASE = 1 is higher than MODE[7:6]) [00]: V_INI, [01]: V_PVI, [1x]: V_SVI OC_CH[5:4]: Channel current OCP setting [00]: Isens = 50uA(Default). [01]: Isens = 60uA. [10]: Isens = 70uA. [11]: Isens = 40uA TM[3:2]: VR_HOT# warning level setting [00]: 30% of 5VCC(Default). [01]: 40% of 5VCC. [10]: 50% of 5VCC. [11]: 60% of 5VCC TM[1:0]: Thermal shutdown level setting [00]: 50% of 5VCC(Default). [01]: 60% of 5VCC. [10]: 70% of 5VCC. [11]: 80% of 5VCC
0xD4	R/W	V_PVI0[7:0]	Set by R1	V_{REF} when VID[2:0] = [000] at PVI mode, V_{REF}= V_PVI0[7:0]*5mV + 600mV
0xD5	R/W	V_PVI1[7:0]	Set by R1	V_{REF} when VID[2:0] = [001] at PVI mode, V_{REF}= V_PVI1[7:0]*5mV + 600mV
0xD6	R/W	V_PVI2[7:0]	Set by R1	V_{REF} when VID[2:0] = [010] at PVI mode, V_{REF}= V_PVI2[7:0]*5mV + 600mV
0xD7	R/W	V_PVI3[7:0]	Set by R1	V_{REF} when VID[2:0] = [011] at PVI mode, V_{REF}= V_PVI3[7:0]*5mV + 600mV
0xD8	R/W	V_PVI4[7:0]	Set by R1	V_{REF} when VID[2:0] = [100] at PVI mode, V_{REF}= V_PVI4[7:0]*5mV + 600mV
0xD9	R/W	V_PVI5[7:0]	Set by R1	V_{REF} when VID[2:0] = [101] at PVI mode, V_{REF} = V_PVI5[7:0]*5mV + 600mV
0xDA	R/W	V_PVI6[7:0]	Set by R1	V_{REF} when VID[2:0] = [110] at PVI mode, V_{REF} = V_PVI6[7:0]*5mV + 600mV
0xDB	R/W	V_PVI7[7:0]	Set by R1	V_{REF} when VID[2:0] = [111] at PVI mode, V_{REF} = V_PVI7[7:0]*5mV + 600mV
0xDC	R/W	WDT[7:4],xxxx	00h	WDT[7]: Enable watch dog timer WDT[6]: Time-out indicator (If time-out set to 1, cleared after reading, read only) WDT[5:4]: Time-out duration, [11]=>3200ms, [10]=>1600ms, [01]=>800ms, [00]=>400ms
0xDD	R	FLAG[7:3], IICVID[2:0]	xxh	FLAG[7]: VRHOT# warning FLAG[6]: UVP (Under Voltage Protection) FLAG[5]: OCP (Over Current Protection) FLAG[4]: TSD (Thermal Shut Down) FLAG[3]: OVP (Over Voltage Protection) IICVID[2:0]: Read back VID[2:0]

uPI Confidential

Table 2. I2C Register Mapping

Reg Addr	Name	Type	Default Value	Description
0x01	VM0[7:0]	R/W	00h	Set IMON voltage level 0, V_{IMON} > level 0 => LCS0 (highest voltage)
0x02	VM1[7:0]	R/W	00h	Set IMON voltage level 1, level 0 > V_{IMON} > level 1 => LCS1
0x03	VM2[7:0]	R/W	00h	Set IMON voltage level 2, level 1 > V_{IMON} > level 2 => LCS2
0x04	VM3[7:0]	R/W	00h	Set IMON voltage level 3, level 2 > V_{IMON} > level 3 => LCS3
0x05	VM4[7:0]	R/W	00h	Set IMON voltage level 4, level 3 > V_{IMON} > level 4 => LCS4
0x06	VM5[7:0]	R/W	00h	Set IMON voltage level 5, level 4 > V_{IMON} > level 5 => LCS5
0x07	VM6[7:0]	R/W	00h	Set IMON voltage level 6, level 5 > V_{IMON} > level 6 => LCS6, level 6 > V_{IMON} => LCS7
0x08	VM_Hys[2:0]	R/W	00h	Set VM state hysteresis, 0~105mV, 8 steps
0x09	VS0[7:0]	R/W	00h	VID setting register of LS0 in auto-phase mode.
0x0A	VS1[7:0]	R/W	00h	VID setting register of LS1 in auto-phase mode.
0x0B	VS2[7:0]	R/W	00h	VID setting register of LS2 in auto-phase mode.
0x0C	VS3[7:0]	R/W	00h	VID setting register of LS3 in auto-phase mode.
0x0D	VS4[7:0]	R/W	00h	VID setting register of LS4 in auto-phase mode.
0x0E	VS5[7:0]	R/W	00h	VID setting register of LS5 in auto-phase mode.
0x0F	VS6[7:0]	R/W	00h	VID setting register of LS6 in auto-phase mode.
0x10	VS7[7:0]	R/W	00h	VID setting register of LS7 in atuo-phase mode.
0x11	IICFREQ0[7:0] IICF0[7:6]; IICF1[5:4] IICF2[3:2]; IICF3[1:0]	R/W	00h	IICF0[7:6]: freq of LCS0; IICF1[5:4]: freq of LCS1; IICF2[3:2]: freq of LCS2; IICF3[1:0]: freq of LCS3; 00: 1.0xF0; 01: 1.2xF0; 10: 1.4xF0, 11: 0.8xF0
0x12	IICFREQ1[7:0] IICF4[7:6]; IICF5[5:4] IICF6[3:2]; IICF7[1:0]	R/W	00h	IICF4[7:6]: freq of LCS4; IICF5[5:4]: freq of LCS5; IICF6[3:2]: freq of LCS6; IICF7[1:0]: freq of LCS7; 00: 1.0xF0; 01: 1.2xF0; 10: 1.4xF0, 11: 0.8xF0
0x13	IICPHS0[7:0] IICP0[7:4]; IICP1[3:0]	R/W	00h	IICP0[7:4]: phase number of LCS0; IICP1[3:0]: phase number of LCS1; 0000: all phase; 0001: 1 phase; 0010: 2 phase; 0011: 3 phase; 0100: 4 phase ; 0101: 5 phase; 0110: 6 phase; 0111: 6 phase; 1xxx: all phase
0x14	IICPHS1[7:0] IICP2[7:4]; IICP3[3:0]	R/W	00h	IICP2[7:4]: phase number of LCS2; IICP1[3:0]: phase number of LCS3; 0000: all phase; 0001: 1 phase; 0010: 2 phase; 0011: 3 phase; 0100: 4 phase ; 0101: 5 phase; 0110: 6 phase; 0111: 6 phase; 1xxx: all phase
0x15	IICPHS2[7:0] IICP4[7:4]; IICP5[3:0]	R/W	00h	IICP4[7:4]: phase number of LCS4; IICP1[3:0]: phase number of LCS5 0000: all phase; 0001: 1 phase; 0010: 2 phase; 0011: 3 phase; 0100: 4 phase ; 0101: 5 phase; 0110: 6 phase; 0111: 6 phase; 1xxx: all phase
0x16	IICPHS3[7:0] IICP6[7:4]; IICP7[3:0]	R/W	00h	IICP6[7:4]: phase number of LCS6; IICP1[3:0]: phase number of LCS7; 0000: all phase; 0001: 1 phase; 0010: 2 phase; 0011: 3 phase; 0100: 4 phase ; 0101: 5 phase; 0110: 6 phase; 0111: 6 phase; 1xxx: all phase

uPI Confidential

Table 2. I2C Register Mapping (cont).

Reg Addr	Name	Type	Default Value	Description
0x17	EN[7:0]	R/W	00h	Enable[7]: AUTOPHASE = 1, Enable AutoPhase Enable[6:5]: reserved Enable[4]: ENDROOPB = 0, Enable droop Enable[3:0]: reserved.
0x18	IMONAD[7:0]	R	xxh	V_{IMON} = IMON[7:0]*10mV ~ IMON[7:0]*10mV + 10mV
0x19	PhaseNo[7:0]	R	xxh	PhaseNo[7:4]: Maximal phase number PhaseNo[3:0]: Operating phase number

uPI Confidential

Table 3. VID Table for 0x8Bh, 0xD2h, 0xD4h~0xDBh, and 0x09h~0x10h Registers

Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)
0x00	0.600	0x20	0.760	0x40	0.920	0x60	1.080	0x80	1.240	0xA0	1.400	0xC0	1.560	0xE0	1.720
0x01	0.605	0x21	0.765	0x41	0.925	0x61	1.085	0x81	1.245	0xA1	1.405	0xC1	1.565	0xE1	1.725
0x02	0.610	0x22	0.770	0x42	0.930	0x62	1.090	0x82	1.250	0xA2	1.410	0xC2	1.570	0xE2	1.730
0x03	0.615	0x23	0.775	0x43	0.935	0x63	1.095	0x83	1.255	0xA3	1.415	0xC3	1.575	0xE3	1.735
0x04	0.620	0x24	0.780	0x44	0.940	0x64	1.100	0x84	1.260	0xA4	1.420	0xC4	1.580	0xE4	1.740
0x05	0.625	0x25	0.785	0x45	0.945	0x65	1.105	0x85	1.265	0xA5	1.425	0xC5	1.585	0xE5	1.745
0x06	0.630	0x26	0.790	0x46	0.950	0x66	1.110	0x86	1.270	0xA6	1.430	0xC6	1.590	0xE6	1.750
0x07	0.635	0x27	0.795	0x47	0.955	0x67	1.115	0x87	1.275	0xA7	1.435	0xC7	1.595	0xE7	1.755
0x08	0.640	0x28	0.800	0x48	0.960	0x68	1.120	0x88	1.280	0xA8	1.440	0xC8	1.600	0xE8	1.760
0x09	0.645	0x29	0.805	0x49	0.965	0x69	1.125	0x89	1.285	0xA9	1.445	0xC9	1.605	0xE9	1.765
0x0A	0.650	0x2A	0.810	0x4A	0.970	0x6A	1.130	0x8A	1.290	0xAA	1.450	0xCA	1.610	0xEA	1.770
0x0B	0.655	0x2B	0.815	0x4B	0.975	0x6B	1.135	0x8B	1.295	0xAB	1.455	0xCB	1.615	0xEB	1.775
0x0C	0.660	0x2C	0.820	0x4C	0.980	0x6C	1.140	0x8C	1.300	0xAC	1.460	0xCC	1.620	0xEC	1.780
0x0D	0.665	0x2D	0.825	0x4D	0.985	0x6D	1.145	0x8D	1.305	0xAD	1.465	0xCD	1.625	0xED	1.785
0x0E	0.670	0x2E	0.830	0x4E	0.990	0x6E	1.150	0x8E	1.310	0xAE	1.470	0xCE	1.630	0xEE	1.790
0x0F	0.675	0x2F	0.835	0x4F	0.995	0x6F	1.155	0x8F	1.315	0xAF	1.475	0xCF	1.635	0xEF	1.795
0x10	0.680	0x30	0.840	0x50	1.000	0x70	1.160	0x90	1.320	0xB0	1.480	0xD0	1.640	0xF0	1.800
0x11	0.685	0x31	0.845	0x51	1.005	0x71	1.165	0x91	1.325	0xB1	1.485	0xD1	1.645	0xF1	1.805
0x12	0.690	0x32	0.850	0x52	1.010	0x72	1.170	0x92	1.330	0xB2	1.490	0xD2	1.650	0xF2	1.810
0x13	0.695	0x33	0.855	0x53	1.015	0x73	1.175	0x93	1.335	0xB3	1.495	0xD3	1.655	0xF3	1.815
0x14	0.700	0x34	0.860	0x54	1.020	0x74	1.180	0x94	1.340	0xB4	1.500	0xD4	1.660	0xF4	1.820
0x15	0.705	0x35	0.865	0x55	1.025	0x75	1.185	0x95	1.345	0xB5	1.505	0xD5	1.665	0xF5	1.825
0x16	0.710	0x36	0.870	0x56	1.030	0x76	1.190	0x96	1.350	0xB6	1.510	0xD6	1.670	0xF6	1.830
0x17	0.715	0x37	0.875	0x57	1.035	0x77	1.195	0x97	1.355	0xB7	1.515	0xD7	1.675	0xF7	1.835
0x18	0.720	0x38	0.880	0x58	1.040	0x78	1.200	0x98	1.360	0xB8	1.520	0xD8	1.680	0xF8	1.840
0x19	0.725	0x39	0.885	0x59	1.045	0x79	1.205	0x99	1.365	0xB9	1.525	0xD9	1.685	0xF9	1.845
0x1A	0.730	0x3A	0.890	0x5A	1.050	0x7A	1.210	0x9A	1.370	0xBA	1.530	0xDA	1.690	0xFA	1.850
0x1B	0.735	0x3B	0.895	0x5B	1.055	0x7B	1.215	0x9B	1.375	0xBB	1.535	0xDB	1.695	0xFB	1.855
0x1C	0.740	0x3C	0.900	0x5C	1.060	0x7C	1.220	0x9C	1.380	0xBC	1.540	0xDC	1.700	0xFC	1.860
0x1D	0.745	0x3D	0.905	0x5D	1.065	0x7D	1.225	0x9D	1.385	0xBD	1.545	0xDD	1.705	0xFD	1.865
0x1E	0.750	0x3E	0.910	0x5E	1.070	0x7E	1.230	0x9E	1.390	0xBE	1.550	0xDE	1.710	0xFE	1.870
0x1F	0.755	0x3F	0.915	0x5F	1.075	0x7F	1.235	0x9F	1.395	0xBF	1.555	0xDF	1.715	0xFF	1.875

UPI Confidential

Absolute Maximum Rating

Supply Input Voltage, 5VCC (Note 1) ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN5x5-40L θ_{JA} ---------- 36°C/W
VQFN5x5-40L θ_{JC} ---------- 3°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN5x5-40L ---------- 2.78W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +150°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC5} ---------- 4.5V to 5.5V

Electrical Characteristics

(5VCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Input Voltage	V_{CC5}		4.5	--	5.5	V
V_{CC5} POR Threshold			4.0	4.2	4.4	V
V_{CC5} POR Hysteresis		5VCC Falling.	--	0.12	--	V
Supply Current	I_{CC5}	No Switching	--	6	--	mA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Input Bias Current	I_{EA}		-10	--	10	nA
Gain Bandwidth Product	GBW_{EA}		--	10	--	MHz
Voltage Accuracy						
DAC Output Accuracy	V_{FB}	1.0V to 1.875V	-0.5	--	0.5	%
		0.8V to 1.0V	-8	--	8	mV
		0.6V to 0.8V	-10	--	10	mV

UPI Confidential

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Soft Start Current	I_{SS}	Normal	24	32	40	uA
VID Rising Current	I_{SS}	VID transient	--	256	--	uA
EN/ADDR Input						
Chip Eanble Threshold Level	$V_{EN/ADDR}$	$V_{EN/ADDR}$ rising	1.4	--	--	V
Chip Eanble Threshold Level	$V_{EN/ADDR}$	$V_{EN/ADDR}$ falling	--	--	0.4	V
Input Curent	I_{ENPWR}		-1	--	1	uA
VID Input						
VID Input High Threshold Level	$V_{VID[0:2]}$	VID0~VID2 rising	1.4	--	--	V
VID Input Low Threshold Level	$V_{VID[0:2]}$	VID0~VID2 falling	--	--	0.4	V
Oscillator						
Frequency Range	F_{SW}		100	--	1000	kHz
Frequency Variation		R_{RT} = 26kΩ	270	300	330	kHz
Max Duty		R_{RT} = 26kΩ	--	83	--	%
Output Voltage	V_{RT}		0.75	0.80	0.85	V
Current Balance VCCS						
Offset Voltage	$V_{OS(VCCS)}$		-1	--	1	mV
Input Bias Current	I_{EA}		-10	--	10	nA
Gain Bandwidth Product	$G_{BW(VCCS)}$		--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM}$	V_{CC5} = 5V, I_{SOURCE} = 4mA	4.7	--	--	V
PWRGD Ouput						
Output Low Voltage	$V_{OL(PWRGD)}$	I_{SINK} = 4mA	--	--	0.2	V
Current Monitoring						
IMON Output Voltage		Full Load	2.46	2.56	2.66	V
IMON Voltage Variation		Full Load	-6	--	6	%

uPI Confidential

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
OVP Threshold	V_{OVP}	V_{FB}-V_{EAP}	255	300	345	mV
OVP Delay	T_{OVP}		--	20	--	us
UVP Threshold	V_{UVP}	V_{FB}-V_{EAP}	-345	-300	-255	mV
UVP Delay	T_{UVP}		--	10	--	us
Channel Current OCP Delay	T_{OCP1}		--	80	--	us
IMON OCP Level			2.46	2.56	2.66	V
Total Current OCP Delay	T_{OCP2}		--	80	--	us

Note 1. Stresses listed as the above " Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

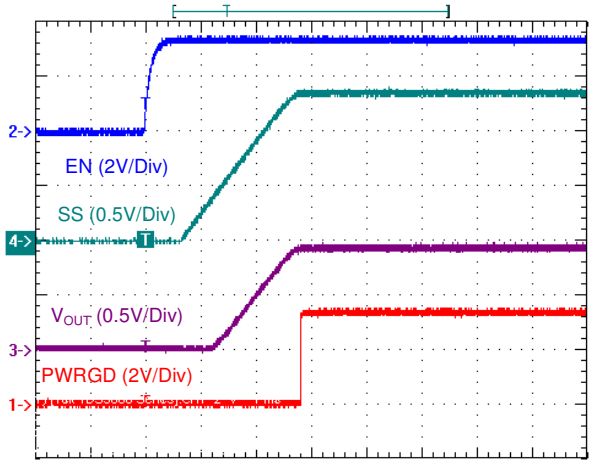
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

uPI Confidential

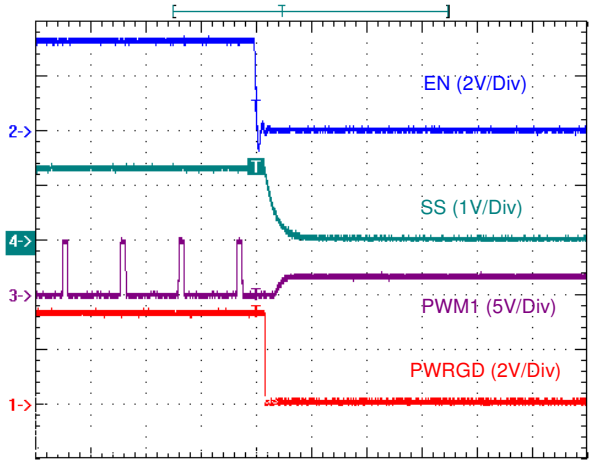
Typical Operation Characteristics

Turn On Waveforms



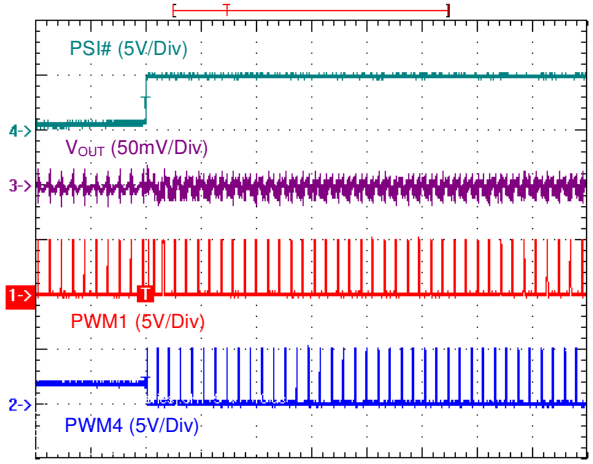
Time (1ms/Div)

Turn Off Waveforms



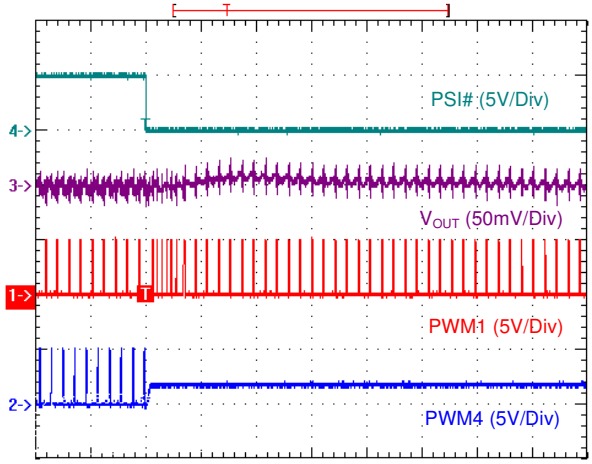
Time (2us/Div)

PSI# Rising



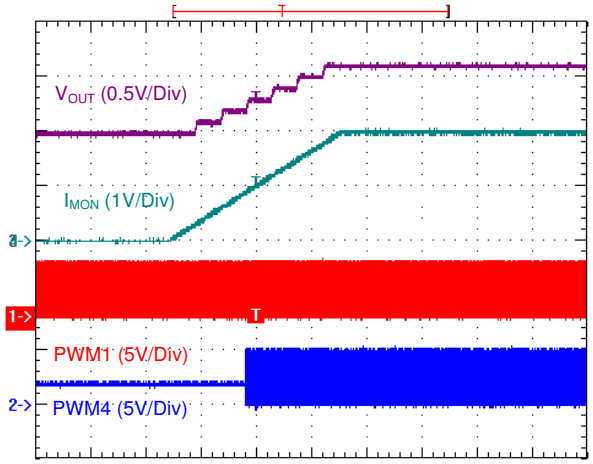
Time (10us/Div)

PSI# Falling



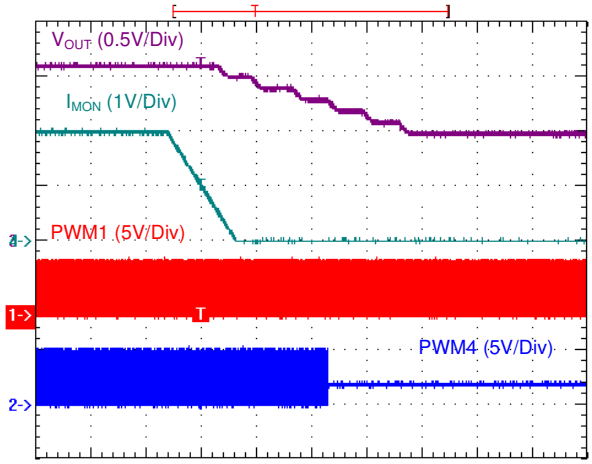
Time (10us/Div)

Auto Phase



Time (400us/Div)

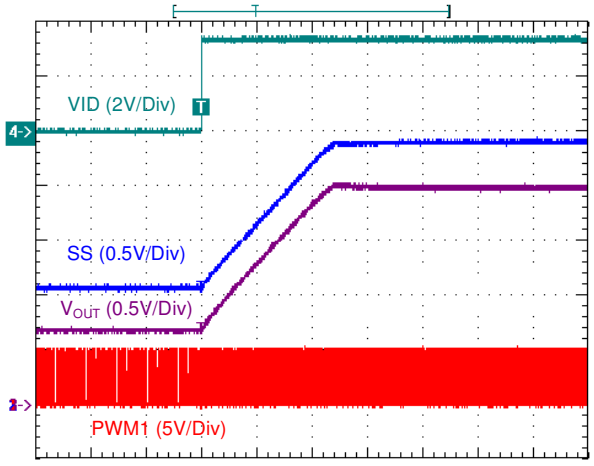
Auto Phase



Time (1ms/Div)

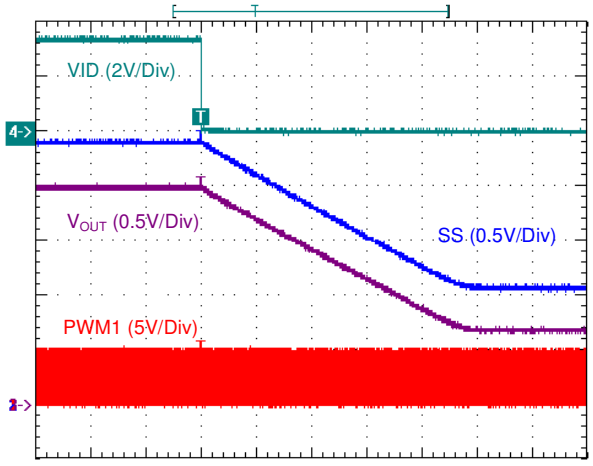
Typical Operation Characteristics

VID High



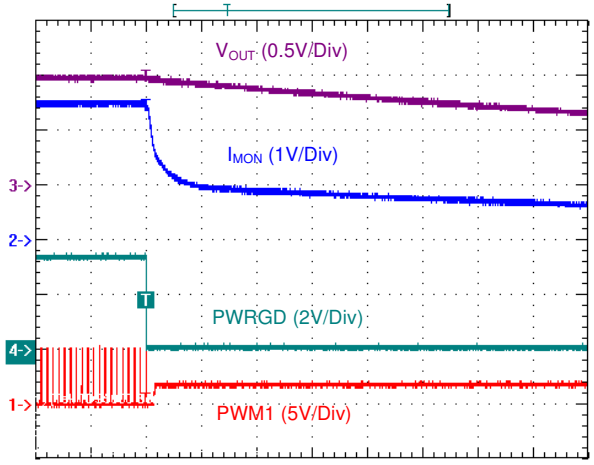
Time (400us/Div)

VID Low



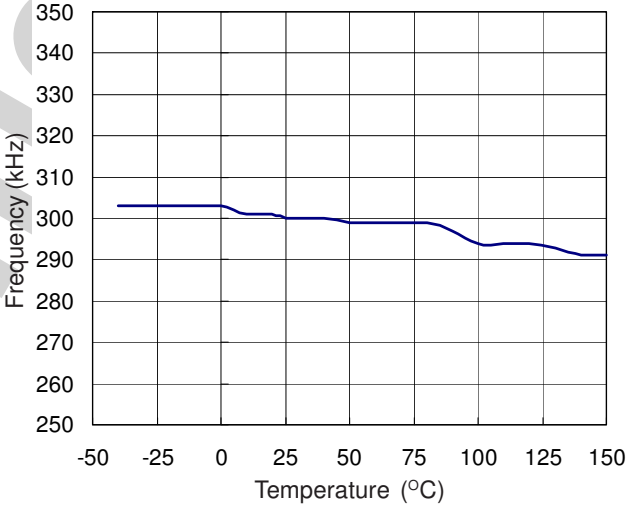
Time (400us/Div)

Over Current Protection

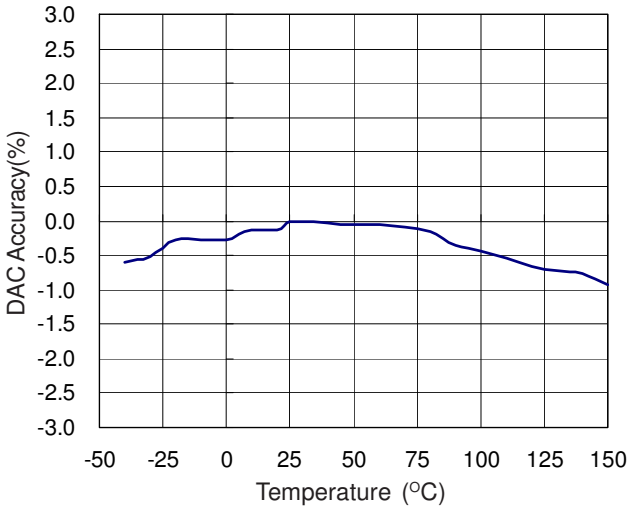


Time (20us/Div)

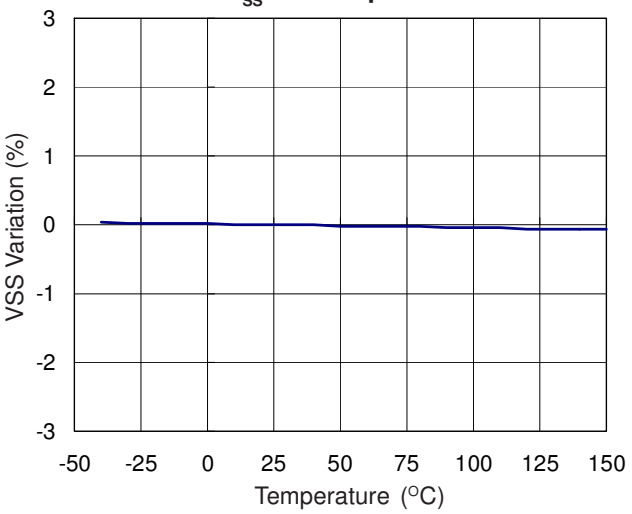
Frequency vs. Temperature



DAC vs. Temperature



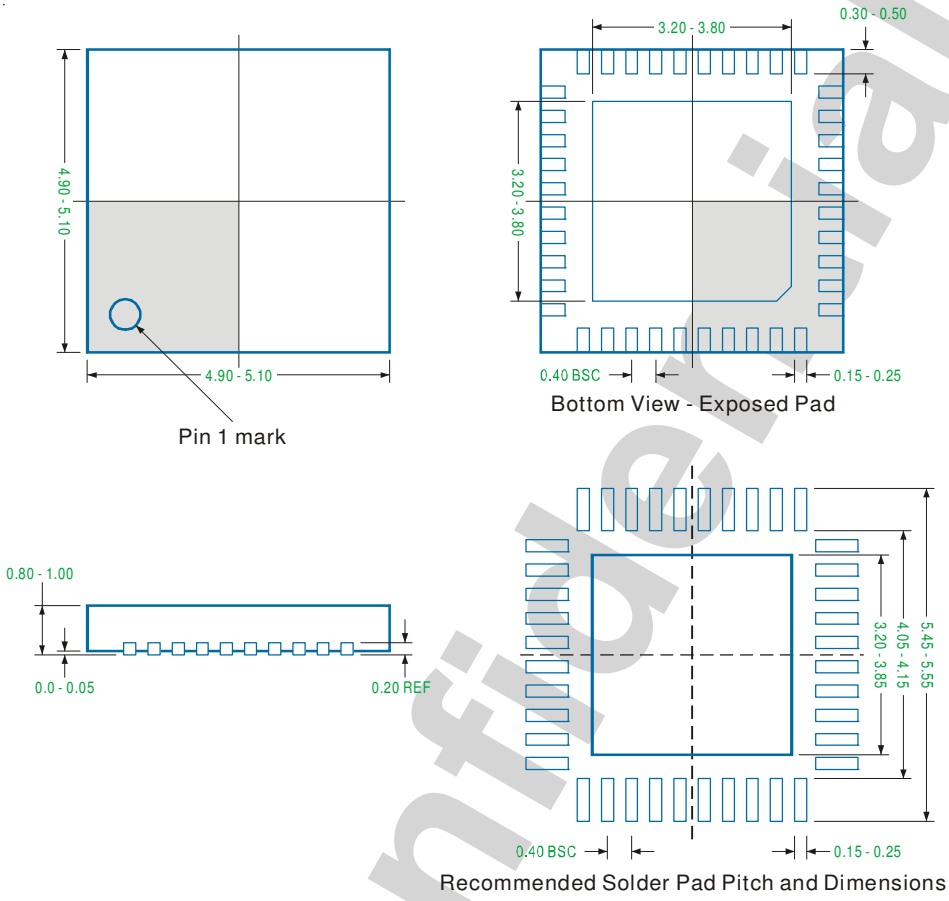
V_{SS} vs. Temperature



Confidential

Package Information

VQFN5x5 - 40L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

uPI Confidential

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

COPYRIGHT (c) 2011, UPI SEMICONDUCTOR CORP.

uPI Confidential

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064