HMC4069LP4E

v02.0316

2.9 GHz INTEGER-N SYNTHESIZER (N = 2 - 32)

Typical Applications

The HMC4069LPE is ideal for:

- Point-to-Point Radios
- Satellite Communication Systems
- Military Applications
- Sonet Clock Generation

Features

Ultra Low SSB Phase Noise Floor:
-151dBc/Hz @ 10kHz offset @ 100MHz

Integrated Output Resistors

Improved Input Sensitivity

Lock Detect and Invert Functionality

24-Pin 4 x 4mm SMT Package

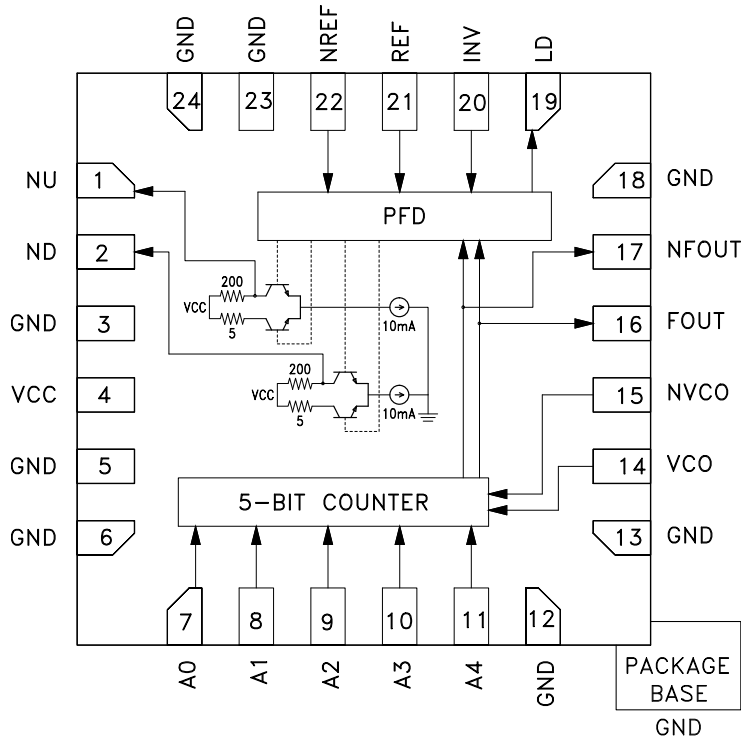
General Description

The HMC4069LP4E is an Integer-N synthesizer which incorporates a 10 to 1300MHz digital phase-frequency detector with a 10 to 2900MHz 5-bit frequency counter. It is intended for use in low phase noise synthesizer applications.

The combination of high frequency of operation along with its ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast switching and very low phase noise. When used in conjunction with a differential loop amplifier, the HMC4069LP4E generates output voltages that can be used to phase lock a VCO to a reference oscillator.

The device is packaged in a 24-pin, 4 x 4mm leadless QFN surface mount package with an exposed ground paddle for improved RF and thermal performance.

Functional Diagram



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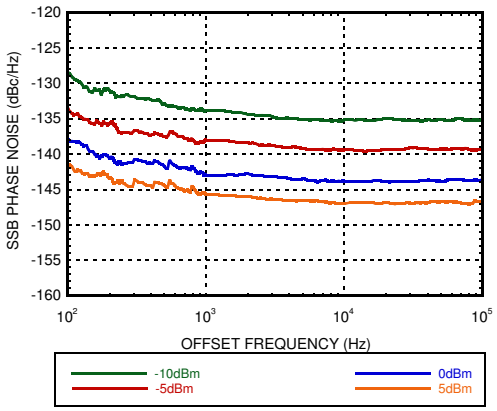
Electrical Specifications, T_A = +25° C, Vcc = 5.0V

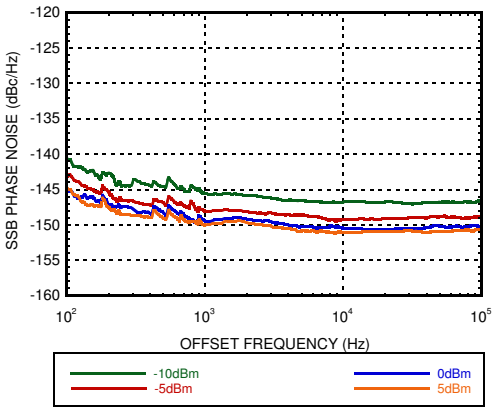
Parameter	Conditions	Min.	Typ.	Max.	Units
REF Input Frequency	Min must be Square Wave Max can be Sine or Square Wave	10	100	1300	MHz
VCO Input Frequency		10		2900	
Input Power Range		-10	5	+5	dBm
Programmable Division Ratios (A0 - A4)		2		32	
Output Voltage Swing (NU / ND)	Driving High-Z Load / Op-Amp		2		Vp-p
PFD Gain	Gain = Vpp / 2∏ Rad		0.32		V / Rad
SSB Phase Noise [1]	@ 10kHz Offset with 100 MHz REF / VCO @ +5 dBm		-151		dBc/Hz
Logic Input Voltages (INV, A0 - A4)	CMOS / TTL Logic Low CMOS / TTL Logic High	0.0 1.8		1.1 5.0	V
Lock Detect Output Voltage	Filtering & 1kΩ Pull-Up Required CMOS / TTL Logic Low = Unlocked MOS / TTL Logic High = Locked	0.0 2.7		0.5 5.0	V
Lock Detect Sink Current			5		mA
Supply Voltage (Vcc)		4.75	5.00	5.25	V
Supply Current (Icc)	Vcc = 5.0V		295		mA
Test Port Output Voltage (FOUT / NFOUT)	Driving High-Z Load Only		300		mVp-p
Temperature Range		-40		+85	°C

[1] Square wave input achieves best phase noise at lower REF/VCO frequencies (see comparison plots on preceding page)

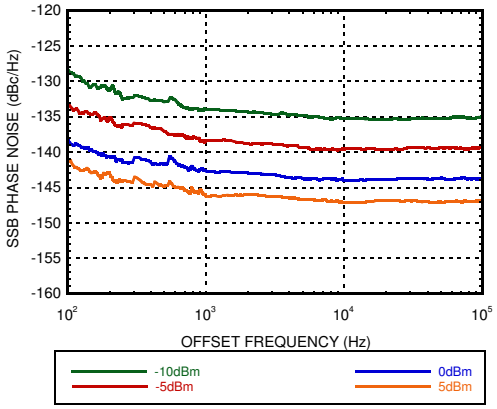
Phase Noise Floor, Vcc = 4.75V REF = 100MHz Sine Wave



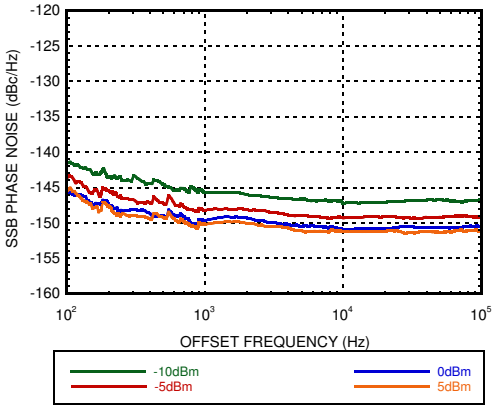
Phase Noise Floor, Vcc = 4.75V REF = 100MHz Square Wave



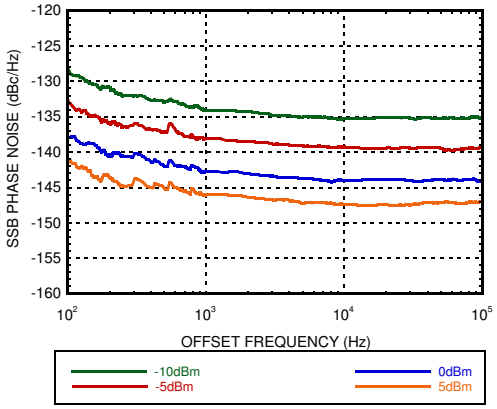
Phase Noise Floor, Vcc = 5.00V REF = 100MHz Sine Wave



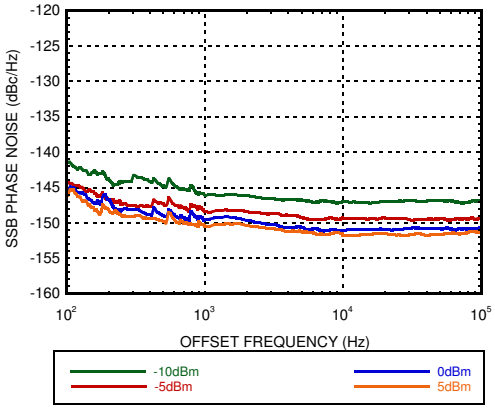
Phase Noise Floor, Vcc = 5.00V REF = 100MHz Square Wave



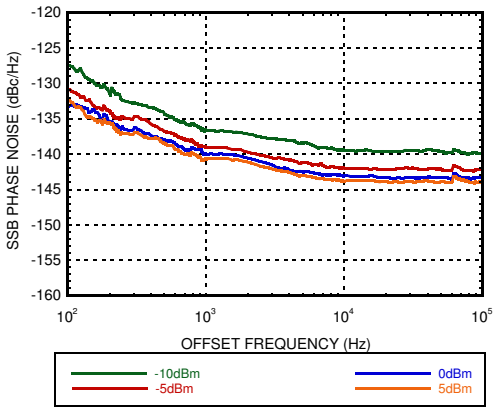
Phase Noise Floor, Vcc = 5.25V REF = 100MHz Sine Wave



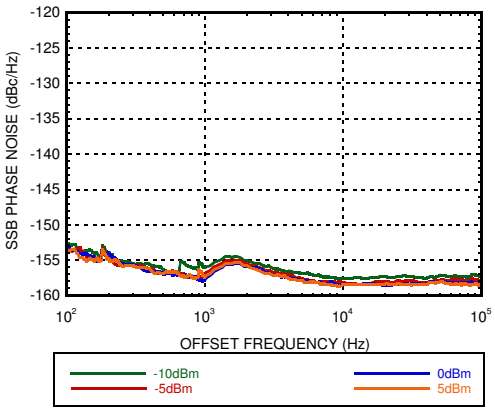
Phase Noise Floor, Vcc = 5.25V REF = 100MHz Square Wave



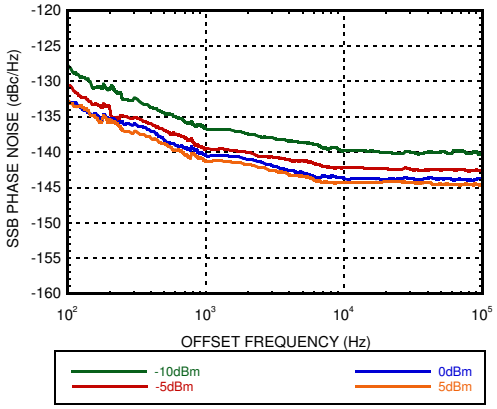
Phase Noise Floor, Vcc = 4.75V REF = 1000MHz Sine Wave



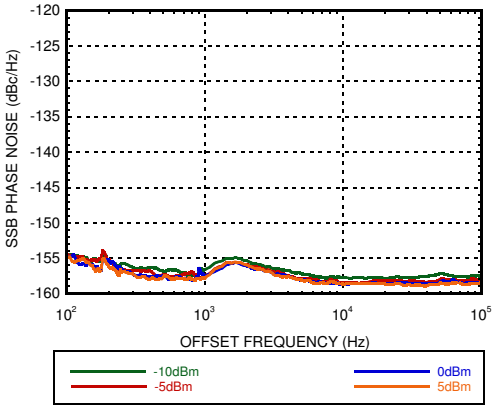
Phase Noise Floor, Vcc = 4.75V REF = 10MHz Square Wave



Phase Noise Floor, Vcc = 5.00V REF = 1000MHz Sine Wave



Phase Noise Floor, Vcc = 5.00V REF = 10MHz Square Wave



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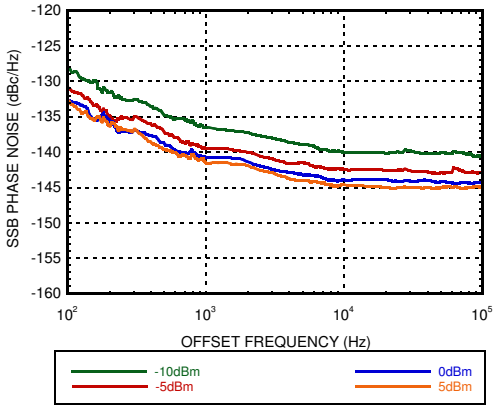

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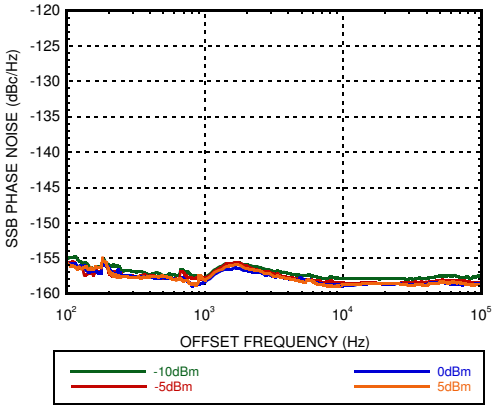
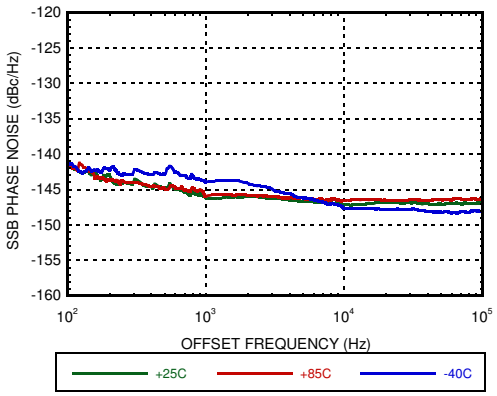
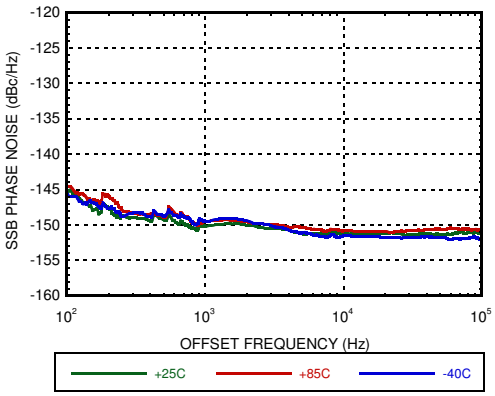


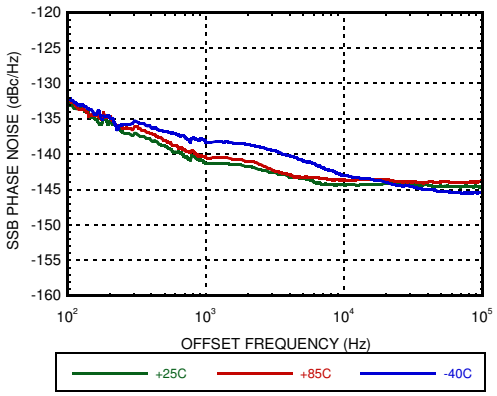
Phase Noise Floor, Vcc = 5.00V REF = 100MHz Sine Wave



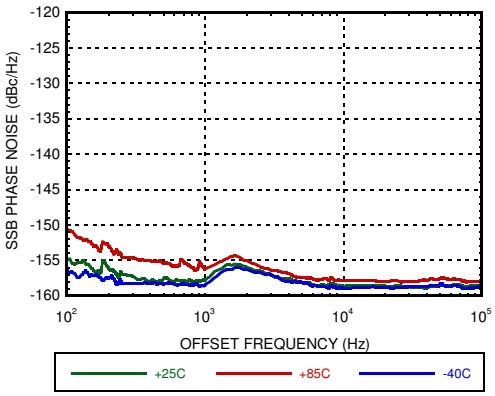
Phase Noise Floor, Vcc = 5.00V REF = 100MHz Square Wave



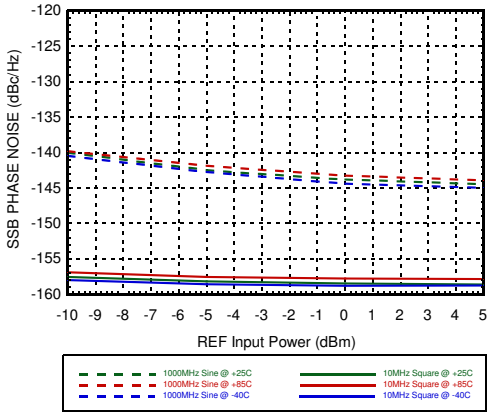
Phase Noise Floor, Vcc = 5.00V REF = 1000MHz Sine Wave



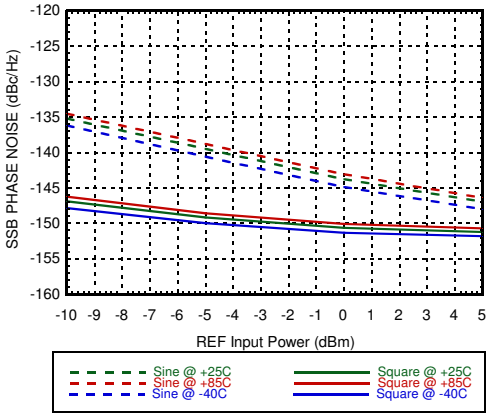
Phase Noise Floor, Vcc = 5.00V REF = 10MHz Square Wave



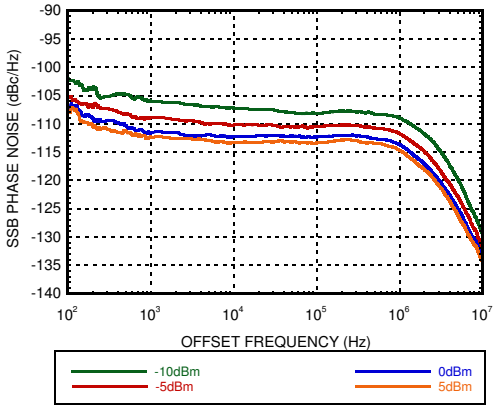
Phase Noise Floor, Vcc = 5.00V REF = 10 & 1000MHz, ≥10kHz offset



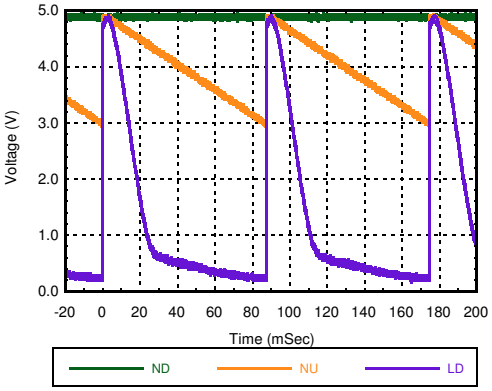
Phase Noise Floor, Vcc = 5.00V REF = 100MHz, ≥10kHz offset



Typical PLL Performance, Vcc = 5.00V REF = 100MHz Square Wave VCO = 10GHz, N = 100, T = +25C



PFD Outputs ND, NU, LD, Vcc = 5.00V Forced PFD Difference ≈ 11Hz High-Z Scope, BW = 20MHz, T = +25C



Typical Supply Current vs. Vcc

Vcc (Vdc)	Icc (mA)
4.75	279
5.00	300
5.25	324

Typical ND & NU Voltages, Vcc = +5V

Symbol	Characteristics	+25C			Units
		Min.	Typ.	Max.	
Voh	Output High Voltage	4.9	5.0	5.1	V
Vol	Output Low Voltage	2.9	3	3.1	V

Reliability Information

Junction Temperature To Maintain 1 Million Hour MTTF	135 °C
Nominal Junction Temperature (T = +85 °C)	99.3 °C
Thermal Resistance (junction to ground paddle)	9.5 °C/W
Operating Temperature	-40 to +85 °C

Programming Truth Table

Function	(LSB) A0	A1	A2	A3	A4
Output Low	0	0	0	0	0
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1

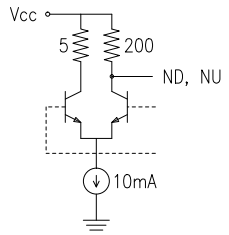
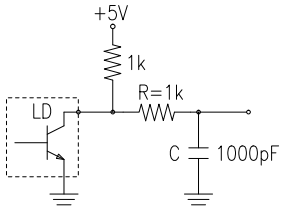
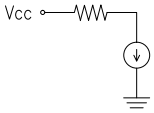
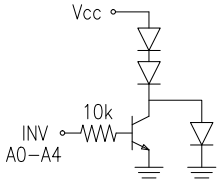
Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm
Supply Voltage (Vcc)	+5.5V
Logic Inputs (INV, A0 - A4)	-0.5 to (0.5V + Vcc)
PFD Outputs (ND, NU)	2.5 to (0.5V + Vcc)
Storage Temperature	-65 to +150 °C
ESD Sensitivity (HBM)	Class 1B
ESD Sensitivity (CDM)	Class C2

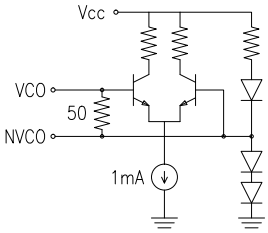
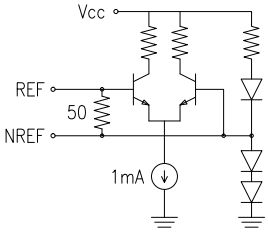
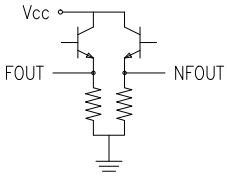
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Notes:
1. All data shown is typical and actual performance may vary depending upon implementation.
2. Phase Noise data taken utilizing 2-unit cancellation method with VCO ≥ 2400MHz and healthy power level.
3. Only one PFD output will be active with a forced frequency difference, depending upon which input frequency is higher.
4. Without oscilloscope bandwidth limiting, there will be narrow pulses on NU, ND, & LD, at the input frequencies. These pulses may create spectral content, which is normally surpressed with the loop filter and lock detect filter.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	NU	$\overline{\text{Up Output}}$ Do not load output below 2.5V or damage can occur.	
2	ND	$\overline{\text{Down Output}}$ Do not load output below 2.5V or damage can occur.	
19	LD	Lock Detect Output Open collector pulsed output. Requires external 1kΩ Pullup to Vcc and filtering. Average “LOW” = UNLOCKED Avereage “HIGH” = LOCKED	
3, 5, 6, 12, 13, 18, 23, 24, Paddle	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
4	Vcc	Supply Voltage, +5.00V	
7 - 11	A0 - A4	Control inputs, bits 0 - 4 CMOS / TTL compatible See Programming Truth Table	
20	INV	PFD INVERT Function to swap REF & VCO CMOS / TTL compatible Logic “LOW” = NORMAL Logic “HIGH” = INVERT	

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
14	VCO	Differential VCO Inputs Pins are DC coupled, External DC blocks required	
15	NVCO		
21	REF	Differential REF Inputs Pins are DC coupled, External DC blocks required	
22	NREF		
16	FOUT	Diffential Test Port Outputs from 5-Bit Counter Pins are DC coupled, External DC blocks or High-Z probes only Leave unconnected for normal operation	
17	NFOUT		

PFD Functionality

The phase frequency detector functionality of the HMC4069LP4E is such that it compares the rising edge the two input signals (REF / VCO). This information is then used to pulse the ND and NU outputs depending upon which input signal is greater in frequency.

Under normal operation the ND pin will be active when VCO frequency is greater than the REF frequency; NU would remain constant. Conversly, when the VCO frequency is lower than the REF frequency, then NU would be active and ND would remain constant. Here, the term “active” means that the output will on average, vary between 3 - 5V, and the term “remain constant” means that the output will remain at approximately 5V.

INVERT Functionality

The INV pin effectively swaps the REF and VCO input signals, such that the NU and ND pin responses are swapped. This has the advantage of easily correcting a layout issue if the loop filter op-amp inputs were swapped.

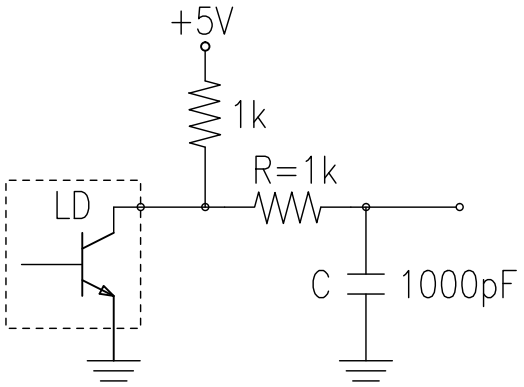
A logic “LOW” on this pin will configure the device for normal operation, and a logic “HIGH” cause the input signals to swap. The evaluation board has a 10kΩ resistor pull up resistor to 5V. A jumper must be installed connecting the INV pin to ground for normal operation.

Lock Detect Functionality

The LD pin is an open collector pulsed output transistor. It requires an external 1k pull up resistor to Vcc (5V), as well as a simple RC filter.

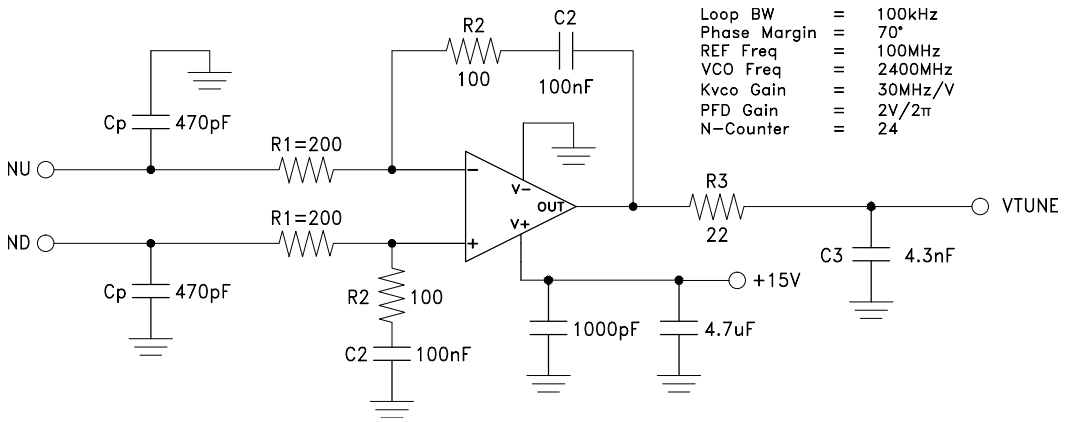
Since the pin will produce very narrow pulses at each zero crossing of the REF and VCO input signals, filtering is necessary to create an average voltage which can be used to drive an LED or system input logic. When the device is “LOCKED”, that transistor will effectively be “OFF”, and the filtered output voltage will be “HIGH”.

Below is an example of an RC filter for the lock detect pin. The value of resistor “R” should be greater than 100Ω to limit any surge current from flowing when the output transistor is “ON”. The value of capacitor “C” should be selected such that the filter cutoff is much less than the REF frequency, but not excessively large (slow) that it will inhibit detection of lock status.

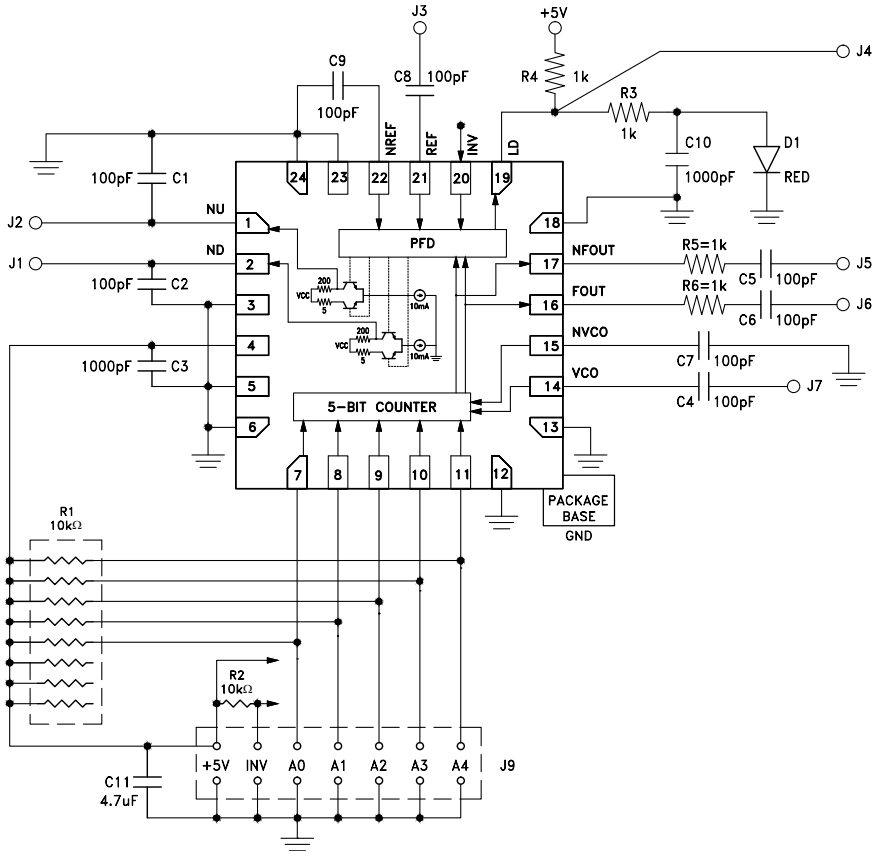


Typical Loop Filter

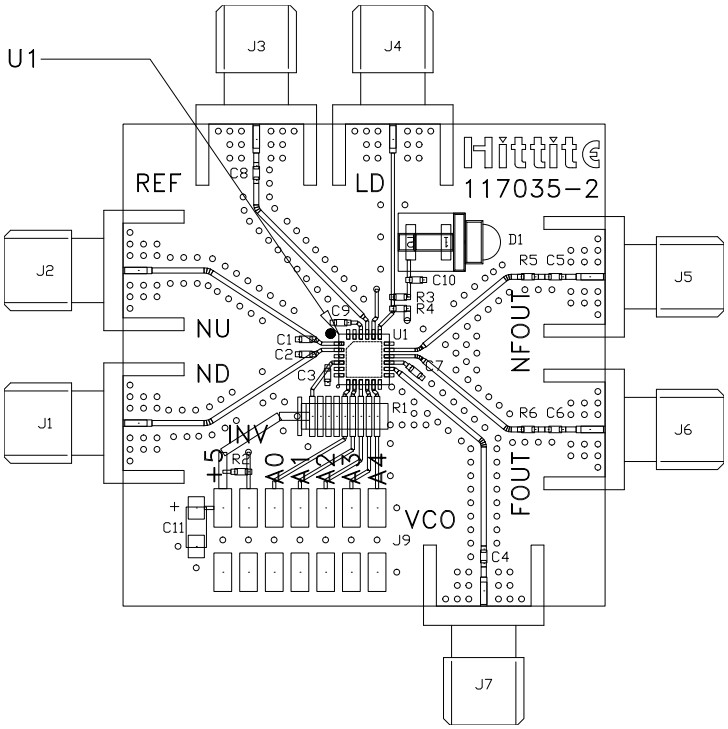
A diffential op-amp loop filter is required in order to integrate the ND and NU pulses into a usable tune voltage to drive the oscillator in a PLL. The loop filter synthesis can be performed using a variety of simulation tools. Below is an example of a third-order filter produced with the listed PLL parameters for loop bandwidth, etc.



Evaluation PCB Circuit



Evaluation PCB



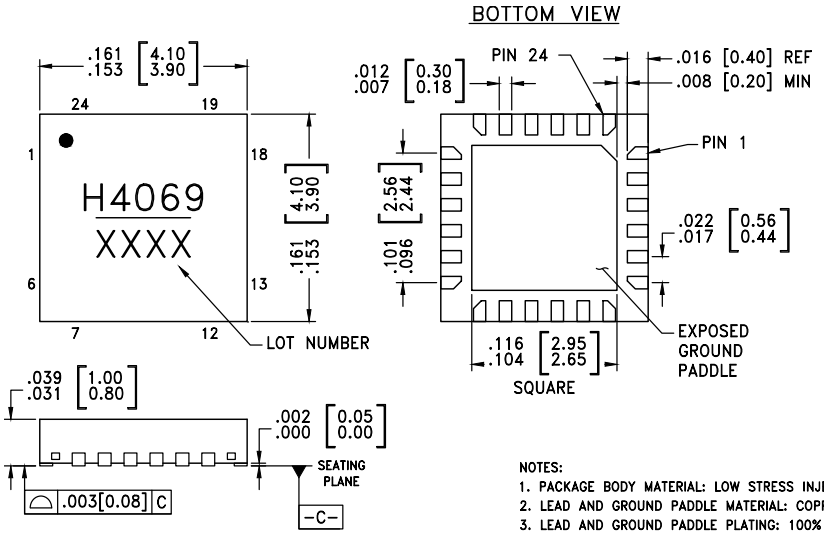
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50Ω impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes.

List of Materials for Evaluation PCB EV1HMC4069LP4 [1]

Item	Description
PCB [2]	117035 Eval Board
U1	HMC4069LP4E, Synthesizer w/ Lock Detect and Invert functions
J1 - J7	PCB Mount SMA RF Connector
J9	2mm, 14-pin, DC Header
Qty 6	2mm Shunt/Jumper
C1, C2, C4 - C9	100pF Ceramic Capacitor, 5%, 50V, 0402
C3, C10	1000pF Ceramic Capacitor, 5%, 50V, 0402
C11	4.7µF, Tantalum Capacitor, 16V, 20%, 3216
R1	8 x 10kΩ Resistor Array, 2%
R2	10kΩ Resistor, 5%, 1/10W, 0402
R3 - R6	1kΩ Resistor, 1%, 1/10W, 0402
D1	Red LED, 5.3 x 4.6 x 4.8mm

[1] Reference this part number when ordering complete PCB
[2] Circuit Board Material: Arlon 25FR

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO ADI APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC4069LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H4069 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX