Data Sheet

CADEKA
Amplify the Human Experience

COMLINEAR® CLC3800, CLC3801

Triple, Standard Definition Video Amplifiers

FEATURES

- Integrated 4th-order, 8MHz filters
- Integrated 6 or 9dB video drivers
- 8.8mA total supply current
- 0.08%/0.04° differential gain/phase error
- DC coupled inputs
- AC or DC coupled outputs
- DC-coupled outputs remove the need for AC-coupling capacitors
- Each channel can drive $2V_{pp}$ into 1, 2, or 3 video loads (150Ω, 75Ω or 50Ω)
- 0.1% THD
- Operates from 3V to 7V supplies
- Pb-free SOIC-8 package

APPLICATIONS

- Cable or satellite set-top-box (STB)
- Portable DVD players
- DVD players
- Portable media players with video out
- Video on demand
- Personal video recorders

General Description

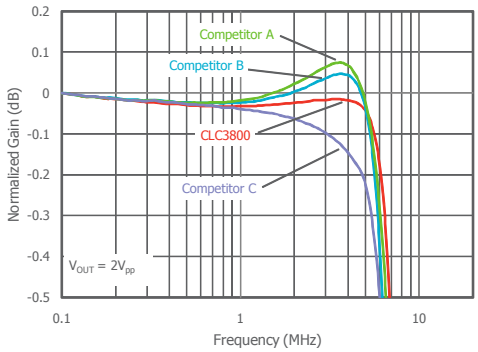
The CLC3800 (6dB) and CLC3801 (9dB) are triple low cost video amplifiers capable of driving $2V_{pp}$ into 1 (150Ω), 2 (75Ω), or 3 (50Ω) video loads. The CLC3800 and CLC3801 feature integrated 8MHz, 4th-order low pass filters designed to cleanly pass standard definition video signals while filtering out noise and other unwanted signals , resulting in a crisper, cleaner video signal. The 4th-order filters provide improved image quality when compared to 2nd-order passive filtering solutions.

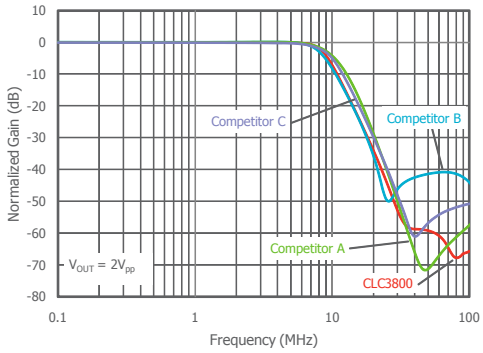
The CLC3800 video amplifier offers a fixed gain of 6dB. This integrated gain compensates for the voltage drop inherent in properly terminated video loads; ensuring a $1V_{pp}$ video signal is present at the load. If additional gain is required, the CLC3801 video amplifier offers a fixed gain of 9dB.

All three video amplifiers can be driven by DC-coupled signals. Their outputs can drive either AC- or DC-coupled loads.

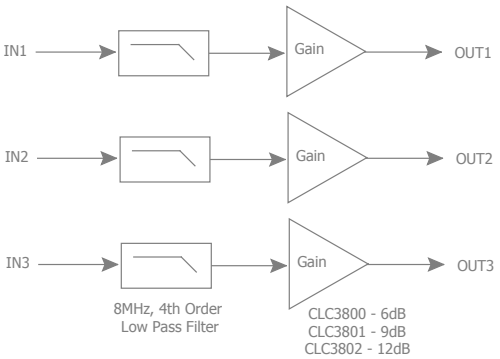
These video amplifiers operate from 3V to 7V supplies and consume 8.8mA of supply current, making them well suited for battery powered devices.

Competitive Comparison Plots (continued on page 11)





Functional Block Diagram



Ordering Information

Part Number	Gain	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC3800ISO8X	6dB	SOIC-8	Yes	Yes	-40°C to +125°C	Reel
CLC3801ISO8X†	9dB	SOIC-8	Yes	Yes	-40°C to +125°C	Reel
CLC3800ILP8X*	6dB	DFN-8	Yes	Yes	-40°C to +125°C	Reel

*Future product offering. †Not recommended for new design. Moisture sensitivity level for all parts is MSL-1.

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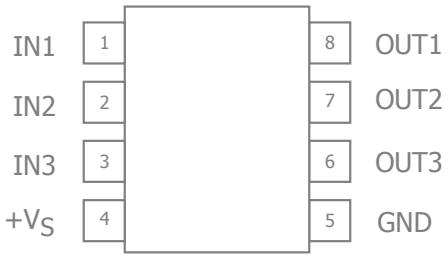
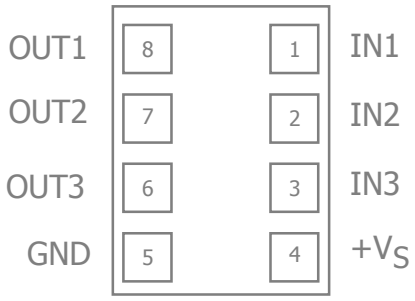
SOIC Pin Configuration



SOIC Pin Assignments

Pin No.	Pin Name	Description
1	IN1	Input, channel 1
2	IN2	Input, channel 2
3	IN3	Input, channel 3
4	$+V_S$	Positive supply
5	GND	Ground
6	OUT3	Output, channel3
7	OUT2	Output, channel 2
8	OUT1	Output, channel 1

DFN Pin Configuration



Bottom View

DFN package: Use Pb-free solder ONLY

DFN Pin Configuration

Pin No.	Pin Name	Description
1	IN1	Input, channel 1
2	IN2	Input, channel 2
3	IN3	Input, channel 3
4	$+V_S$	Positive supply
5	GND	Ground
6	OUT3	Output, channel3
7	OUT2	Output, channel 2
8	OUT1	Output, channel 1

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Electrical Characteristics at 3V

T_A = 25°C, V_S = +3V, input is DC-coupled, input source resistance = 37.5Ω, R_L = 150Ω thru a 220µF AC-coupling capacitor, V_{IN} = 1V_{pp}; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
F_{-1dB}	-1dB Bandwidth	R_L=150Ω, AC-coupled		7.6		MHz
		R_L=75Ω, DC-coupled		7.6		MHz
F_{-3dB}	-3dB Bandwidth	R_L=150Ω, AC-coupled		8.5		MHz
		R_L=75Ω, DC-coupled		8.5		MHz
F_{SB}	Stopband Attenuation	at 27MHz, R_L=150Ω, AC-coupled		48		dB
		at 27MHz, R_L=75Ω, DC-coupled		48		dB
DG	Differential Gain	NTSC (3.58MHz), AC-coupled		0.7		%
		NTSC (3.58MHz), DC-coupled		0.62		%
		NTSC (3.58MHz), DC-coupled, R_L=75Ω		0.24		%
DP	Differential Phase	NTSC (3.58MHz), AC-coupled		0.3		°
		NTSC (3.58MHz), DC-coupled		0.13		°
		NTSC (3.58MHz), DC-coupled, R_L=75Ω		0.25		°
Time Domain Response						
GD	Group Delay	Delta delay between 400kHz and 3.58MHz		5.6		ns
PD	Propogation Delay	Delay from input to output, 4.5MHz		65		ns
Distortion/Noise Response						
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz, active video range + sync		0.1		%
		V_{OUT} = 1.4V_{pp}, 3.58MHz, active video range		0.9		%
		V_{OUT} = 2V_{pp}, 1MHz, active video range + sync, R_L=75Ω, DC-coupled		0.1		%
		V_{OUT}= 1.4V_{pp}, 3.58MHz, active video range, R_L=75Ω, DC-coupled		0.9		%
SNR	Signal to Noise Ratio	NTC-7 Weighting 100kHz to 4.2MHz		77		dB
CLG	Chroma / Luma Gain	400kHz to 3.58MHz (NTSC)		±1		%
		400kHz to 4.43MHz (PAL)		±1		%
X_{TALK}	Crosstalk	Channel-to-channel at 1MHz		60		dB
		Channel-to-channel at 1MHz, R_L=75Ω, DC-coupled		58		dB
DC Performance						
G	Gain(1)	DC, CLC3800, R_L=75Ω, DC-coupled	5.7	6.0	6.3	dB
		DC, CLC3801, R_L=75Ω, DC-coupled	8.6	9.0	9.4	dB
		DC, CLC3802, R_L=75Ω, DC-coupled	TBD	12	TBD	dB
G_{MATCH}	Inter-Channel Gain Matching(1)	400kHz, R_L=75Ω, DC-coupled		0.08	0.2	dB
V_{OS}	Output Offset Voltage(1)	V_{IN}=0V, no load	230	330	390	mV
I_b	Input Bias Current(1)	V_{IN}=0V, no load		1.4	5	µA
V_{IN}	Input Voltage Range(1)	CLC3800		0 to 1.25		V
		CLC3801		0 to 0.9		V
V_O	Output Voltage, CLC3800(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		2.5		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	2.35	2.5	2.66	V
	Output Voltage, CLC3801(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		2.5		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	2.32	2.5	2.69	V
	Output Voltage, CLC3802(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		TBD		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	TBD	TBD	TBD	V
PSRR	Power Supply Rejection Ratio	DC , no load, V_S = 3V to 5.5V		52		dB
I_S	Supply Current(1)	No load, all 3 channels		8.8	15	mA

Notes:
1. 100% tested at 25°C
2. Designed to handle SD video from -40°C to +125°

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Electrical Characteristics

T_A = 25°C, V_S = +5V, input is DC-coupled, input source resistance = 37.5Ω, R_L = 150Ω thru a 220µF AC-coupling capacitor, V_{IN} = 1V_{pp}; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
F_{-1dB}	-1dB Bandwidth	R_L=150Ω, AC-coupled		7.7		MHz
		R_L=75Ω, DC-coupled		7.7		MHz
F_{-3dB}	-3dB Bandwidth	R_L=150Ω, AC-coupled		8.6		MHz
		R_L=75Ω, DC-coupled		8.6		MHz
F_{SB}	Stopband Attenuation	at 27MHz, R_L=150Ω, AC-coupled		48		dB
		at 27MHz, R_L=75Ω, DC-coupled		48		dB
DG	Differential Gain	NTSC (3.58MHz), AC-coupled		0.17		%
		NTSC (3.58MHz), DC-coupled		0.08		%
		NTSC (3.58MHz), DC-coupled, R_L=75Ω		0.03		%
DP	Differential Phase	NTSC (3.58MHz), AC-coupled		0.18		°
		NTSC (3.58MHz), DC-coupled		0.04		°
		NTSC (3.58MHz), DC-coupled, R_L=75Ω		0.04		°
Time Domain Response						
GD	Group Delay	Delta delay between 400kHz and 3.58MHz		5.6		ns
PD	Propogation Delay	Delay from input to output, 4.5MHz		65		ns
Distortion/Noise Response						
THD	Total Harmonic Distortion	V_{OUT}= 2V_{pp}, 1MHz, active video range + sync		0.1		%
		V_{OUT}= 1.4V_{pp}, 3.58MHz, active video range		0.5		%
		V_{OUT}= 2V_{pp}, 1MHz, active video range + sync, R_L=75Ω, DC-coupled		0.15		%
		V_{OUT}= 1.4V_{pp}, 3.58MHz, active video range, R_L=75Ω, DC-coupled		0.6		%
SNR	Signal to Noise Ratio	NTC-7 Weighting 100kHz to 4.2MHz		77		dB
CLG	Chroma / Luma Gain	400kHz to 3.58MHz (NTSC)		±1		%
		400kHz to 4.43MHz (PAL)		±1		%
X_{TALK}	Crosstalk	Channel-to-channel at 1MHz		-61		dB
		Channel-to-channel at 1MHz, R_L=75Ω, DC-coupled		-58		dB
DC Performance						
G	Gain(1)	DC, CLC3800, R_L=75Ω, DC-coupled	5.7	6.0	6.3	dB
		DC, CLC3801, R_L=75Ω, DC-coupled	8.6	9.0	9.4	dB
		DC, CLC3802, R_L=75Ω, DC-coupled	TBD	12	TBD	dB
G_{MATCH}	Inter-Channel Gain Matching(1)	400kHz, R_L=75Ω, DC-coupled		0.08	0.2	dB
V_{OS}	Output Offset Voltage(1)	V_{IN}=0V, no load	230	330	390	mV
I_b	Input Bias Current(1)	V_{IN}=0V, no load		1.4	5	µA
VR_{IN}	Video Range - Input(1)	CLC3800	0 to 1.1	0 to 1.4		V
		CLC3801	0 to 0.78	0 to 1		V
V_O	Output Voltage, CLC3800(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		2.5		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	2.35	2.5	2.66	V
	Output Voltage, CLC3801(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		2.5		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	2.32	2.5	2.69	V
	Output Voltage, CLC3802(2)	V_{IN}=1.1V_{pp}, R_L=150Ω, AC-coupled		TBD		V
		V_{IN}=1.1V_{pp}, R_L=75Ω, DC-coupled(1)	TBD	TBD	TBD	V
PSRR	Power Supply Rejection Ratio	DC, no load		53		dB
I_S	Supply Current(1)	Total		9.5	15	mA

Notes:

1. 100% tested at 25°C
2. Designed to handle SD video from -40° to +125°

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V
Output Short Circuit Current		+110, -85	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W
8-Lead DFN		60		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8	DFN-8
Human Body Model (HBM), output ESD protection	5kV	TBD
Charged Device Model (CDM)	2kV	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+125	°C
Supply Voltage Range	3		7	V

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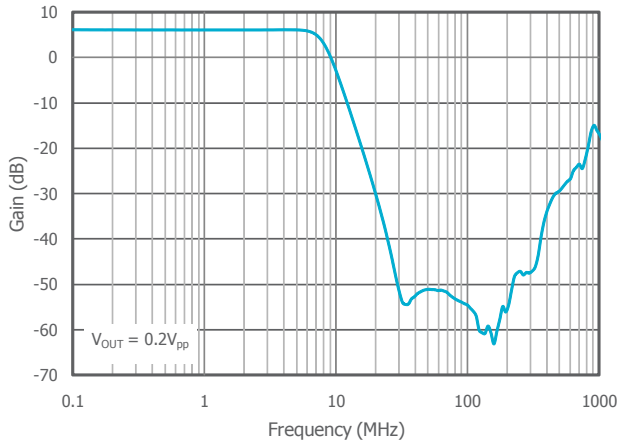
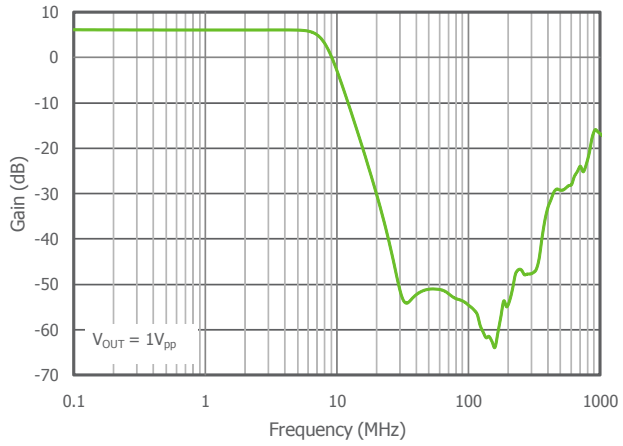
Typical Performance Characteristics at V_S = 5V

T_A = 25°C, V_s = +5V, input is DC-coupled, input source resistance = 37.5Ω, R_L = 150Ω thru a 220µF AC-coupling capacitor, V_{IN} = 1V_{pp}; unless otherwise noted.

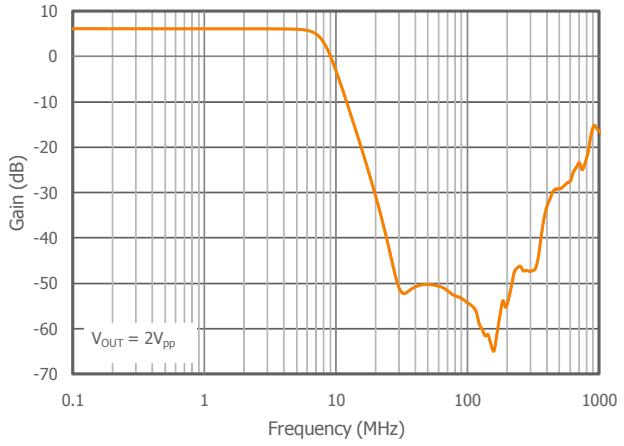
Frequency Response (V_{OUT} = 0.2V_{pp})



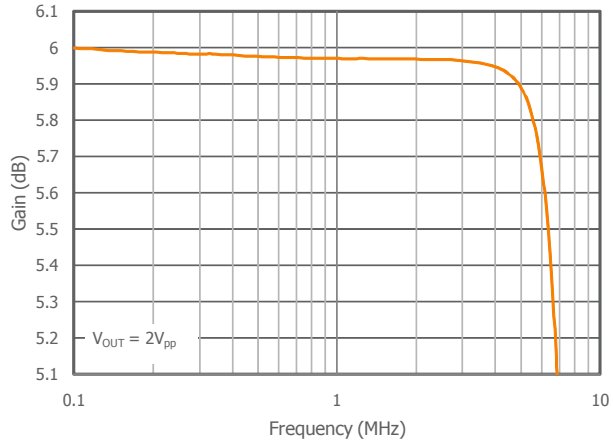
Frequency Response (V_{OUT} = 1V_{pp})



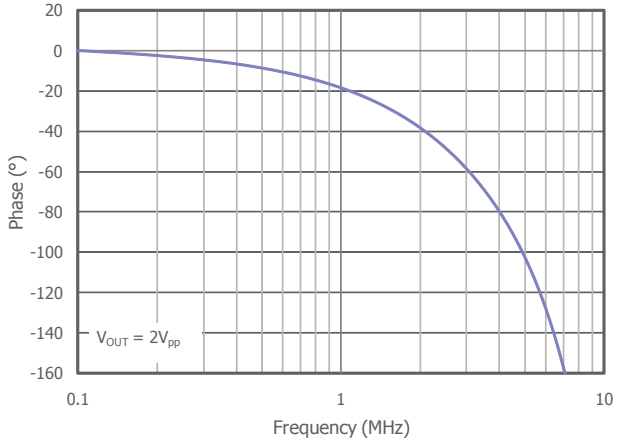
Frequency Response (V_{OUT} = 2V_{pp})



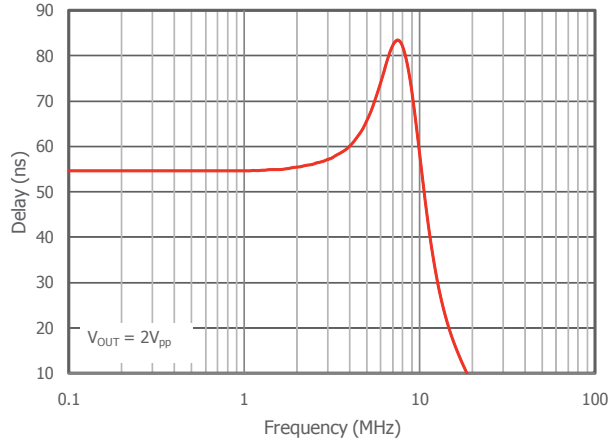
Frequency Response (V_{OUT} = 2V_{pp})



Phase vs. Frequency



Group Delay vs. Frequency



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Typical Performance Characteristics at V_S = 5V

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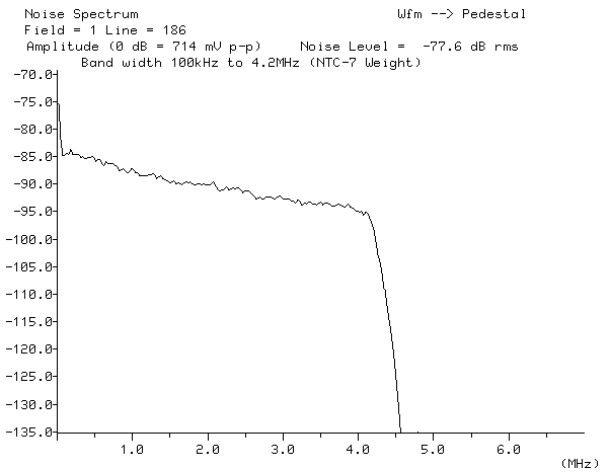
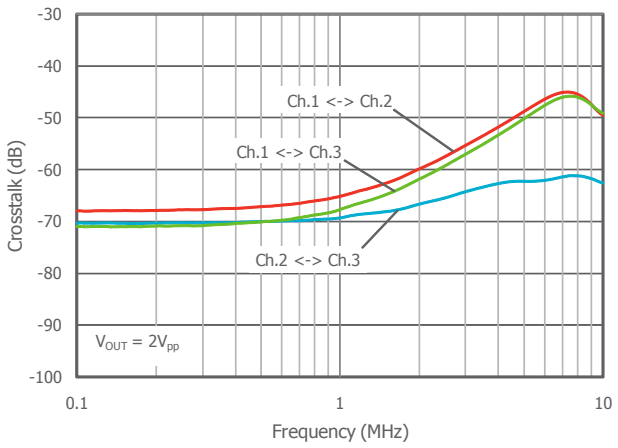
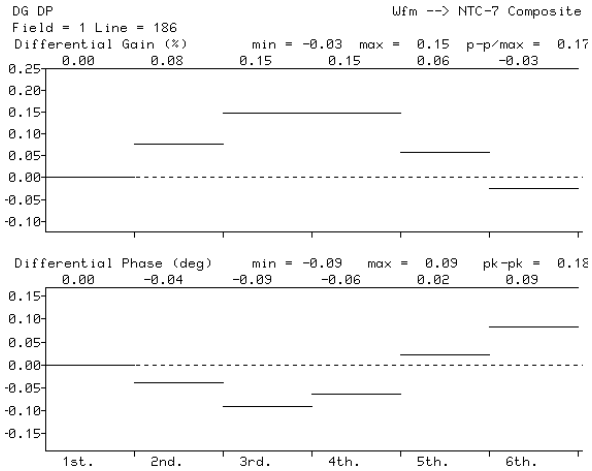
Noise vs. Frequency (SNR)



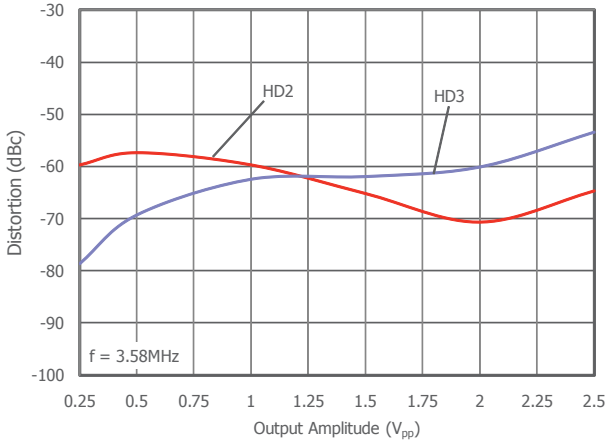
Crosstalk vs. Frequency



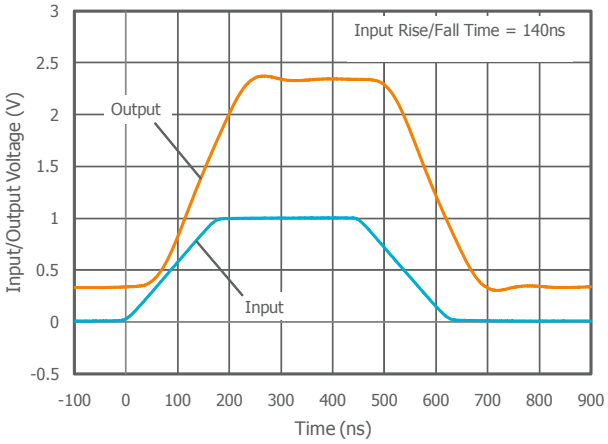
Differential Gain and Phase



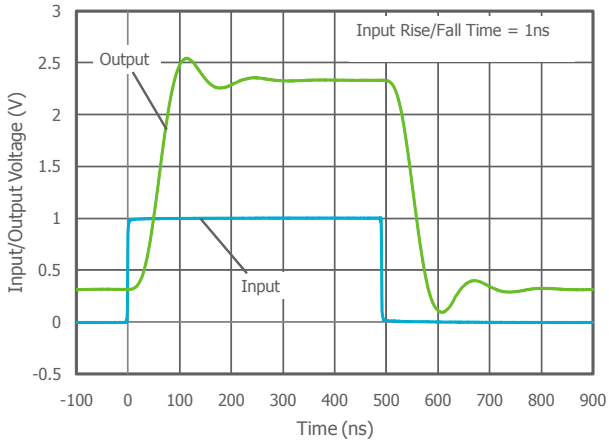
Harmonic Distortion vs. Output Voltage



Large Signal Pulse Response



Large Signal Pulse Response



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Typical Performance Characteristics at V_S = 3V

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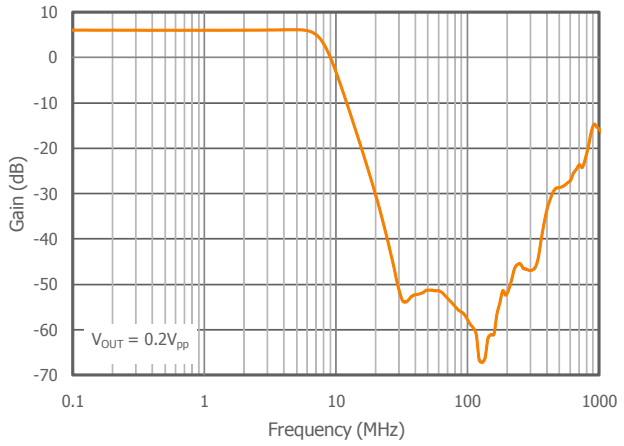
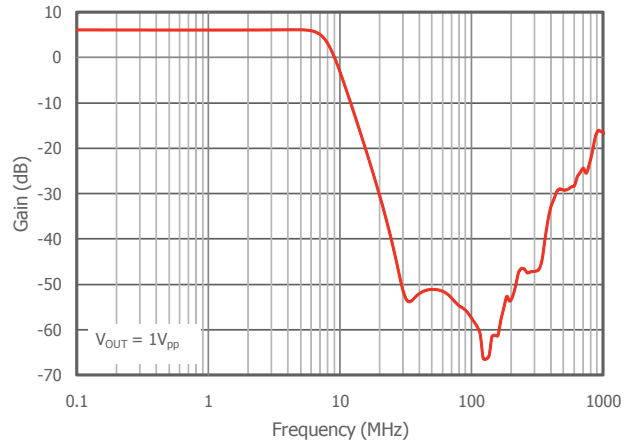
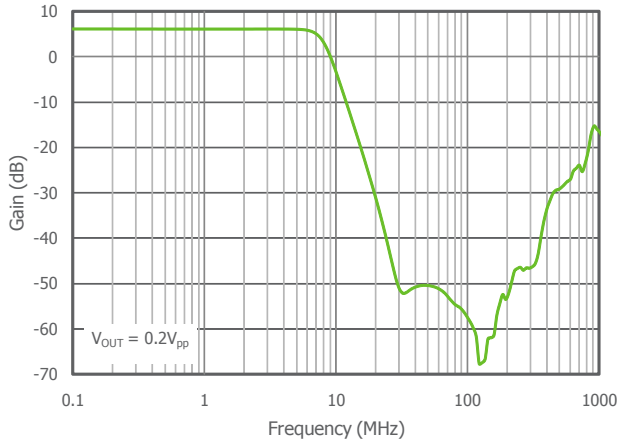
Frequency Response (V_{OUT} = 0.2V_{pp})



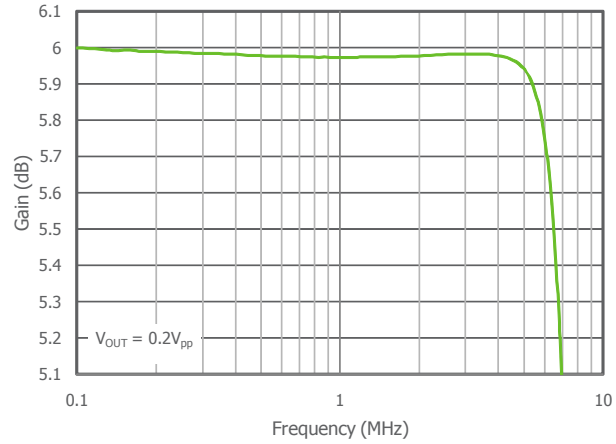
Frequency Response (V_{OUT} = 1V_{pp})



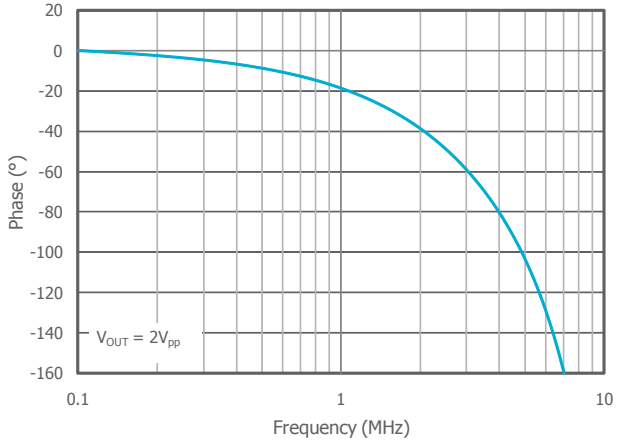
Frequency Response (V_{OUT} = 2V_{pp})



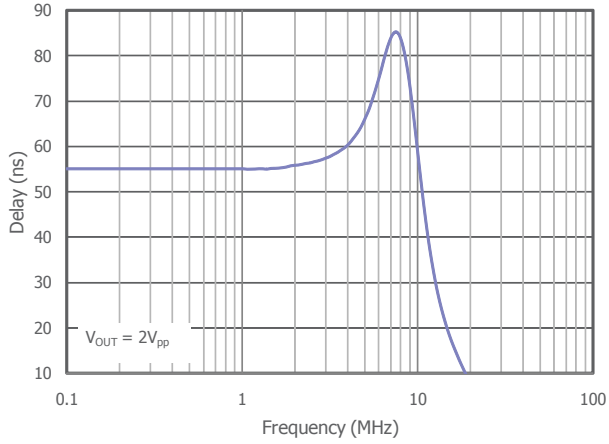
Frequency Response (V_{OUT} = 2V_{pp})



Phase vs. Frequency



Group Delay vs. Frequency



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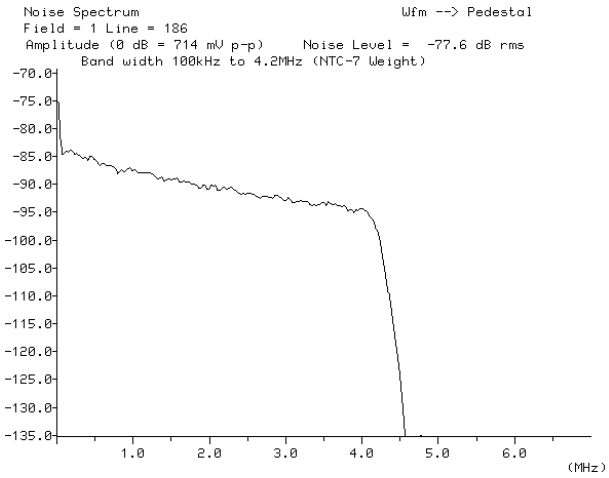
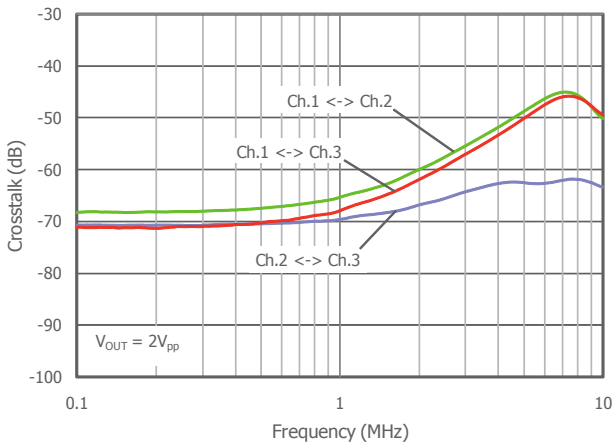
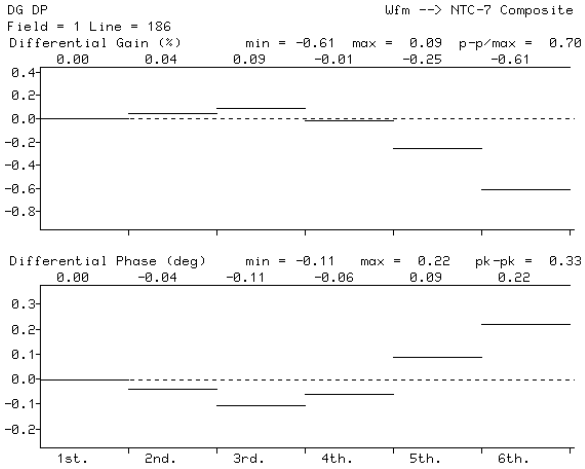
Noise vs. Frequency (SNR)



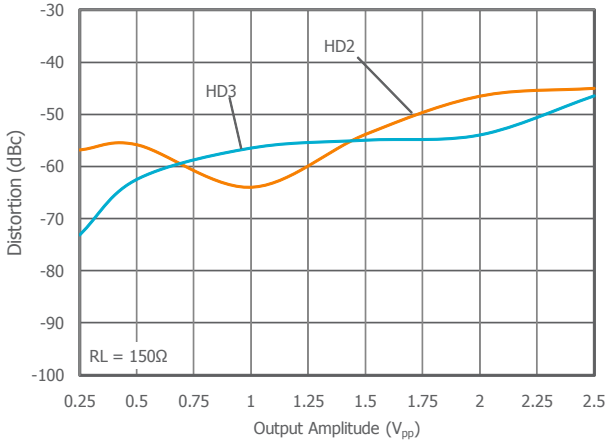
Crosstalk vs. Frequency



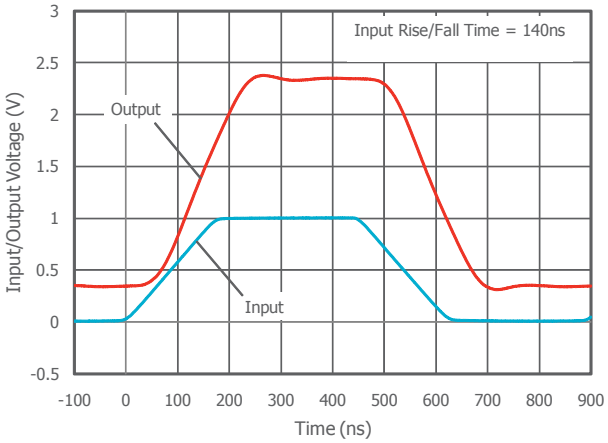
Differential Gain and Phase



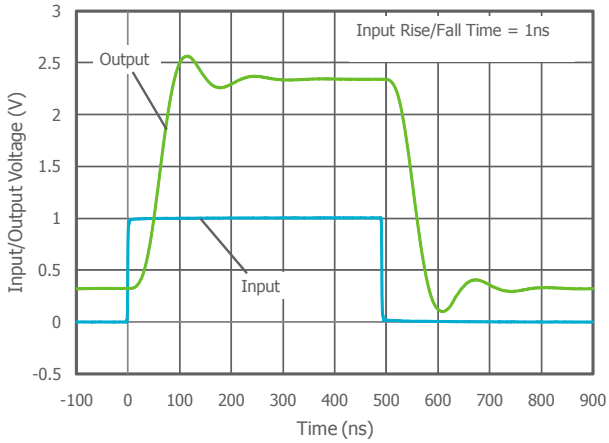
Harmonic Distortion vs. Output Voltage



Large Signal Pulse Response



Large Signal Pulse Response



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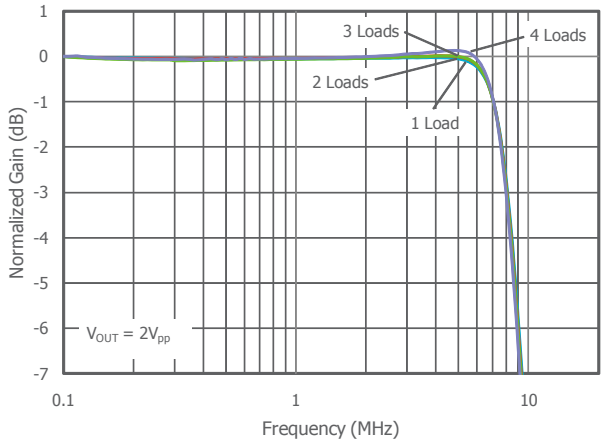
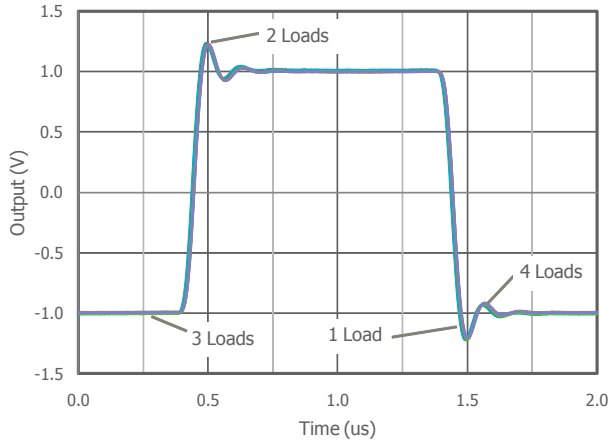
Typical Performance Characteristics Driving Multiple Video Loads

T_A = 25°C, V_S = +5V, input is DC-coupled, input source resistance = 37.5Ω, R_L = 150Ω thru a 220µF AC-coupling capacitor, V_{IN} = 1V_{pp}; unless otherwise noted. 1 Load = 150Ω, 2 Loads = 75Ω, 3 Loads = 50Ω, 4 Loads = 37.5Ω.

Frequency Response



Pulse Response



Differential Gain and Phase

Vs=5V_NTC7 VIDEO, AC COUPLED IN/OUT

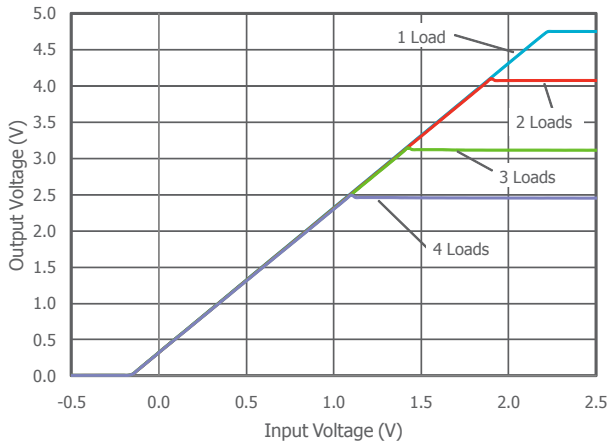
RL OHM	SINK TIP IN V	DG %	DP deg
150	-0.12	0.16	0.17
	0	0.18	0.2
	0.1	0.2	0.17
75	-0.12	0.32	0.38
	0	0.32	0.38
	0.1	0.34	0.39
50	-0.12	0.4	0.5
	0	0.4	0.51
	0.1	0.41	0.51
37.5	-0.12	0.45	0.59
	0	0.45	0.59
	0.1	0.46	0.58

Total Harmonic Distortion

Vout=2Vpp_1MHz_AC OUT

VS V	SINK TIP IN V	RL OHM	HD2 dbc	HD3 dbc	THD %
5	0	37.5	-65.17	-67.33	0.069
5	0.1	37.5	-62.5	-65.17	0.093
5	0	50	-64.67	-65.5	0.079
5	0.1	50	-68.67	-68.83	0.052
5	0	75	-71.17	-68.17	0.048
5	0.1	75	-73.33	-67.67	0.047
5	0	150	-74.33	-71.33	0.033
5	0.1	150	-74.67	-72.33	0.03

Output Voltage Swing



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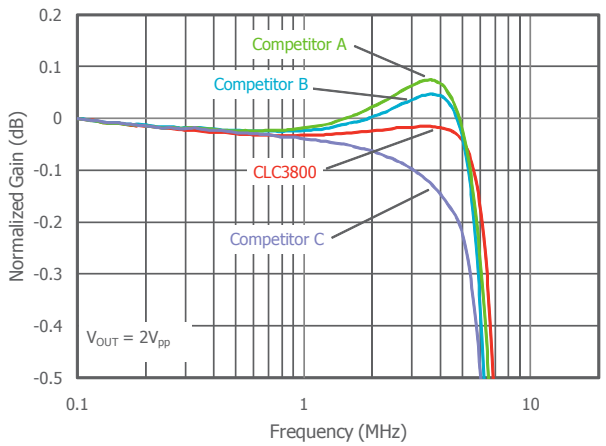
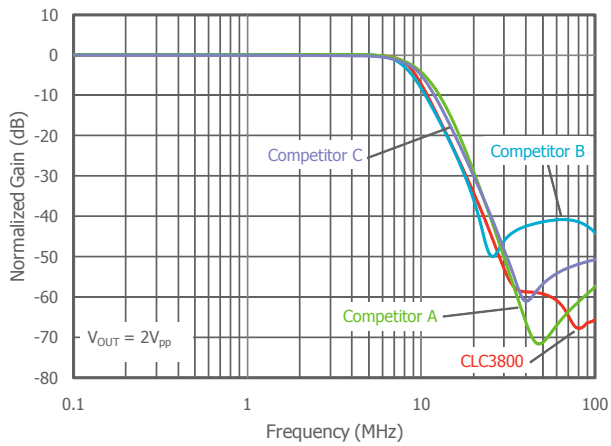
Typical Competitive Comparison Plots

T_A = 25°C, V_S = +5V, input is DC-coupled, input source resistance = 37.5Ω, R_L = 150Ω thru a 220µF AC-coupling capacitor, V_{IN} = 1V_{pp}; unless otherwise noted.

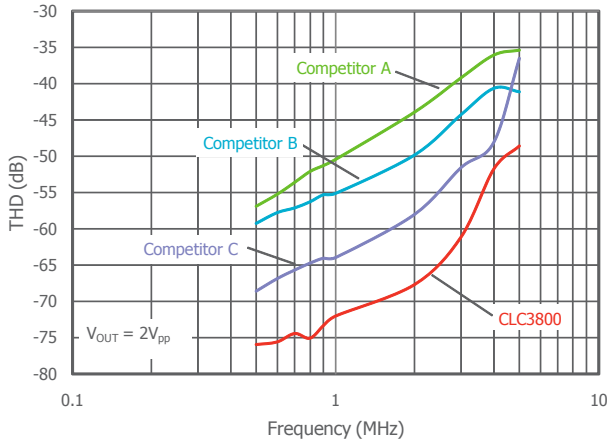
Frequency Response



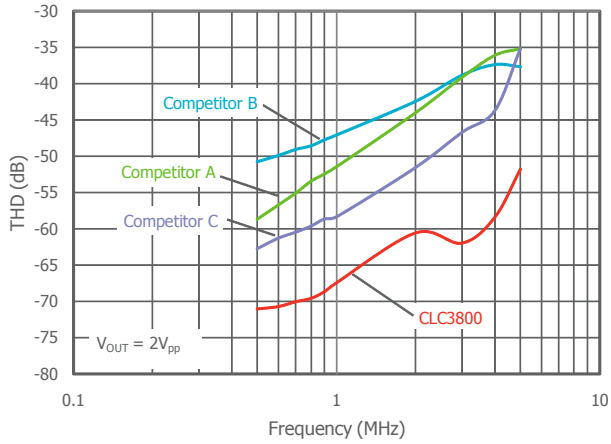
Frequency Response



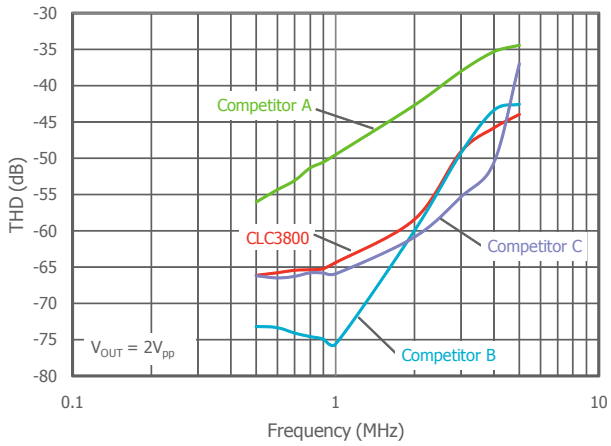
Total Harmonic Distortion (R_L = 150Ω)



Total Harmonic Distortion (R_L = 75Ω)



Total Harmonic Distortion DC-Coupled Out (R_L = 75Ω)



Signal to Noise Ratio and Differential Gain/Phase

PART	CH.	DG %	DP deg	SNR db RMS
CLC3800	1	0.22	0.18	-77.4
	2	0.22	0.17	-77.4
	3	0.24	0.18	-77.5
Comp B	1	0.12	0.85	-80.9
	2	0.16	0.69	-80
	3	0.19	0.52	-80.7
Comp C	1	0.04	0.24	-80.6
	2	0.03	0.19	-80.3
	3	0.04	0.11	-80.7
Comp A	1	0.06	1.31	-80
	2	0.08	1.29	-79.8
	3	0.21	1.21	-79.8

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Application Information

Basic Operation

The CLC3800, CLC3801, and CLC3802 are 3-channel video amplifiers that operate with single supply voltages from 3V to 7V. They are designed to accept DC-coupled inputs and will drive AC- or DC-coupled outputs. Each channel integrates a DC offset, 4th order Butterworth filters, and fixed gain video drivers. The filtering is appropriate for standard definition video signals and has a -3dB cutoff of 8.6MHz. This cutoff provides an excellent compromise between flat in-band response and high frequency noise reduction. The input signals are level shifted prior to the input filters and output amplifiers.

Inputs: DC-Coupled

The inputs must be DC-coupled. Many DACs provide a current output that is resistively terminated to ground. These DACs are conveniently DC-coupled to the inputs of the CLC3800, CLC3801, or CLC3802 as shown in Figure 1. DC-coupled inputs use fewer components and lowers the overall system cost.

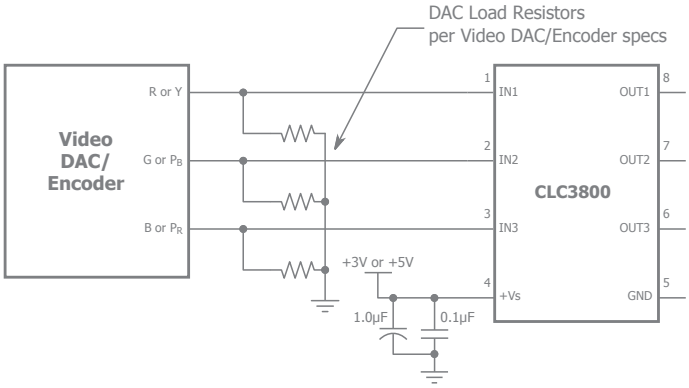

Figure 1. Typical Input Configuration

The input termination/source resistance is set by the application. Any value up to several kΩ can be used. Lower values reduce noise, but if higher values are needed, there is little effect on filter shape or distortion performance of the CLC380x. If the CLC380x is located on the same board as the video source, and within a few inches, the input termination resistance is determined by the requirements of the Video DAC or Encoder. If a cable is needed to connect the CLC380x to the video source, the termination must match the cable impedance which is 75Ω for standard video cable.

The CLC380x Family of video amplifiers add a DC offset, raising the input signal by approximately 330mV. For example, when 0V is applied to the input, the output becomes approximately 330mV above ground. This offset eliminates sync tip clipping. Figure 2 illustrates a typical DC-coupled input signal and resulting output signal after exiting the CLC3800.

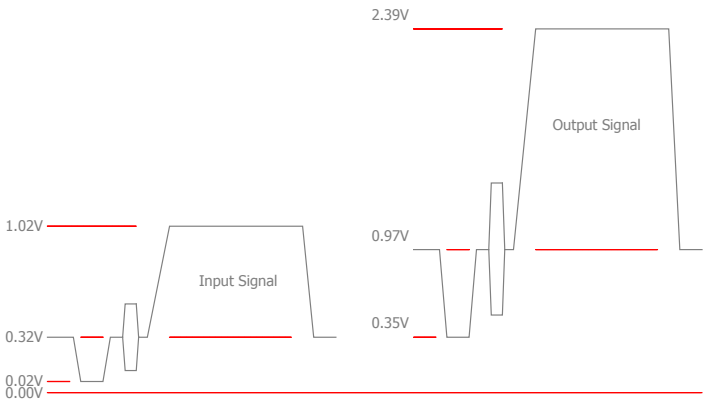

Figure 2. Typical DC-coupled Signal for CLC3800

The input voltage range is typically 0V to 1.4V for the CLC3800 at 5V supply. Due to the internal fixed gain of 6dB (for the CLC3800) and the internal level shift of nominally 330mV, the V_{IN} range is generally limited by the output. V_{IN} and V_{OUT} are fully detailed in the Electrical Characteristics section.

Outputs: AC- or DC-Coupled

Each channel of the CLC3800, CLC3801, and CLC3802 can drive either AC- or DC-coupled loads. Each channel can drive single or dual video loads, 150Ω (1 video load) or 75Ω (2 video loads). Figure 3 shows the typical configuration for driving either AC- or DC-coupled loads.

With DC-coupled loads, AC-coupling capacitors are not used. Match the series termination resistors to the typical cable impedance, 75Ω for standard video cable. Keep the output connection to the series termination resistors as short as possible. If driving 2 video loads, place both resistors close to the CLC3800.

With AC-coupled loads, use an AC-coupling capacitor of at least 220µF in a 75Ω environment. A value of at least 220µF will ensure that low frequencies are passed, preventing video droop across the line, referred to as "tilt".

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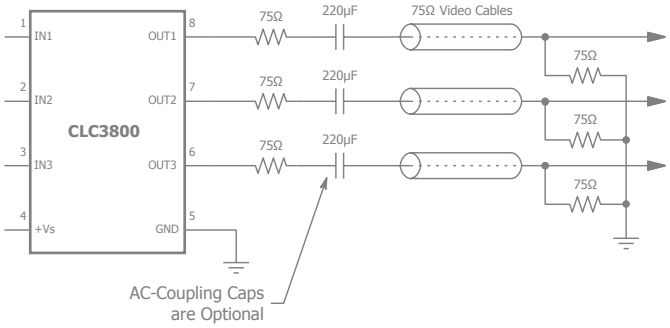

Figure 3. Typical Output Configuration

Power Supply Decoupling

For optimum performance, power supply decoupling is required. Figure 4 shows the recommended usage of power supply decoupling capacitors. The 0.1µF decoupling capacitor must be placed as close to pin 4 as possible, < 0.1" or < 2.5mm, to be effective. The larger, 1µF capacitor can be placed further away.

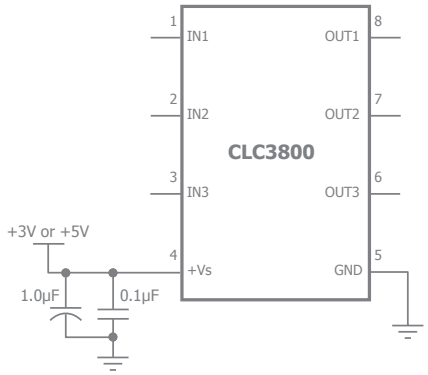

Figure 4. Recommended Power Supply Decoupling

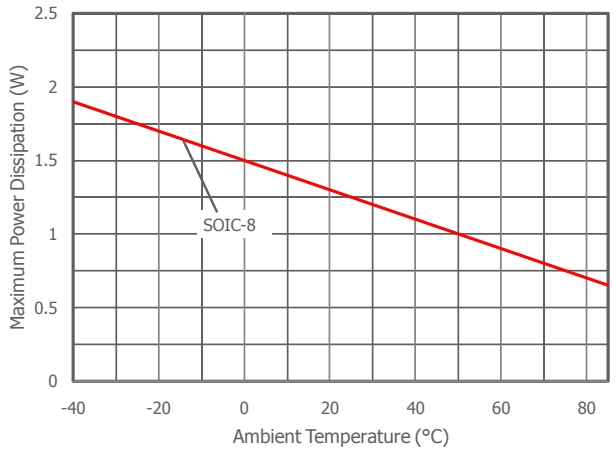

Figure 5. Maximum Power Derating

Power Dissipation Considerations with DC-Coupled Loads

When driving DC loads, the supply current is much higher than in AC applications and care must be taken to dissipate the extra heat generated. The output signal will swing from about 0.3V to 2.3V for full swing video. In the worst case condition, an all white screen with dual DC loads, the additional thermal rise over the quiescent condition is about 20°C. An easy way to help distribute this extra heat is to place a ground plane under the part and add ground plane on the bottom of the board immediately under the part with vias between the two planes.

The CLC3800 is designed primarily for low voltage operation with supply values between 3.0V and 5.5V, but larger supplies can be used. In this situation, DC loads may not be possible due to thermal considerations. With single DC loads on all three channels and a 12V supply, the thermal rise is an additional 45° this gives a total temperature rise of about 57°.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 1µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor <0.75 inches of the power pin
- Place the 0.1µF capacitor <0.1 inches of the power pin
- Remove the ground plane near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB021	CLC3800, CLC3801 in SOIC packages

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Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-11. Application Note AN-6 provides a detailed description of the evaluation board.

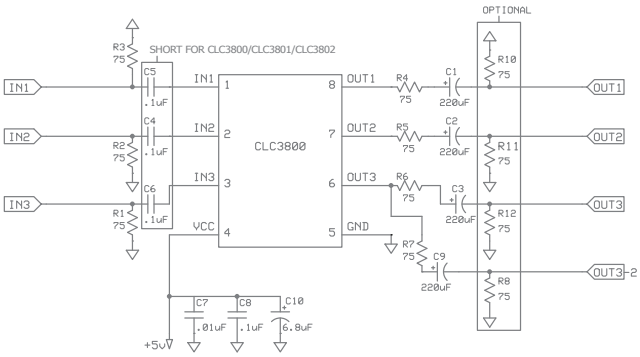

Figure 9. CEB021 Schematic

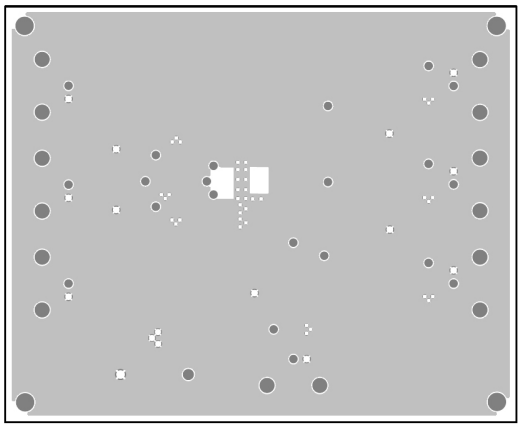

Figure 11. CEB006 Bottom View

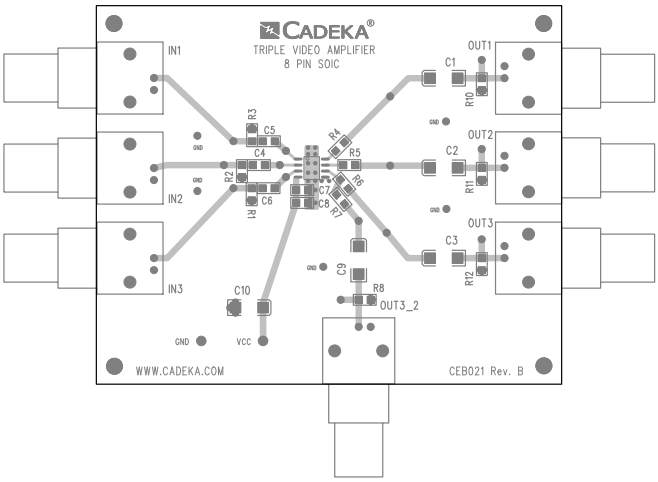

Figure 10. CEB021 Top View

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Typical Application Circuits

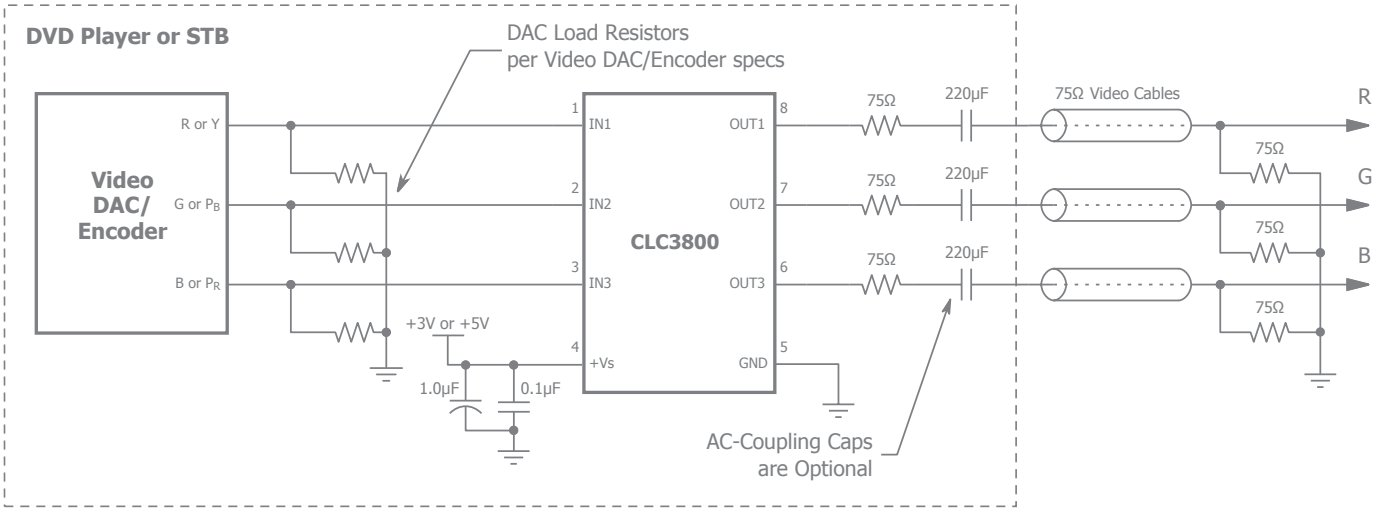


Figure 11. Typical Configuration for Component Video (RGB, YP_BP_R, or YUV)

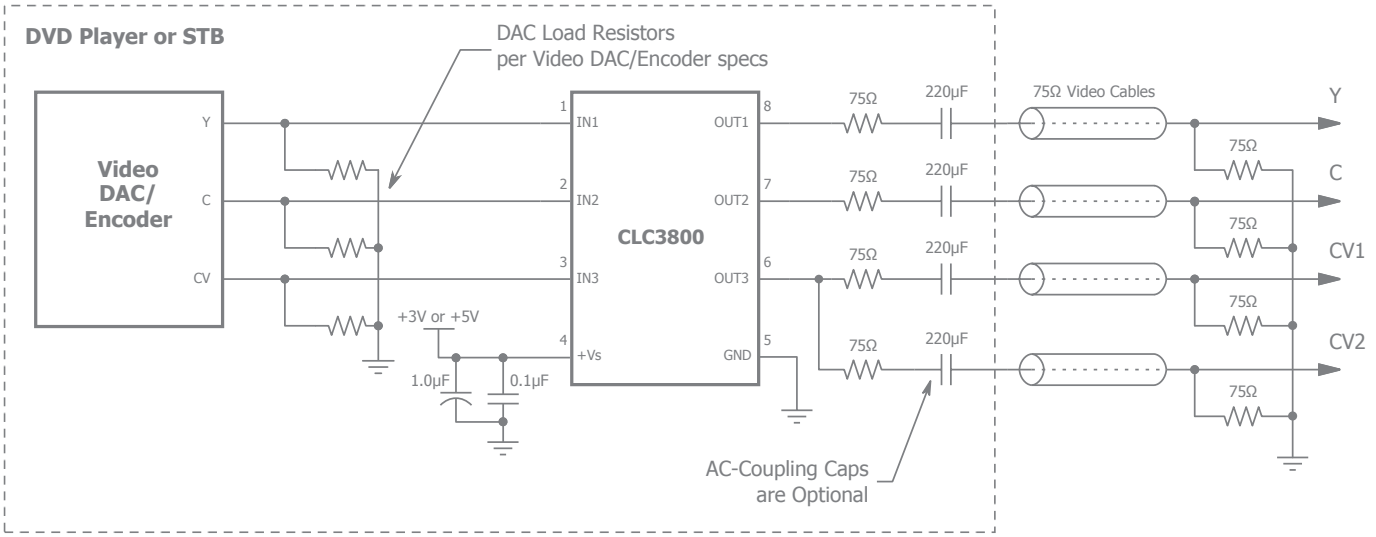


Figure 11. Typical Configuration for Composite Video an extra composite output is available to drive an RF modulator

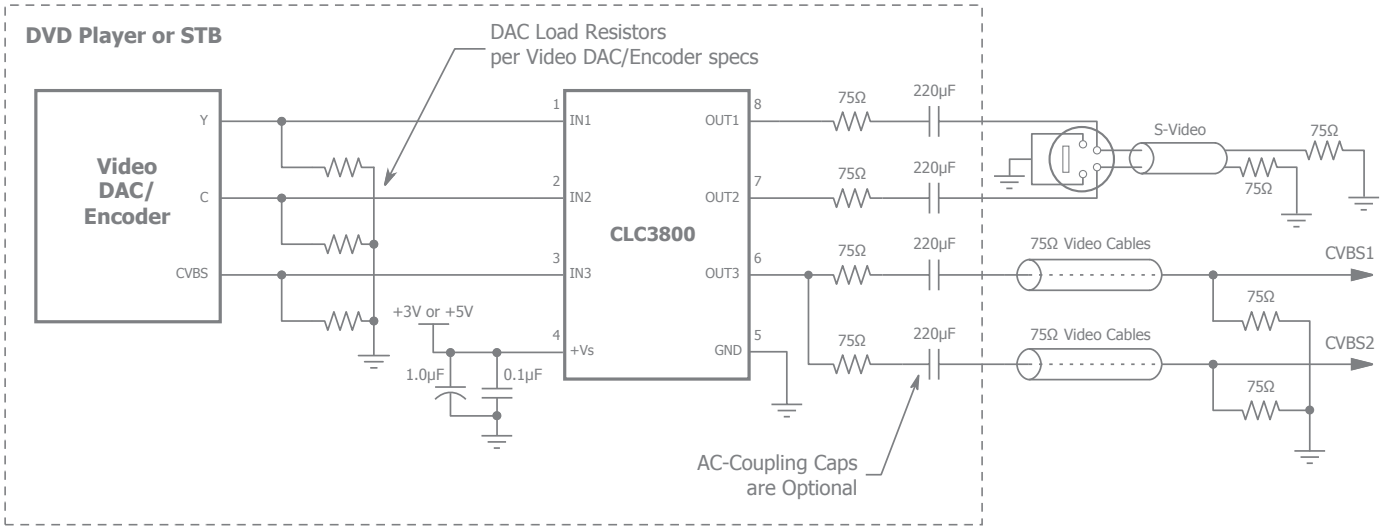


Figure 11. Typical Configuration for Composite (CVBS) and S-Video

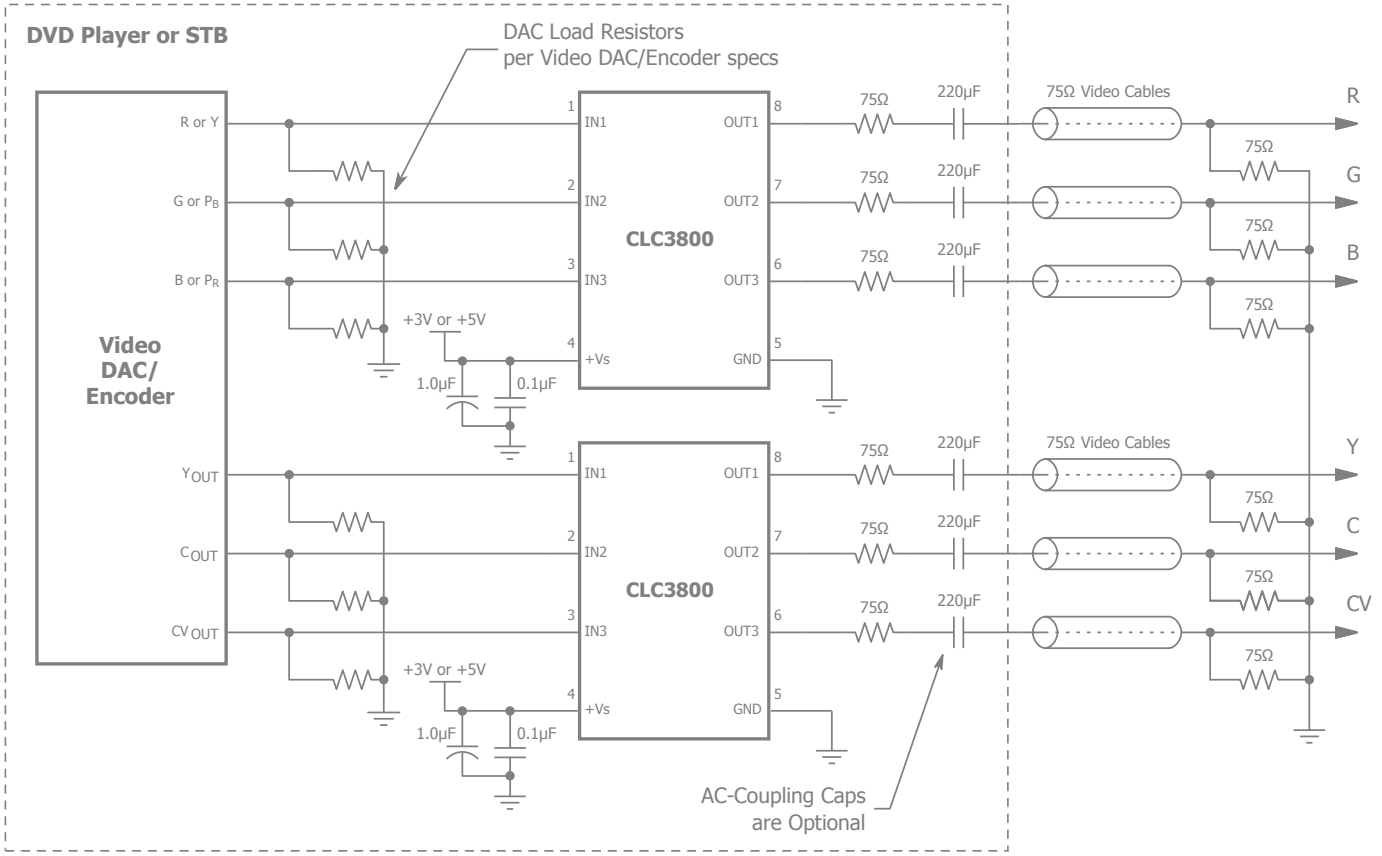
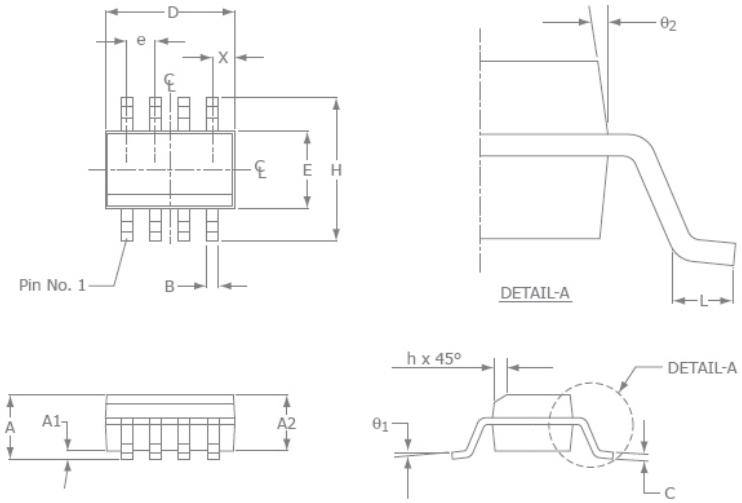


Figure 11. Typical Configuration for 6-channel application

Mechanical Dimensions

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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