AN1636
APPLICATION NOTE

UNDERSTANDING AND MINIMISING ADC CONVERSION ERRORS

By Microcontroller Division Applications

1 INTRODUCTION

The purpose of this document is to explain the different ADC errors and the techniques that application developers can use to minimise them. The ADC (Analog to Digital Converter) is an important peripheral that connects the analog world to the digital world of microcontrollers.

In this application note the ADC embedded in the ST7 microcontroller is used as an example, however the same principles to apply to other ADCs.

The accuracy of analog to digital conversion has an impact on overall system quality and efficiency. To be able to improve accuracy you need to understand the errors associated with the ADC and the parameters affecting them.

The ADC itself, cannot ensure the accuracy of results, It depends on your overall system design. For this reason, you need to do some careful preparation before starting your development.

Lots of parameters affect the ADC accuracy depending on the application. Some of these factors are: PCB layout, voltage source, I/O switching and analog source impedance.

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1 WHAT IS AN ADC?

An analog to digital converter is a peripheral which converts analog signals in a defined range to the digital outputs.

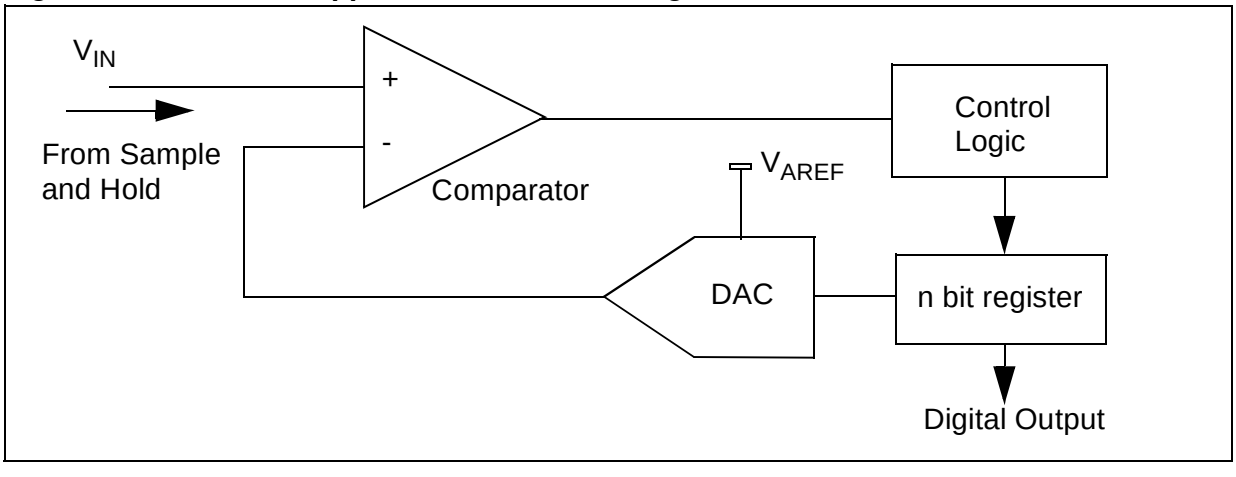
In the real world, signals are mostly available in analog form. To use a microcontroller in this type of system, an ADC is required, so that the signals can be converted to the digital values. The application software can then process the digital outputs and take decisions depending on the application or system requirements.

The limitation imposed by the finite number of digital outputs decides how close the output is to the analog input. The more bits there are in the output, the closer the digital result will be to the analog signal. In other words, the resolution of the ADC is defined by the number of bits in the digital result (8 bits, 10 bits etc) and the input voltage range.

Successive Approximation Method

Different techniques are available for converting analog signals to digital outputs. The Successive approximation method is the most popular technique. It is also known as Successive approximation Register (SAR) technique. This technique uses binary search method. It consists of a high speed comparator, DAC (digital to analog converter), and control logic. Refer to Figure 1.

Figure 1. Successive Approximation Block Diagram



The SAR starts by forcing the MSB (Most Significant bit) high (for example in an 8 bit ADC it becomes 1000 0000), the DAC converts it to $V_{AREF}/2$. The analog comparator compares the input voltage with $V_{AREF}/2$. If the input voltage is greater than the voltage corresponding to the MSB, the bit is left set, otherwise it is reset.

V_{AREF} is the reference voltage used by ADC for conversions. The details are mentioned in Section 2.5

After this comparison is done, the next significant bit is set (=V_{AREF}/4) and a comparison is done again with the input voltage. The procedure is followed till all the bit positions are compared.

At the end of all the bit comparisons we get the corresponding digital output for the analog input.

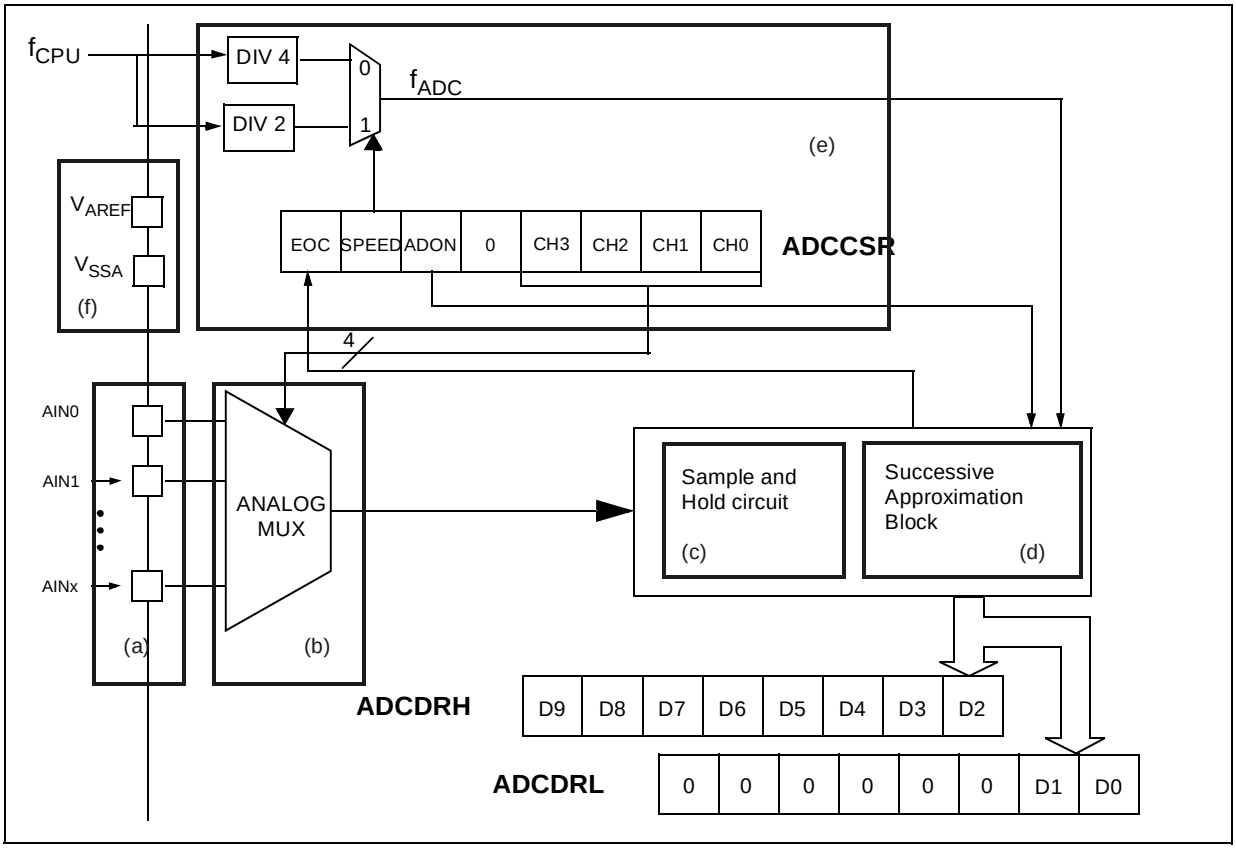
The successive approximation steps are shown in Table 1. As you can see, the digital output obtained from the ADC is B2h when the analog input is 3.5V.

Table 1. 8-bit ADC successive approximation steps

Steps	Vin = 3.5v, V_{AREF}= 5V			
	Digital code	DAC output	Comparator output	digital output (for steps)
1	1000 0000	2.5v	1	1000 0000
2	1100 0000	3.76v	0	1000 0000
3	1010 0000	3.13v	1	1010 0000
4	1011 0000	3.45	1	1011 0000
5	1011 1000	3.6	0	1011 0000
6	1011 0100	3.52	0	1011 0000
7	1011 0010	3.49	1	1011 0010
8	1011 0011	3.509	0	1011 0010
				Final output = B2h

2 ADC BLOCK DESCRIPTION

Figure 2. ADC Block diagram



The ADC can be divided into the following blocks.

a. Analog input pins

b. Analog multiplexer

c. Sample and Hold circuit

d. Successive approximation block

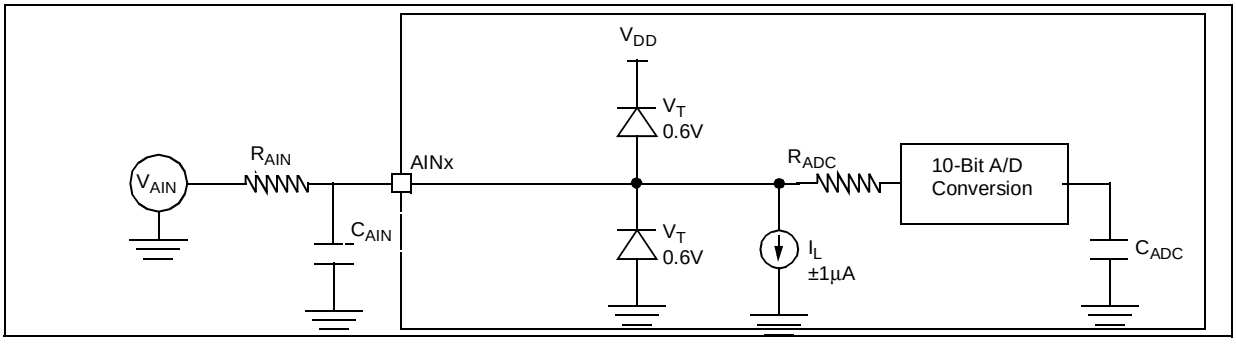
e. Control block

f. Analog supply/ reference

2.1 ANALOG INPUT PINS

Several analog input pins are available to connect different analog signals. These are internally multiplexed to use same sample and hold circuit and SAR logic.

Figure 3. Electrical diagram of typical ADC application

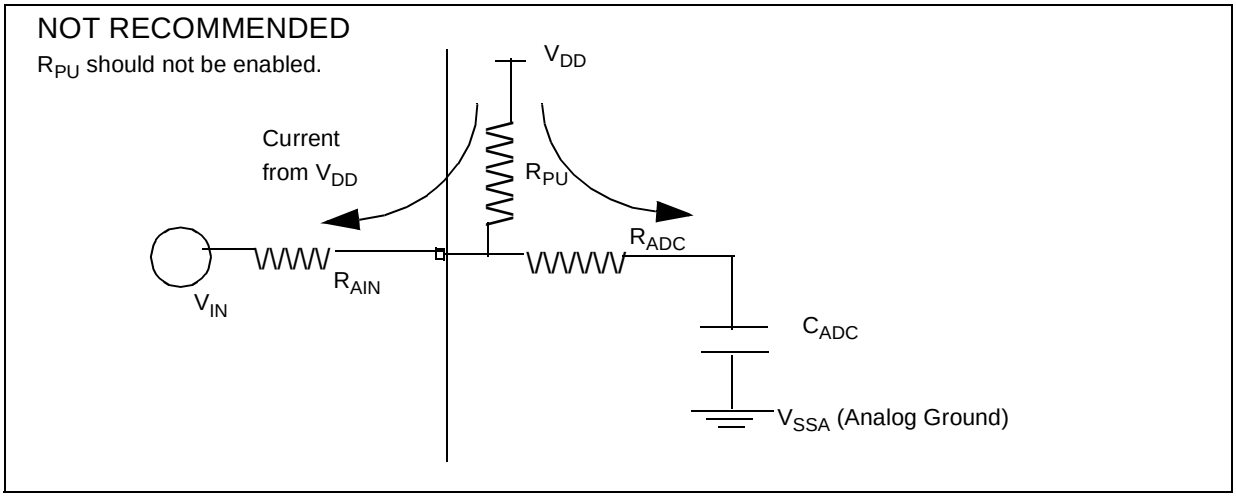


Configuring the analog pin

Choose any I/O port that has analog input capability (AIN alternate function) and configure it as floating input. You can do this by writing '0' in the DDR and OR register bits of the corresponding port. At reset, most of the ST7 IOs are configured by default as floating input.

The pin should NOT be configured as floating input with pull-up. This configuration reduces the ADC accuracy. The reason being the potential divider formed between the pull-up resistance and R_{ADC}. Also some current flows from V_{DD} to the analog source. This current is drawn from the V_{DD} supply. Also there is a potential divider formed between V_{DD}, R_{PU} and R_{AIN}, where R_{AIN} is the series impedance of the voltage source.

Figure 4. Analog input with pull-up



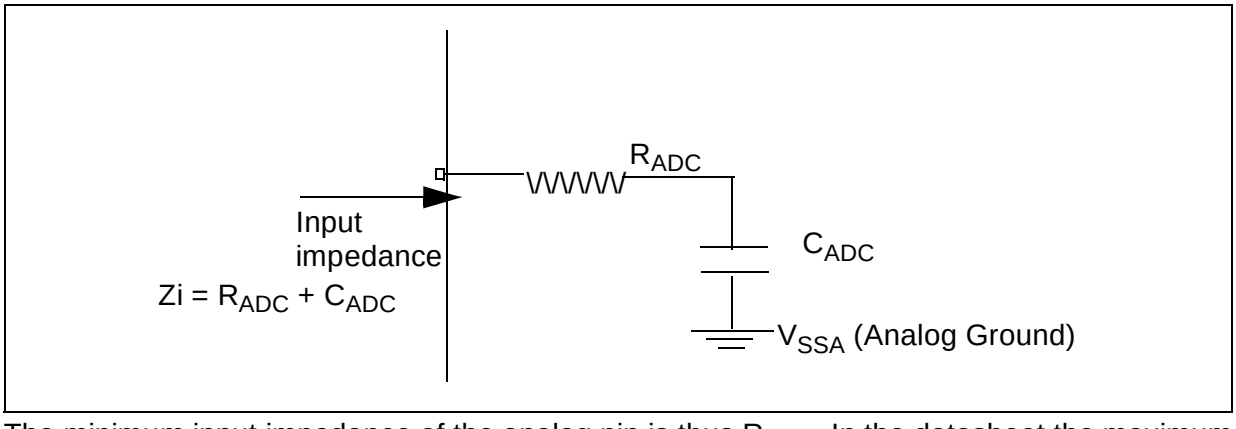
Configuring the analog input as floating input with pull-up (instead of floating input) will cause more current to be drawn from the V_{DD} supply. There is also an affect on the accuracy of the ADC and the digital output converted by ADC may not be accurate.

Analog Pin Input Impedance

R_{ADC} and C_{ADC} (hold capacitor) define the input impedance of the analog pins. R_{ADC} is also called as Rss (Resistance of sampling switch and internal trace/resistance). Please refer to the Sample and Hold circuit explanation in Section 2.3.

If the hold capacitor is fully discharged, the minimum input impedance is R_{ADC}. As the hold capacitor starts to charge, the current flowing into the pin will reduce. If the hold capacitor is charged to a level equal to the external voltage there will be only minimal charging current flowing into the analog input.

Figure 5. Analog input pin Impedance



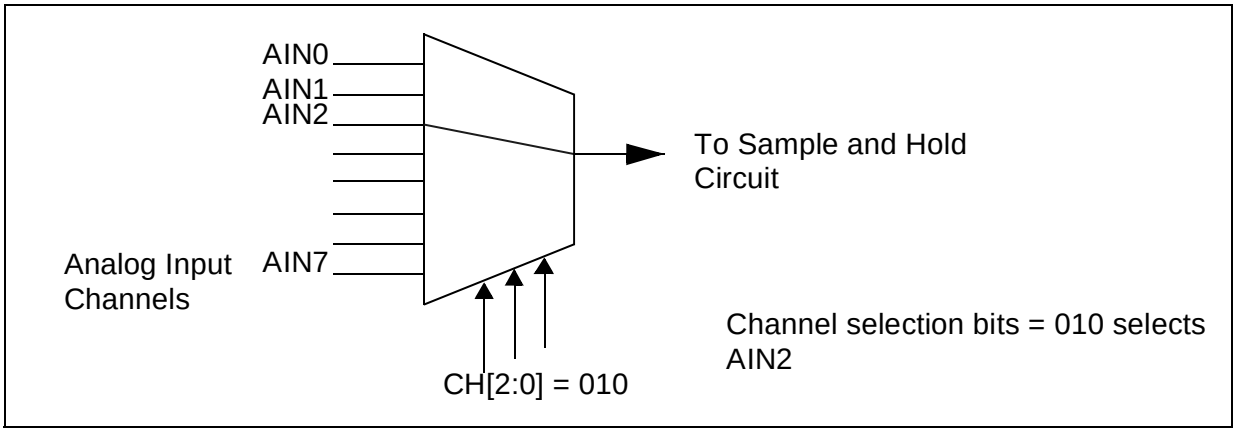
The minimum input impedance of the analog pin is thus R_{ADC}. In the datasheet the maximum value of R_{ADC} is specified instead of a typical value, so that the user can calculate the affect of external resistance on sampling. This is explained in Section 4.4.

2.2 ANALOG MULTIPLEXER

The ADC can have several analog input pins. These pins are connected internally to the Analog to Digital converter using the analog multiplexer. You can select each pin simply by writing in the appropriate control register. This allows a single Sample and Hold circuit and Analog to Digital Converter block to be used to convert several analog input sources.

This allows you to switch the analog channels and convert them one by one through software control.

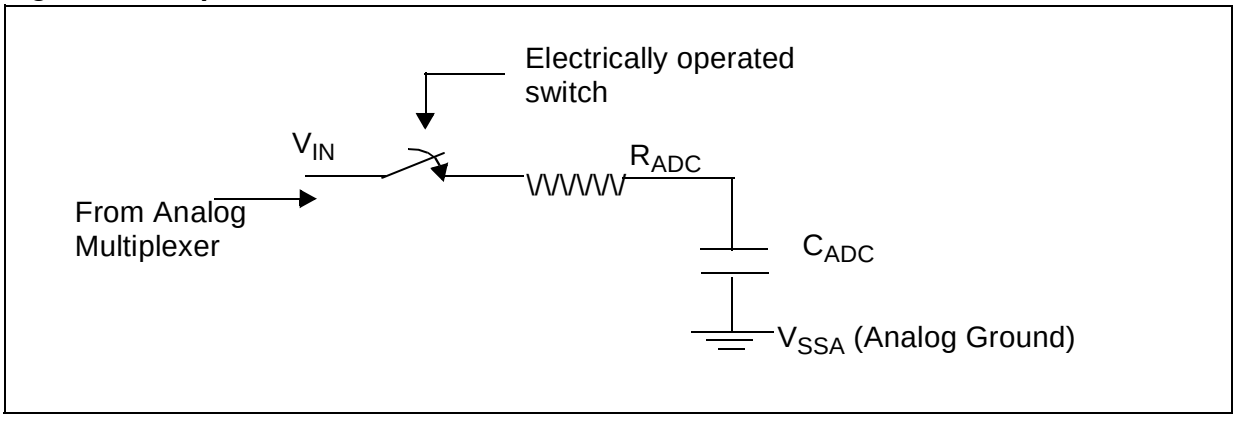
Figure 6. Analog multiplexer



2.3 SAMPLE AND HOLD CIRCUIT

The sample and hold circuit samples the input signal and charges the internal hold capacitor C_{ADC} to the voltage equal to V_{IN} through R_{ADC}. The analog pin is then disconnected and the voltage across the capacitor is then converted to digital code using successive approximation.

Figure 7. Sample and Hold circuit

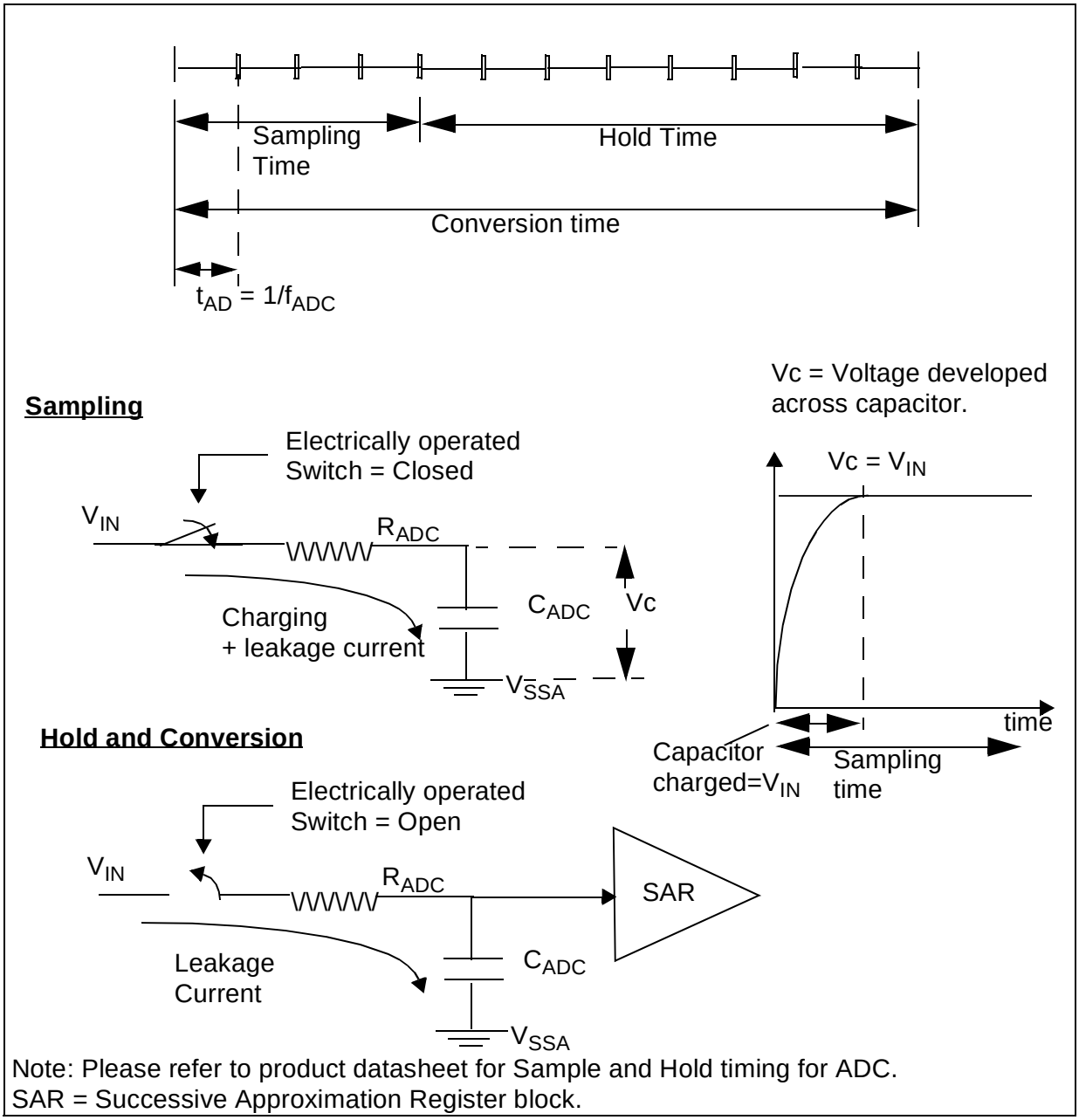


The sample and hold circuit consists of an electrically operated analog switch, internal charging resistance and hold capacitor.

As soon as the ADC conversion starts, the electrically operated switch is closed, connecting the hold capacitor to the analog input through the internal ADC resistance R_{ADC}. This causes a charging current to flow into the analog input and the capacitor starts to charge. The time the switch remains closed is decided by the f_{ADC}. It is called **sampling time**. The sampling time is generally indicated in the datasheet as a multiple of f_{ADC} clock periods.

Time period $t_{AD} = 1/f_{ADC}$

Figure 8. Sample and Hold timing and electrical diagram



Note: Please refer to product datasheet for Sample and Hold timing for ADC.
SAR = Successive Approximation Register block.

After the sampling time, the input capacitor has the same voltage as the input, the analog switch is then disconnected from the input and successive approximation conversion is started, to convert the voltage stored in the hold capacitor. This time is known as **Hold time**. It is also expressed in multiples of t_{AD} ($1/f_{ADC}$).

The total conversion time of the ADC is the addition of sampling time and hold time. The sample and hold circuit is also known as track and hold.

2.4 CONTROL BLOCK

This block consists of logic which controls the sample and hold circuit, starts the SAR and then generates the conversion of the 'conversion complete' signal for the microcontroller.

2.5 ANALOG SUPPLY AND REFERENCE

Depending on microcontroller and packaging, the analog supply pins are generally available on the package.

V_{DDA} - analog supply (or, V_{AREF} - reference voltage)

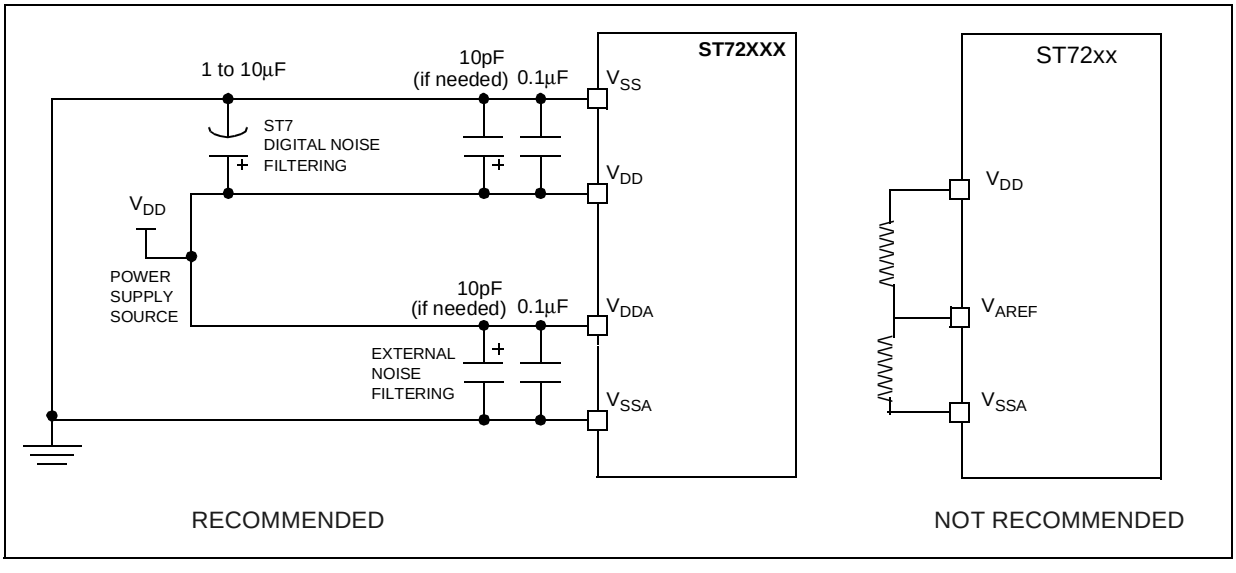
V_{SSA}- analog ground.

If these pins are not available the V_{DDA} (analog supply) is shorted to V_{DD} and V_{SSA} is shorted to V_{SS} internally.

Separate analog power supply pins are available to the user to improve the ADC performance. It is recommended to put the filtering capacitor between V_{DDA} and V_{SSA} so that power supply noise (or ripples) on V_{DDA} are filtered and do not affect the ADC accuracy.

The V_{AREF} pins are available instead of V_{DDA} when the analog supply voltage can be different from the V_{DD}. You may choose to keep V_{AREF} shorted to V_{DD} if a dual supply is to be avoided.

Figure 9. Analog Supply block



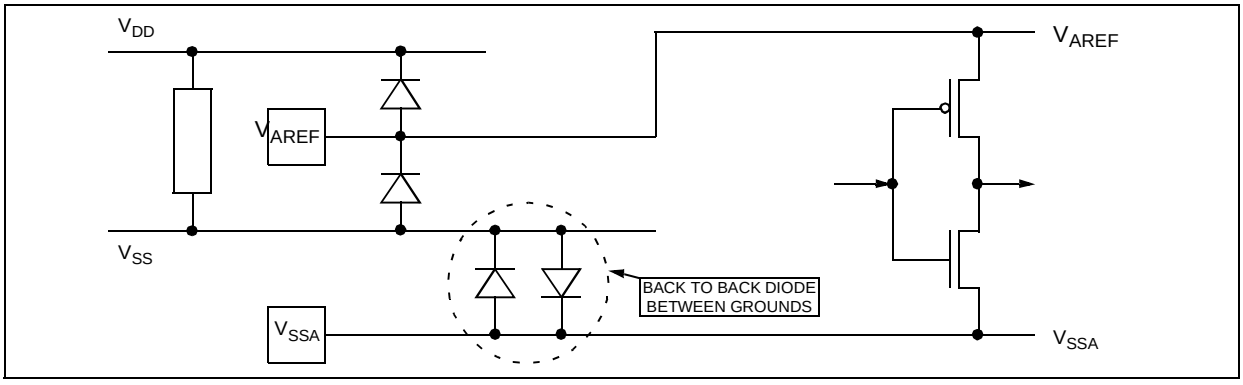
As these pins provide power supply to the analog block, you should not connect a resistor in series with V_{AREF}. This will cause the voltage to drop due to the current flowing through the resistor and hence will affect the accuracy of the ADC.

Do not leave the V_{DDA}/V_{AREF}, V_{SS} pins unconnected. If your application does not use the ADC, you must connect these pins as follows: V_{DDA} must be connected to $V_{DD,}$ and V_{SSA}

must be connected to the V_{SS} of the microcontroller. V_{SSA} cannot have any voltage other than V_{SS}.

Make sure that V_{AREF} is not greater than V_{DD}. There is a protection diode from V_{AREF} to V_{DD}. Similarly V_{SSA} should not be less than or greater than V_{SS}. There are protection diodes connected back-to-back between V_{SSA} and V_{SS}.

Figure 10. Multisupply Configuration



3 ADC TERMINOLOGY

There are some terms associated with the ADC which we should understand before we move further.

3.1 REFERENCE VOLTAGE

The ADC requires a reference voltage to which the analog input is compared to produce the digital output. The digital output is the ratio of the analog input with respect to this reference voltage.

digital value =((Analog input voltage)/(reference voltage high- reference voltage low)) * (2^n-1)

where n = number of bits of ADC digital output.

The reference voltage is the maximum input voltage that can be converted by the ADC. V_{AREF} is the reference voltage for the ADC. If V_{AREF} is not available V_{DDA} is used as reference.

For example: for 10-bit ADC, V_{IN}=1V, V_{AREF}=5V,

Digital value = (1V/5V) *1023 = 204d = 0CCh

3.2 RESOLUTION

The ADC resolution is defined as the smallest incremental voltage that can be recognized and hence it causes a change in the digital output. It is usually expressed as the number of bits output by the ADC.

Hence an ADC which converts the analog signal to a 10-bit digital value, has a resolution of 10 bits.

The smallest incremental voltage that can be recognized is expressed in terms of LSB.

$1LSB = (V_{AREF} - V_{SSA})/2^n$

where LSB = Least significant bit.

n = number of bits output by the ADC.

V_{AREF} = Reference voltage

V_{SSA} = Analog ground

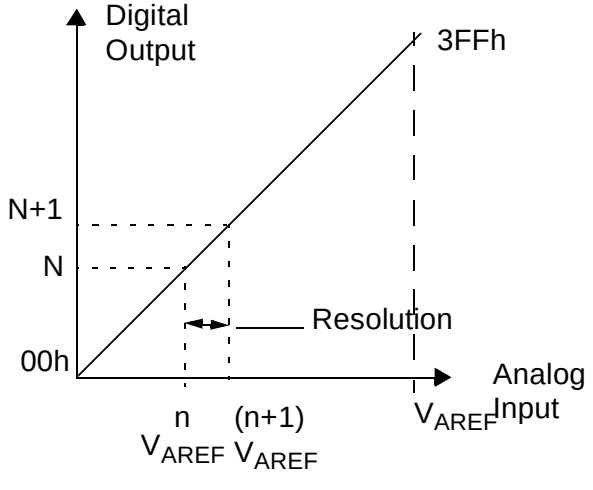
An ADC which has 'n' bit digital output, provides 2^n digital values. It includes both 0 and 2^n-1.

With a 5V reference voltage, the resolution is 5 (volts) /2^{10} = 5 (volts)/1024 = 4.88 mV.

This means that for a change in 4.88mV analog input the ADC converted digital value will change by 1LSB.

In reality there are 2^n-1 steps. So the actual resolution is $1LSB = (V_{AREF} - V_{SSA})/(2^n - 1)$. As in practice there is very little difference between the two calculated values because 'n' is quite a large number, both definitions are used.

Figure 11. Resolution representation

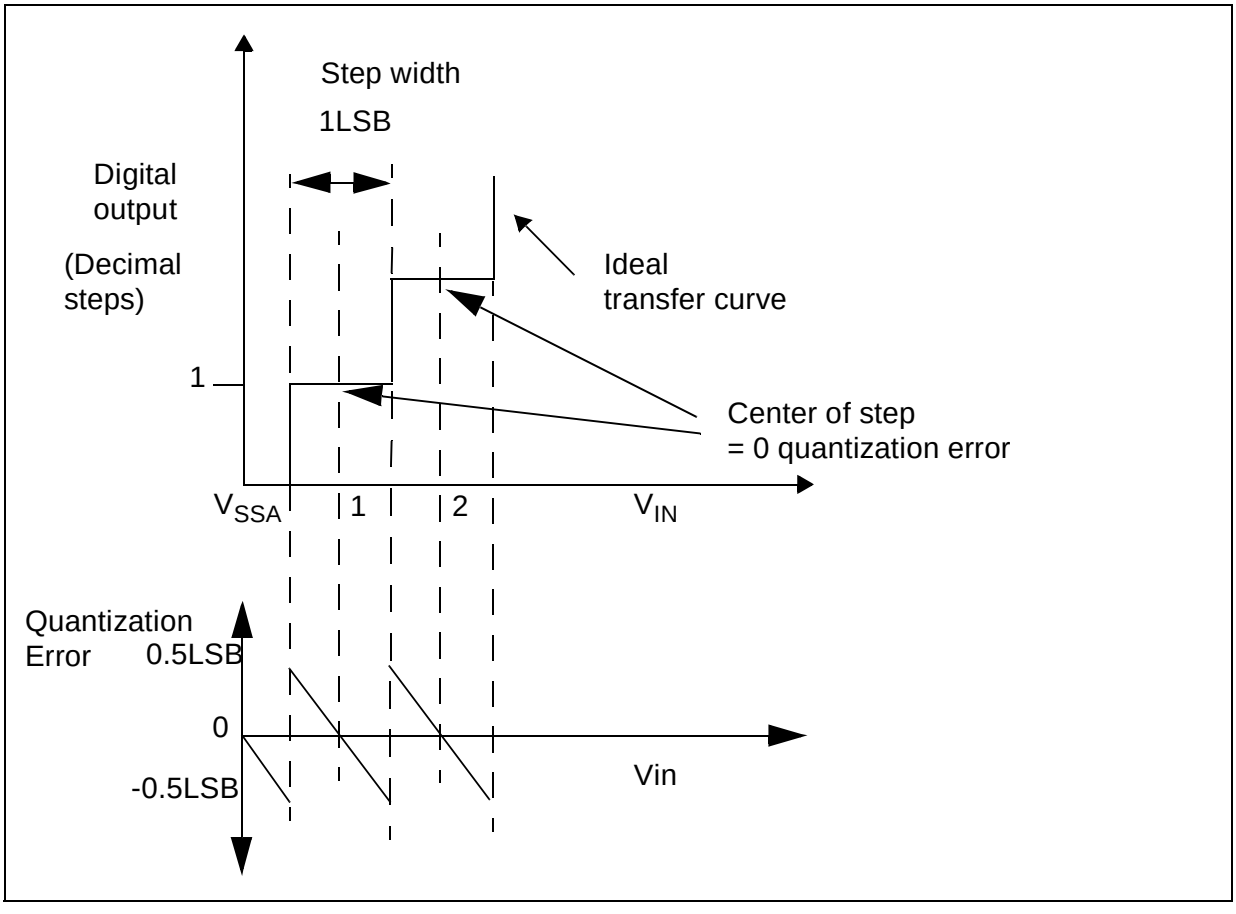


3.3 QUANTIZATION

In theory, the continuous analog signal can be broken into an infinite number of digital steps, but the quantization of an analog signal by the ADC can be done only in the finite number of steps which can be produced by the ADC.

The quantization error is the error introduced because of the process of quantization. Ideally any analog input voltage can be maximum of 1/2 LSB away from its nearest digital code. So the quantization error is 0.5LSB for the ADC.

Figure 12. Quantization of analog signal



3.4 MONOTONICITY

Monotonicity is defined as a property of the ADC transfer function, which ensures that converted digital values will never decrease if the analog input does not decrease and conversion results will never increase if the analog input does not increase. This property is inherent to the design of the ADC, subject to the accuracy specified in the datasheet in each case.

3.5 BIPOLAR AND UNIPOLAR ADC INPUT

ADCs that can accept both positive and negative analog signals are known as bipolar.

ADCs that can accept only positive input voltage are known as unipolar. ADCs embedded in microcontrollers are unipolar, as the input cannot decrease below the analog ground.

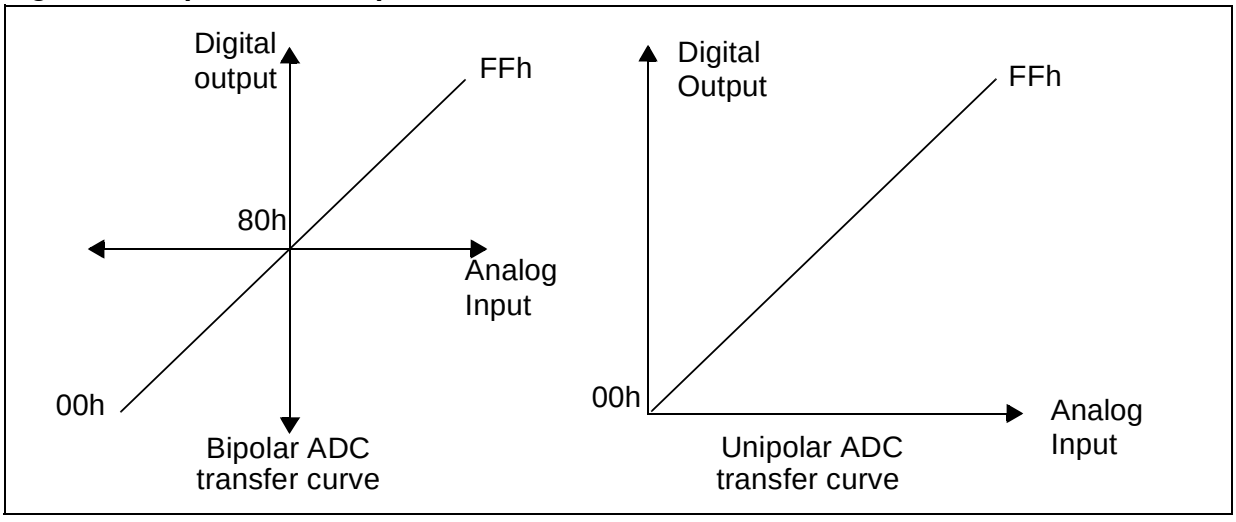
ST7 microcontrollers have unipolar input ADCs and have an input range from 0V to V_{AREF}.

In an 8-bit ADC, for example,

– A unipolar ADC with an input range of 0V to 5V will output the digital code 00h for 0V and FFh for 5V.

– A bipolar ADC with an input range of -5V to +5V will output the digital code 00h for -5V, 80h for 0V and FFh for +5V.

Figure 13. Bipolar and Unipolar ADC transfer curves



3.6 HARDWARE AVERAGING

To improve ADC accuracy, you can perform a number of ADC conversions and use the average of these conversions to obtain more accurate digital output. In hardware averaging ADCs, this technique is embedded in the hardware and the averaging is done by the hardware itself. The final digital output received from ADC is actually the average of the conversions.

This hardware averaging technique is implemented in some ST7 microcontrollers. The conversion time is thus increased as several conversions are performed.

3.7 SAMPLING THEOREM

The sampling theorem states that to convert the analog signal with frequency ‘f’, the ADC sampling frequency must be at least twice the analog signal frequency. So the sampling frequency must be at least ‘2*f’.

Sampling the signal at twice the analog signal frequency will not result in a loss of information. If sampling frequency is less, then the information will be lost. This is a standard theorem that applies to ADCs in general.

For example: an ADC with a conversion time of 10µs can be used to sample an analog signal with a time period of 20µs, i.e. 50kHz. (1/20µs).

4 SOURCES OF ERROR

4.1 POWER SUPPLY NOISE

The analog power supply is used as the reference voltage for conversion. As the ADC output is the ratio between the analog signal voltage and the supply voltage, any noise on the analog reference will cause a change in the converted digital value.

For example: with a 5V supply (analog reference) and 1V signal, the converted result is

(1/5)*1023 = 204d = CCh

But with 40mV ripple peak-to-peak in the power supply, the converted value is

(1/5.04)*1023 = 202d = CAh (when V_{AREF} was at its peak).

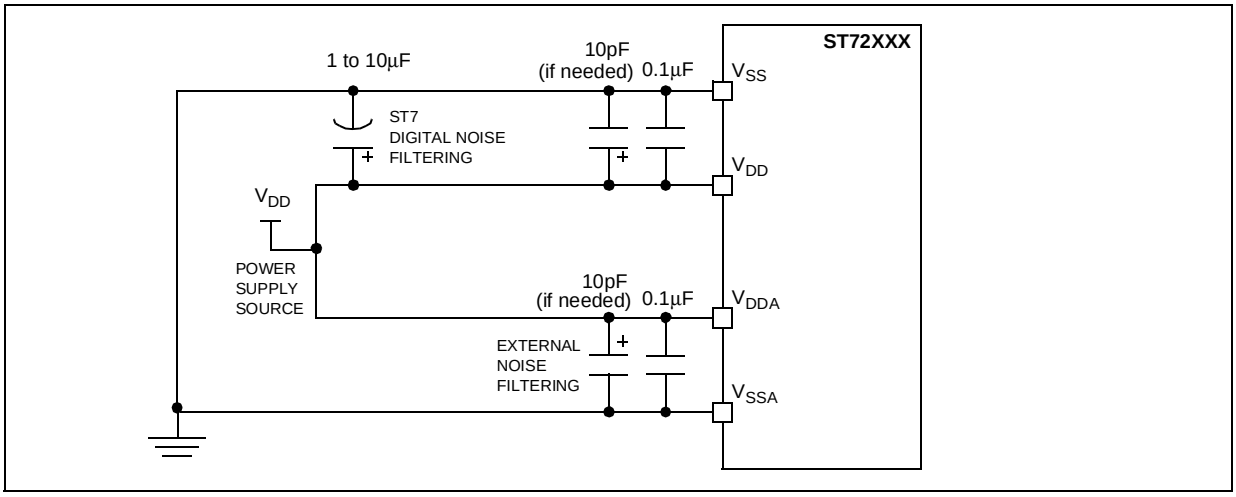
The SMPS (Switch mode power supply) normally has internal fast switching power transistors. This introduces high frequency noise in the output. The switching noise is in the range of 15-1Mhz. You can filter this noise by putting low value capacitors (10pf - 22pf) on the power supply rail. Low value capacitors have low reactance whereas high value capacitors have high reactance.

Linear regulators have better output in terms of noise. The mains must be stepped down, rectified and filtered and then fed to linear regulators. It is highly recommended to have the filter capacitors at the rectifier output. Please refer to the datasheet of the linear regulator in each case. Generally 0.01uF is recommended.

If you are using a switching power supply, it is recommended to have a linear regulator to supply the analog section.

It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1uF and optionally, if needed 10pF capacitors as close as possible to the ST7 power supply pins and a 1 to 10uF capacitor close to the power source.

Figure 14. Power supply filtering



The capacitors allow the AC signals to pass through them. The small value capacitors filter high frequency noise and the high value capacitors filter low frequency noise. Ceramic capacitors are generally available in small values (1pf to 0.1 µf) and small voltages 16V to 50V. It is recommended to place the ceramic capacitors close to the main supply pins (V_{DD} & V_{SS} and analog supply pins (V_{DDA} & V_{SSA}). These filter the noise induced in the PCB tracks. Small capacitors can react fast to current surges and discharge quickly for fast current requirements. Tantalum capacitors can also be used along with ceramic capacitors.

High value capacitors (10µf to 100µf) which are generally electrolytic, you can use them to filter low frequency noise. It is recommended to put them near the power source. You can also filter high frequency noise using a ferrite inductance in series with the power supply. Ferrites cause low DC loss (negligible) unless the current is high. This is because the series resistance of the wire is very low. But for high frequency, the impedance offered is high.

In most ST7 microcontrollers the V_{DD} & V_{SS} pins are placed close to each other. Similarly V_{AREF} & V_{SSA} pins are placed closed to each other. This allows you to put a capacitor very close to the microcontroller with very short leads. For multiple V_{DD} & V_{SS} pins, use separate decoupling capacitors.

4.2 POWER SUPPLY REGULATION

The power supply should have good line and load regulation. As the ADC uses V_{AREF} as the analog reference and the digital value is the ratio of analog input signal and V_{AREF}. So V_{AREF} must remain stable at different loads.

Whenever the load is increased by switching-on a part of the circuit, the increase in current must not cause the voltage to decrease. If the voltage remains stable over a wide range of current the power supply has good load regulation.

If the voltage decreases, the decrease in V_{AREF} changes the ratio of the analog signal to V_{AREF}.

$$\text{digital output} = (V_{IN}/V_{AREF}) * (2^n-1)$$

A change in V_{AREF} will make a change in the digital output.

For example: for the L7805 voltage regulator, (Please refer to the L7805 datasheet for details).

Line regulation is 20mV typical for I(load) between 1mA to 100mA.

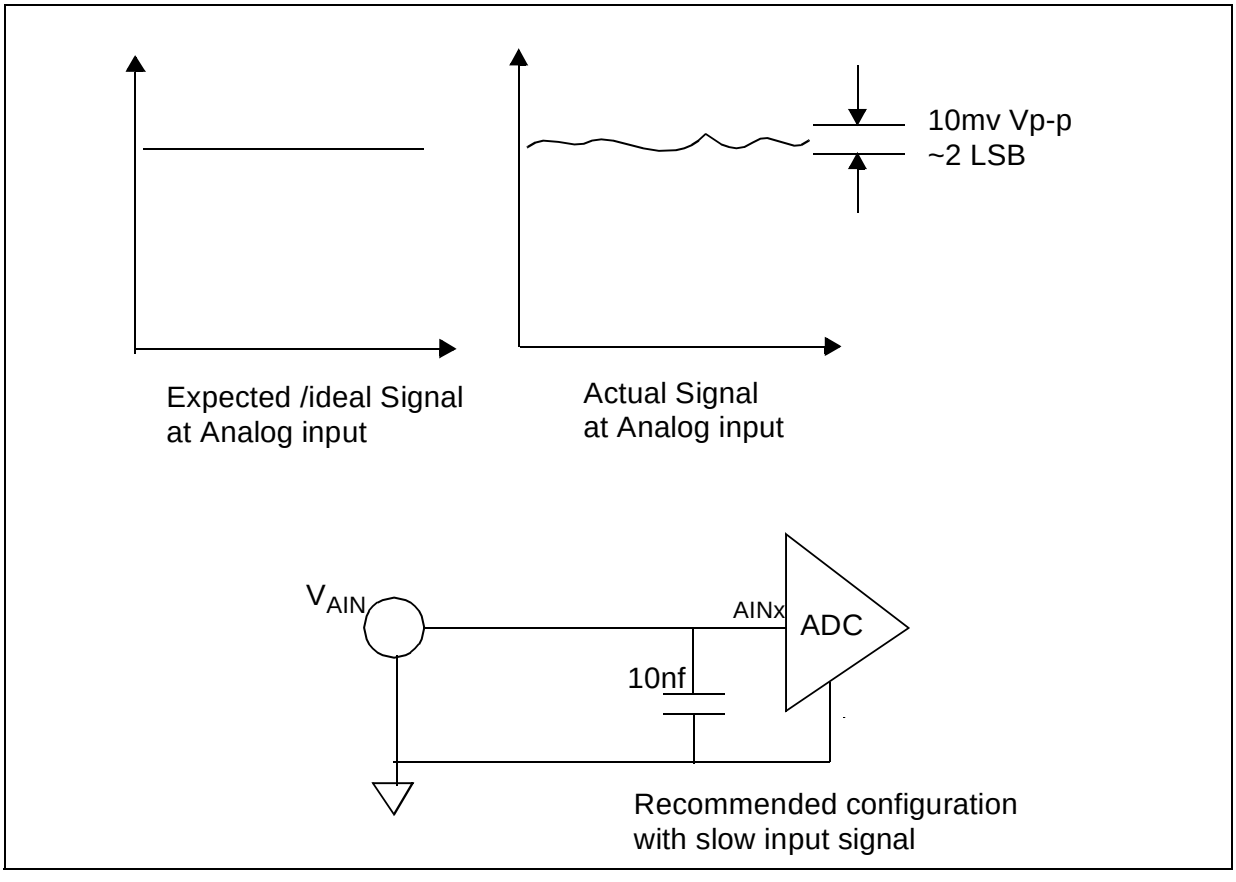
Similarly, Line regulation is 18mV typical for rectified voltage between 7V to 20V.

4.3 ANALOG INPUT SIGNAL NOISE

The analog signal to be converted may have some noise superimposed on it. There may be a high frequency noise signal. It is recommended to connect a 10nf capacitor to the analog input signal. You can also add a low pass filter but this will affect F_{AIN}, so you should use this only if the input signal frequency is low.

F_{AIN} is the frequency of the analog input signal. For other details refer to Section 4.5.

Figure 15. Noise in analog input signal



4.4 EFFECT OF ANALOG SOURCE RESISTANCE

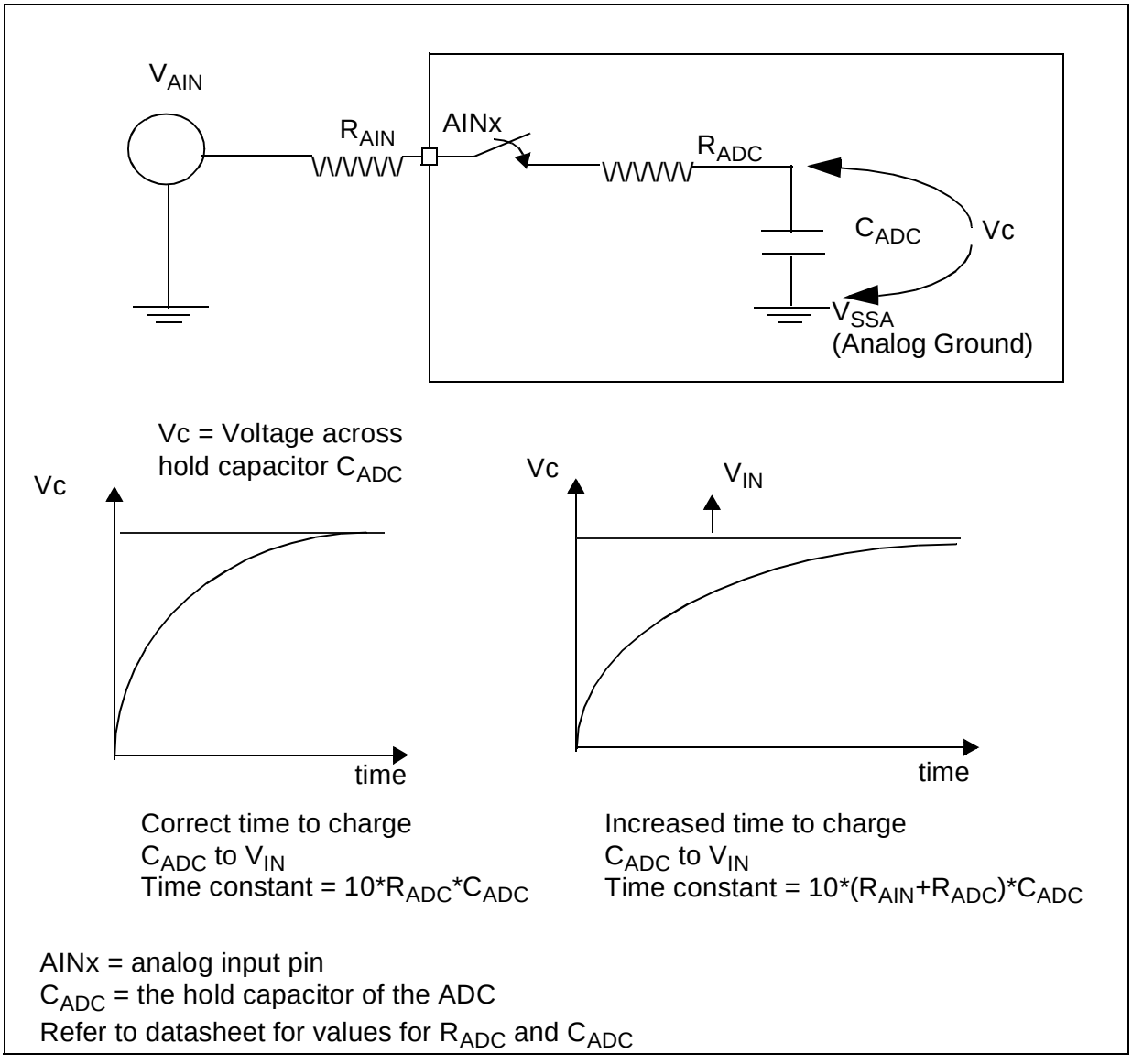
The impedance of the analog signal source or series resistance (R_{AIN}) between source and pin will cause a voltage drop across it because of current flowing into the pin.

The R_{ADC} and C_{ADC} form an RC network. The charging of the capacitor is controlled by R_{ADC}. When there is R_{AIN} in series, the effective value of charging of C_{ADC} will be governed by $R_{ADC}+R_{AIN}$, So the charging time constant will become $(R_{ADC}+R_{AIN})*C_{ADC}$. The sampling time for ADC should be greater than 10 times the RC time constant. Please refer to the explanation in Section 4.5.

With external input resistance, the sampling time required by the ADC will also increase. The ADC has a fixed sampling time depending on f_{ADC}. With the addition of source resistance, the time required to fully charge the hold capacitor will increase. If the sampling time is less than the time required to fully charge the C_{ADC} through $R_{ADC}+R_{AIN,}$ the digital value converted by the ADC will be less than the actual value.

Sampling time > $10*(R_{ADC}+R_{AIN})*C_{ADC}$

Figure 16. Effect of source impedance on internal sampling

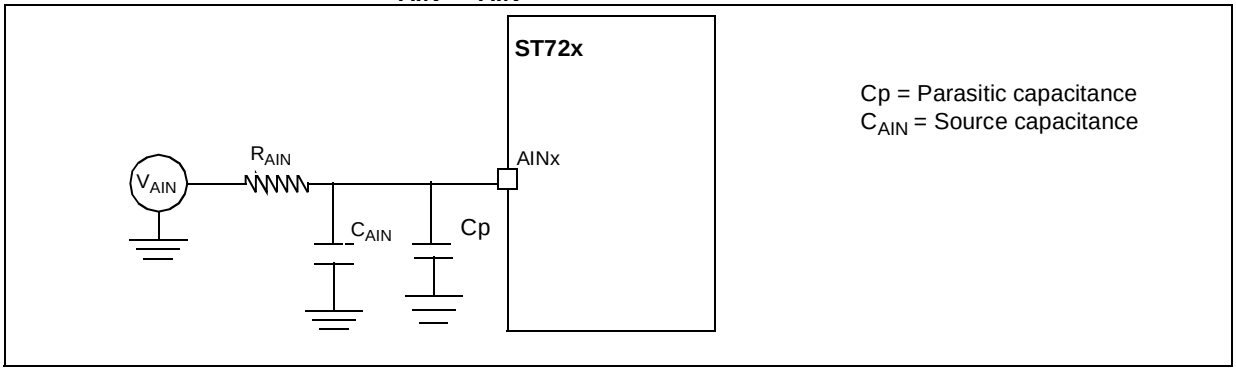


4.5 EFFECT OF SOURCE CAPACITANCE

You have to take the capacitance and resistance at the source into account when converting analog signals. The source resistance and capacitance form an RC network and the ADC conversion results may not be accurate unless the external capacitor is fully charged to the level of the input voltage.

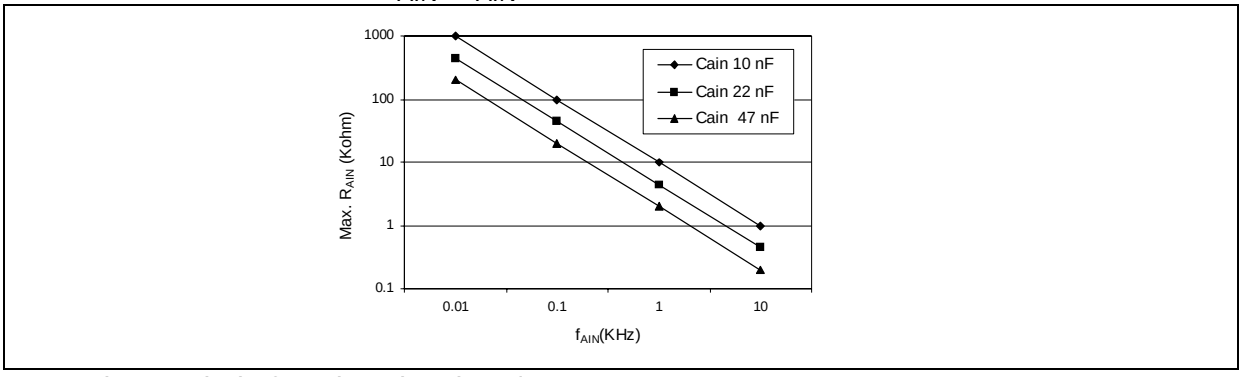
The external capacitance at source is denoted by C_{AIN}.

Figure 17. ADC input with R_{AIN}, C_{AIN}



The external capacitance will not allow the voltage of the analog input to be exactly the same as V_{IN} if it is not fully charged by the analog source. If the analog input signal varies, then the analog signal frequency (F_{AIN}) should be such that the time period of this analog signal is at least 10 * R_{AIN} * C_{AIN}.

Figure 18. Recommended R_{AIN}, C_{AIN} values



T_{AIN} = time period of analog signal = $1/F_{AIN}$

T_{AIN} >= 10 * R_{AIN} * C_{AIN}.

F_{AIN} = 1/ T_{AIN} <= 1/ (10 * R_{AIN} * C_{AIN})

For example:

For R_{AIN} = 10K, C_{AIN} = 10nf

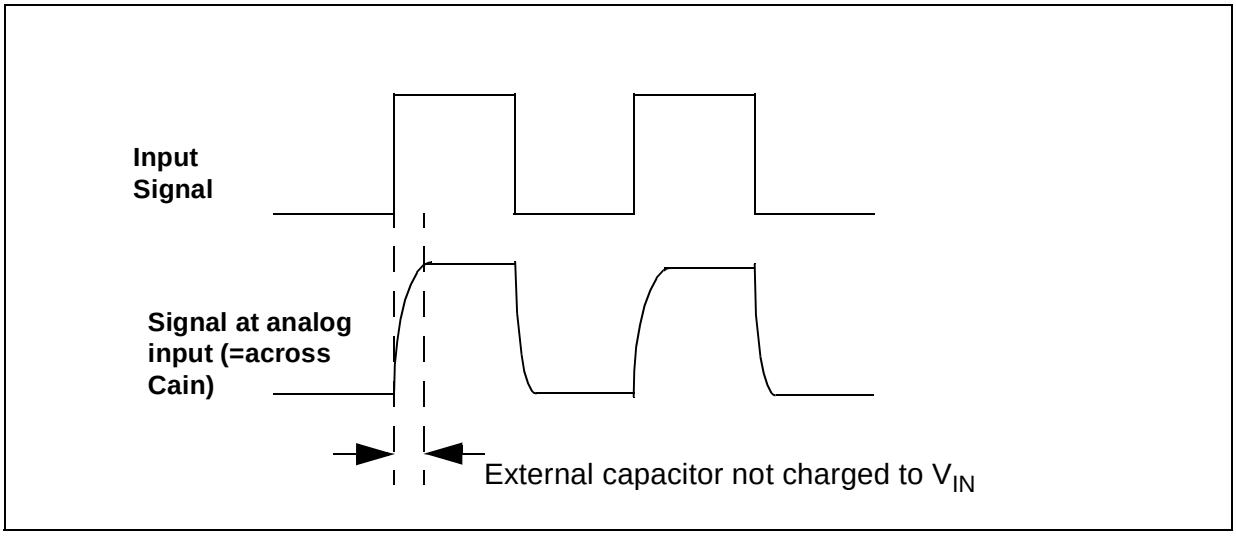
T_{AIN} = 10 R_{AIN} * C_{AIN}

= 10 * 10K* 10n

= 1000µs = 1ms

F_{AIN} = $1/T_{AIN}$ = 1/1ms = 1KHz maximum.

Figure 19. Effect of external R and C.



The voltage across the capacitor follows the following equation:

$Vc = V_{IN} (1 - e^{-t/RC})$

Vc = Voltage across capacitor

V_{IN} = Voltage from voltage source

e = Exponential constant = 2.71 (approx.)

t= Time, after which voltage across the capacitor is to be calculated.

R = Resistance used to charge the capacitor

C= Capacitance value.

R*C = time constant of RC network

Table 2. Voltage across the capacitor

t/RC	Vc/V_{IN}	Vc
1	$(1- (2.71)^{-1})$	$0.63*V_{IN}$
2	$(1- (2.71)^{-2})$	$0.86*V_{IN}$
3	$(1- (2.71)^{-3})$	$0.94*V_{IN}$
4	$(1- (2.71)^{-4})$	$0.98*V_{IN}$
8	$(1- (2.71)^{-8})$	$0.9996*V_{IN}$
10	$(1- (2.71)^{-10})$	0.9999Vin

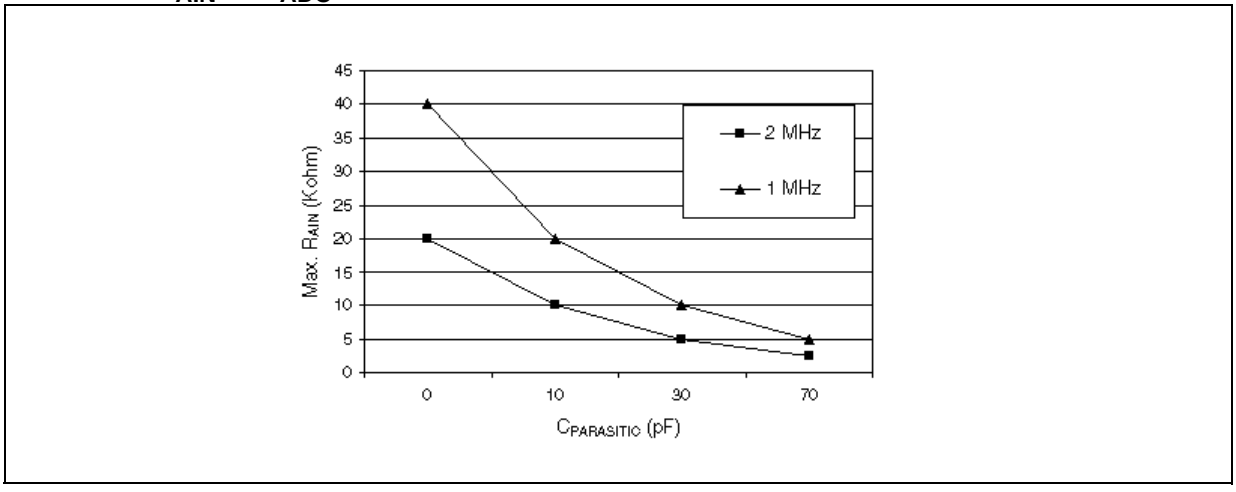
It should be noted that when the ratio of t/RC increases, the voltage developed across the capacitor becomes nearly equal to V_{IN}. The conversion result will be correct only when the capacitor is fully charged.

Therefore, t >= 10*R*C.

The parasitic capacitance formed at the analog input because of track paths etc. appears in parallel with external capacitance. So it must be added to C_{AIN}. However when the parasitic capacitance value is much less than C_{AIN}, it can be ignored.

When C_{AIN} is small (for example $C_{AIN} < 100*C_{ADC}$), it may not be able to hold the V_{IN} voltage effectively. So when ADC conversion is started, C_{ADC} will appear across the C_{AIN} through R_{ADC} causing C_{AIN} to effectively discharge. So we need to consider the sampling time required with external resistance and capacitance.

Figure 20. R_{AIN} Vs f_{ADC}



For example:

With R_{AIN}=10K, C_{AIN} (or Cparasitic) = 10pf, C_{ADC}=6pf

Time for charging external capacitor = $R_{AIN}*C_{AIN}$= 10k* 10pf = 100ns

$10*R_{AIN}*C_{AIN}$ = 1us.

Time for charging hold capacitor $C_{ADC} = (R_{AIN}+R_{ADC})* C_{ADC}$

RC = 12K*6pf =72ns

10RC = 720ns = 0.72us

Total time = 1us + 0.72µs = 1.72µs. (approx.)

So, for ADCs with f_{ADC}=2Mhz, sampling time = $4*t_{AD}$= 2µs.

With total time of 1.72µs obtained with R_{AIN} and Cparasitic, the sampling time of 2µs is already at its upper limit. If the resistance is higher, f_{ADC} must be decreased to increase the sampling time. So f_{ADC} less than 2MHz can be used. It can be noted that for f_{ADC} = 1MHz, R_{ADC} can be up to 20 kOhm.

At lower $f_{ADC,}$ we can start the ADC conversion as the sampling time is long enough to charge both C_{ADC} and C_{AIN} (or Cparasitic).

4.6 EFFECT OF INJECTION CURRENT

ST microcontrollers have robust tolerance of additional leakage current introduced on analog input signals as an effect of negative injection current. Negative injection current on any analog pin (or closely placed digital input pin) may introduce leakage current into the ADC input. The worst case is the adjacent analog channel. Negative injection current is introduced when $V_{IN}<V_{SS}$. Therefore current flows out from the I/O pin.

Analog pins can be protected against negative injection by adding a Schottky diode (pin to ground).

For example:

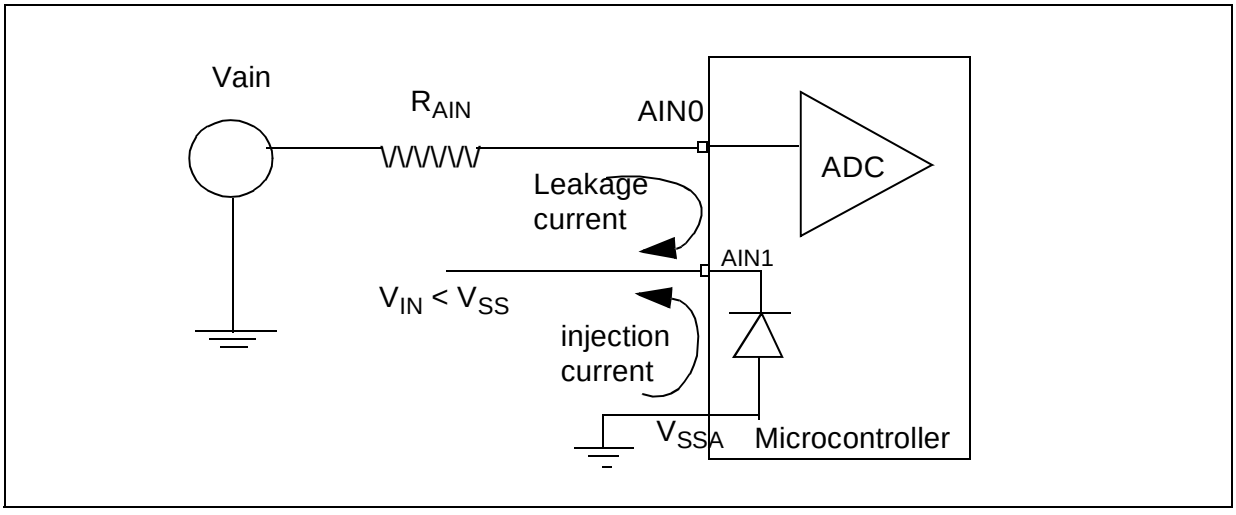
For an injection of 0.8mA on the analog input pin ST specifies a maximum leakage current of 1.6µA (please refer to the respective product datasheet)

as Voltage = Current * Resistance. The voltage drop due to this leakage current across R_{AIN} is:

$V\ (R_{AIN})= R_{AIN} * I_{Leak}$

If source series resistance R_{AIN} is 10K, the leakage current will introduce 1.6µA*10kohm = 16mV for 10-bit ADC, 1LSB = 5V/1023 = 4.8mV. A drop of 16mV will correspond to approximately a drop of 4LSB. This means that all the digital converted values will contain an error of 4LSB. This means that after the ADC converts the input signal, the digital output will always be 4LSB less than it should be.

Figure 21. Effect of injection current



This demonstrates that the source impedance should be as small as possible to obtain maximum accuracy. With no negative injection current, no loss of accuracy is expected.

Positive injection current is introduced when $V_{IN} > V_{DD}$. Therefore current flows into the I/O pin. Positive injection current within the limit does not cause any loss of accuracy.

Minimizing Injection current

Check the application to verify if any digital or analog input voltages can be less than V_{SS} or V_{SSA}. In this case negative injection current will flow from the pins. Negative injection current will have greater affect on the accuracy, when a digital input is close to the analog input being converted.

It is recommended to connect a Schottky diode from V_{SSA} to the IO which can have the negative injection current.

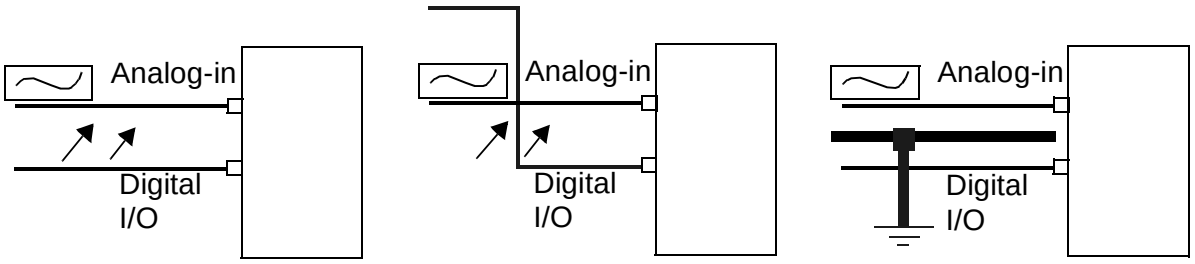
4.7 I/O PIN CROSS-TALK

Switching the I/Os may induce some noise in the analog input of the microcontroller. This is because of capacitive coupling between the I/Os. The cross-talk may be introduced by PCB tracks running close to each other or crossing over each other.

Within the microcontroller there can be non-negligible effect on I/Os because of switching etc. Internally switching digital signals and I/Os introduces high frequency noise. If high sink I/Os are switched, this may induce some voltage dips in the power supply because of the current surges.

A digital track crossing over an analog input track on the PCB may affect the analog signal.

Figure 22. Cross-talk between I/Os



Digital and analog signal passing close to each other

Digital and analog signal tracks crossing each other on different side of the PCB

Recommended Grounding between signals

Shielding the analog signal by placing ground tracks across it helps reduce noise produced by cross talk etc.

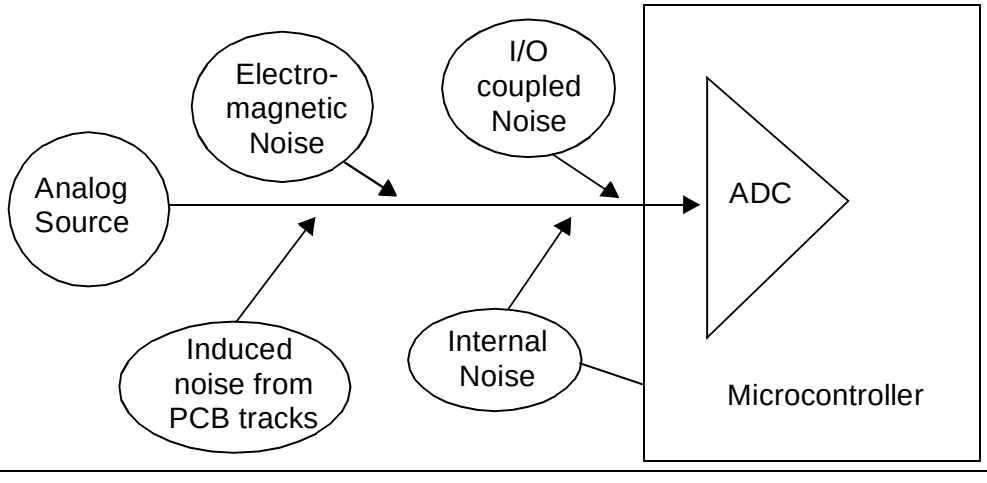
4.8 EMI-INDUCED NOISE

Electromagnetic emissions from neighboring circuits may introduce high frequency noise into an analog signal because the PCB tracks may act like an antenna.

You can reduce the emission noise by proper shielding and layout techniques. The possible sources of emissions must be physically separated from the receptors. You can separate them electrically by proper grounding and shielding.

You can minimize the reception noise by using filtering techniques so that high frequency noise is filtered.

Figure 23. EMI sources



Shielding

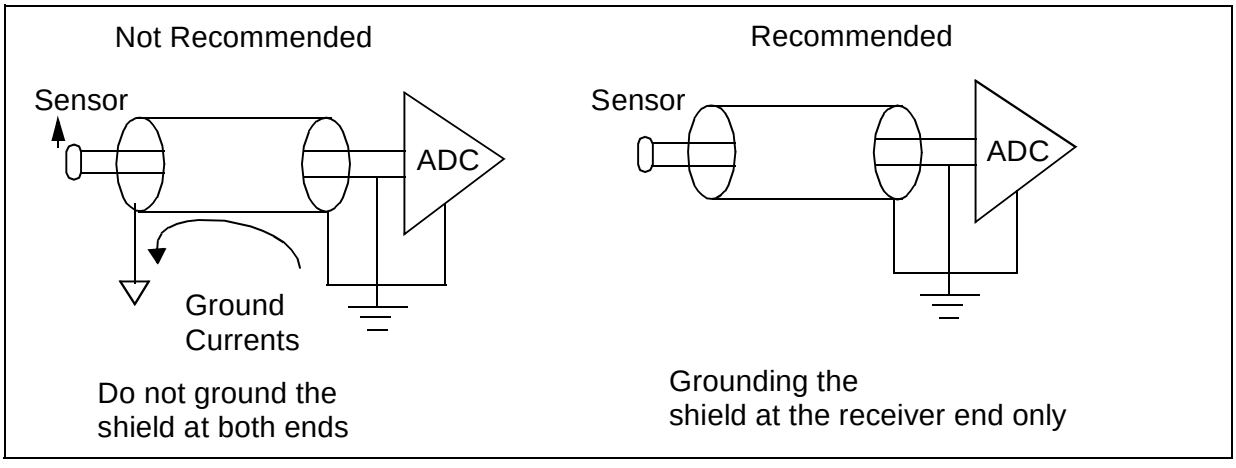
Placing ground tracks alongside sensitive analog signals provides shielding on the PCB. The other side of the two-layer PCB should also have a ground plane. This prevents interference and I/O cross-talk affecting the signal.

Signals coming from distant locations (like sensors etc) should be connected to the PCB using shielded cable. Care should be taken to minimize the length of the paths of these types of signal on the PCB.

The shield should not be used to carry the ground reference from the sensor or analog source to the microcontroller. A separate wire should be used as ground. The shield should be grounded at only one place near the receiver such as the analog ground of the microcontroller.

Grounding the shield at both the ends (source and receiver) may cause ground loops to be formed and making the current flow from the shield.

Figure 24. Shielding



If the current is flowing through the shield, it will act like an antenna and the purpose of shielding will be lost.

The shielding concept also applies to grounding the chassis of the application if it is metallic. This also helps to remove EMI and EMC interference. In this case the mains ‘Earth Ground’ is used to shield the chassis. Similarly DC ground can also be used for shielding in case ‘Earth Ground’ is not available.

5 DIFFERENT TYPES OF A/D CONVERTER ERRORS

Different error types are specified for A/D Converters. These errors are normally expressed as multiples of LSB for easy reference. The resolution in terms of voltage depends on the reference voltage. You can calculate the error in terms of voltage by multiplying the (*number of LSB*) with (*voltage corresponding to 1LSB*).

5.1 OFFSET ERROR

This is defined as the deviation between the first actual transition and the first ideal transition. The first transition is when the digital output of ADC changes from 0 to 1. In an ideal case we should get a digital output of 1, when the analog input is between 0.5 LSB to 1.5LSB. The first transition in an ideal case will be at 0.5 LSB. Offset error is represented as E_O.

Example 1:

In a 10-bit ADC, ideally 2.44mV (0.5 LSB = 0.5 * 4.88mV) input should generate a corresponding digital output of 1. But in practice the ADC may still show the reading as 0. If we get a digital output of 1 from an analog input of 10mV, then:

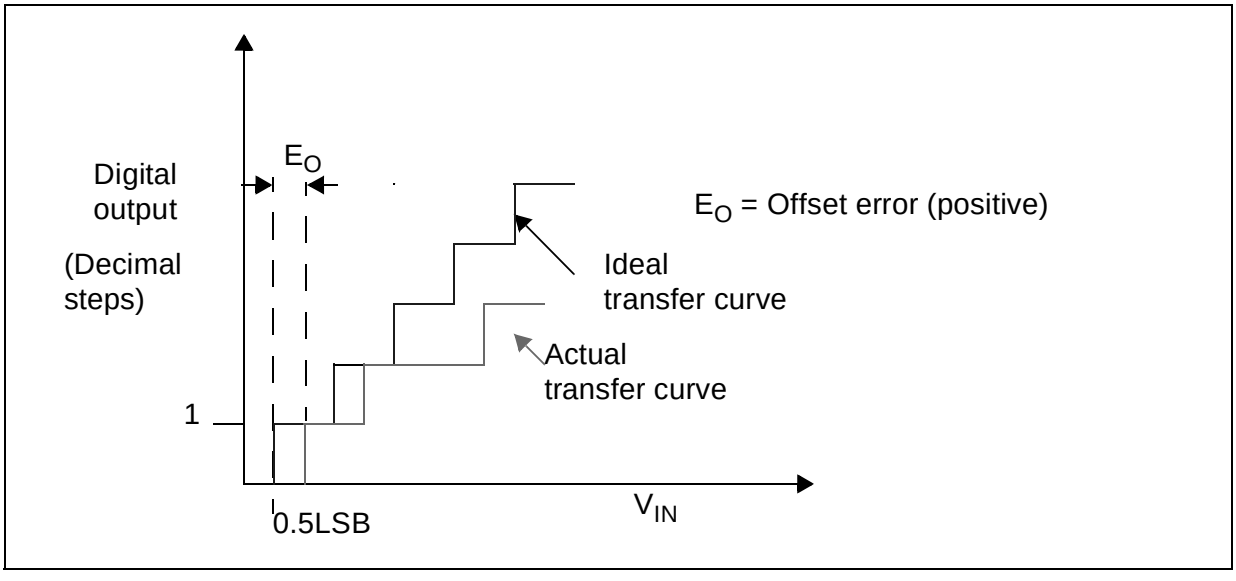
Offset error = Actual transition - Ideal transition

E_O = 10mV - 2.44mV = 7.56 mV

E_O = 7.56mV / 4.88 mV = 1.54 LSB

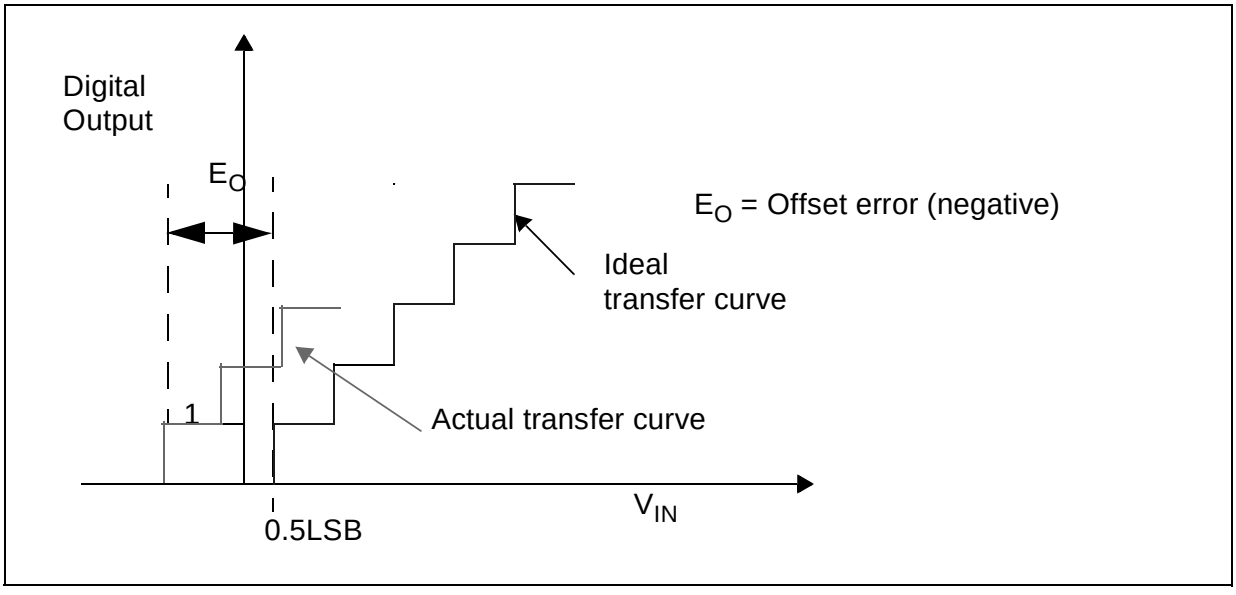
When an analog input voltage of greater than 0.5LSB generates the first transition, then the offset error will be positive.

Figure 25. Positive offset error representation



When the analog input voltage $V_{IN} = V_{SSA}$ and the ADC generates a non-zero digital output then the offset error will be negative. This will mean that theoretically (or by Extrapolation) a negative voltage will generate the first transition. As specified in the datasheet, any voltage less than V_{SSA} will cause the digital output to be 0.

Figure 26. Negative offset error representation



5.2 GAIN ERROR

Gain Error is defined as the deviation between the last actual transition and the last ideal transition. Gain error is represented as E_G.

The last actual transition means the transition from 3FE to 3FF for a 10-bit ADC. In an ideal case we should get a transition from 3FE to 3FF from a 10-bit ADC, when the analog input is equal to V_{AREF}-0.5LSB. So for V_{AREF}= 5V, last ideal transition shall be at 4997.12 mV.

If ADC provides the 3FFh reading for $V_{IN} < V_{AREF}$-0.5LSB, then we have a negative gain error.

Example

For a 10-bit ADC and V_{AREF} =5v

If V_{IN} = 4990 mV generates transition from 3FE to 3FF then,

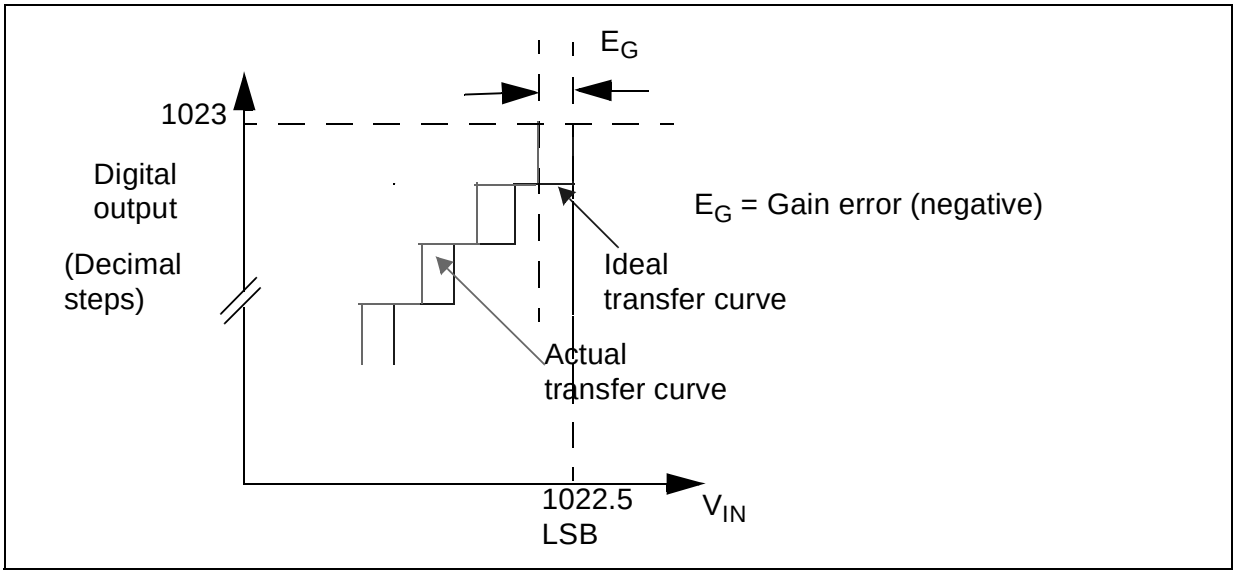
Gain error E_G = Last actual transition - ideal transition

E_G = 4990mV - 4997.12 mV

E_G = - 7.12 mV

E_G = (-7.12mV / 4.88mV) LSB = -1.45 LSB

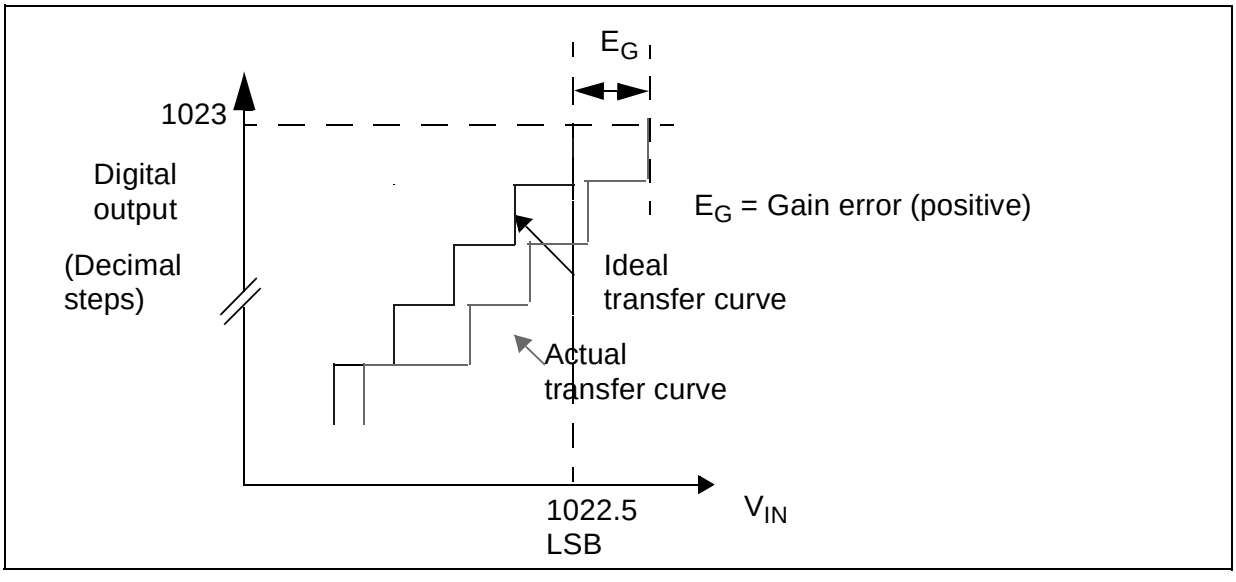
Figure 27. Negative Gain error representation



If we do not get full scale reading (3FF for a 10-bit ADC) for V_{IN} equal to V_{AREF} the gain error will be positive.

This means theoretically (or by extrapolation), a voltage greater than V_{AREF} will cause the last transition.

Figure 28. Positive Gain error representation



5.3 DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is defined as the maximum deviation between actual steps and the ideal steps. Here ‘ideal’ is not for the ideal transfer curve but for the resolution of the ADC. DLE is represented as $E_{D.}$

DLE = Actual step width - 1LSB

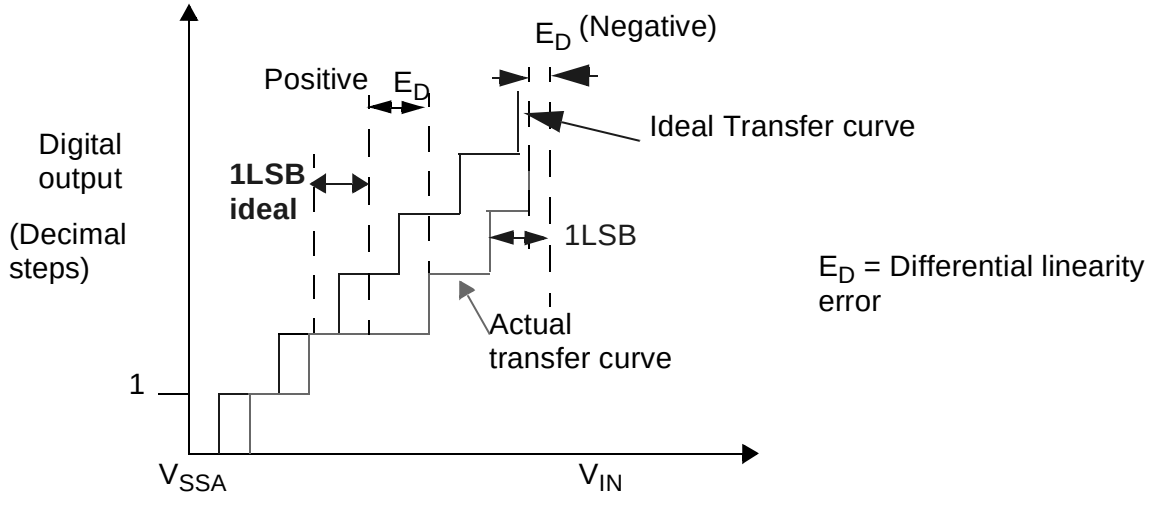
Ideally analog input voltage change of 1LSB should cause a change in the digital code. If an analog input voltage greater than 1LSB is required for a change in digital code, then the ADC has the differential linearity error. DLE thus corresponds to additional maximum voltage that is required to change one digital code to the next digital code.

DLE is also known as DNL, Differential Non-Linearity error.

Example:

For a range of analog input we should get the same digital output. Ideally the step width should be 1LSB. Suppose we get same digital output for a range of analog input voltage 1V to 1.010V then the step width will be 1.010V-1V = 10mV. DLE is thus the voltage difference between the higher (1.010V) and lower analog voltage (1V) subtracted by the voltage corresponding to 1LSB.

Figure 29. Differential Error representation



Note: In this example the actual curve is shown to have an offset error from ideal curve.

With a 10-bit ADC and V_{AREF} = 5V, an analog input of 1V can provide results varying from CBh to CDh.

Similarly for 1.010V, i.e. 206d = CEh, the results may vary from CDh to CFh.

So, total voltage range corresponding to the step CDh is 1.010 V - 1V

= 10mV

E_D= 10mV - 4.88 mV

E_D= 5.12 mV

E_D= (5.12mV/4.88mV) LSB

E_D= 1.04 LSB

Here we assume that any voltage greater than 1.010 V will not result in the digital code equal to CDh.

When the step width is less than 1LSB, DLE will be negative.

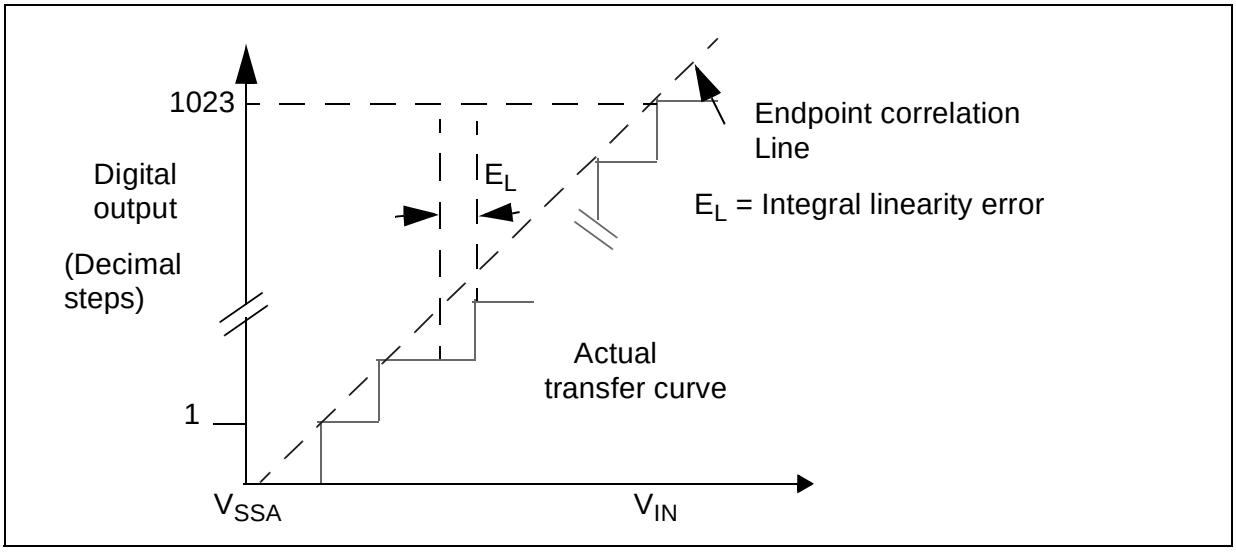
5.4 INTEGRAL LINEARITY ERROR

Integral Linearity Error is maximum deviation between any actual transition and the endpoint correlation line. ILE is represented as E_L.

The endpoint correlation line can be defined as the line on the A/D transfer curve that connects the first actual transition and last actual transition. ILE is the deviation from this line for each transition. The endpoint correlation line thus corresponds to the actual transfer curve and has no relation to the ideal transfer curve.

ILE is also known as INL, Integral Non linearity Error. ILE is the integral of DLE over the full range.

Figure 30. Integral error representation



Example:

If we get the first transition from 0 to 1 at 10mV (offset error) and we get the last transition (3FE to 3FF) at 4.990V (gain error) then the line on transfer curve connecting the actual digital code 1 and the actual digital code 3FF will be the endpoint correlation line.

5.5 TOTAL UNADJUSTED ERROR

TUE is defined as the maximum deviation between the actual and the ideal transfer curves. It is a parameter which specifies the total errors that can occur causing maximum deviation between the ideal digital output and actual digital output. It is the maximum deviation recorded between ideal expected value and actual value obtained from the ADC for any input voltage. TUE is represented as E_T.

TUE is not the sum of E_O, E_G, E_L, E_D. The offset error affects the digital result at lower voltages whereas the gain error affects the digital output for higher voltages.

Example:

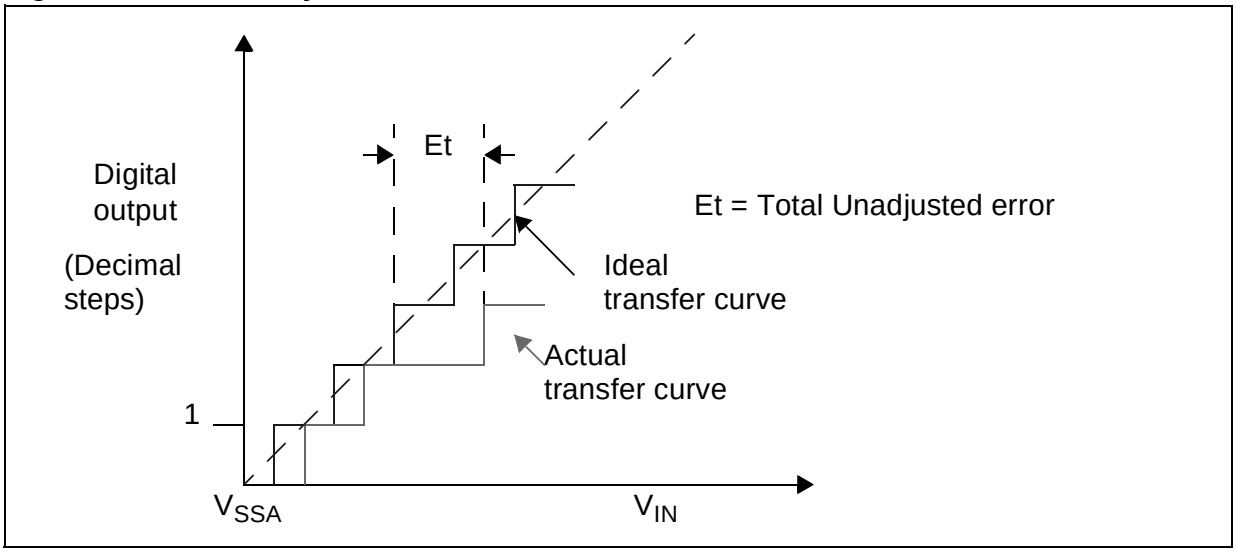
With a 10-bit ADC and V_{AREF}=5V and 1V input, the ideal result is CCh. But if on conversion we get the result CEh, this deviation may be because of offset, DLE and INL errors occurring simultaneously.

TUE = absolute (actual value - ideal case value).

= CEh - CCh

= 2h

Figure 31. Total unadjusted error



Using error parameters

1. The TUE is NOT the sum of all the errors E_O, E_G, E_L, E_D. It is the maximum error which can occur between ideal and expected digital values. It can be the effect of either a single error or two errors occuring simultaneously.
2. As ILE is the integral of DLE, it can be considered as indicative of maximum error. Do not add both DLE and ILE together to calculate the maximum error which can occur at any digital step.
3. Integral Linearity Error is the maximum deviation between any actual transition and the end point correlation line. So it represents the linearity of the ADC.
4. ILE and DLE are dependent on the ADC design. It is difficult to calibrate them.
5. The ILE and DLE can be minimized by doing multiple conversions and then averaging.
6. Offset and Gain errors can be easily cancelled / compensated using software techniques.
7. The maximum values for errors specified in datasheet are the worst error values measured in the laboratory test environment for full voltage range.
8. As already mentioned, all the ADCs provide the digital converted output in ratio with the reference voltage. To convert analog voltage accurately, the ADC needs to have an accurate V_{AREF} otherwise the digital output received may not be the correct value.

Example:

In the widely used 7805 voltage regulator, the datasheet (L78M05C) specifies Vo min.= 4.8V and Vomax = 5.2v. This variation is 0.2V from required 5V. Hence a variation of 200mv. With an analog input of 1V and with V_{AREF}=5V, the expected digital output should be (1/5)*1023 = 204d = CCh

But if V_{AREF} = 4.8v, the digital output = (1/4.8)*1023 = D5h

So the power supply variation has caused a change of D5-CC = 9.

In this case to measure the true input voltage, all the relevant parameters must be verified and crosschecked. For example, if a precision voltage regulator such as the L78M05AB is used, it provides Io=350mA and Vomin=4.9V, Vo max = 5.1V.

6 PCB LAYOUT RECOMMENDATIONS

For best ADC conversion accuracy, you should follow these PCB layout guidelines.

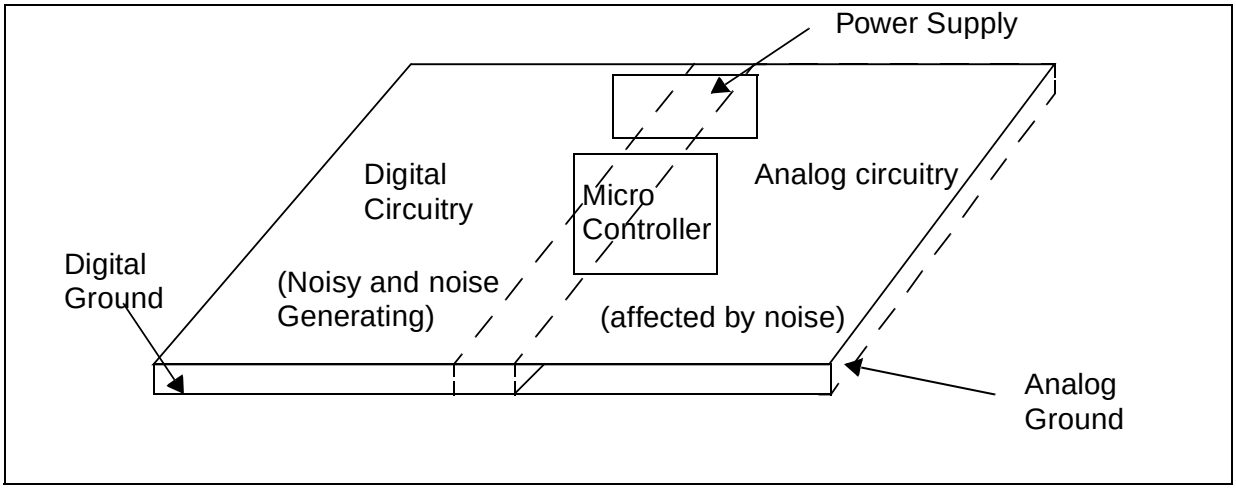
1. Separate the analog and digital layouts

It is recommended to separate the analog and digital circuitry on the PCB. They should be placed in different parts of the PCB. This also avoids tracks crossing each other. The tracks carrying digital signals may introduce high frequency noise in analog signals because of coupling. The digital signals produce high frequency noise because of fast switching.

Coupling of the capacitive nature is formed because of the metal connections (tracks) separated by the dielectric provided by the PCB base (glass, ceramic or plastic).

It is recommended to use different planes for analog and digital ground. If there is a lot of analog circuitry then an analog ground plane is recommended. Analog ground must be placed below the analog circuitry.

Figure 32. Separating the analog and digital layouts



2. Separate power supplies for analog and digital circuits

It is desirable to have separate analog and digital power supplies in cases where there is a lot of analog and digital circuits external to the microcontroller. Depending on the microcontroller package, different analog and digital power supply and ground pins are available. Internally V_{AREF} and V_{DD} pins are not connected except for protection through Schottky diodes. These pins can be powered from separate power supplies.

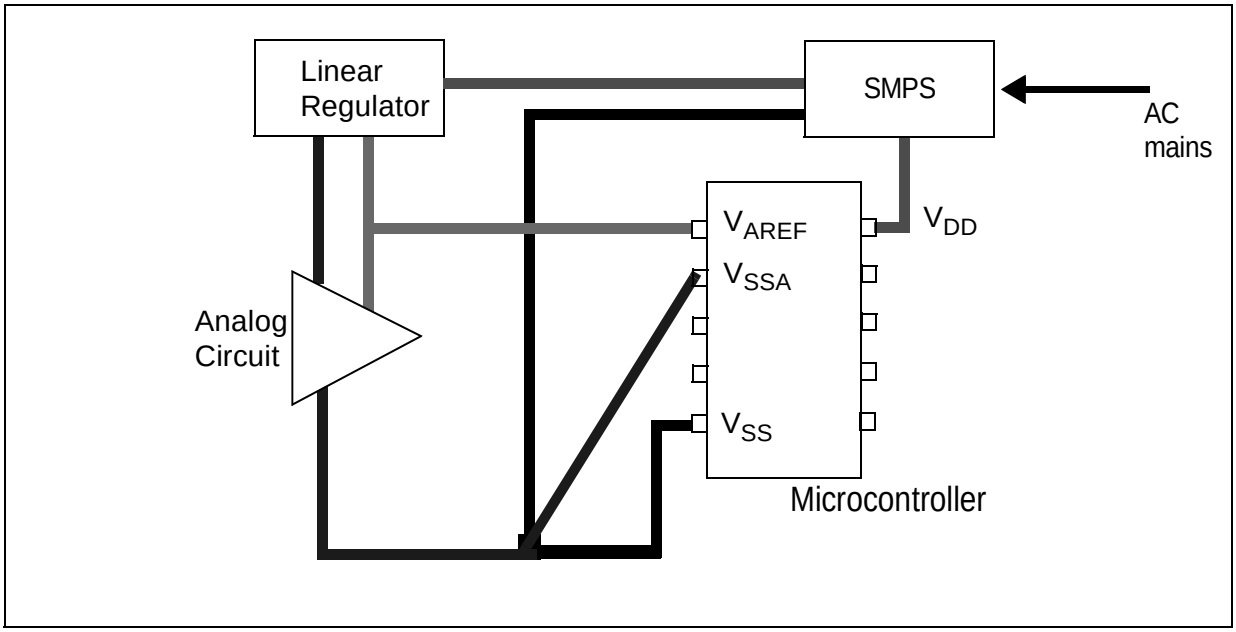
In low pin-count packages, separate analog and digital supply and ground pins may not be available. In this case they are internally shorted. So V_{DDA} and V_{DD} are internally connected in packages which have fewer pins.

As mentioned earlier, if you use a switching type power supply for the digital circuitry, you should use a separate linear supply for the analog circuit.

Also, if you expect a lot of noise on the DC power supply due to I/O switching etc, a separate supply for the analog section is preferable.

Important: Separate Analog and Digital supplies are recommended only if the microcontroller has V_{AREF} pins for the ADC reference voltage (instead of V_{DDA}). If the microcontroller does not have V_{AREF} pins, then the difference between V_{DDA} and V_{DD} should not be more than the difference specified in the datasheet (check the Absolute maximum ratings). Generally the difference between V_{DDA} and V_{DD} is specified as 50mV, hence separate supplies are not recommended.

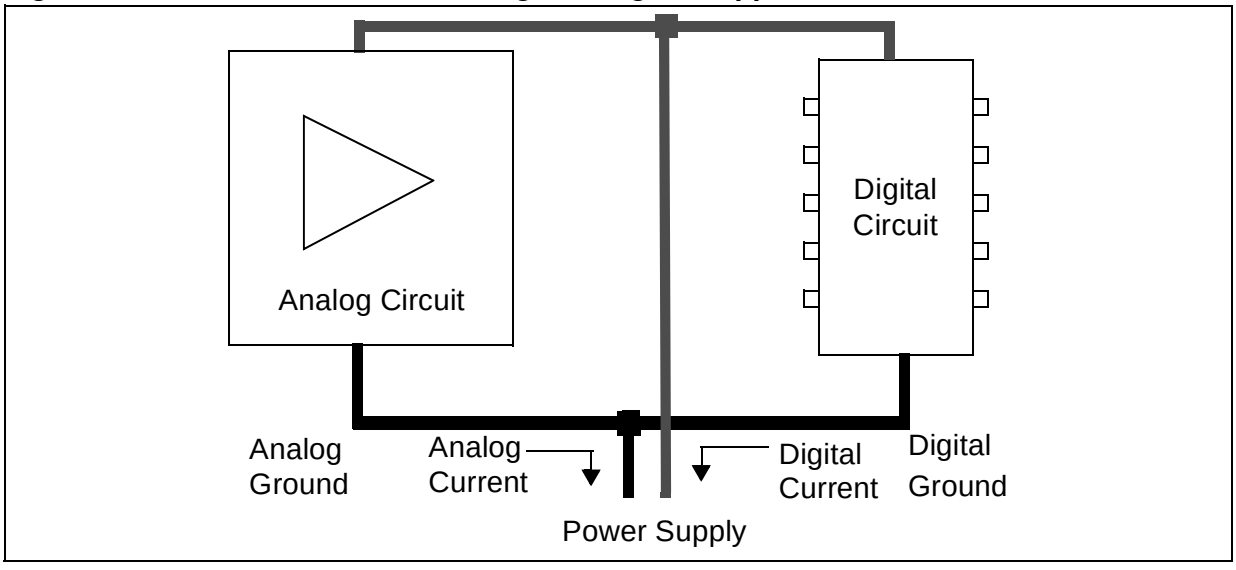
Figure 33. Separating the analog and digital supplies



3. Connect analog and digital power supplies in a star network

It is recommended to connect the analog and digital grounds in star network. This means that you must connect the analog and digital grounds only at one point. This avoids noise being introduced in the analog power supply section, because of digital signal switching and also avoids current surges affecting the analog section.

Figure 34. Star connection for analog and digital supplies



4. Using separate PCB layers for supply and ground

Two-Layer PCBs

For two layer PCBs it is recommended to provide a maximum area for the ground. The power supply (V_{DD}, V_{DDA}) should run through thick tracks. The ground area between two layers can be shorted together via multiple connections in the overlap region if they are same ground signals. The unused area of the PCB can be filled with the ground area.

The other convention is to fill the unused area of PCB on one layer with positive supply (V_{DD}) and unused area on other plane for Ground. The advantage is reduced inductance for power and ground signals. Maximum ground area on PCB provides a good shielding effect and reduces the electromagnetic induction susceptibility of the circuit.

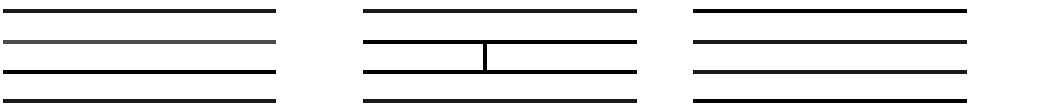
Multilayer PCBs

Wherever possible, try to use multilayered PCBs and use separate layers on the PCB for power and ground. The V_{DD}, V_{SS} pins of the various ICs can be directly connected to the

power planes thus reducing the tracks needed to connect the supply and ground. Longer tracks will have a high inductive effect. The analog ground can be connected at one point to this ground plane, this should be near to the power supply.

A full ground plane provides a good shielding effect and reduces the Electromagnetic induction susceptibility of the circuit.

Figure 35. Multlayer PCB configurations



1. Top layer and bottom layer for SMD components
2. Second layer as power plane
3. Third layer ground layer

1. Top layer and bottom layer for SMD components
2. Second layer as digital ground plane.
3. Third layer as analog ground

Digital and analog ground connected at one point near power supply

1. Top layer and bottom layer for components and ground plane (Analog and digital)
2. Second and third layer for tracks

There will be tracks passing vertically through the ground and supply planes.
SMD: Surface mounted devices

The disadvantage of multilayer PCBs is the higher cost of manufacturing and the fact that they are more difficult to debug.

Single-layer PCBs

Single-layer PCBs are used to save cost. They can be used only in simple applications when the number of connections is very limited. It is recommended to fill the unused area with ground. Jumpers can be used to connect different parts of the PCB.

5. Component placement and routing

Place the components and route the signal traces on the PCB to shield the analog inputs. Analog signal paths should run over the analog ground plane.

Components like resistors and capacitors must be placed with their leads very short. Surface mounted devices (SMD), resistors and capacitors can be used. SMD capacitors can be placed close to the microcontroller for decoupling.

The tracks for the power should be wide, as the series resistance of these tracks will cause the voltage drop if the tracks are narrow. Narrow power tracks will have non-negligible finite resistance. High load current will cause some voltage drop across these tracks.

Quartz crystals must be surrounded by ground tracks/plane. The other side of the two layer PCB below the crystal should preferably be covered by the ground plane. Most crystals have a metallic body that should be grounded. The crystal should be placed close to the microcontroller. Surface mounted crystals are available and can be used.

6. Software considerations

Do not toggle digital outputs on the same I/O port as the A/D input being converted. This will introduce switching noise into the analog inputs.

Toggling high sink I/Os may introduce high frequency noise in the power supply, this may affect the conversion results.

7 HOW POWER SAVING MODES AFFECT THE ADC

Wait mode

ADC can be used when the microcontroller is in Wait mode. You can take advantage of the reduced internal noise in the microcontroller to improve ADC conversion results.

Halt mode

Entering Halt mode will disable the ADC, irrespective of whether the ADON bit is set or not. This is because executing the HALT instruction shuts down the ADC.

Exiting from Halt mode requires some stabilization time before ADC conversion should be started. This conversion time is very small. Please refer to the datasheets.

Table 3. Summary Table

ST7 Modes	Oscillator/CPU/Peripheral Status					Effect on ADC
	Oscillator	CPU	MCCSR-OIE Bit	MCCSR-SMS Bit	ADC	
Run	On	On	X	Reset	On	Use the ADC as mentioned in datasheet.
Slow	On	On	X	Set	On	Take care that f_{ADC} does not fall below f_{ADC} min.
Wait	On	Off	X	Reset	On	If ADC has exit-from Wait capability, this mode is recommended.
Slow-Wait	On	Off	X	Set	On	If ADC has exit-from Wait capability, this mode is recommended.

ST7 Modes	Oscillator/CPU/Peripheral Status					Effect on ADC
	Oscil-lator	CPU	MCCSR-OIE Bit	MCCSR-SMS Bit	ADC	
Active-Halt	On	Off	Set	X	Off	Exit from Halt mode requires stabilization time before conversion starts.
Halt	Off	Off	Reset	X	Off	Exit from Halt mode requires stabilization time before conversion starts.

Note: Reset=0, Set=1

Rules and Recommendations for using the ADC in Power Saving Mode

Different power saving modes for ST7 can be selected depending on power saving requirements of the application, the following rules and recommendations should be applied when using the ADC.

1. When switching to Slow mode from Run mode care should be taken that the f_{ADC} should not fall below the f_{ADC} minimum specified. Otherwise the conversion results are not guaranteed. Similarly when application switches to Slow-wait mode after recovering from Wait mode, f_{ADC} shall be in specified range.
2. Similarly, when switching back from Slow mode to Run mode (or Slow-Wait to Wait mode), if ADC conversion is intended, the f_{ADC} should not increase above the f_{ADC} max specified in the data sheet. Conversion results are not guaranteed outside the operating frequency range of ADC.
3. For ADCs with Wait mode wake up capability, it is recommended to use Wait mode for ADC conversion. This will improve results because the CPU is off in Wait mode, and this reduces the noise generated by digital switching.
4. If the ADC does not have an interrupt capability for waking up from Wait mode, then any other interrupt (for example a Timer interrupt) can be used to take advantage of the reduced internal noise in Wait mode. Before entering Wait mode, ADC conversion can be started, and the results can be read after exit from Wait mode.
5. If ADC is off/disabled, leakage current can flow into the ADC if the analog channels are connected to the analog input pins. This is because of finite impedance of IO pins.
6. If the ADC is not used in the application, and you want to save power consumption, then you must disable the ADC through software.
7. When entering a power saving mode, disable the ADC if you do not need it to perform conversion while the microcontroller is in power saving mode. If the ADC is not disabled before

entering power saving mode (except Halt or Active-Halt), the internal analog circuit will consume some current.

8 RELATED DOCUMENTATION

You can refer to the following application notes for additional useful information:

AN435: Designing with microcontrollers in noisy environment

AN898: EMC General Information

AN901: EMC Guidelines for microcontroller - based applications

AN1015: Software techniques for improving microcontroller EMC performance

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