Data Sheet

32

V850E2/FL4-H

32-bit Single-Chip Microcontroller

µPD70F3564

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R01DS0144ED0100
2013-05-24

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Notes for CMOS Devices

(1) Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All text and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Table of contents

Chapter 1 Overview

1.1 Naming

1.1.1 Alternative function pins

Peripheral	Prefix	Function name	Suffix
Short-cut of macro name	Consecutive number for same peripheral module[a]	Peripheral Macro pin naming	Consecutive number for same pin names[a]

a) This is an option that can be omitted if meaning is obvious

Example:

– TAUB0I0, TAUB1I5
– URTE0TX, URTE0RX, URTE1TX, URTE1RX
– CSIG0SO, CSIG0SI, CSIG0SC, CSIG0RY

1.1.2 Power supply pins

Function	Prefix	Kind of supply	Suffix
Symbol	Consecutive number for different functions[a]	VDD or VSS	Consecutive number for different pins with same meaning[a]

a) This is an option that can be omitted if meaning is obvious

Example:

– E0VDDn, REG0VSS

Table 1-1 Selection for Functions

Function	Explanation
C	Core supply
REG	Internal regulator supply
OSC	Oscillator supply
F	Flash module supply
E	Standard buffer supply (mainly 5V or up to 40Mhz)
B	Standard buffer supply (mainly 3.3V or beyond 40Mhz)
A	Analog module supply (e.g. ADC)

If not mentioned otherwise this document neglects suffixes for power supply pins with same functions that can be treated as equal.

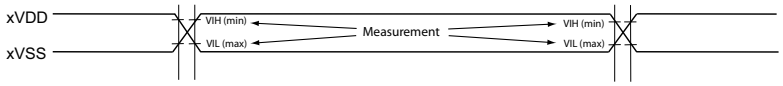
1.2 Pin Groups

Symbol	Pin group supplied by	Related pins / ports
PgE0	E0VDD / E0VSS	JP0, P0, _RESET, FLMD0, WAKE, PWDG, VCPC0IN, VCPC1IN
PgE1	E1VDD / E1VSS	P1, P2, P3, P4
PgB0	B0VDD / B0VSS	P21, P24, P25, P27
PgOSC	OSCVDD / OSCVSS	X1, X2, XT1, XT2
PgA0	A0VDD / A0VSS	P10, P11, ADCA0Im
PgA1	A1VDD / A1VSS	P12, P13

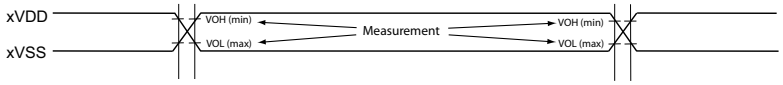
1.3 General measurement conditions

1.3.1 AC characteristic measurement condition

AC test input waveform

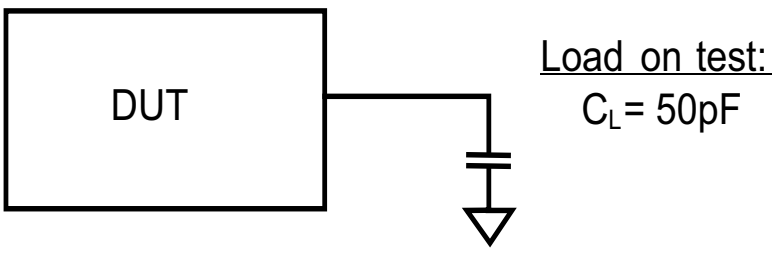


AC test output waveform



Standard AC test condition is 70%/30% of the applied IO supply voltage (XmVDD) if not otherwise stated in the according AC timing specification of an interface.

AC Test Condition: Ext. Capacitive Load



Chapter 2 Absolute maximum ratings

2.1 Supply voltages

Table 2-1 VDD Data

Parameter	Symbol	Condition	Ratings	Unit
System	CVDD		-0.5 ~ 1.6	V
System	FVDD		-0.5 ~ 6.0	V
	OSCVDD		-0.5 ~ 6.0	V
	REG0VDD		-0.5 ~ 6.0	V
	REG1VDD		-0.5 ~ 6.0	V
	REG2VDD		-	V
	REG3VDD		-	V
Ports	E0VDD		-0.5 ~ 6.0	V
	E1VDD		-0.5 ~ 6.0	V
Port	B0VDD		-0.5 ~ 6.0	V
ADCA0	A0VREFP		-0.3 ~ A0VDD+0.3 -0.3~6.0	V
ADCA0	A0VDD		-0.5 ~ 6.0	V
ADCA1	A1VDD		-0.5 ~ 6.0	V
	A1VREFP		-0.3 ~ A1VDD+0.3 -0.3~6.0	V

Table 2-2 VSS Data

Parameter	Symbol	Condition	Ratings	Unit
System	CVSS		-0.5 ~0.5	V
System	FVSS		-0.5 ~0.5	V
	OSCVSS		-0.5 ~0.5	V
	REG0VSS		-0.5 ~0.5	V
	REG1VSS		-0.5 ~0.5	V
	REG2VSS		-	V
	REG3VSS		-	V
Ports	E0VSS		-0.5 ~0.5	V
	E1VSS		-0.5 ~0.5	V
	B0VSS		-0.5 ~0.5	V
ADC0	A0VSS		-0.5 ~0.5	V
	A0VREFM		-0.3 ~ A0VDD+0.3 -0.3~6.0	V
ADC1	A1VSS		-0.5 ~0.5	V
	A1VREFM		-0.3 ~ A1VDD+0.3 -0.3~6.0	V

2.2 Port voltages

Table 2-3 Port Input voltage

Parameter	Pin Group	Symbol[a]	Condition	Ratings	Unit
Input voltage[b]	PgE0	V_{I0}	E0VDD≤5.5	-0.5 ~ E0VDD+0.5	V
	PgE1	V_{I1}	E1VDD≤5.5	-0.5 ~ E1VDD+0.5	V
	PgB0	V_{I2}	B0VDD≤5.5	-0.5 ~ B0VDD+0.5	V
	PgOSC	V_{I5}	OSCVDD≤5.5	-0.5 ~ OSCVDD+0.5	V
	PgA0	V_{I3}		A0VDD+0.3	V
	PgA1	V_{I4}		A1VDD+0.3	V

a) The symbols reflect all supplies within the device series. Therefore not every symbol is available for each product.

b) The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

2.3 Port current

Table 2-4 High level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
High level output current	PgE0	IOH	1 pin of PgE0	-10	mA
			Power supply of PgE0	-50	
	PgE1		1 pin of PgE1	-10	
			Power supply of PgE1	-150	
	PgA0		1 pin of PgA0	-10	
			Power supply of PgA0	-25	
High level output current	PgA1	IOH	1 pin of PgA1	-10	mA
			Power supply of PgA1	-25	
High level output current	PgB0	IOH	1 pin of PgB0	-10	mA
			Power supply of PgB0	-200	

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

Table 2-5 Low level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
Low level output current	PgE0	IOL	1 pin of PgE0	10	mA
			Power supply of PgE0	50	
	PgE1		1 pin of PgE1	10	
			Power supply of PgE1	150	
	PgA0		1 pin of PgA0	10	
			Power supply of PgA0	25	
Low level output current	PgA1	IOL	1 pin of PgA1	10	mA
			Power supply of PgA1	25	
Low level output current	PgB0	IOL	1 pin of PgB0	10	mA
			Power supply of PgB0	150	

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

2.4 Capacitance

Parameter	Symbol	Condition	Max. spec	Unit
Input capacitance	C_I	f = 1 MHz 0V for non measurement pins	15	pF
Input/Output capacitance	C_{IO}		15	pF
Output capacitance	C_O		15	pF

2.5 Thermal characteristics

Table 2-6 Thermal characteristics

Parameter	Symbol	Condition	Ratings	Unit
Storage temperature	T_{STG}		-65 ~150	°C
Operating ambient temperature	T_a	(A) grade products	-40 ~85	
		(A1) grade products	-40 ~110	
Junction temperature	T_j		-40 ~150	

This section specifies the absolute maximum limitation of operating and storage temperature.

The device's functions are not guaranteed outside of the specified maximum temperature ratings.

Chapter 3 Power supply specification

3.1 Requirements for external power supply connections

The user has to ensure a low resistive connection of all VSS pins on the PCB. This specification denotes ground supply pins as:

- VSS = OSCVSS = REGnVSS = EnVSS = BnVSS = AnVSS = AnVREM = CVSS = 0V

in the further text.

With

- EnVSS = E0VSS = E1VSS
- BnVSS = B0VSS
- REGnVSS = REG0VSS = REG1VSS
- AnVSS = A0VSS = A1VSSAnVREFM = A0VREFM = A1VREFM

The user has to ensure a low resistive connection of all VDD pins to the related power supply. This specification denotes power supply pins as:

- EnVDD, BnVDD, FVDD, REGnVDD, OSCVDDCVDD, AnVDD and AnVREFP.

in the further text.

With

- EnVDD = E0VDD = E1VDD
- BnVDD = B0VDD
- REGnVDD = REG0VDD = REG1VDD.
- AnVDD = A0VDD = A1VDD
- AnVREFP = A0VREFP = A1VREFP
- I/OVDD = AnVDD, EnVDD, B0VDD, FVDD, OSCVDD

3.2 Power area definitions

The device consists of the following power areas:

- AWO (Always On area)
- ISO0 (Isolated area 0)
- ISO1 (Isolated area 1)

The table below lists the related core and port voltage supply of each power area:

Table 3-1 Power areas supply voltages

Power Area	Supply voltage	Related pins
AWO	Core supply	REG0VDD, REG0VSS, REG0C
	Port Supply	E0VDD, E0VSS
	Other	OSCVDD, OSCVSS FVDD0
ISO0	Core supply	REG1VDD, REG1VSS CVDD, CVSS
	Port Supply	E1VDD, E1VSS
	Other	A0VREFP, A0VREFM A0VDD, A0VSS
ISO1	Core supply	REG1VDD, REG1VSS CVDD, CVSS
	Port Supply	B0VDD, B0VSS
	Other	A1VDD, A1VSS A1VREFP, A1VREFM

3.3 Power supply groups

For each of the following power supply groups the same voltage must by supplied:

Table 3-2 Power supply groups

Power supply group	Related pins
#1	REG0VDD, REG1VDD, FVDD, OSCVDD, E0VDD, E1VDD
#2	B0VDD
#3	-
#4	CVDD
#5	A0VDD, A0VREFP
#6	A1VDD, A1VREFP
#7	All VSS

3.4 Supply voltages

Table 3-3 VDD Data

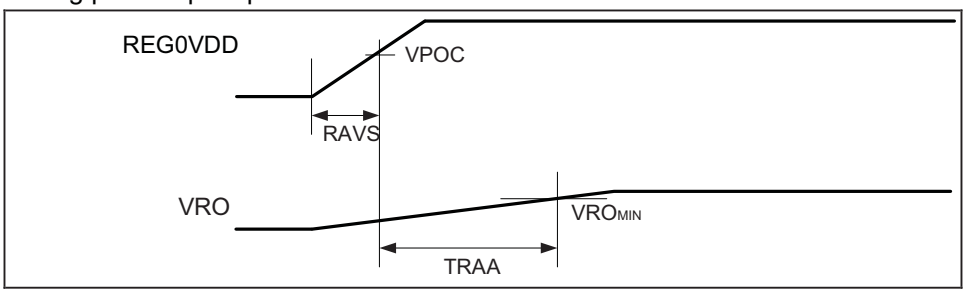
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
System supply voltage	FVDD		VPOC	-	5.5	V
System supply voltage	OSCVDD		VPOC	-	5.5	V
System supply voltage	REG0VDD	REG0VDD = REG1VDD	VPOC	-	5.5	V
System supply voltage	REG1VDD		VPOC	-	5.5	V
System supply voltage	REG2VDD		-	-	-	V
System supply voltage	REG3VDD		-	-	-	V
System supply voltage	CVDD		1.1	-	1.3	V
System supply voltage slopes	AIVS	REG1VDD = 3.0V to 5.5V	-	-	5.6	V/ms
Port supply voltages	E0VDD		VPOC	-	5.5	V
Port supply voltages	E1VDD		VPOC	-	5.5	V
Port supply voltages	B0VDD	B0VDD ≤ power supply group #1 voltages	VPOC	-	5.5	V
ADC supply voltages	A0VDD	12bit resolution	4.5	-	5.5	V
ADC supply voltages	A0VDD	10bit resolution	VPOC	-	5.5	V
ADC supply voltages	A0VREFP		A0VDD	-	A0VDD	V
ADC supply voltages	A1VDD	12bit resolution	4.5	-	5.5	V
ADC supply voltages		10bit resolution	VPOC	-	5.5	V
ADC supply voltages	A1VREFP	A1VREFP-A1VREFM > A1VDD/2	A1VDD	-	A1VDD	V

3.4.1 AWO Regulator characteristics

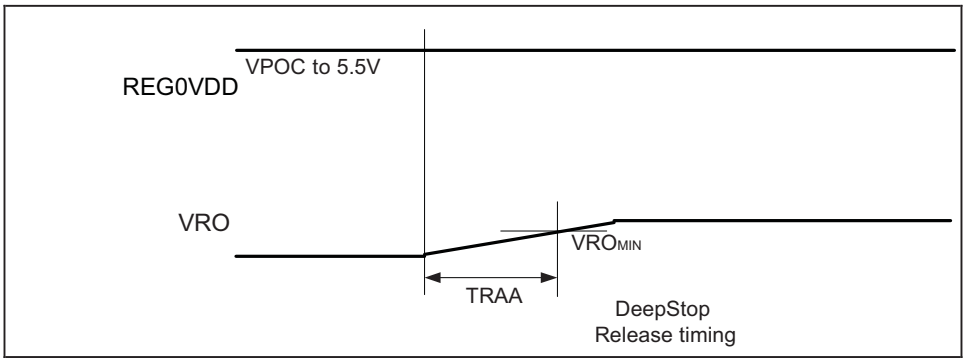
Table 3-4 AWO Regulator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Regulator Output voltage	VRO		1.1	1.2	1.3	V
System supply voltage slope	RAVS	0V to 3.0V	-	-	1800	V/ms
Capacitance on REG0C	REG0C		3.29	4.7	6.11	µF
Output voltage stabilization time	TRAA	After REG0VDD reaches 3.0V	-	-	1	ms
		After DeepStop mode	-	-	0.5	ms

During power-up sequence



After DeepStop mode



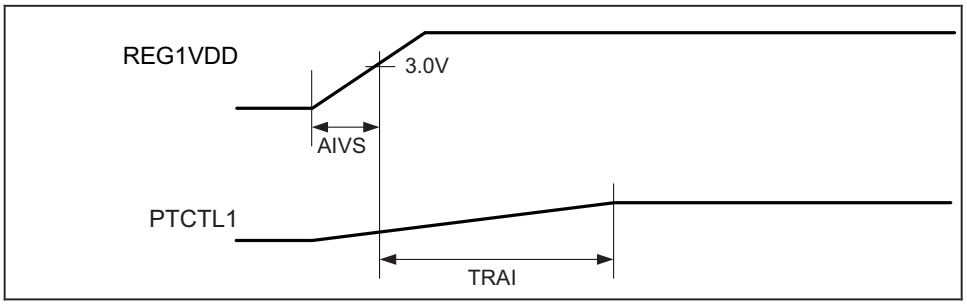
3.4.2 Amplifier characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
System supply voltage	REG1VDD		VPOC		5.5	V
Capacitance on CVDD	CVDDC	For each CVDD[a]	3.29	4.7	6.11	µF
Voltage slope	AIVS	3.0V to 5.5V	-	-	5.6	V/ms

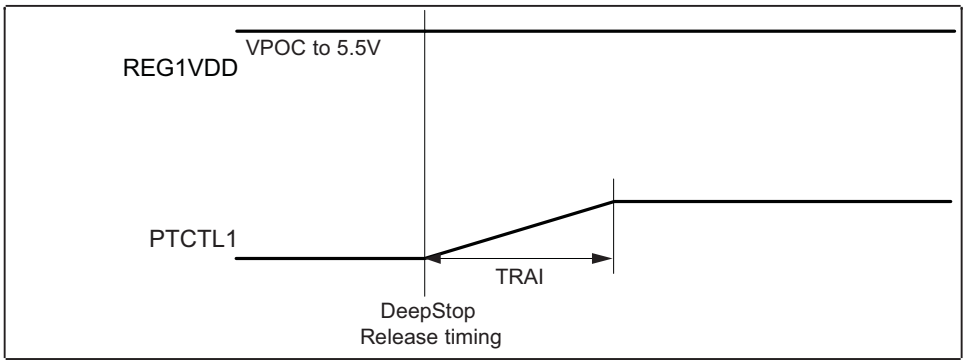
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
PTCTL1 stabilization time	TRAI	After REG1VDD reaches 3.0V	-	-	1	ms
		After DeepStop mode	-	-	0.5	ms
PTCTL1 output current	IPTCTL		-	-	1.55	mA

a) Required when using an external power transistor such as 2SD1584 (base connected to PTCTL1)

During power-up sequence



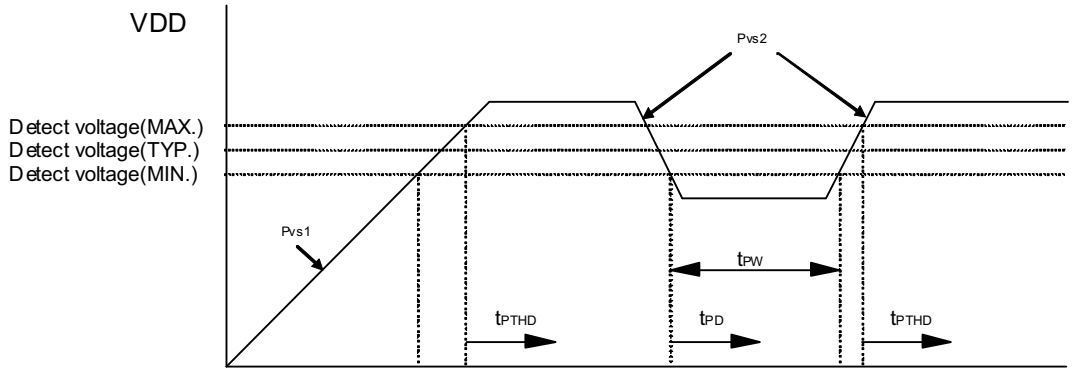
After DeepStop mode



3.4.3 POC characteristics

Table 3-5 POC characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VPOC		2.8	2.9	3.0	V
Voltage slope 1	PVS1		0.18	-	1800	V/ms
Voltage slope 2	PVS2		0.0018	-	1800	V/ms
Response time 1	tPTHD	From detect voltage to release of reset signal. Voltage slope = PVS1, PVS2	-	-	2	ms
Response time 2	tPD	From detect voltage to occurence of reset signal Voltage slope = PVS2	-	-	2	ms
VDD minimum width	tPW		0.2	-	-	ms



3.4.4 Voltage Comparator characteristics

Table 3-6 VCMP characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Input voltage range of VCPCnIN	VICMP		REG0VSS	-	REG0VDD	V

Note VDD: REG0VDD

3.5 Power-up/-down sequence of external supply voltages

3.5.1 External FLMDn Resistors

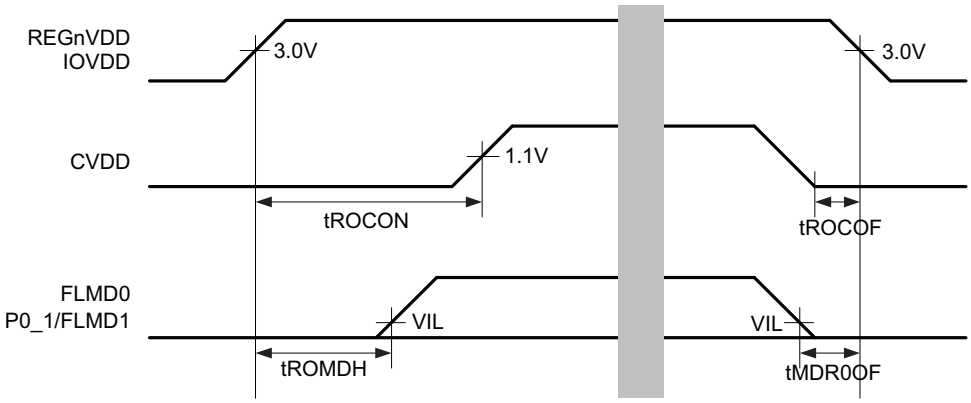
Valid for all conditions described in the following

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 external pull-down resistor	R1		82	-	-	kΩ
FLMD1 external pull-down resistor	R2		-	10	-	kΩ

3.5.2 Condition 1

RESET, WAKE and PTCTL1 are not used
Normal operating mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (rise)	tR0CON		1	-	10	ms
REG0VDD, IOVDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		2	-	-	ms
FLMD0,1 (≤VIL) to REG0VDD, IOVDD (fall)	tMDR0OF		0	-	-	ms
CVDD (0V) to REG0VDD, IOVDD (fall)	tCR0OF		0	-	-	ms



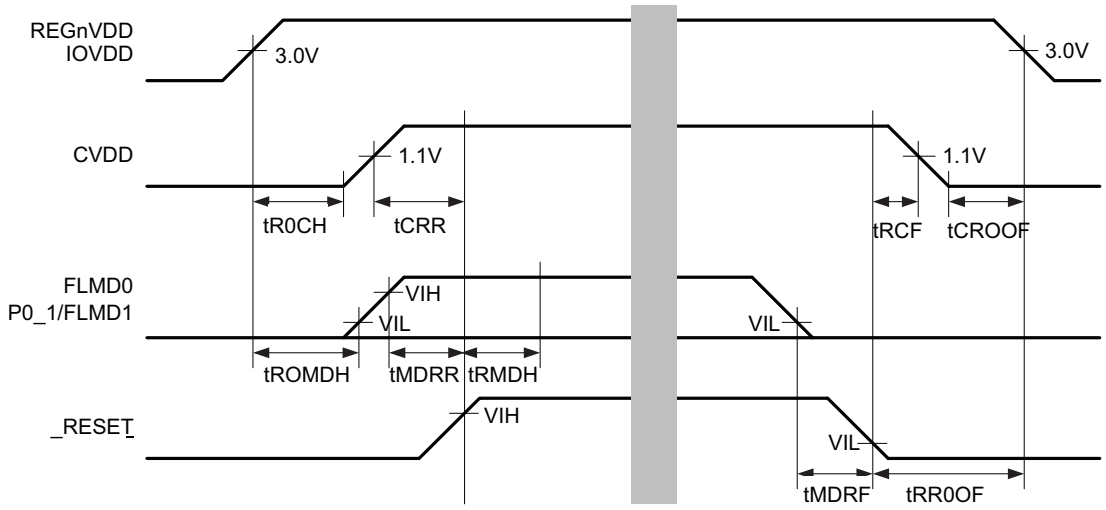
Note IOVDD: AnVDD, B0VDD, EnVDD, FVDD, OSCVDD

3.5.3 Condition 2

RESET is used; WAKE and PTCTL1 are not used
Normal operating mode / Serial programming mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REGnVDD, IOVDD (rise) to CVDD (0V) hold time	tR0CH		1	-	-	ms
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		1	-	-	ms
CVDD (rise) to _RESET (rise)	tCRR		0	-	-	ms
FLMD0,1 (≥VIH or VIL1) [a] to _RESET(≤VIL) (rise)	tMDRR		1	-	-	ms
_RESET (rise) to FLMD0,1(≥VIH or ≤VIL) hold time	tRMDH		1	-	-	ms
FLMD0,1,MODE0,1(≤VIL) to _RESET (≥VIH) (fall) setup time	tMDRF		0	-	-	ms
_RESET (fall) to CVDD (fall)	tRCF		0	-	-	ms
CVDD (0V) to REGnVDD, IOVDD (fall)	tCR0OF		0	-	-	ms
_RESET (≤VIL) (fall) to REGnVDD, IOVDD (fall) hold time	tRR0OF		0	-	-	ms

a) In case of BSCAN mode set also the MODE0,1 pins.

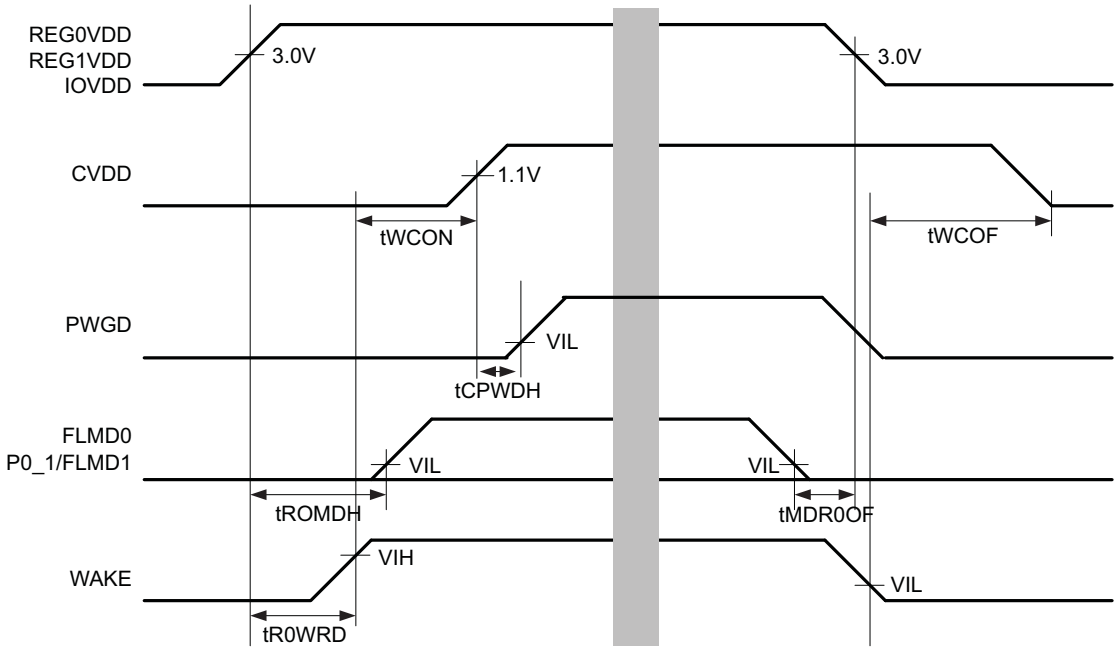


Note There is no specification for _RESET rise and fall times.

3.5.4 Condition 3

RESET is not used; WAKE/PWGD is used
Normal operating mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to WAKE (rise) output delay time	tR0WRD		-	-	2	ms
WAKE (rise) to CVDD (rise)	tWCON		0	-	8	ms
CVDD (rise) to PWGD (rise)	tCPWDH		0	-	-	ms
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		2	-	-	ms
FLMD0,1 (≤VIL) to REG0VDD, IOVDD (fall)	tMDR0OF		0	-	-	ms
WAKE (fall) to CVDD (0V)	tWCOF		0	-	8	ms



The WAKE signal falls at the same time as the fall of the IOVDD voltage due to the lack of output voltage.

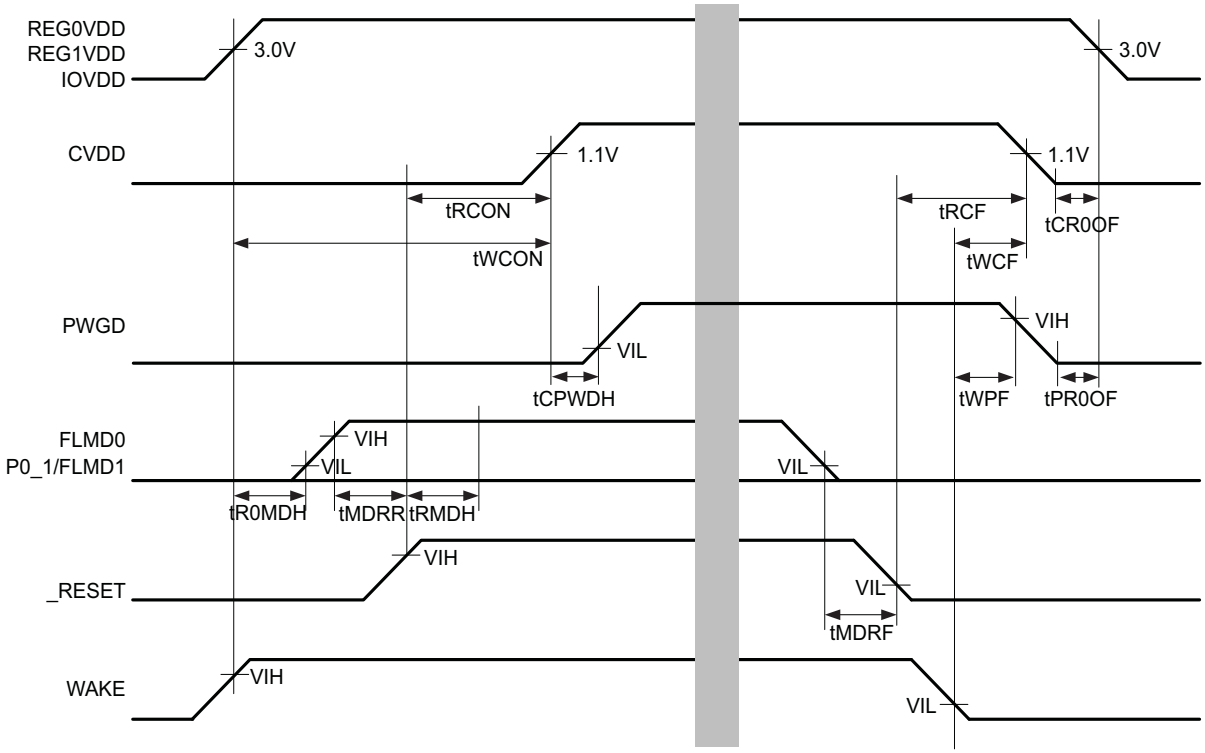
Even if REG0VDD keeps some voltage, the WAKE signal falls at least 2ms after the POC detection.

3.5.5 Condition 4

RESET and WAKE/PWGD are used.
Normal operating mode / Serial programming mode / BSCAN mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1 (≤VIL) hold time	tR0MDH		1	-	-	ms
FLMD0,1 (VIH or VIL) [a] to _RESET (rise)	tMDRR		1	-	-	ms
_RESET (rise) to CVDD (rise)	tRCON		0	-	10	ms
WAKE (rise) to CVDD (rise)	tWCON		0	-	-	ms
CVDD (rise) to PWGD (rise)	tCPWDH		0	-	-	ms
_RESET (rise) to FLMD0,1(VIH or VIL) [a] hold time	tRMDH		1	-	-	ms
FLMD0,1 (≤VIL) to _RESET (fall)	tMDRF		0	-	-	ms
_RESET (fall) to CVDD (fall)	tRCF		0	-	10	ms
WAKE (fall) to CVDD (fall)	tWCF		0	-	-	ms
PWGD (VIH) to CVDD (fall)	tPCS		0	-	-	ms
CVDD (0V) to REG0VDD, IOVDD (fall)	tCR0OF		0	-	-	ms

a) In case of BSCAN mode set also the MODE0,1 pins.

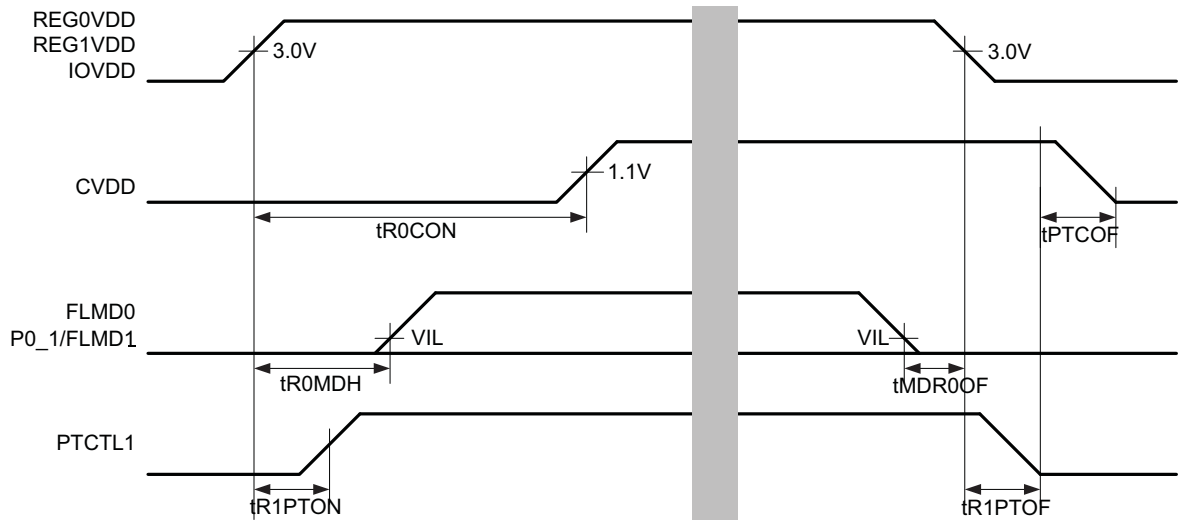


3.5.6 Condition 5

PTCTL1 is used

Normal operating mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to PTCTL1 (rise) setup time	tR1PTON		-	-	1	ms
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (rise) byPTCTL1 (rise)	tR0CON		1	-	10	ms
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		2	-	-	ms
FLMD0,1 (≤VIL) to REG0VDD, REG1VDD, IOVDD (fall)	tMDR0OF		0	-	-	ms
REG0VDD, REG1VDD, IOVDD (fall) to PTCTL1 (fall)	tR1PTOF		-	-	1	ms
PTCTL1 (fall) to CVDD (fall)	tPTCOF		0	-	8	ms



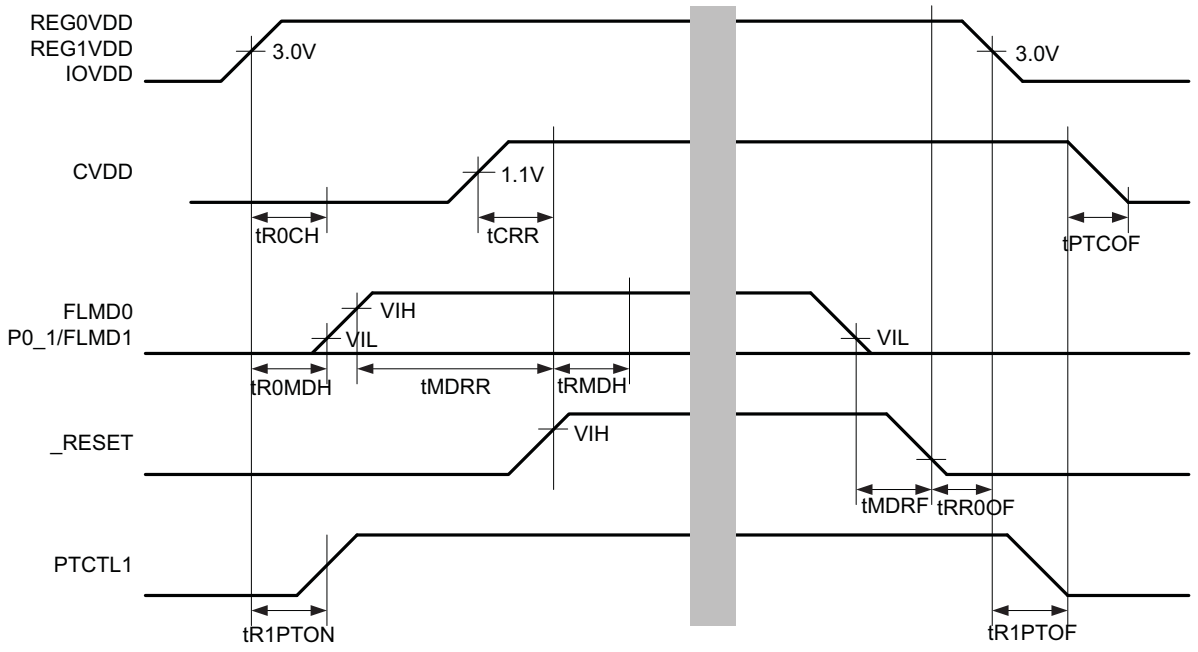
3.5.7 Condition 6

RESET is used; PTCTL1 is used

Normal operating mode / Serial programming mode / BSCAN mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (0V) hold time	tR0CH		-	-	1	ms
REG1VDD (rise) to PTCTL1 (rise) setup time	tR1PTON		-	-	1	ms
REG0VDD, IOVDD (rise) to FLMD0,1 (≤VIL) hold time	tR0MDH		1	-	-	ms
CVDD (rise) to _RESET (rise)	tCRR		0	-	-	ms
FLMD0,1 (VIH or VIL) [a] to _RESET (rise)	tMDRR		1	-	-	ms
_RESET (rise) to FLMD0,1 (VIH or VIL) hold time	tRMDH		1	-	-	ms
FLMD0,1,MODE0,1 (≤VIL) [a] to _RESET (fall)	tMDRF		0	-	-	ms
_RESET (fall) to REG0VDD, IOVDD (fall)	tRR0OF		0	-	-	ms
REG1VDD (fall) to PTCTL1 (fall)	tR1PTOF		-	-	1	ms
PTCTL1 (fall) to CVDD (fall)	tPTCOF		0	-	8	ms

a) In case of BSCAN mode set also the MODE0,1 pins.



Note There is no specification for _RESET rise and fall times.

Chapter 4 Clock generators

4.1 CPU clock

Table 4-1 CPU clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
CPU clock frequency	fCPU	PLL based	-	-	160	MHz
		SSCG based	-	-	176.64	MHz

4.2 Peripheral clock

Table 4-2 Peripheral clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Peripheral clock frequency	fPERI		-	-	80	MHz

4.3 Oscillator characteristics

4.3.1 Main oscillator

A ceramic or crystal resonator can be connected to the main clock input pins as shown in figure *4-1 “Recommended Main Oscillator Circuit”*

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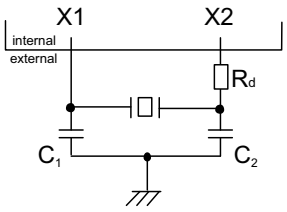

Figure 4-1 Recommended Main Oscillator Circuit

Caution Values of C_1, C_2 and R_d and the best setting for MOSCC.AMPSEL[1:0] register depend on the used ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

The main oscillator amplifier gain for the external resonator can be selected by MOSCC.MOSCCAMPSEL[1:0]. Thereby it can be adjusted to support a wide

range of frequencies to cope with different external resonators and their external circuitry.

As an example a typical setting for quartz crystals is shown in Table *4-3 "Typical setting of MOSCC.AMPSEL[1:0] for different quartz crystals frequencies"*.

Note For details to the setting of MOSCC.MOSCCAMPSEL[1:0] please refer to the user manual.

Table 4-3 Typical setting of MOSCC.AMPSEL[1:0] for different quartz crystals frequencies

MOSCC.AMPSEL[1:0]	Amplification gain	Typical condition for quartz crystals
00	high	$16 < f_{MOSC} \leq 20$ MHz
01	medium	$8 < f_{MOSC} \leq 16$ MHz
10	low	$4 < f_{MOSC} \leq 8$ MHz
11	very low	4 MHz

(1) Main oscillator charactrisitics

Table 4-4 Main oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MainOSC frequency	f_{MOSC}		4	-	20	MHz

Cautions

1. External clock input is prohibited.
2. General guidance for PCB layout:
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with other signal lines.
   - Do not route this circuit close to a signal line with high fluctuating current flow.
   - Always make the ground point of the oscillator capacitor the same potential as REG0VSS and OSCVSS.
   - Do not ground the capacitor to a ground pattern with high current flow.
   - Do not tap signals from the oscillator.

4.3.2 Sub-oscillator

A crystal resonator can be connected to the sub clock input pins as shown in figure *4-2 "Recommended Sub Oscillator Circuit"*

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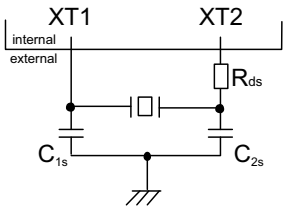


Figure 4-2 Recommended Sub Oscillator Circuit

Caution Values of C_{1s}, C_{2s} and R_{ds} depend on the used crystal and must be specified in cooperation with crystal manufacturer.

(1) Sub-oscillator characteristics

Table 4-5 Sub-oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MainOSC frequency	fSOSC		-	32.768	-	kHz

4.3.3 Internal oscillator

Table 4-6 Internal oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Lowspeed OSC frequency	fRL	• Other than DeepStop mode • DeepStop mode with PSC0.REGSTP = 0	220.8	240	259.2	kHz
	fRLLP	• DeepStop mode with PSC0.REGSTP = 1	216	240	264	kHz
Highspeed OSC frequency	fRH	• Other than DeepStop mode • DeepStop mode with PSC0.REGSTP = 0	7.2	8.0	8.8	MHz
	fRHLP	• DeepStop mode with PSC0.REGSTP = 1	6.64	8.0	8.8	MHz
Highspeed OSC stabilization time	TRHSTB		-	-	19	µs

4.4 PLL Characteristics

Table 4-7 PLL characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Input frequency	fxn	PLL mode and SSCG mode	4	-	20	MHz
Output frequency	fxxn	PLL mode	25	-	160	MHz
		SSCG mode	22.40	-	176.6	MHz
Lock time	TLCKPn	PLL mode	-	-	650	µs
	TLCKSn	SSCG mode	-	-	1300	µs
Period jitter[a]	t_{PJn}	Peak to peak, fixed frequency mode, Pr=2	-150	-	150	ps
Long term jitter[a]	t_{LTJn}	PLL mode, Peak to peak, term=1µs f_{VCOOUT}=160MHz (Pr=2)	-1.275	-	1.275	ns

a) Not tested in production. Specified by design.

Chapter 5 Supply current specification

5.1 Total supply current for µPDF70F3564

Table 5-1 Total supply current

Item	Power[a]		Condition[b]						Specification				Unit
	ISO0	ISO1	8MHz intOSC	Main OSC	Sub OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	
RUN mode	ON	ON	ON	ON	ON	ON	160	WORKING		247	394	416	mA
	ON	ON	ON	ON	ON	ON	160	STOPPED		153	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING		30	60	62	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED		22	-	-	mA
	ON	OFF	ON	ON	ON	ON	160	WORKING		176	285	300	mA
	ON	OFF	ON	ON	ON	ON	160	STOPPED		140	-	-	mA
	ON	OFF	ON	OFF	ON	OFF	8	WORKING		24	50	52	mA
	ON	OFF	ON	OFF	ON	OFF	8	STOPPED		21	-	-	mA
HALT mode	ON	ON	ON	ON	ON	ON	160	WORKING		236	305	311	mA
	ON	ON	ON	ON	ON	ON	160	STOPPED		150	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING		29	50	51	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED		21	-	-	mA
STOP mode	ON	ON	OFF	OFF	OFF	OFF	-	STOPPED		2.5	57	67	mA
	ON	OFF	OFF	OFF	OFF	OFF	-	STOPPED		2.2	49	57	mA
DEEPSTOP mode	OFF	OFF	OFF	OFF	OFF	OFF	-	STOPPED		0.06	3.4	3.6	mA
	OFF	OFF	ON	OFF	OFF	OFF	-	STOPPED		0.60	8.0	9.2	mA
	OFF	OFF	ON	OFF	ON	OFF	-	STOPPED		0.60	8.1	9.2	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.

Notes

1. The above currents do not include port buffer currents or ADC currents.
2. The currents in run mode include currents for self-programming and EEPROM emulation.
3. The current of FlexRay is not included in case of CPU frequency = 8MHz.
4. The ‘typical’ specification is for reference only and not a guaranteed value. The ‘typical’ specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=FVDD=OSCVDD=EmVDD=B0VDD=AmVDD=AmVREFP=5.0V (n=0-3, m=0-1).
   - CVDD = 1.2V
   - REGnVSS=OSCVSS=EmVSS=B0VSS=AmVSS=AmVREFM=0V (n=0-3, m=0-1)

5.2 CVDD supply current for µPDF70F3564

Table 5-2 CVDD supply current

Item	Power[a]		Condition[b]						Specification				Unit
	ISO0	ISO1	8MHz intOSC	Main OSC	Sub OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	
RUN mode	ON	ON	ON	ON	ON	ON	160	WORKING		216	347	365	mA
	ON	ON	ON	ON	ON	ON	160	STOPPED		129	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING		18	41	43	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED		11	-	-	mA
	ON	OFF	ON	ON	ON	ON	160	WORKING		145	237	250	mA
	ON	OFF	ON	ON	ON	ON	160	STOPPED		116	-	-	mA
	ON	OFF	ON	OFF	ON	OFF	8	WORKING		12	32	33	mA
	ON	OFF	ON	OFF	ON	OFF	8	STOPPED		9	-	-	mA
HALT mode	ON	ON	ON	ON	ON	ON	160	WORKING		205	267	272	mA
	ON	ON	ON	ON	ON	ON	160	STOPPED		126	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING		17	35	36	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED		10	-	-	mA
STOP mode	ON	ON	OFF	OFF	OFF	OFF	-	STOPPED		1.7	37	43	mA
	ON	OFF	OFF	OFF	OFF	OFF	-	STOPPED		1.3	28	33	mA
DEEPSTOP mode	OFF	OFF	OFF	OFF	OFF	OFF	-	STOPPED		0.0	0.0	0.0	mA
	OFF	OFF	ON	OFF	OFF	OFF	-	STOPPED		0.0	0.0	0.0	mA
	OFF	OFF	ON	OFF	ON	OFF	-	STOPPED		0.0	0.0	0.0	mA

a) The AWO is always ON.
b) The 240kHz IntOSC is always ON.

Notes

1. The above currents do not include port buffer currents or ADC currents.
2. The currents in run mode include currents for self-programming and EEPROM emulation.
3. The current of FlexRay is not included in case of CPU frequency = 8MHz.
4. The ‘typical’ specification is for reference only and not a guaranteed value. The ‘typical’ specification is applicable under the following conditions:
   - Ta = 25°C
   - REGnVDD=FVDD=OSCVDD=EmVDD=B0VDD=AmVDD=AmVREFP=5.0V (n=0-3, m=0-1).
   - CVDD = 1.2V

   REGnVSS=OSCVSS=EmVSS=B0VSS=AmVSS=AmVREFM=0V (n=0-3, m=0-1)

5.3 Voltage Comparator characteristics

Table 5-3 VCMP characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VCMP current	IVCMP			200	300	µA

Chapter 6 I/O specification

6.1 Port Characteristics

6.1.1 Condition settings

Some of the conditions mentioned in this chapter can be selected by software. The related register settings are described below:

(1) Input characteristic

The input characteristics can be selected by the registers PIS and PISE with the following coding:

Table 6-1 Input characteristic selection

PISE	PIS	Reference in UserManual	Electrical characteristic
0	0	Type 1	CMOS[a]
0	1	Type 2	Schmitt2
1	0	Type 3	Schmitt1
1	1	Type 4	Schmitt4

a) Default setting after reset

6.1.2 PgE0

Table 6-2 PgE0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·E0VDD	-	E0VDD+0.3	V
		Schmitt1	0.7·E0VDD	-	E0VDD+0.3	
		Schmitt2	0.8·E0VDD	-	E0VDD+0.3	
		Schmitt4 (E0VDD=VPOC~3.0)	0.84·E0VDD	-	E0VDD+0.3	
		Schmitt4 (E0VDD=3.0~5.5)	0.8·E0VDD	-	E0VDD+0.3	
Low level input voltage	VIL	CMOS	-0.5	-	0.3·E0VDD	V
		Schmitt1	-0.5	-	0.3·E0VDD	
		Schmitt2	-0.5	-	0.2·E0VDD	
		Schmitt4 (E0VDD=VPOC~3.0)	-0.5	-	0.4·E0VDD	
		Schmitt4 (E0VDD=3.0~5.5)	-0.5	-	0.5·E0VDD	
High level output voltage	VOH	IOH = -5mA	E0VDD-1.0	-		V
		IOH = -100µA	E0VDD-0.5	-		
Low level output voltage	VOL	IOL = 5mA	-	-	0.4	V
		IOL = 100µA	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-		V
		Schmitt2	0.3	-		
		Schmitt4	0.1	-		
Internal pull-up resistor	RU		20	40	100	kΩ
Internal pull-down resistor	RD		20	40	100	kΩ
High level port output current	IOH	Power supply of PgE0	-	-	-20	mA
Low level port output current	IOL	Power supply of PgE0	-	-	20	mA
High level input leakage current	ILIH	VI = E0VDD	-	-	0.5	µA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	µA
High level output leakage current	ILOH	VO = E0VDD	-	-	0.5	µA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	µA
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns

6.1.3 PgE1

Table 6-3 PgE1 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·E1VDD	-	E1VDD+0.3	V
		Schmitt1	0.7·E1VDD	-	E1VDD+0.3	
		Schmitt2	0.8·E1VDD	-	E1VDD+0.3	
		Schmitt4 (E1VDD=VPOC~3.0)	0.84·E1VDD	-	E1VDD+0.3	
		Schmitt4 (E1VDD=3.0~5.5)	0.8·E1VDD	-	E1VDD+0.3	
Low level input voltage	VIL	CMOS	-0.5	-	0.3·E1VDD	V
		Schmitt1	-0.5	-	0.3·E1VDD	
		Schmitt2	-0.5	-	0.2·E1VDD	
		Schmitt4 (E1VDD=VPOC~3.0)	-0.5	-	0.4·E1VDD	
		Schmitt4 (E1VDD=3.0~5.5)	-0.5	-	0.5·E1VDD	
High level output voltage	VOH	IOH = -5mA[a]	E1VDD-1.0	-		V
		IOH = -100µA	E1VDD-0.5	-		
Low level output voltage	VOL	IOL = 5mA[a]	-	-	0.4	V
		IOL = 100µA	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-		V
		Schmitt2	0.3	-		
		Schmitt4	0.1	-		
Internal pull-up resistor	RU		20	40	100	kΩ
Internal pull-down resistor	RD		20	40	100	kΩ
High level port output current	IOH	Power supply of PgE1	-	-	-150	mA
Low level port output current	IOL	Power supply of PgE1	-	-	150	mA
High level input leakage current	ILIH	VI = E1VDD	-	-	0.5	µA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	µA
High level output leakage current	ILOH	VO = E1VDD	-	-	0.5	µA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	µA
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns

a) The maximum number of PgE1 pins with ‘ON’ signal at the same time is 5 in ‘Slow mode’.
The maximum number of PgE1 pins with ‘ON’ signal at the same time is 8 in ‘Fast mode’.
See the UM for the related description of the Port drive strength control.

6.1.4 PgB0

Table 6-4 PgB0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·B0VDD	-	B0VDD+0.3	V
		Schmitt1	0.7·B0VDD	-	B0VDD+0.3	
		Schmitt2	0.8·B0VDD	-	B0VDD+0.3	
		Schmitt4 (B0VDD=VPOC~3.0)	0.84·B0VDD	-	B0VDD+0.3	
		Schmitt4 (B0VDD=3.0~5.5)	0.8·B0VDD	-	B0VDD+0.3	
Low level input voltage	VIL	CMOS	-0.5	-	0.3·B0VDD	V
		Schmitt1	-0.5	-	0.3·B0VDD	
		Schmitt2	-0.5	-	0.2·B0VDD	
		Schmitt4 (B0VDD=VPOC~3.0)	-0.5	-	0.4·B0VDD	
		Schmitt4 (B0VDD=3.0~5.5)	-0.5	-	0.5·B0VDD	
High level output voltage	VOH	IOH = -5mA[a]	B0VDD-1.0	-	-	V
		IOH = -100µA	B0VDD-0.5	-	-	
Low level output voltage	VOL	IOL = 5mA[a]	-	-	0.4	V
		IOL = 100µA	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-	-	V
		Schmitt2	0.3	-	-	
		Schmitt4	0.1	-	-	
Internal pull-up resistor	RU		20	40	100	kΩ
Internal pull-down resistor	RD		20	40	100	kΩ
High level port output current	IOH	Power supply of PgB0	-	-	-150	mA
Low level port output current	IOL	Power supply of PgB0	-	-	150	mA
High level input leakage current	ILIH	VI =B0VDD	-	-	0.5	µA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	µA
High level output leakage current	ILOH	VO = B0VDD	-	-	0.5	µA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	µA
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns

a) The maximum number of PgB0 pins with ‘ON’ signal at the same time is 5 in ‘Slow mode’ (Except the pins related to the external memory interface (MEMC)).
The maximum number of PgB0 pins with ‘ON’ signal at the same time is 8 in ‘Fast mode’.
See the UM for the related description of the Port drive strength control.

6.1.5 PgA0 and PgA1

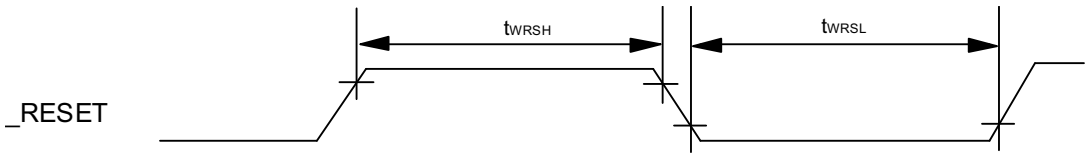
Table 6-5 PgA0 and PGA1 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·AnVDD	-	AnVDD+0.3	V
Low level input voltage	VIL	CMOS	-0.5	-	0.3·AnVDD	V
High level output voltage	VOH	IOH = -1mA	AnVDD-1.0	-	-	V
		IOH = -100µA	AnVDD-0.5	-	-	
Low level output voltage	VOL	IOL = 1mA	-	-	0.4	V
		IOL = 100µA	-	-	0.4	
High level port output current	IOH	Power supply of PgA0 and PgA1	-	-	-20	mA
Low level port output current	IOL	Power supply of PgA0 and PgA1	-	-	20	mA
High level input leakage current	ILIH	VI = AnVDD	-	-	0.2	µA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.2	µA
High level output leakage current	ILOH	VO = AnVDD	-	-	0.2	µA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.2	µA
Output frequency	fO		-	-	25	MHz
Rise time (output)	tKRP		-	-	15	ns
Fall time (output)	tKFP		-	-	15	ns

Chapter 7 Peripherals specification

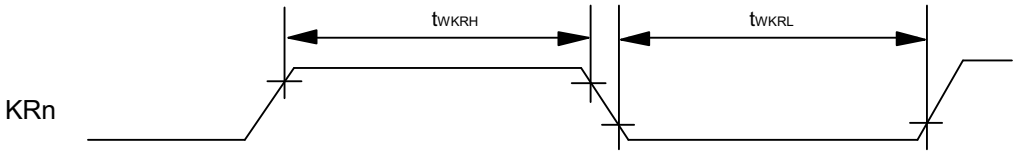
7.1 Reset timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
RESET input High level width	tWRSH	Highspeed OSC is operating	450	-	-	ns
		Highspeed OSC is stopped	4.7	-	-	µs
RESET input Low level width	tWRSL	Highspeed OSC is operating	450	-	-	ns
		Highspeed OSC is stopped	4.7	-	-	µs



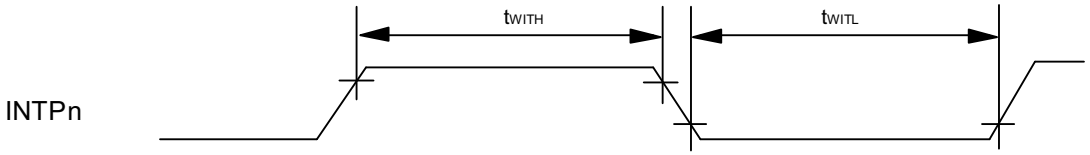
7.2 NMI timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
NMI input High level width	tWNIH		300	-	-	ns
NMI input Low level width	tWNIL		300	-	-	ns



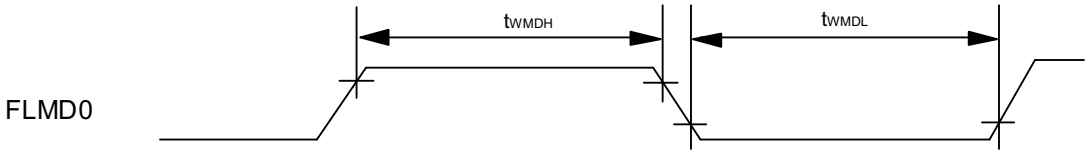
7.3 INTP timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
INTPn input High level width	tWITH		300	-	-	ns
INTPn input Low level width	tWITL		300	-	-	ns



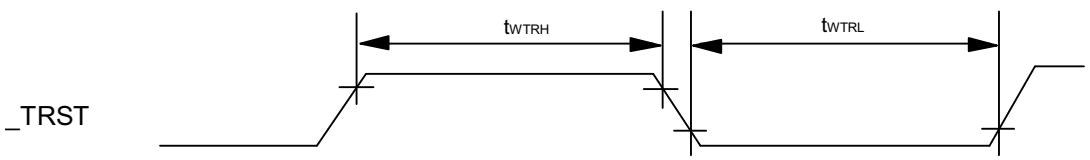
7.4 FLMD0 timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 input High level width	tWMDH		300	-	-	ns
FLMD0 input Low level width	tWMDL		300	-	-	ns
FLMD0 external pull down resistor	R_{FLMD0}		82	-	-	kΩ



7.5 _DCUTRST timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
_DCUTRST input High level width	tWRH		450	-	-	ns
_DCUTRST input Low level width	tWTRL		450	-	-	ns



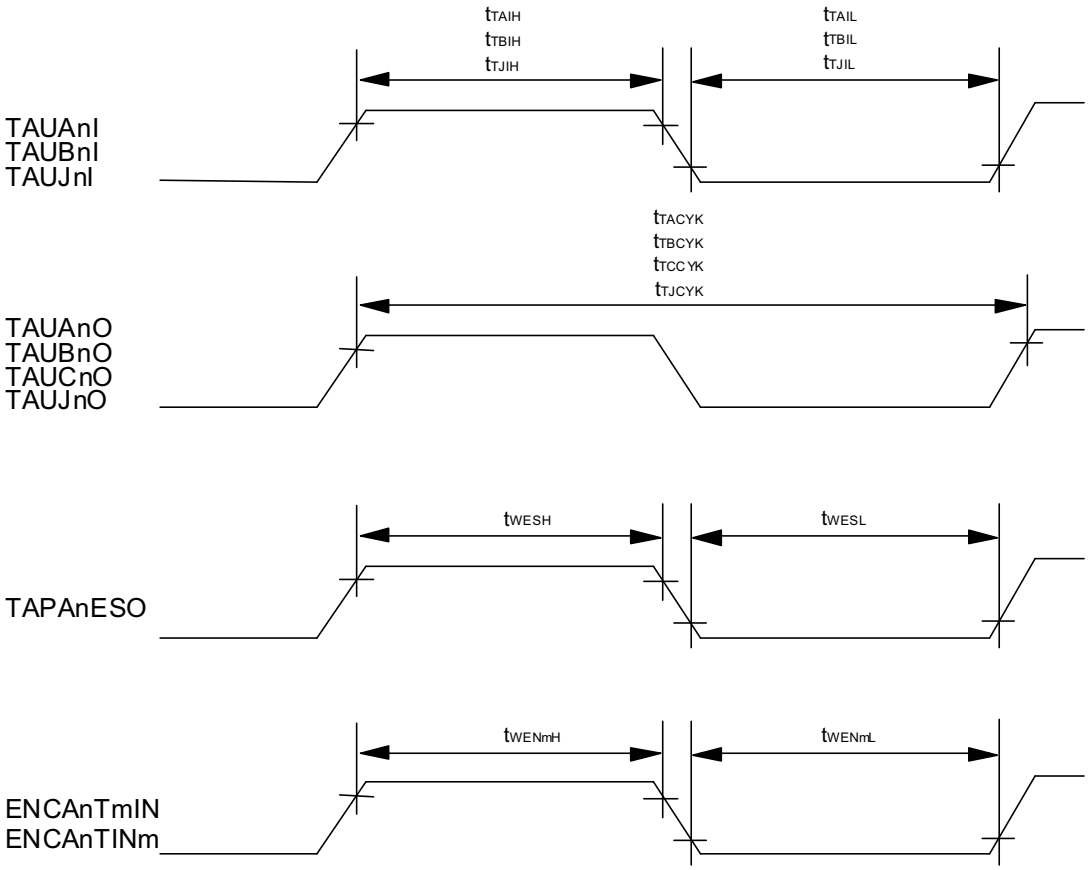
7.6 Timer timing

Table 7-1 Timer timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
TAUAnI input High level width	tTAIH	n=0	a,b	-	-	ns
TAUAnI input Low level width	tTAIL	n=0	a,b	-	-	ns
TAUBnI input High level width	tTBIH	n=1	a,b	-	-	ns
TAUBnI input Low level width	tTBIL	n=-1	a,b	-	-	ns
TAUJnI input High level width	tTJIH	n=0,1	300	-	-	ns
TAUJnI input High level width	tTJIH		4.7	-	-	µs
TAUJnI input High level width	tTJIH		b	-	-	ns
TAUJnI input Low level width	tTJIL	n=0,1	300	-	-	ns
TAUJnI input Low level width	tTJIL		4.7	-	-	µs
TAUJnI input Low level width	tTJIL		b	-	-	ns
TAUAnO output cycle	tTACYK	n=0	-	-	20	MHz
TAUBnO output cycle	tTBCYK	n=1	-	-	20	MHz
TAUCnO output cycle	tTCCYK	n=2-7	-	-	20	MHz
TAUJnO output cycle	tTJCYK	n=0,1	-	-	20	MHz
TAPAnESO input High level width	tWESH	n=0	300	-	-	ns
TAPAnESO input Low level width	tWESL	n=0	300	-	-	ns
ENCAnTmIN high level width	tWENmH	n=0, m=A,B,Z	a,b	-	-	ns
ENCAnTmIN low level width	tWENmL	n=0, m=A,B,Z	a,b	-	-	ns
ENCAnTINm high level width	tWENmH	n=0, m=0-1	a,b	-	-	ns
ENCAnTINm low level width	tWENmL	n=0, m=0-1	a,b	-	-	ns

a) With digital noise filter enabled: 2, 3, 4 or 5 x Tsamp + 20 (Tsamp shows sampling period specified in Noise filter macro. More than 1 PCLK width of Timer macro must be kept regarding DNF pass through pulse width.

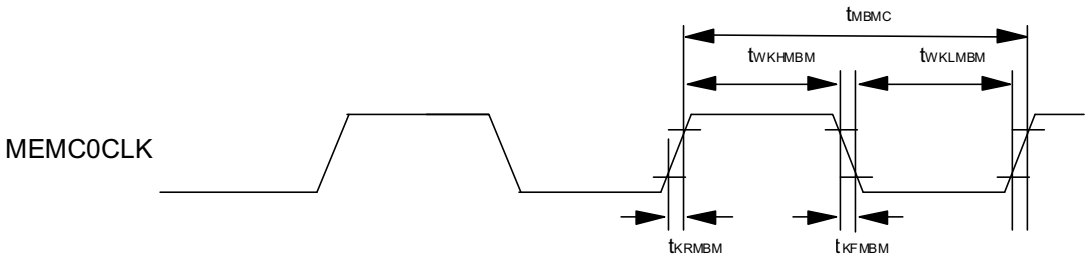
b) With digital noise filter disabled: 1xtSYNC+20 (tSYNC: 1 PCLK of Timer macro)



7.7 Multiplexed bus timing

Table 7-2 MEMC0CLK timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MEMC0CLK output cycle	tMEMC		25	-	-	ns
MEMC0CLK high level width	tWKHMEM		tMEMC / 2 - 10	-	-	ns
MEMC0CLK low level width	tWKLMEM		tMEMC / 2 - 10	-	-	ns
MEMC0CLK rise time	tKRMEM		-	-	10	ns
MEMC0CLK fall time	tKFMEM		-	-	10	ns

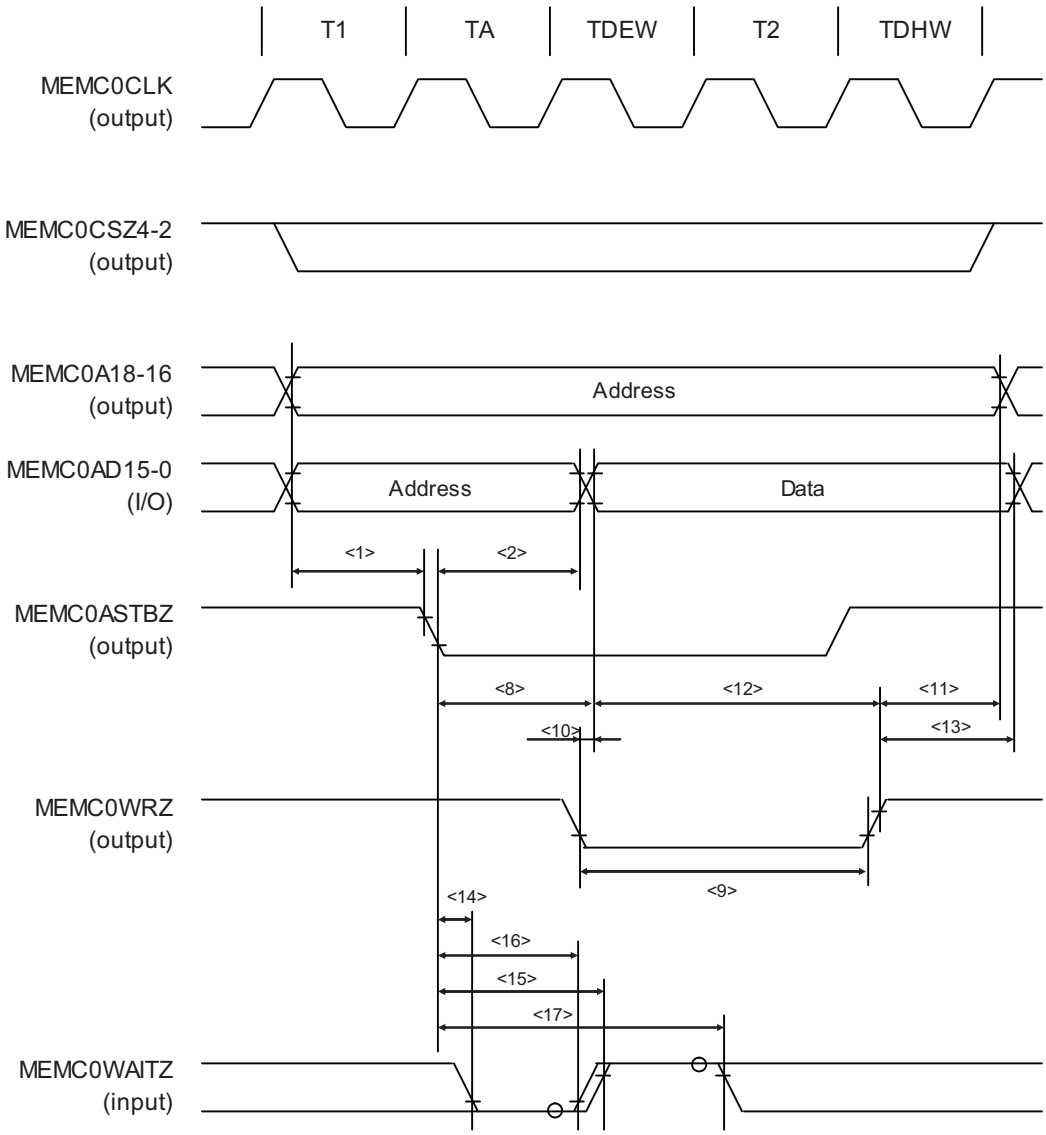


7.7.1 MEMC0CLK asynchronous timing

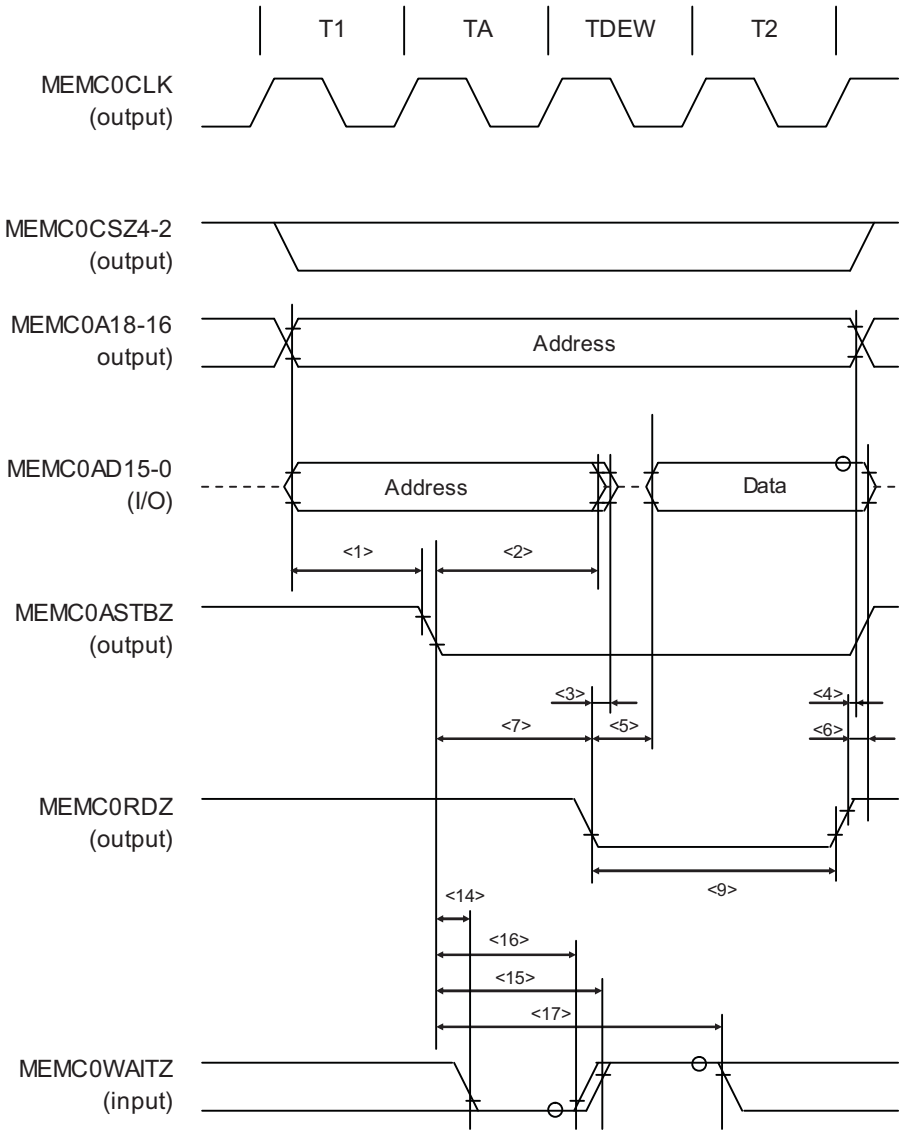
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Bus operational period	T	-	25	-	-	ns
Address setup time to MEMC0ASTBZ (f)	tSAST	<1>	(1+ASW)·T-15	-	-	ns
Address hold time from MEMC0ASTBZ (f)	tHSTA	<2>	(1+AHW)·T-15	-	-	ns
Address float delay time from MEMC0RDZ (f)	tFRDA	<3>	-	-	6	ns
Address hold time from MEMC0RDZ (r)	tHRDA	<4>	0	-	-	ns
Data input delay time from MEMC0RDZ (f)	tDRDID	<5>	6	-	(1+w)·T-35	ns
Data input hold time from MEMC0RDZ (r)	tHRDID	<6>	0	-	-	ns
Delay time from ASTB(f) to MEMC0RDZ (f)	tDSTRD	<7>	(1+AHW)·T-15	-	-	ns
Delay time from ASTB(f) to MEMC0WRZ (f)	tDSTWR	<8>	(1+AHW)·T-15	-	-	ns
MEMC0RDZ, MEMC0WRZ low level width	tWRDST	<9>	(1+w)·T-10	-	-	ns
Data output delay time from MEMC0WRZ (f)	tDWROD	<10>	-	-	10	ns
Address hold time from MEMC0WRZ (r)	tHWRA	<11>	T-15	-	-	ns
Data output setup time to MEMC0WRZ (r)	tSODWR	<12>	(1+w)·T-15	-	-	ns
Data output hold time from MEMC0WRZ (r)	tHWROD	<13>	T-15	-	-	ns
MEMC0WAITZ setting delay from MEMC0ASTBZ (f)	tSSTWT1	<14>	-	-	(1+AHW)·T - (2·HEAPCLK+35)	ns
MEMC0WAITZ hold time from MEMC0ASTBZ (f)	tSSTWT2	<15> w≥1	-	-	(1+w+AHW)·T - (2·HEAPCLK+35)	ns
MEMC0WAITZ setting delay from Address	tHSTWT1	<16> w≥1	(w+AHW)·T-(2*HEAPCLK+20)	-	-	ns
MEMC0WAITZ hold time from Address	tHSTWT2	<17> w≥1	(1+w+AHW)·T-2*HEAPCLK+20)	-	-	ns

Notes
1. ASW: Number of Address Setup Wait for multiplex bus
2. AHW: Number of Address Hold Wait for multiplex bus
3. w: Number of data wait
4. In case the bus operational period (T) is shorter then 41ns, tDRDID requires at least 1 data wait (w=1).

(1) Multiplex write cycle (Asynchronous; 1 data wait)



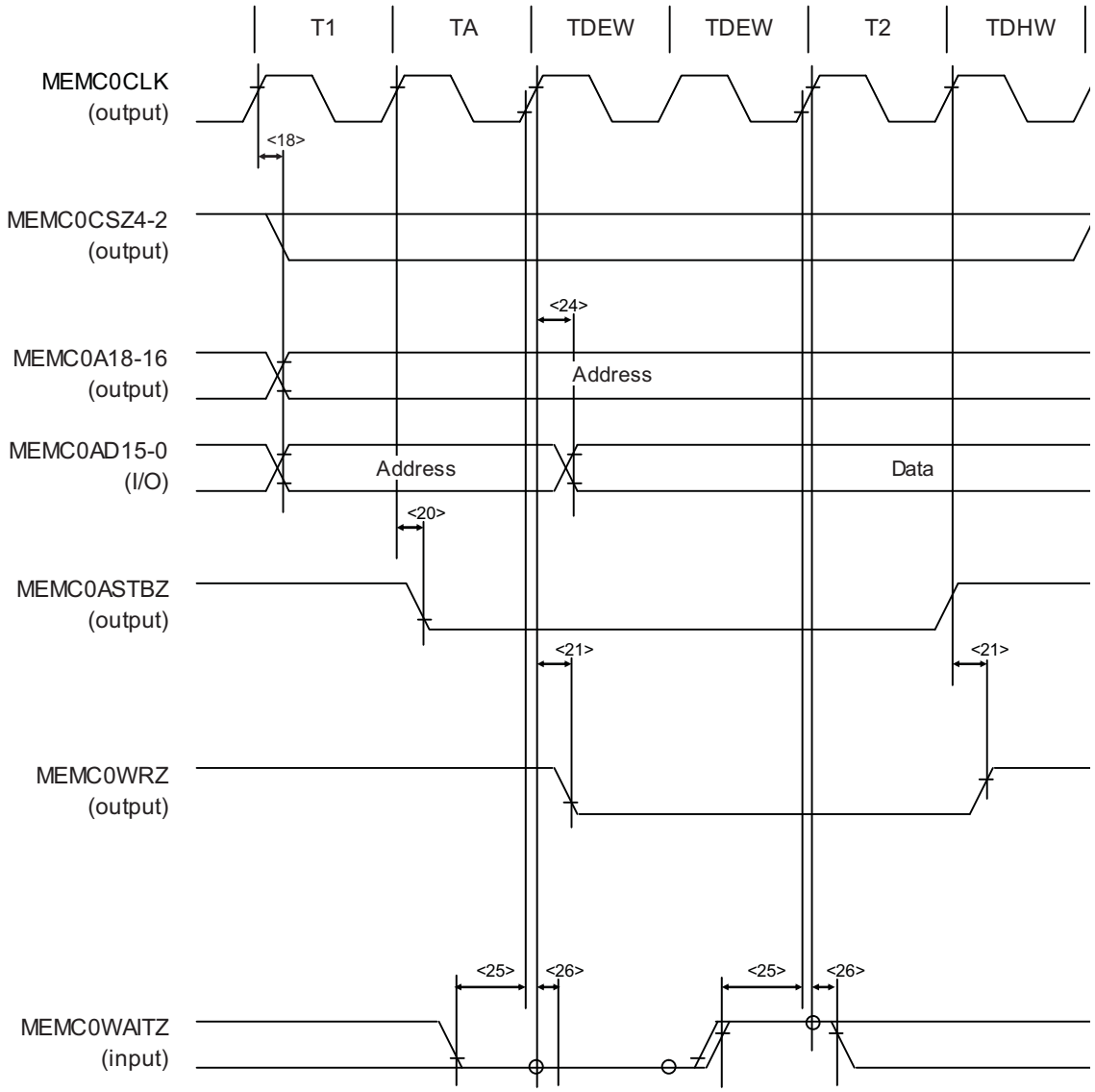
(2) Multiplex read cycle (Asynchronous; 1 data wait)



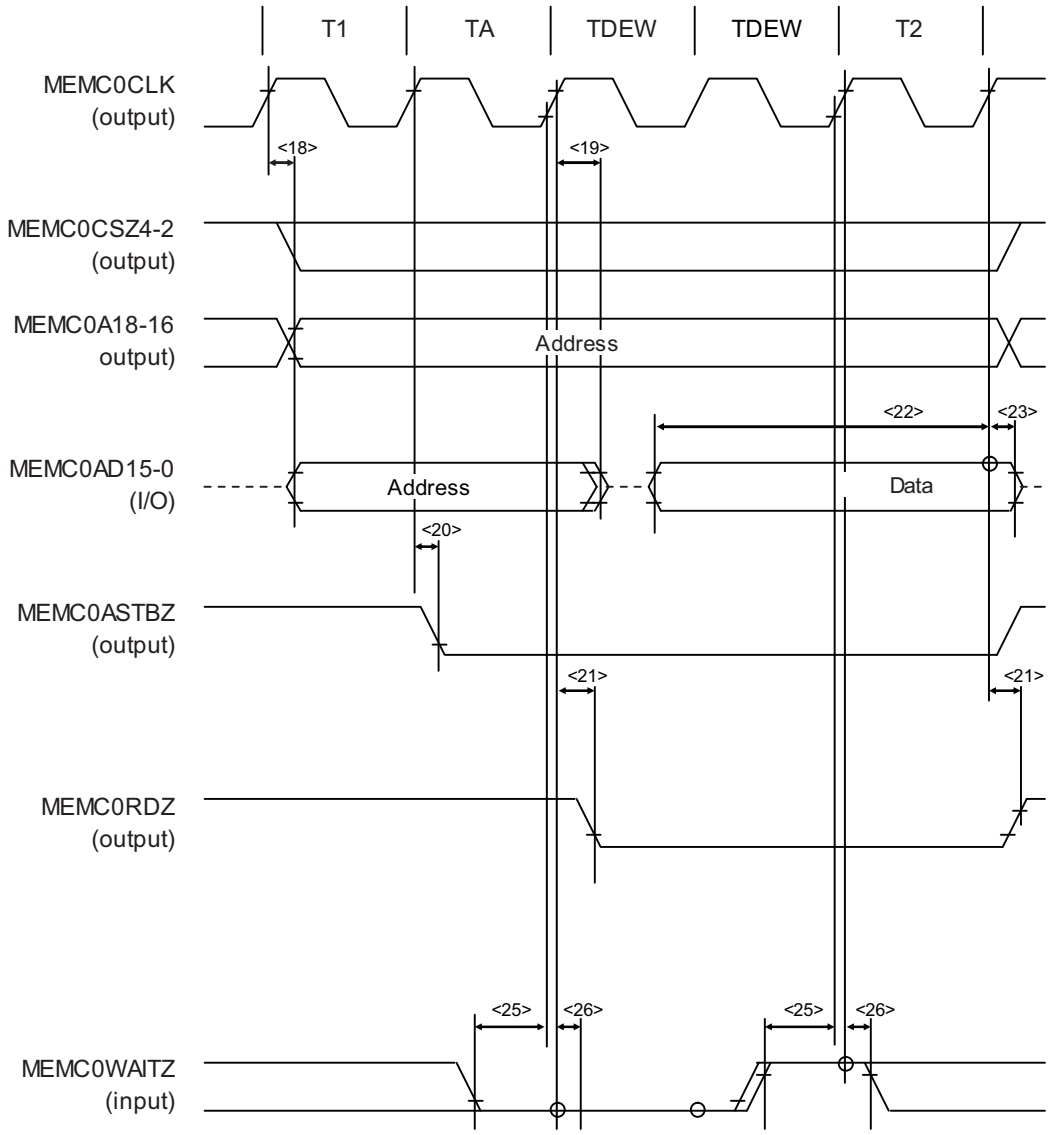
7.7.2 MEMC0CLK synchronous timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Bus operational period	T		25	-	-	ns
Delay time from MEMC0CLK (r) to address	tDKA	<18>	0	-	12	ns
Delay time from MEMC0CLK (r) to address float	tFKA	<19>	0	-	12	ns
Delay time from MEMC0CLK (r) to ASTB (f)	tDKST	<20>	0	-	11	ns
Delay time from MEMC0CLK (r) to MEMC0RDZ and MEMC0WRZ	tDKRDWR	<21>	-2.5	-	6	ns
Data input setup time (from MEMC0CLK (r))	tSIDK	<22>	10	-	-	ns
Data input hold time (from MEMC0CLK (r))	tHKID	<23>	2.5	-	-	ns
Data output delay time (from MEMC0CLK (r))	tDKOD	<24>	-	-	11	ns
MEMC0WAITZ setup time (to MEMC0CLK (r))	tSWTK	<25> B0VDD≥3.5V	23	-	-	ns
		<25> B0VDD<3.5V	27	-	-	ns
MEMC0WAITZ hold time (from MEMC0CLK (r))	tHKWT	<26>	2.5	-	-	ns

(1) Multiplex write cycle (Synchronous; 1 data wait)



(2) Multiplex read cycle (Synchronous; 1 data wait)



7.8 CSI timing

7.8.1 Master modes

(1) CSIG timing

Table 7-3 CSIG timing (Master mode)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		12.5	-	-	ns
CSIGnSC cycle time	tKCYMGn		100	-	-	ns
CSIGnSC high level width	tKWHMGn		0.5 · tKCYMGn-10	-	-	ns
CSIGnSC low level width	tKWLMGn		0.5 · tKCYMGn-10	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSIMGn	CSIGnSC@PDSC=1	30	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSIMGn	CSIGnSC@PDSC=0	38	-	-	ns
CSIGnSI hold time (vs. CSIGnSC)	tHSIMGn		0	-	-	ns
CSIGnSO output delay (vs. CSIGnSC)	tDSOMGn		-	-	7	ns
CSIGnRYI setup time (vs. CSIGnSC)	tSRYIGn	CSIGnCTL1.CSIGnSIT=x CSIGnCTL1.CSIGnHSE=1	2 · tKCYGn+25	-	-	ns
CSIGnRYI High level width	tWRYIGn	CSIGnCTL1.CSIGnHSE=1	tKCYGn- 5.0	-	-	ns

Note n: Number of macro instances. Refer to the User Manual for the detailed specification.

(2) CSIH timing master mode

Table 7-4 CSIH timing (Master mode)

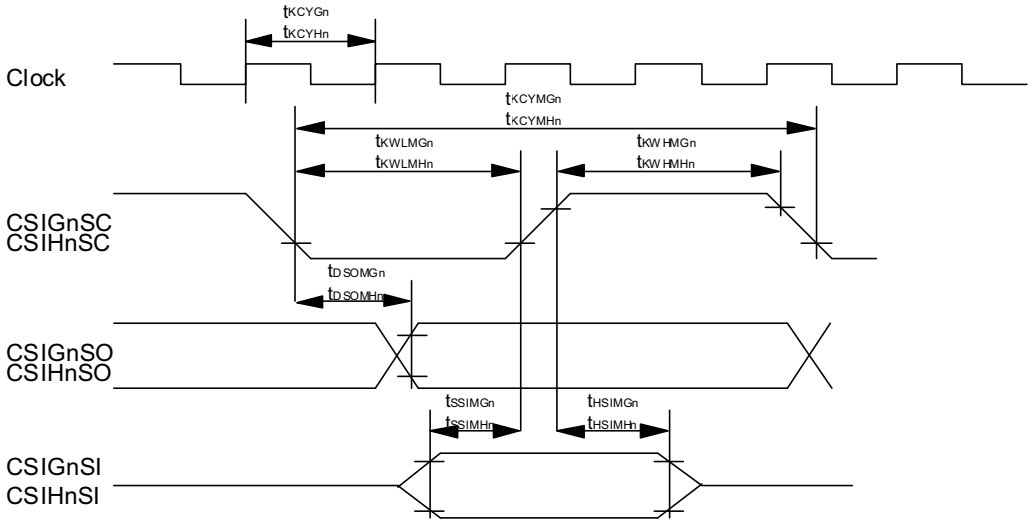
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYHn		12.5	-	-	ns
CSIHnSC cycle time	tKCYMHn		100	-	-	ns
CSIHnSC high level width	tKWHMHn		0.5 · tKCYMHn-10	-	-	ns
CSIHnSC low level width	tKWLMHn		0.5 · tKCYMHn-10	-	-	ns
CSIHnSI setup time (vs. CSIHnSC)	tSSIMHn	CSIHnSC@PDSC=1	30	-	-	ns
		CSIHnSC@PDSC=0	38	-	-	ns
CSIHnSI hold time (vs. CSIHnSC)	tHSIMHn		0	-	-	ns
CSIHnSO output delay (vs. CSIHnSC)	tDSOMHn		-	-	7	ns
CSIHnRYI setup time (vs. CSIHnSC)	tSRYIHn	CSIHnCTL1.CSIHnSIT=x CSIHnCTL1.CSIHnHSE=1	2 · tKCYHn+25	-	-	ns
CSIHnRYI High level width	tWRYIHn	CSIHnCTL1.CSIHnHSE=1	tKCYHn- 5.0	-	-	ns
CSIHnCSS0-7 inactive width	tWSCSBHn		CSIDLE × tKCYMHn - 5.0	-	-	ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	tSSCSBHn0	CSIHnCTL1.CSIHnDAP=0	CSSETUP × tKCYMHn-5.0	-	-	ns
	tSSCSBHn1	CSIHnCTL1.CSIHnDAP=1	(CSSETUP + 0.5) × tKCYMHn-5.0	-	-	ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	tHSCSBHn0	CSIHnCTL1.CSIHnSIT=0	CSHOLD × tKCYMHn-10.0	-	-	ns
	tHSCSBHn1	CSIHnCTL1.CSIHnSIT=1	(CSSHOLD + 0.5) × tKCYMHn-5.0	-	-	ns

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. CSSETUP: Value of CSIHnCFG0-7.CSIHnSP0-7[3:0]
3. CSHOLD: Value of CSIHnCFG0-7.CSIHnHD0-7[3:0]
4. CSIDLE: Value of CSIHnCFG0-7.CSIHnID0-7[2:0]

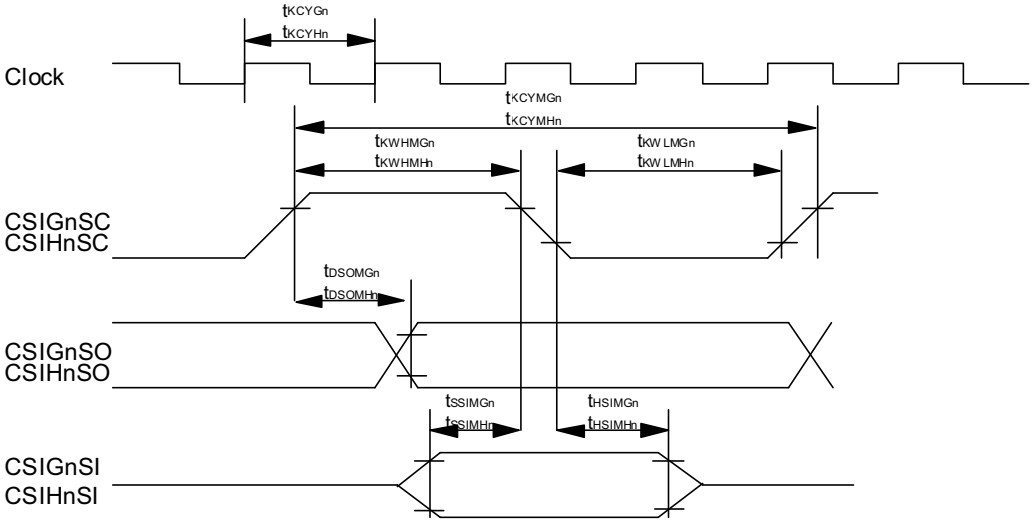
(3) Timing diagrams

SCKO / SI / SO

CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0 / 0 or 1 / 1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0 /0 or 1/1)



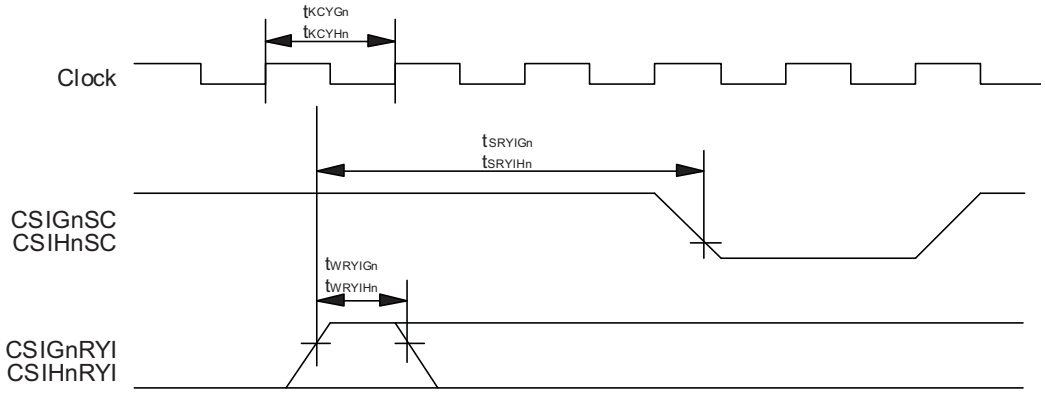
CSIG(CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1 / 0 or 0 / 1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/ 0 or 0/ 1)



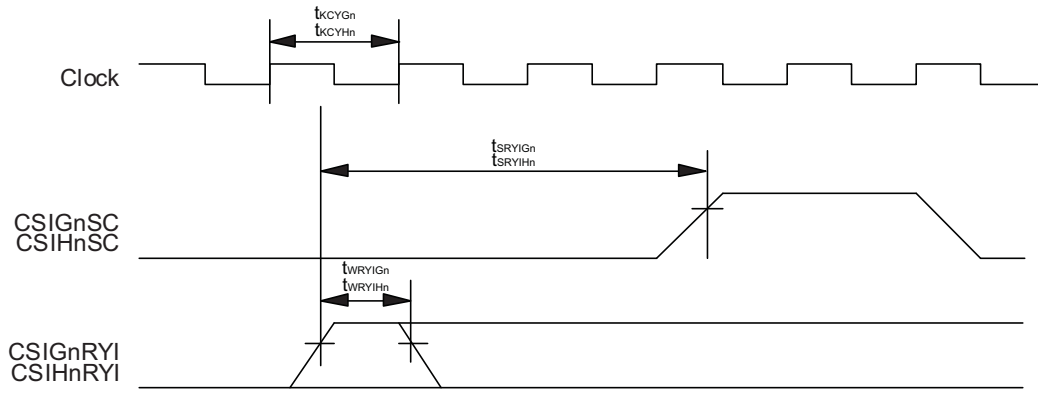
RYI

CSIGnCTL1 : CSIGnHSE=1, CSIGnCTL1 : CSIGnSIT = 0)
CSIHnCTL1 : CSIHnHSE=1, CSIHnCTL1 : CSIHnSIT = 0)

CSIG (CSIGnCTL1 :CSIGnCKR= 0)
CSIH (CSIHnCFGm:CSIHnCKPm= 0)

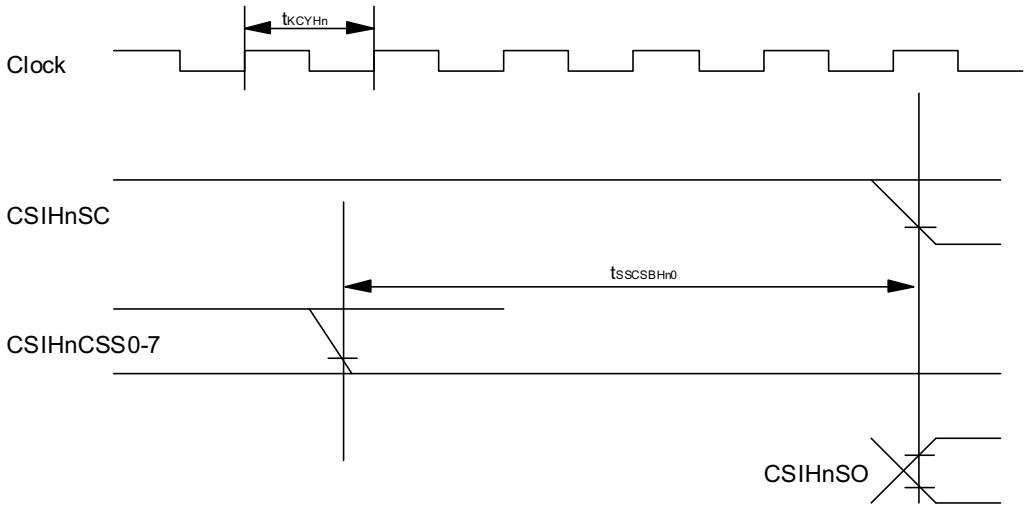


CSIG (CSIGnCTL1 :CSIGnCKR= 1)
CSIH (CSIHnCFGm:CSIHnCKPm= 1)

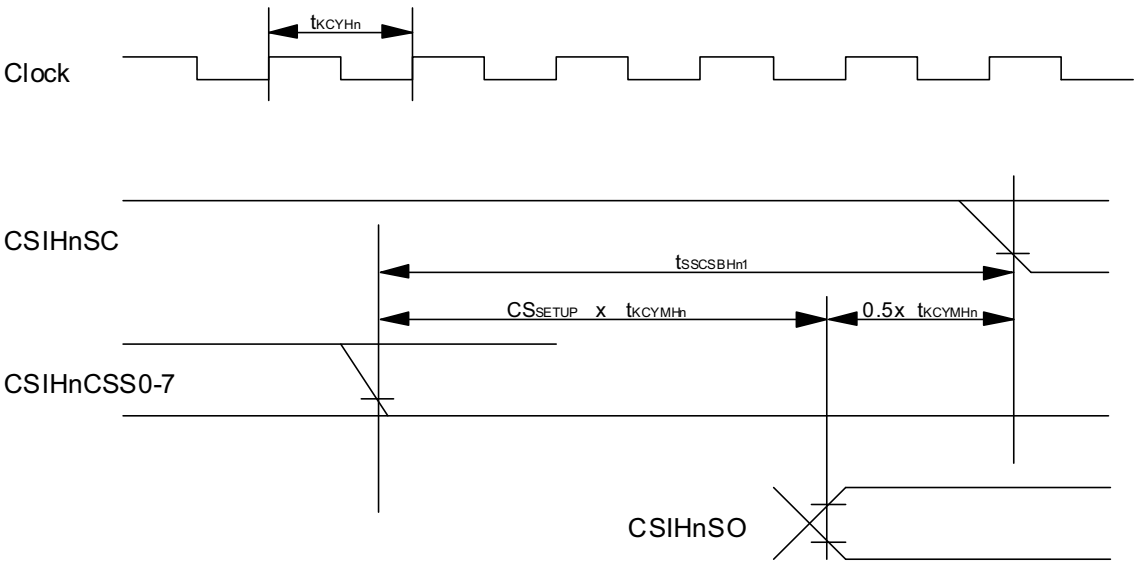


CSSn

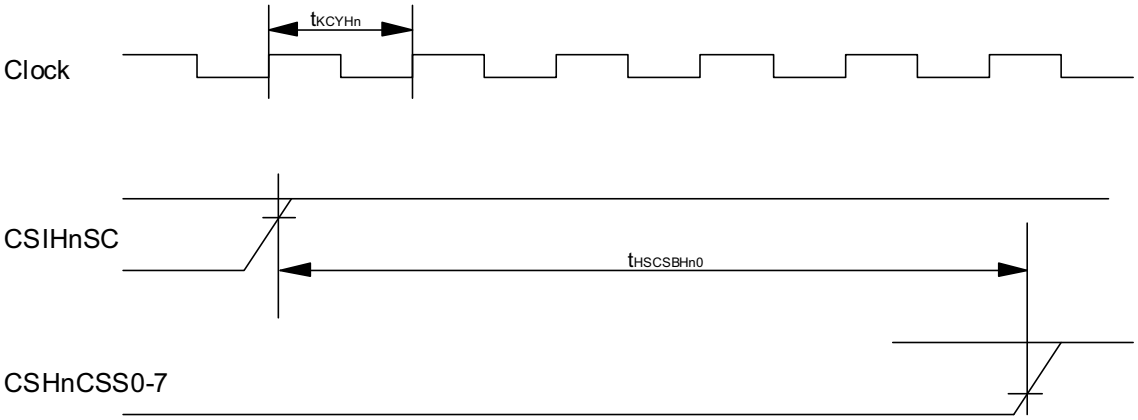
CSIHnCFGm:CSIHnCKPm= 0,CSIHnCFGm:CHIHnDAPm= 0



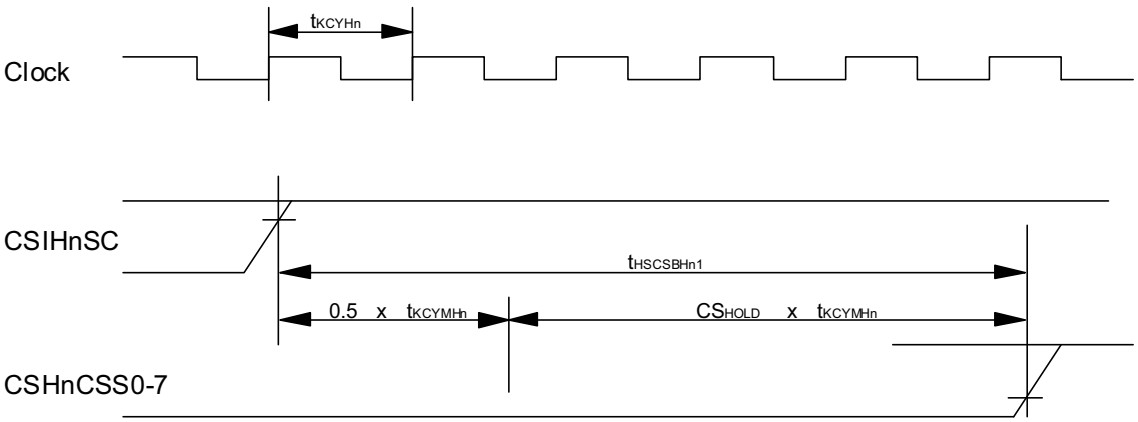
CSIHnCFGm:CSIHnCKPm= 0,CSIHnCFGm:CHIHnDAPm= 1



CSIHnCTL1 : CSIHnSIT=0, CSIHnCFGm: CSIHnCKPm= 0,CSIHnCFGm: CHIHnDAPm= 0



CSIHnCTL1 : CSIHnSIT=1, CSIHnCFGm: CSIHnCKPm= 0,CSIHnCFGm: CHIHnDAPm= 0



7.8.2 Slave mode

(1) CSIG timing slave mode

Table 7-5 CSIG timing (Slave mode)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		12.5	-	-	ns
CSIGnSC cycle time	tKCYSGn		200	-	-	ns
CSIGnSC high level width	tKWHSGn		0.5 · tKCYSGn-10	-	-	ns
CSIGnSC low level width	tKWLSGn		0.5 · tKCYSGn-10	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSISGn		20	-	-	ns
CSIGnSI hold time (vs. CSIGnSC)	tHSISGn		tKCYGn+5.0	-	-	ns
SO output delay (vs SCKI)	tDSOSGn		-	-	35	ns
CSIGnRYO output delay	tSRYOGn		-	-	35	ns
_CSIGnSSI setup time (vs CSIGnSC)	tSSSISGn		0.5 · tKCYSn-5.0	-	-	ns
_CSIGnSSI hold time (vs CSIGnSC)	tHSSISGn		tKCY+5.0	-	-	ns

Note n: Number of macro instances. Refer to the User Manual for the detailed specification.

(2) CSIH timing slave mode

Table 7-6 CSIH timing (Slave mode)

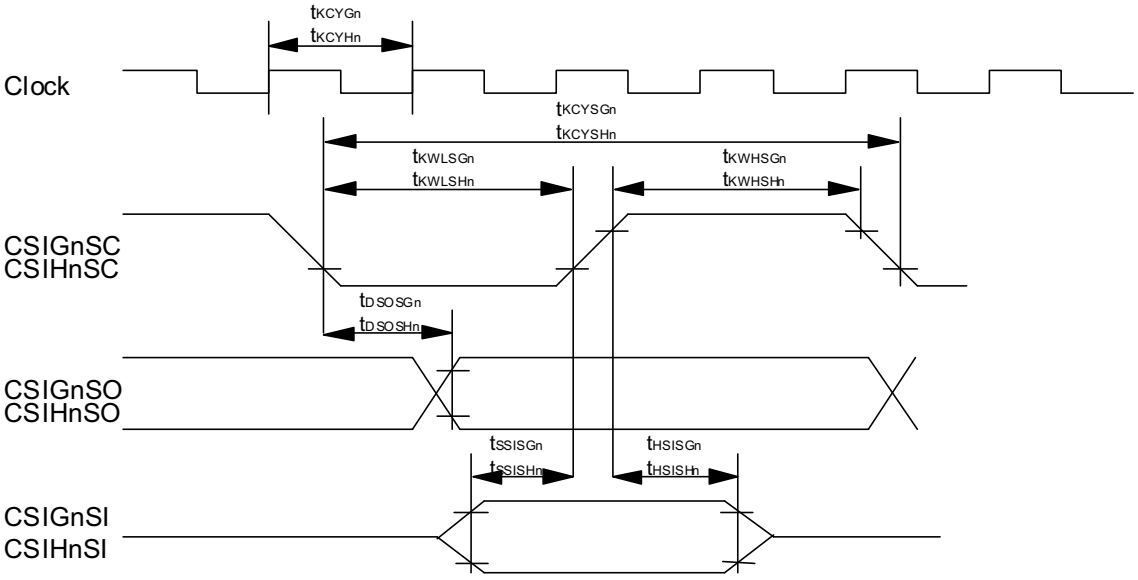
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYHn		12.5	-	-	ns
CSIHnSC cycle time	tKCYSHn		200	-	-	ns
CSIHnSC high level width	tKWHSHn		0.5 · tKCYSHn-10	-	-	ns
CSIHnSC low level width	tKWLSHn		0.5 · tKCYSHn-10	-	-	ns
CSIHnSI setup time (vs. CSIHnSC)	tSSISHn		20	-	-	ns
CSIHnSI hold time (vs. CSIHnSC)	tHSISHn		tKCYHn+5.0	-	-	ns
SO output delay (vs SCKI)	tDSOSHn		-	-	35	ns
CSIHnRYO output delay	tSRYOHn		-	-	35	ns
CSIHnSSI setup time (vs. CSIHnSC)	tSSSISHn		0.5 · tKCYSn-5:0	-	-	ns
CSIHnSSI hold time (vs. CSIHnSC)	tHSSISHn		tKCYn* 5.0	-	-	ns

Note n: Number of macro instances. Refer to the User Manual for the detailed specification.

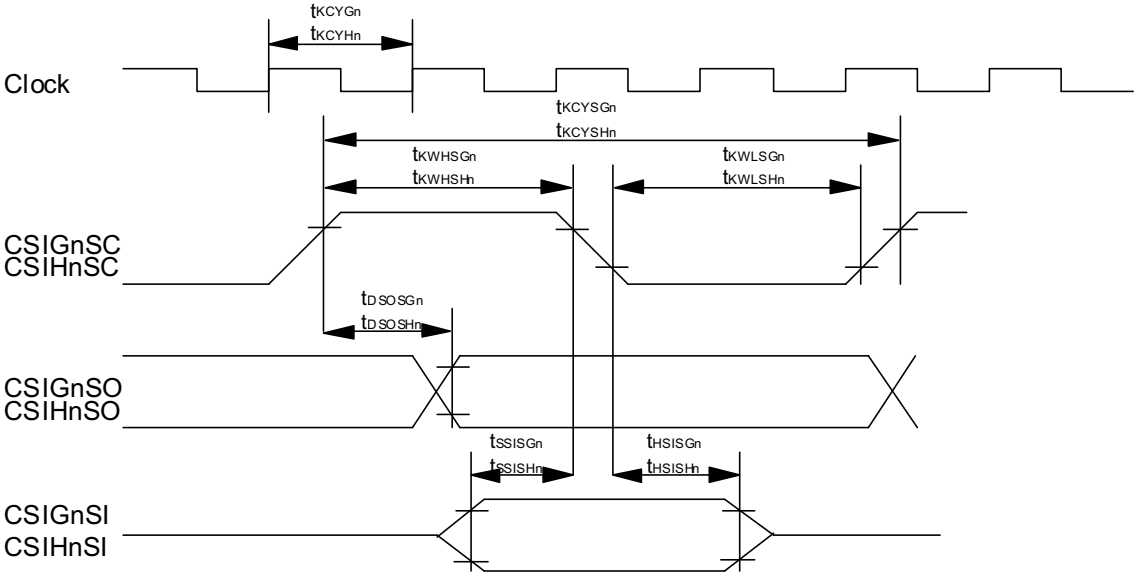
(3) Timing diagrams

SCKO / SI / SO

CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0 or 1/1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/0 or 1/1)

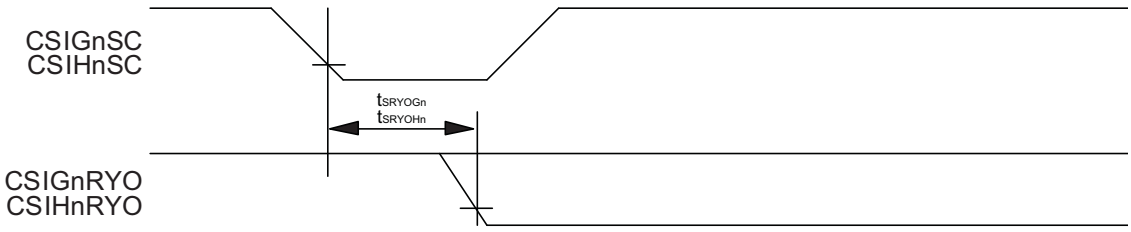


CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0 or 0/1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/0 or 0/1)

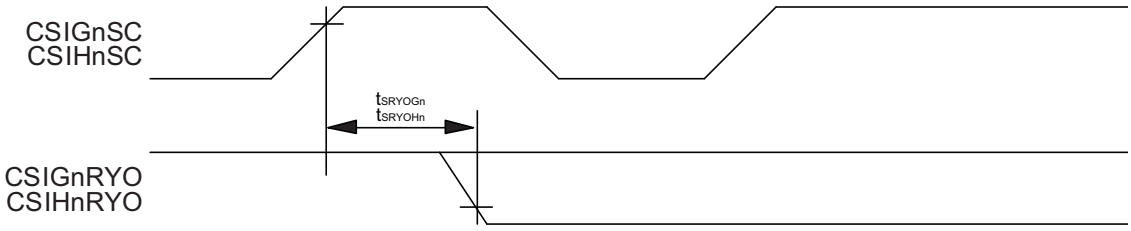


RYO

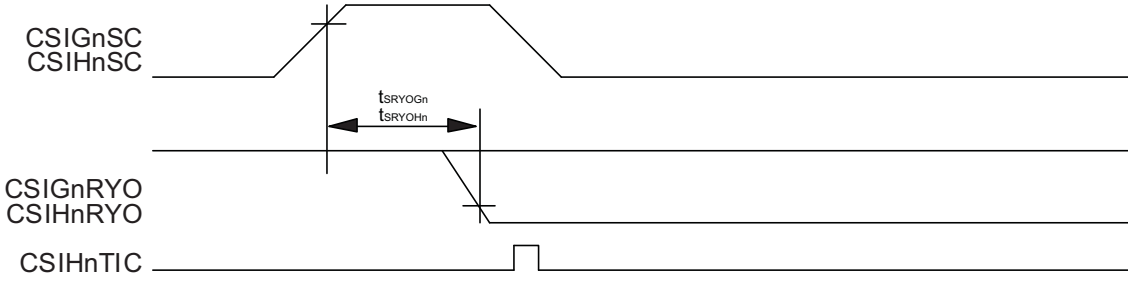
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/0)



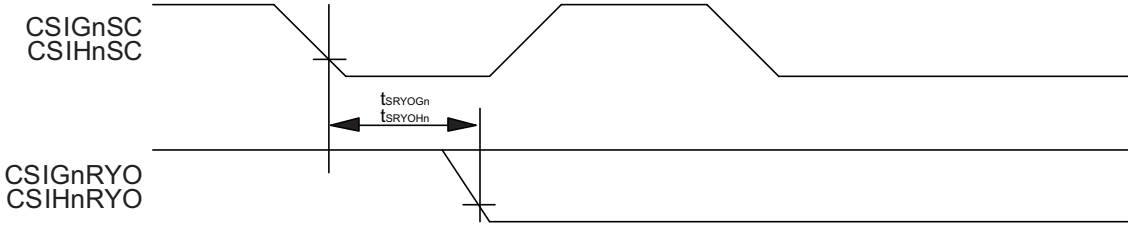
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/1)



CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/0)

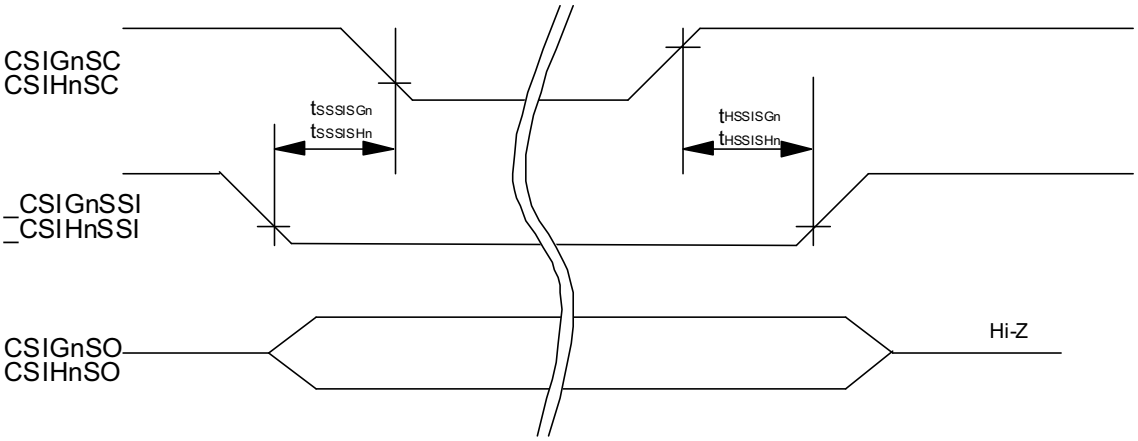


CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/1)
CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/1)

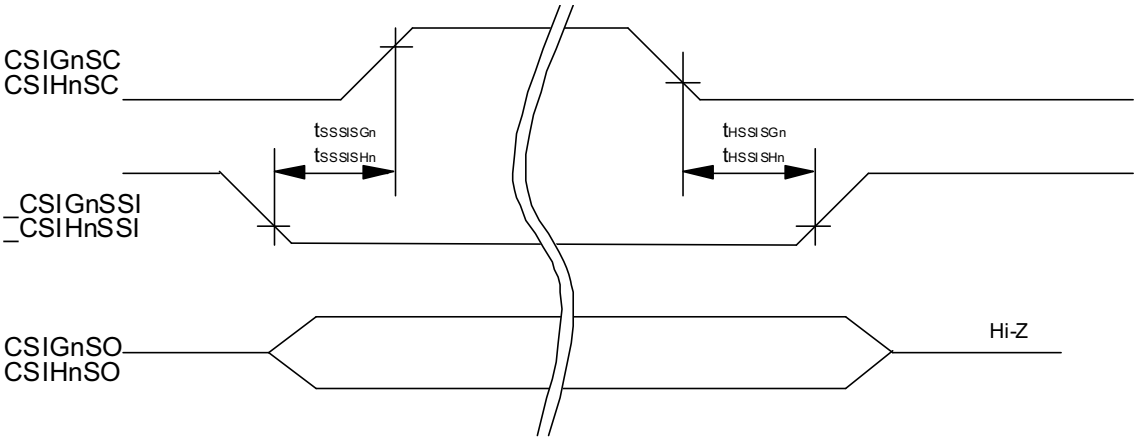


SSI:

CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 0/0 or 1/1)
CSIH (CSIHnCTL1 : CSIHnSSE=1, CSIHnCFGm : CSIHnCKPm / CSIHnCFGm : CHIHnDAPm = 0/0 or 1/1)



CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 1/0 or 0/1) n=0, 4
CSIH (CSIHnCTL1 : CSIHnSSE=1, CSIHnCFGm : CSIHnCKPm / CSIHnCFGm : CHIHnDAPm = 1/0 or 0/1)

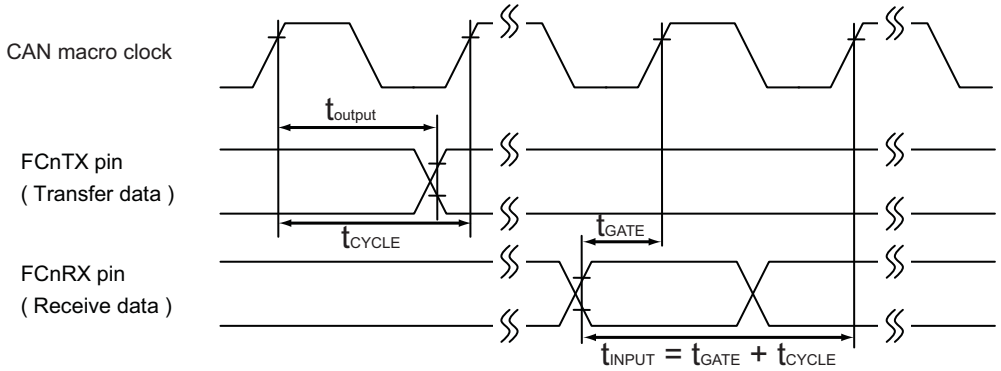


7.9 UART timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	1.5	Mbps

7.10 FCN timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	1	Mbps
Internal delay time	tINTDEL		-	-	37.5	ns
CAN Node delay time	tNODE	tCYCLE = 62.5ns	-	-	100	ns



CAN node delay time (t_{NODE}) = INPUT delay time (t_{input}) + Output delay time (t_{output})
Internal delay time (t_{INTDEL}) = Internal gate delay time (t_{GATE}) + Output delay time (t_{output})

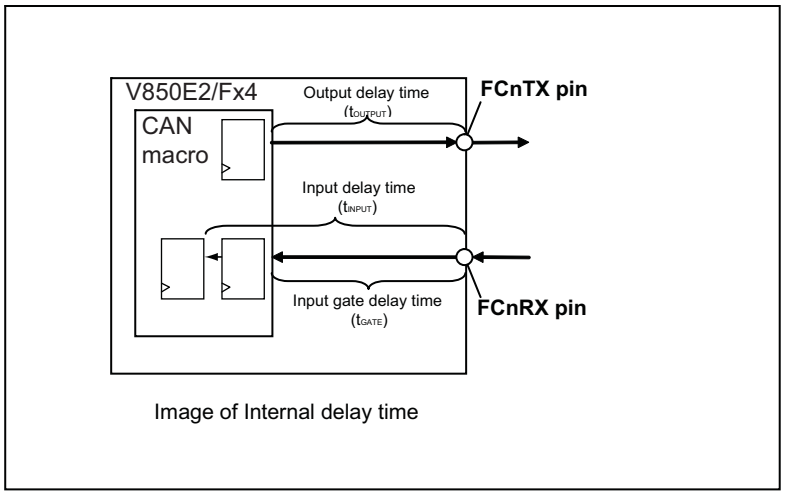
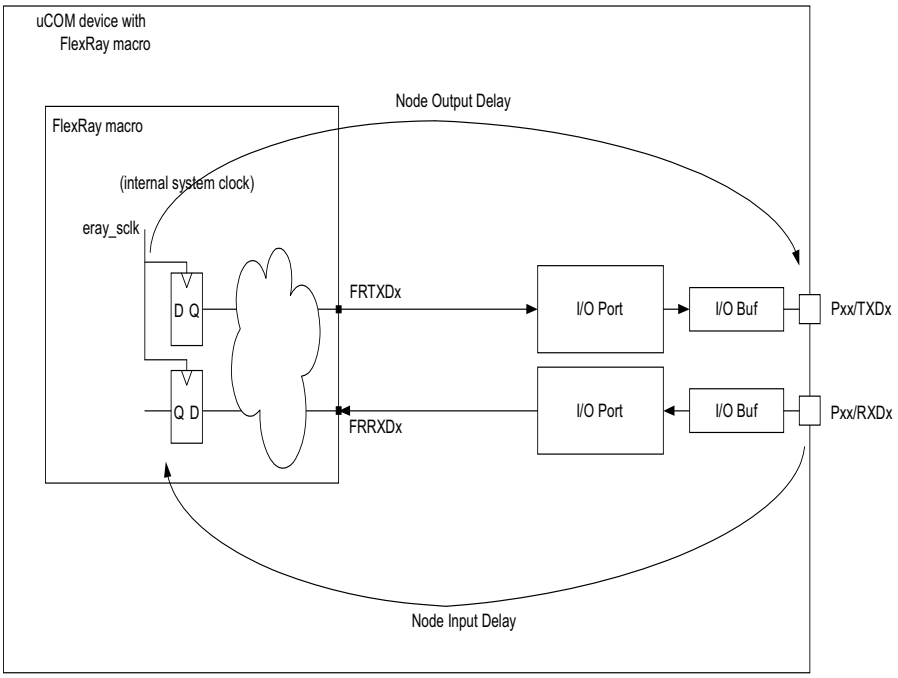
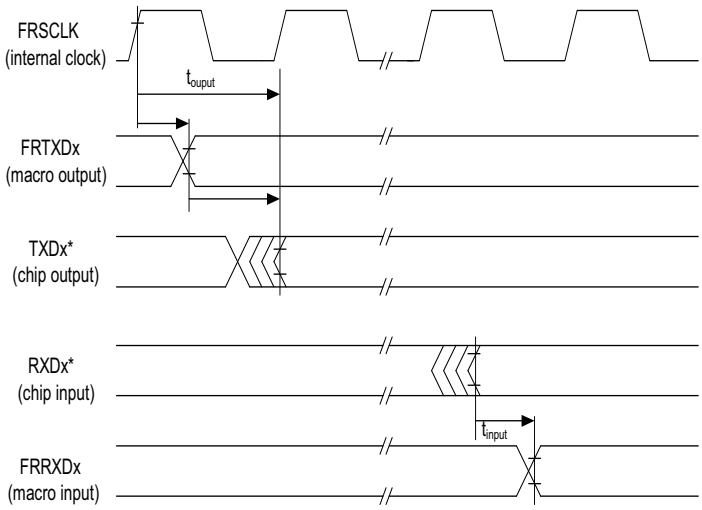


Image of Internal delay time

7.11 FlexRay timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	10	Mbps
Node Output Delay	tOUTPUT	FLX0TXDA, FLX0TXDB,	-	-	25	ns
		FLX0TXENA, FLX0TXENB	-	-		
Node Input Delay	tINPUT	FLX0RXDA, FLX0RXDB	-	-	10	ns





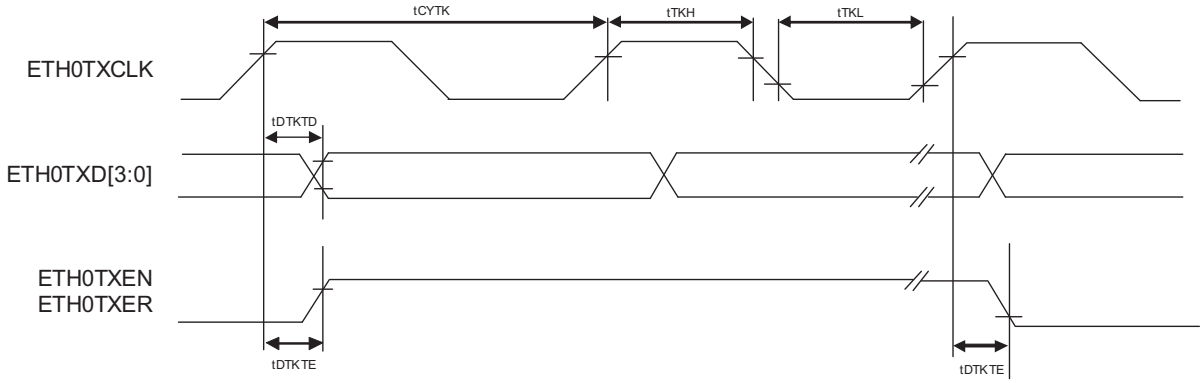
Port	Name	Condition	Ratings			Unit
			Min	Typ	Max	
FLX0TXENA FLX0TXENB	$dTxEN_{RISE-FALL}$	Cload=25pF, measured at 20-80% E1VDD	-	-	9	ns
	dCCTxEN01		-	-	25	ns
	dCCTxEN10		-	-	25	ns
FLX0TXDA FLX0TXDB	dCCTxAsym	measured at 50% E1VDD	-	-	2.45	ns
	dCCTxDRISE25 + dCCTxDFALL25	Cload=25pF, measured at 20-80% E1VDD	-	-	9	ns
		Cload=10pF, measured at 20-80% E1VDD at the end of a 50ohm, 1ns microstripline	-	-	9	ns
	dCCTxD01	-	-	-	25	ns
	dCCTxD10	-	-	-	25	ns
FLX0RXDA FLX0RXDB	dCCRxAsmAccept	measured at 50% of E1VDD Input signal: Cload=25pF, 6.5ns (20-80% E1VDD)	-	-	5.5	ns
	C_CCRxD	-	-	-	10	pf
	uLogic_1	-	35	-	70	%
	uLogic_0	-	30	-	65	%
	dCCRxD01	-	-	-	10	ns
	dCCRxD10	-	-	-	10	ns

7.12 Ethernet timing (MII interface)

7.12.1 Transmission interface

(CL = 30pF)

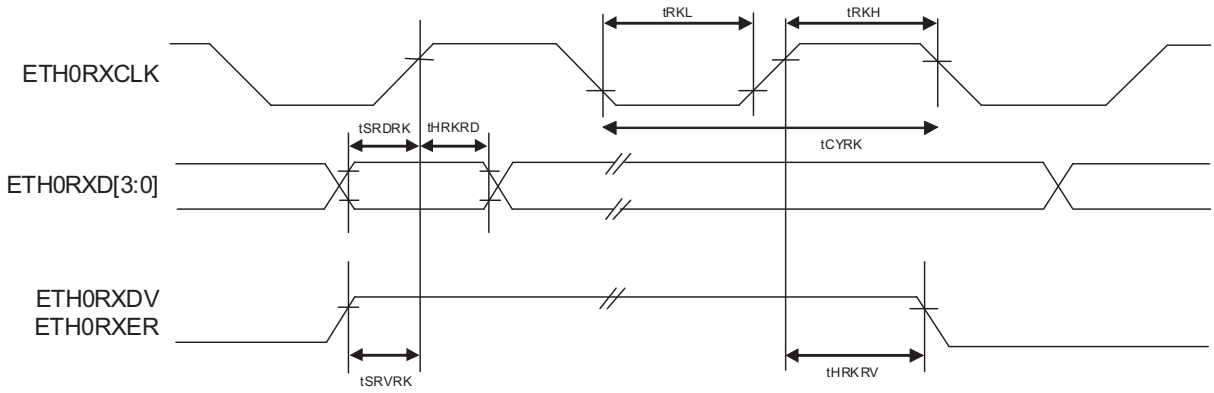
Item	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ETH0TXD[3:0] delay vs ETH0TXCLK(r)	tDTKTD		0	-	25	ns
ETH0TXEN, ETH0TXER delay vs ETH0TXCLK(r)	tDTKTE		0	-	25	ns
ETH0TXCLK clock period	tCYTK		40	-	-	ns
ETH0TXCLK high level width	tTKH		0.4·tCYTK	-	0.6·tCYTK	ns
ETH0TXCLK low level width	tTKL		0.4·tCYTK	-	0.6·tCYTK	ns



7.12.2 Reception interface

(CL=30pF)

Item	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ETH0RXD[3:0] hold time vs ETH0RXCLK(r)	tHRKRD		5	-	-	ns
ETH0RXD[3:0] setup time vs ETH0RXCLK(r)	tSRDRK		5	-	-	ns
ETH0RXER, ETH0RXDV hold time vs ETH0RXCLK(r)	tHRKRV		5	-	-	ns
ETH0RXER, ETH0RXDV setup time vs ETH0RXCLK(r)	tSRVRK		5	-	-	ns
ETH0RXCLK clock period	tCYRK		40	-	-	ns
ETH0RXCLK high level width	tRKH		0.4·tCYRK	-	0.6·tCYRK	ns
ETH0RXCLK low level width	tRKL		0.4·tCYRK	-	0.6·tCYRK	ns



Management Interface

(CL = 30pF)

Item	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ETH0MDC clock period	tCYMDC		400	-	-	ns
ETH0MDO delay vs ETH0MDC(r)	tDMCMD		0	-	300	ns
ETH0MDI setup time vs ETH0MDC(r)	tSMDMC		50	-	-	ns
ETH0MDI hold time vs ETH0MDC(r)	tHMCMD		50	-	-	ns

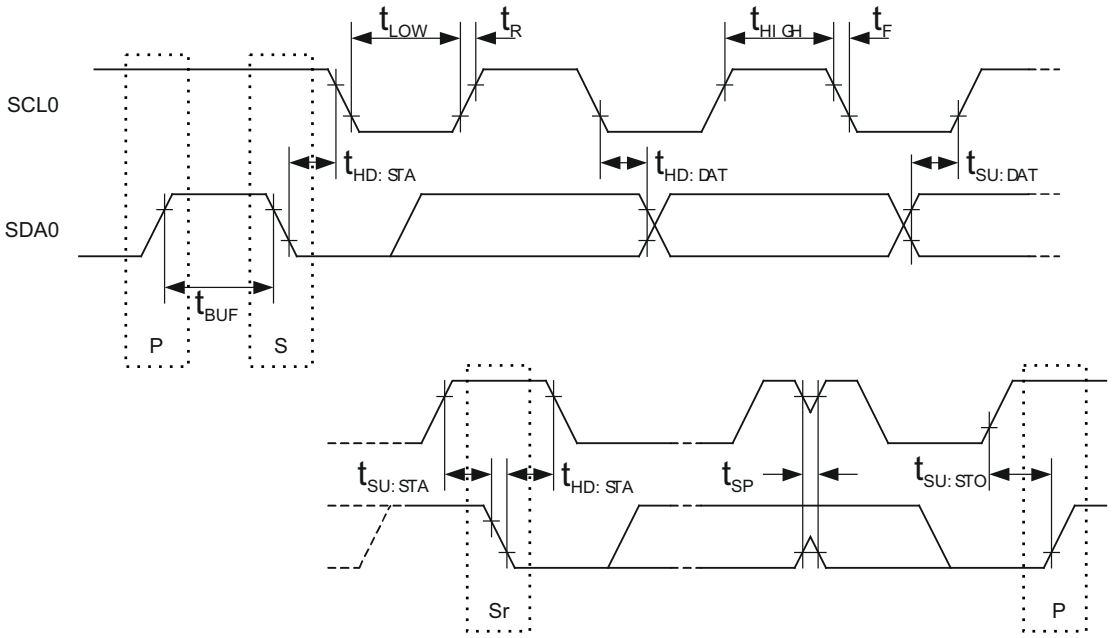
7.13 IIC timing

Table 7-7 Normal mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0		100	kHz
Bus free time (between stop condition and start condition)	tBUF		4.7	-	-	µs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	tHD:STA		4	-	-	µs
SCL clock low state hold time	tLOW		4.7	-	-	µs
SCL clock high state hold time	tHIGH		4	-	-	µs
Setup time for start/restart condition	tSU:STA		4.7	-	-	µs
Data hold time	tHD:DAT	CBUS compatible	5	-	-	µs
		IIC bus	0	-	-	µs
Data setup time	tSU:DAT		250	-	-	ns
Rising transition time of SDA or SCL	tR		-	-	1000	ns
Falling transition time of SDA or SCL	tF		-	-	300	ns
Setup time of stop condition	tSU:STO		4	-	-	µs
Bus capacitance	Cb		-	-	400	pF

Table 7-8 Fast mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0	-	400	kHz
Bus free time (between stop condition and start condition)	tBUF		1.3	-	-	µs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	tHD:STA		0.6	-	-	µs
SCL clock low state hold time	tLOW		1.3	-	-	µs
SCL clock high state hold time	tHIGH		0.6	-	-	µs
Setup time for start/restart condition	tSU:STA		0.6	-	-	µs
Data hold time	tHD:DAT	IIC bus	0	-	0.9	µs
Data setup time	tSU:DAT		100	-	-	ns
Rising transition time of SDA or SCL	tR		20+0.1Cb	-	300	ns
Falling transition time of SDA or SCL	tF		20+0.1Cb	-	300	ns
Setup time of stop condition	tSU:STO		0.6	-	-	µs
Noise elimination width	tSP		0	-	50	ns
Bus capacitance	Cb		-	-	400	pF



Notes 1. P: Stop condition

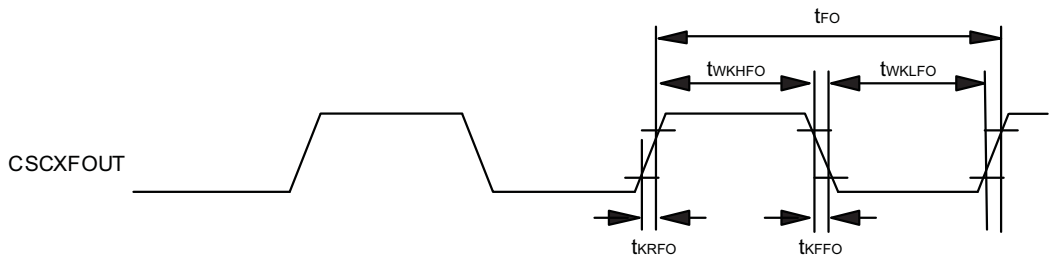
Notes 1. S: Start condition

Notes 1. Sr: Restart condition

7.14 Frequency Output Function (FOUT)

Table 7-9 Frequency Output Function (FOUT)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
CSCXFOUTP output cycle	tFO		50	-	-	ns
CSCXFOUTP high level width	tWKHFO		tFOUT / 2 - 10	-	-	ns
CSCXFOUTP low level width	tWKLFO		tFOUT / 2 - 10	-	-	ns
CSCXFOUTP rise time	tKRFO		-	-	10	ns
CSCXFOUTP fall time	tKFFO		-	-	10	ns

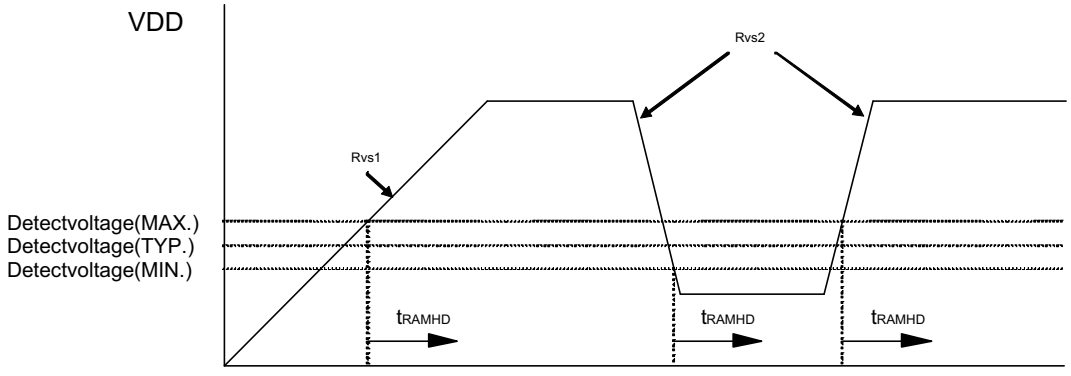


7.15 VLVI characteristics

Table 7-10 VLVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VRAMHF		1.8	1.9	2.0	V
Voltage slope1	Rvs1		0.18	-	1800	V/ms
Voltage slope2	Rvs2		0.0018	-	1800	V/ms
Response time[a]	tRAMHD		-	-	2	ms

a) From detection voltage to setting of VLVF bit (VLVF.bit0)



Note VDD: REG0VDD

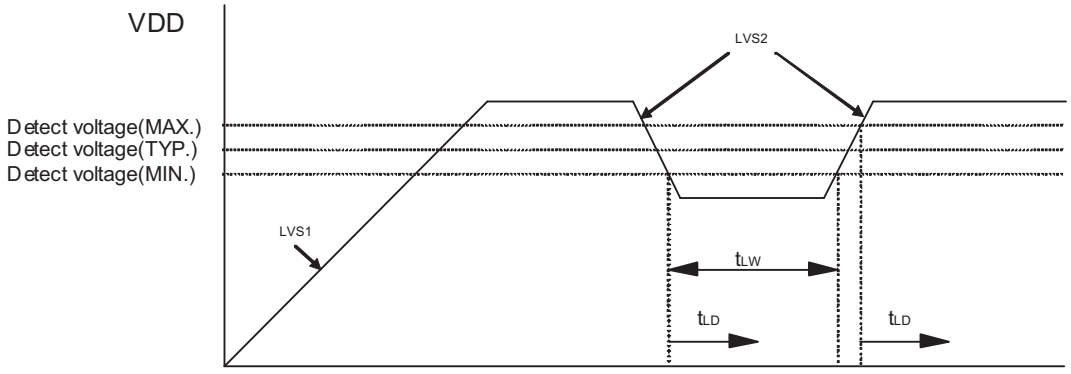
7.16 Voltage comparator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VCMP current	IVCMP		-	200	300	µA
Threshould voltage (rise)	VCMPR		1.745	1.780	1.815	V
Threshould voltage (fall)	VCMPF		1.645	1.680	1.715	V
Voltage slope	VCVS		-	-	50	mV/µs
Detection time	tVCMPD		-	-	2	µs
Stabilization time	tVCMPST	VCMP operation readyness after				

7.17 LVI characteristics

Table 7-11 LVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VLVI0	LVICNT.LVICNT[2:0]=001_B	3.9	4.0	4.1	V
	VLVI1	LVICNT.LVICNT[2:0]=010_B	3.6	3.7	3.8	V
	VLVI2	LVICNT.LVICNT[2:0]=011_B	3.4	3.5	3.6	V
Voltage slope1	LVS1		0.18	-	1800	V/ms
Voltage slope2	LVS2		0.0018	-	1800	V/ms
Response time	tLD		-	-	2.0	ms
VDD minimum width	tLW		2	-	-	ms
Stabilization time	tLVIST	LVICNT0,1 is set to 1, then LVI is ready to operate	-	-	350	µs



7.18 A/D Converter characteristics

7.18.1 12bit A/D (for ADC channels without S/H functionality)

Table 7-12 12bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RESn		12	12	12	bit
Total conversion time	TCONn		1.5	-	10	µs
Overall error[a]	TOEn		-	-	±6.0	LSB
Non-liniarity error[a]	ILEn		-	-	±2.5	LSB
Differencial liniarity error[a]	DLEn		-	-	±1.5	LSB
Zero scale error[a]	ZSEn		-	-	±5.0	LSB
Full scale error[a]	FSEn		-	-	±5.0	LSB
Analog input voltage[a]	VAIN		AnVREFM		AnVREFP	V
Power on stabilization time[b]			-	-	1	µs
AnVDD current	AIDDn	ADAnBPC=0, withDiagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDDnPD	Power down	-	1	-	µA
AnVREFP current	AIREFn		-	650	-	µA
Conversion result by Diagnosis function[c]	TESHn	AnVDD was converted	4015	-	4095	LSB
	TESHLn3	2/3 AnVDD was converted	2691	2731	2771	LSB
	TESHLn2	1/2 AnVDD was converted	2018	2048	2078	LSB
	TESHLn1	1/3 AnVDD was converted	1325	1365	1405	LSB
	TESLn	AGND was converted	0	-	80	LSB

a) The specification does not include the quantization error.
b) 'Power on' refers to
- setting ADCAnGPS = 1
c) The values given do not include influence of injected current

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

7.18.2 12bit A/D (For channel ADCA0I0-5 when the S/H function is not used)

Table 7-13 12bit A/D (When channel Sample & Hold function is not used)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0SN		12	12	12	bit
Total conversion time	TCON0SN		1.5	-	10	µs
Overall error[a]	TOE0SN		-	-	±6.0	LSB
Non-liniarity error[a]	ILE0SN		-	-	±2.5	LSB
Differencial liniarity error[a]	DLE0SN		-	-	±1.5	LSB
Zero scale error[a]	ZSE0SN		-	-	±5.0	LSB
Full scale error[a]	FSE0SN		-	-	±5.0	LSB
Analog input voltage[a]	VAIN0SN		A0VREFM	-	A0VREFP	V
Power on stabilization time[b]			-	-	1	µs
A0VDD current	AIDD0SN	ADA0BPC=0, withDiagnosis function	-	4.0	6.3	mA
		ADA0BPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADA0BPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADA0BPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDD0SNPD	Power down	-	1	-	µA
A0VREFP current	AIREF0SN		-	650	-	µA
Conversion result by Diagnosis function[c]	TESH0SN	A0VDD was converted	4015	-	4095	LSB
	TESHL0SN3	2/3 A0VDD was converted	2691	2731	2771	LSB
	TESHL0SN2	1/2 A0VDD was converted	2018	2048	2078	LSB
	TESHL0SN1	1/3 A0VDD was converted	1325	1365	1405	LSB
	TESL0SN	AGND was converted	0	-	80	LSB

a) The specification does not include the quantization error.

b) 'Power on' refers to
- setting ADCAnGPS = 1

c) The values given do not include influence of injected current

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

7.18.3 12bit A/D (When channel S/H function is used)

Table 7-14 12bit A/D (When channel Sample & Hold function is used [ADCA0I0 to ADCA0I5])

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0S		12	12	12	bit
Total conversion time	TCON0SN		1.8	-	12	µs
Sample & Hold time			50	-	-	µs
Overall error[a]	TOE0S		-	-	±8.0	LSB
Non-liniarity error[a]	ILE0S		-	-	±4.0	LSB
Differencial liniarity error[a]	DLE0S		-	-	±2.5	LSB
Zero scale error[a]	ZSE0S		-	-	±6.0	LSB
Full scale error[a]	FSE0S		-	-	±6.0	LSB
Analog input voltage	VAIN0S		0.2	-	A0VREFP-0.2	V
Power on stabilization time[b]			-	-	1	µs
A0VDD current	AIDD0S	withDiagnosis function	-	Note3	22.1	mA
		w/o Diagnosis function	-	Note3	24.0	mA
	AIDD0SPD	Power down	-	1	-	µA
A0VREFP current	AIREF0S		-	650	-	µA
Conversion result by Diagnosis function[c]	TESHLS3	2/3 A0VDD was converted	2689	2731	2773	LSB
	TESHLS2	1/2 A0VDD was converted	2016	2048	2080	LSB
	TESHLS1	1/3 A0VDD was converted	1323	1365	1407	LSB

a) The specification does not include the quantization error.
b) 'Power on' refers to
- setting ADCAnGPS = 1
c) The values given do not include influence of injected current

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.
3. AIDDn + 1.72mA x (number of channels used with S/H)

7.18.4 10bit A/D (for ADC channels without S/H functionality)

Table 7-15 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RESn		10	10	10	bit
Total conversion time	TCONn		1.5		10	µs
Overall error[a]	TOEn	Excluding quantization error	-	-	±2.0	LSB
Non-liniarity error[a]	ILEn		-	-	±1.5	LSB
Differencial liniarity error[a]	DLEn		-	-	±1.0	LSB
Zero scale error[a]	ZSEn		-	-	±1.5	LSB
Full scale error[a]	FSEn		-	-	±1.5	LSB
Analog input voltage[a]	VAIN		AnVREFM		AnVREFP	V
Power on stabilization time[b]			-		1	µs
AnVDD current	AIDDn	ADAnBPC=0, withDiagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDDnPD	Power down	-	1	-	µA
AnVREFP current	AIREFn		-	500	-	µA
Conversion result by Diagnosis function[c]	TESHn	AnVDD was converted	1003		1023	LSB
	TESHLn3	2/3 AnVDD was converted	673	683	693	LSB
	TESHLn2	1/2 AnVDD was converted	504	512	520	LSB
	TESHLn1	1/3 AnVDD was converted	331	341	351	LSB
	TESLn	AGND was converted	0		20	LSB

a) The specification does not include the quantization error.
b) 'Power on' refers to
- setting ADCAnGPS = 1
c) The values given do not include influence of injected current

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

7.18.5 10bit A/D (For channel ADCA0I0-5 when the S/H function is not used)

Table 7-16 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0SN		10	10	10	bit
Total conversion time	TCON0SN		1.5		10	µs
Overall error[a]	TOE0SN		-	-	±2.0	LSB
Non-liniarity error[a]	ILE0SN		-	-	±1.5	LSB
Differencial liniarity error[a]	DLE0SN		-	-	±1.0	LSB
Zero scale error[a]	ZSE0SN		-	-	±1.5	LSB
Full scale error[a]	FSE0SN		-	-	±1.5	LSB
Analog input voltage[a]	VAIN0SN		AnVREFM		AnVREFP	V
Power on stabilization time[b]			-	-	1	µs
AnVDD current	AIDD0SN	ADAnBPC=0, withDiagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDD0SNPD	Power down	-	1	-	µA
AnVREFP current	AIREF0SN		-	500	-	µA
Conversion result by Diagnosis function[c]	TESH0SN	AnVDD was converted	1003	-	1023	LSB
	TESHL0SN3	2/3 AnVDD was converted	673	683	693	LSB
	TESHL0SN2	1/2 AnVDD was converted	504	512	520	LSB
	TESHL0SN1	1/3 AnVDD was converted	331	341	351	LSB
	TESL0SN	AGND was converted	0	-	20	LSB

a) The specification does not include the quantization error.
b) 'Power on' refers to
- setting ADCAnGPS = 1
c) The values given do not include influence of injected current

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.
3. AIDDn + 1.72mA x (number of channels used with S/H)

7.18.6 10bit A/D (When channel S/H function is used)

Table 7-17 10 bit A/D

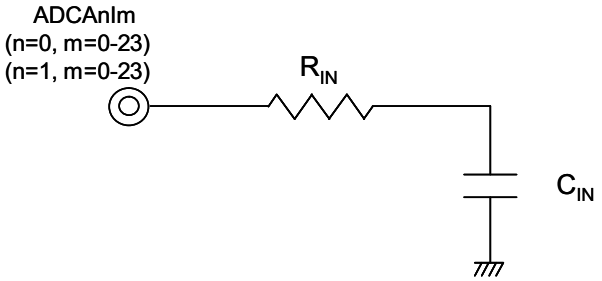
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0S		10	10	10	bit
Total conversion time	TCON0S		1.84	-	12.2	µs
Sample & Hold time			50	-	-	µs
Overall error[a]	TOE0S		-	-	±2.5	LSB
Non-liniarity error[a]	ILE0S		-	-	±2.0	LSB
Differencial liniarity error[a]	DLE0S		-	-	±1.5	LSB
Zero scale error[a]	ZSE0S		-	-	±2.0	LSB
Full scale error[a]	FSE0S		-	-	±2.0	LSB
Analog input voltage[a]	VAIN0S		0.2	-	A0VREFP-0.2	V
Power on stabilization time[b]			-	-	1	µs
AnVDD current	AIDD0S	ADAnBPC=1, with Diagnosis function	-	[c]	22.1	mA
		ADAnBPC=1, w/o Diagnosis function	-	[c]	24.0	mA
	AIDD0SPD	Power down	-	1	-	µA
AnVREFP current	AIREF0S		-	500	-	µA
Conversion result by Diagnosis function[d]	TESHL0S3	2/3 AnVDD was converted	672	683	694	LSB
	TESHL0S2	1/2 AnVDD was converted	503	512	521	LSB
	TESHL0S1	1/3 AnVDD was converted	330	341	352	LSB

a) The specification does not include the quantization error.
b) 'Power on' refers to
- setting ADCAnGPS = 1
c) AIDDn x 1.72 x the number of used channels with Sample & Hold
d) The values given do not include influence of injected current

Notes 1. n: Number of macro instances. Refer to the User Manual for the detailed specification.

2. m: Number of channels. Refer to the User Manual for the detailed specification.

7.18.7 Equivalent circuit



Terminals	Condition		R_{IN}[kΩ]	C_{IN}[pF]
ADCA0I0-ADCA0I5	When S&H is used		0.7	3.6
	When S&H is not used	ADA0BPC=0	1.6	12.6
		ADA0BPC=1	1.5	7.1
ADCA0I6-ADCA0I23	ADA0BPC=0		1.2	11.9
	ADA0BPC=1		1.1	7.1
ADCA1I0-ADCA1I23	ADA0BPC=0		1.2	11.9
	ADA0BPC=1		1.1	7.1

Caution These specifications are not tested in outgoing inspection. Therefore R_{IN} and C_{IN} values are not guaranteed and are reference values only.
Additionally these values are specified as maximum values.

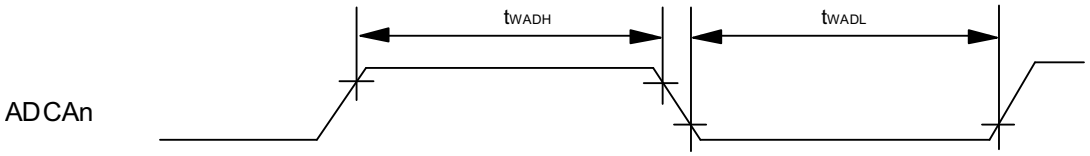
7.18.8 ADTRG timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ADCAnTRGm input High level width	tWADH	with digital noise filter	a	-	-	ns
		without digital noise filter	b	-	-	ns
ADCAnTRGm input Low level width	tWADL	with digital noise filter	a	-	-	ns
		without digital noise filter	b	-	-	ns

a) 2, 3, 4 or 5 x Tsamp + 20 (Tsamp shows sampling period specified in noise filter).
More than 1 PCLK width of ADC macro must be kept regarding DNF pass through pulse width.

b) 1 × tSYNC+20 (tSYNC: 1 PCLK of ADC macro)

Notes
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
2. m: Number of channels. Refer to the User Manual for the detailed specification.

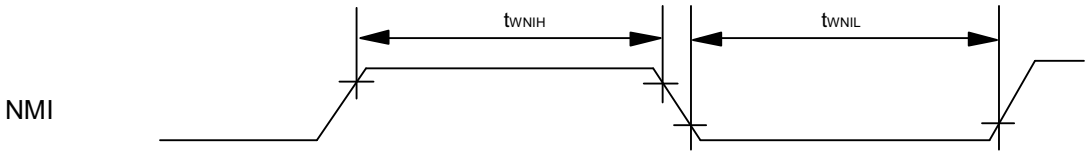


7.19 Key Return

Table 7-18

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
KRn input High level width	tWKRH		300	-	-	ns
KRn input Low level width	tWKRL		300	-	-	ns

Note n: Number of instances. Refer to the User Manual for the detailed specification.



Chapter 8 Memory specification

8.1 Code flash specification

Table 8-1 Code flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes[a]	CWRT	Data retention 20 years	-	-	100	times
Programming Temperature	tPRG	(A) grade products	-40	-	85	°C
		(A1) grade products	-40	-	110	°C

a) Please contact RENESAS sales office regarding specification other than the above.

8.2 Data flash specification

Table 8-2 Data flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes[a]	DWRT1	Data retention 20 years	-	-	1000	times
	DWRT2	Data retention 15 years	-	-	5000	times
	DWRT3	Data retention 5 years	-	-	15000	times
Programming Temperature	tPRG	(A) grade products	-40	-	85	°C
		(A1) grade products	-40	-	110	°C

a) Please contact RENESAS sales office regarding specification other than the above.

8.3 Serial write operation specification

Serial write operation

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 setup time	tDR		1	-	-	ms
RESET release	tPR		2	-	-	ms
FLMD0 pulse input start	tRP		-	100	-	ms
FLMD0 low/high level width	tPW		10	-	100	µs
FLMD0 raise time	tR		-	-	20	ns
FLMD0 fall time	tF		-	-	20	ns
Programming time		per 128 bit	-	-	50	µs
Erase time		per 4KB	-	-	54	ms

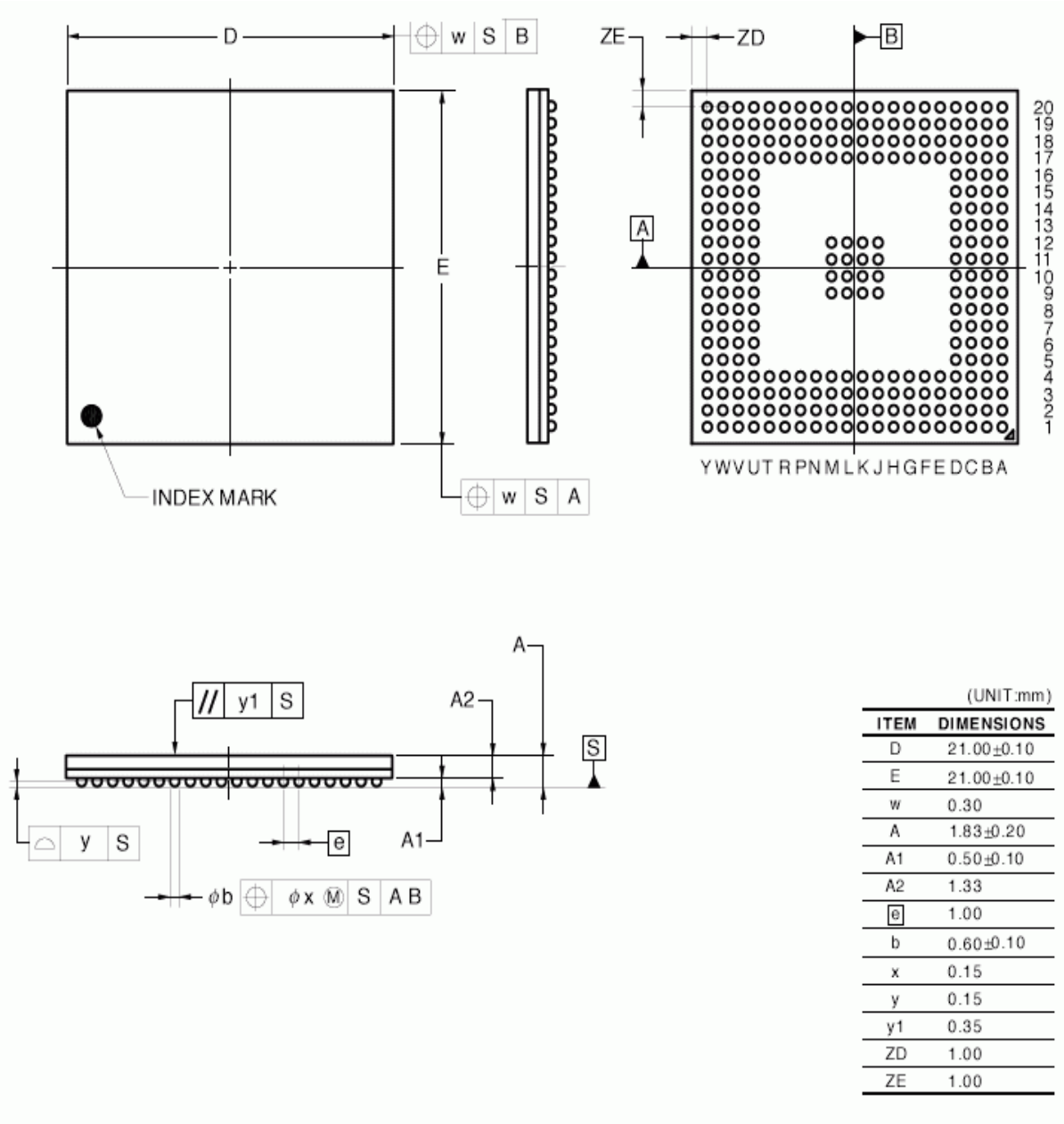
Chapter 9 Pinning and package specification

9.1 Pinning specification PBGA 272

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	E1VSS	FLMD0	P0_15	P0_10	P0_7	P0_4	P0_1	XT1	XT2	X1	JP0_5	JP0_2	VCPC0IN	REG0VSS	_RESET	P24_3	P24_0	P21_3	P27_5	B0VSS	A
B	P4_10	P4_11	P0_14	P0_11	P0_8	P0_5	P0_2	P0_0	OSCVSS	X2	JP0_4	JP0_1	VCPC1IN	REG0C	PWGD	P24_2	P21_2	P21_4	B0VSS	P27_2	B
C	P4_8	P4_9	FVDD	P0_13	P0_12	P0_9	P0_6	P0_3	OSCVDD	E0VSS	JP0_3	JP0_0	WAKE	REG0VDD	P24_4	P24_1	CVDD	B0VSS	P27_1	P27_0	C
D	P4_5	P4_6	P4_7	E0VSS	E0VSS	E0VSS	E0VDD	E0VSS	E0VSS	E0VSS	E0VSS	E0VDD	E0VSS	E0VSS	CVSS	P24_5	B0VSS	P25_15	P25_14	P25_13	D
E	P4_2	P4_3	P4_4	E1VSS													B0VSS	P25_12	P25_11	P25_10	E
F	P3_12	P4_0	P4_1	E1VSS													B0VDD	P25_9	P25_8	P25_7	F
G	P3_9	P3_10	P3_11	E1VDD													B0VSS	P25_6	P25_5	P25_4	G
H	P3_6	P3_7	P3_8	E1VSS													B0VSS	P25_3	P25_2	P25_1	H
J	P3_3	P3_4	P3_5	E1VSS					E1VSS	B0VSS	B0VSS	B0VSS					B0VDD	P25_0	P24_7	P24_6	J
K	P2_3	P3_1	P3_2	E1VDD					E1VSS	E1VSS	B0VSS	B0VSS					B0VSS	P21_1	P21_0	P21_11	K
L	P2_2	P1_15	P3_0	E1VSS					E1VSS	E1VSS	B0VSS	B0VSS					B0VSS	P21_10	P21_9	P21_8	L
M	P1_13	P1_12	P1_14	E1VDD					E1VSS	E1VSS	E1VSS	B0VSS					B0VDD	P13_2	P13_3	P21_7	M
N	P1_10	P1_9	P1_11	E1VSS													B0VSS	P12_15	P13_0	P13_1	N
P	P1_7	P1_6	P1_8	E1VSS													B0VSS	P12_12	P12_13	P12_14	P
R	P1_4	P1_3	P1_5	E1VSS													B0VSS	P12_9	P12_10	P12_11	R
T	P1_1	P11_7	P1_2	E1VSS													B0VSS	P12_6	P12_7	P12_8	T
U	P11_5	P11_4	P11_6	E1VSS	E1VSS	E1VSS	E1VSS	E1VSS	E1VSS	E1VSS	E1VDD	B0VSS	B0VDD	B0VSS	B0VSS	B0VSS	B0VSS	A1VSS	P12_4	P12_5	U
V	P11_2	P11_1	P11_3	A0VSS	P10_8	P10_11	P10_14	ADCA0I1 (P10_1)	CVSS	CVDD	CVDD	REG1VDD	P24_10	P21_6	P24_14	P13_5	P12_0	B0VSS	AVREFP1	AVREFM1	V
W	P11_0	E1VSS	AVREFP0	P10_6	P10_9	P10_12	P10_15	ADCA0I2 (P10_2)	ADCA0I4 (P10_4)	N.C.	REG1VSS	P27_4	P24_9	P21_5	P24_13	P13_4	P13_7	P12_2	B0VSS	A1VDD	W
Y	E1VSS	A0VDD	AVREFM0	P10_7	P10_10	P10_13	ADCA0I0 (P10_0)	ADCA0I3 (P10_3)	ADCA0I5 (P10_5)	P2_0	P2_1	PTCTL1	P24_8	P24_11	P24_12	P24_15	P13_6	P12_1	P12_3	B0VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

V850E2/FL4-H

9.2 Package specification PBGA 272



(UNIT:mm)

ITEM	DIMENSIONS
D	21.00±0.10
E	21.00±0.10
w	0.30
A	1.83±0.20
A1	0.50±0.10
A2	1.33
e	1.00
b	0.60±0.10
x	0.15
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

Revision History

Version	Date	Document number	Description
1.0	2013-05-24	R01DS0144ED0100	Initial release Document was EASE-DS-0032-1.2 Changes: - Added FLMD0 / FLMD1 resistor values - Corrected timing diagram for wake-signal (chapter 3.5.5 Condition 4) - Updated Power Supply Currents (chapter 5.1)