Ordering number : ENA2061

# LV5680NPVC

**Monolithic Linear IC** 

# Multi-Power Supply System IC for Car Audio Systems



http://onsemi.com

#### Overview

The LV5680NPVC is a multi-power supply system IC that provides four regulator outputs and two high side switches as well as a number of protection functions including overcurrent protection, overvoltage protection and overheat protection. It is an optimal power supply IC for car audio and car entertainment systems and similar products.

#### **Features**

• Four regulator output systems

For microcontroller: 5.0V output voltage, 200mA maximum output current

For CD drive: 8.0V output voltage, 1300mA maximum output current

For illumination: 8 to 12V output voltage (output can be set with external resistors), 300mA maximum output

For audio systems: 8 to 9V output voltage (output voltage can be set with external resistors), 300mA maximum output current

• Two V<sub>CC</sub>-linked high side switch systems

EXT: 350mA maximum output current, 0.5V voltage difference between input and output.

ANT: 300mA maximum output current, 0.5V voltage difference between input and output.

• Two V<sub>DD</sub> 5V-linked high side switch systems

SW5V: 200mA maximum output current, 0.2V voltage difference between input and output.

ACC (accessory voltage detection output): 100mA maximum output current, 0.2V voltage difference between input and output.

- Overcurrent protection function
- Overvoltage protection function, typ 21V (excluding V<sub>DD</sub> 5V output)
- Overheat protection function, typ 175°C
- On-chip accessory voltage detection circuit
- P-channel LDMOS used for power output block

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

#### **Specifications**

#### **Absolute Maximum Ratings** at Ta = 25°C

Parameter	Conditions	Conditions	Conditions		Unit
Supply voltage	V <sub>CC</sub> max			36	V
Peak supply voltage	V <sub>CC</sub> peak	See below for the waveform applied.		50	V
Allowable Power dissipation	Pd max	Independent IC	Ta ≤ 25°C	1.5	W
		Al heat sink *		5.6	W
		With an infinity heat sink		32.5	W
Junction temperature	Tj max			150	°C
Operating ambient temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

<sup>\* :</sup> When the Aluminum heat sink (50mm  $\times$  50mm  $\times$  1.5mm) is used

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### Allowable Operating range at $Ta = 25^{\circ}C$

Parameter	Conditions	Ratings	Unit
Operating supply voltage 1	V <sub>DD</sub> output, SW output, ACC output	7.5 to 16	V
Operating supply voltage 2	ILM output at 10V	12 to 16	V
	ILM output at 8V	10 to 16	V
Operating supply voltage 3	Audio output at 9V	10 to 16	V
Operating supply voltage 4	CD output (CD output current = 1.3A)	10.5 to 16	V
	CD output (CD output current ≤ 1A)	10 to 16	V

#### **Electrical Characteristics** at $V_{CC} = 14.4V$ , $Ta = 25^{\circ}C(*6)$

Parameter	Symbol	Conditions		Ratings		Unit
Farameter	Symbol	Conditions	min	typ	max	Offic
Current drain	Icc	$V_{DD}$ no load, CTRL1/2 = $\lceil L/L \rfloor$ , ACC = 0V		400	800	μΑ
CTRL1 Input						
Low input voltage	V <sub>IL</sub> 1		0		0.5	>
M1 input voltage	V <sub>IM1</sub> 1		0.8	1.1	1.4	٧
M2 input voltage	V <sub>IM2</sub> 1		1.9	2.2	2.5	V
High input voltage	V <sub>IH</sub> 1		2.9	3.3	5.5	V
Input impedance	R <sub>IH</sub> 1		350	500	650	kΩ
CTRL2 Input						
Low input voltage	V <sub>IL</sub> 2		0		0.5	V
M input voltage	V <sub>IM</sub> 2		1.1	1.65	2.1	V
High input voltage	V <sub>IH</sub> 2		2.5	3.3	5.5	V
Input impedance	R <sub>IH</sub> 2		350	500	650	kΩ
V <sub>DD</sub> 5V Output *1		The V <sub>DD</sub> 5V output sup	plies the outp	ut currents of	SW 5V and	ACC 5V.
Output voltage 1	V <sub>O</sub> 1	I <sub>O</sub> 1 = 200mA, I <sub>O</sub> 7, I <sub>O</sub> 8 = 0A	4.75	5.0	5.25	V
Output voltage 2	V <sub>O</sub> 1'	I <sub>O</sub> 1 = 200mA, I <sub>O</sub> 7 = 200mA, I <sub>O</sub> 8 = 100mA	4.75	5.0	5.25	V
Output total current	Ito1	$V_{O}1 \ge 4.75V$ , $Ito1 = I_{O}1 + I_{O}7 + I_{O}8$	500			mA
Line regulation	ΔV <sub>OLN</sub> 1	7.5V < V <sub>CC</sub> < 16V, I <sub>O</sub> 1 = 200mA *2		30	90	mV
Load regulation	ΔV <sub>OLD</sub> 1	1mA < I <sub>O</sub> 1 < 200mA *2		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 1	I <sub>O</sub> 1 = 200mA *2		1.0	1.5	٧
Dropout voltage 2	V <sub>DROP</sub> 1'	I <sub>O</sub> 1 = 100mA *2		0.7	1.05	٧
Dropout voltage 3	V <sub>DROP</sub> 1"	$I_01+I_07+I_08 = 500$ mA		2.5	3.75	٧
Ripple rejection	R <sub>REJ</sub> 1	f = 120Hz, I <sub>O</sub> 1 = 200mA *2	40	50		dB
CD Output ; CTRL2 = [H]	•	•		<u>,                                    </u>		
Output voltage	V <sub>O</sub> 2	I <sub>O</sub> 2 = 1000mA	7.6	8.0	8.4	V
Output current	I <sub>O</sub> 2	V <sub>O</sub> 2 ≥ 7.6V	1300			mA
Line regulation	ΔV <sub>OLN</sub> 2	10.5V < V <sub>CC</sub> < 16V, I <sub>O</sub> 2 = 1000mA		50	100	mV

<sup>\*1 :</sup> The V<sub>DD</sub> 5V output also supplies the output currents of SW 5V and ACC 5V. Therefore, the current supply capability of the V<sub>DD</sub> 5V output and its other electrical characteristics are affected by the output statuses of SW 5V and ACC 5V.

Continued on next page.

<sup>\*2 :</sup> SW 5V and ACC 5V are not subject to a load.

0 . 1	c	11	
Continued	from	preceding	g nage

Parameter	Symbol	Conditions	ļ	Ratings		Unit
	-,		min	typ	max	
Load regulation	ΔV <sub>OLD</sub> 2	10mA < I <sub>O</sub> 2 < 1000mA		100	200	mV
Dropout voltage 1	V <sub>DROP</sub> 2	$I_{O}2 = 1000 \text{mA}$		1.0	1.5	V
Dropout voltage 2	V <sub>DROP</sub> 2'	$I_{O}2 = 500 \text{mA}$		0.5	0.75	V
Ripple rejection	R <sub>REJ</sub> 2	f = 120Hz, I <sub>O</sub> 2 = 1000mA	40	50		dB
AUDIO (8-9V) Output ; CTRL2 =	-[M]					
AUDIO_F pin voltage	V <sub>I</sub> 3		1.222	1.260	1.298	V
AUDIO_F pin inflow current	I <sub>IN</sub> 3		-1		1	μΑ
AUDIO output voltage 1	V <sub>O</sub> 3	$I_{O}3 = 200 \text{mA}, R2 = 30 \text{k}\Omega, R3 = 5.6 \text{k}\Omega *3$	7.65	8.0	8.35	V
AUDIO output voltage 2	V <sub>O</sub> 3'	$I_{O}3 = 200$ mA, R2 = $27$ k $\Omega$ , R3 = $4.7$ k $\Omega$ *3	8.13	8.5	8.87	V
AUDIO output voltage 3	V <sub>O</sub> 3"	$I_{O}3 = 200$ mA, R2 = 24k $\Omega$ , R3 = 3.9k $\Omega$ *3	8.6	9.0	9.4	V
AUDIO output current	IO3		300			mA
Line regulation	∆V <sub>OLN</sub> 3	10V < V <sub>CC</sub> < 16V, I <sub>O</sub> 3 = 200mA		30	90	mV
Load regulation	ΔV <sub>OLD</sub> 3	1mA < I <sub>O</sub> 3 < 200mA		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 3	I <sub>O</sub> 3 = 200mA		0.3	0.45	V
Dropout voltage 2	V <sub>DROP</sub> 3'	I <sub>O</sub> 3 = 100mA		0.15	0.23	V
Ripple rejection	R <sub>REJ</sub> 3	f = 120Hz, I <sub>O</sub> 3 = 200mA	40	50		dB
ILM (8-12V) Output ; CTRL1 =	M1]			<u> </u>		
ILM_F pin voltage	V <sub>I</sub> 4		1.222	1.260	1.298	V
ILM output voltage 1	V <sub>O</sub> 4	I <sub>O</sub> 4 = 200mA	11.4	12.0	12.6	V
ILM output voltage 2	V <sub>O</sub> 4'	I <sub>O</sub> 4 = 200mA, R1 = 270kΩ *4	8.5	10.0	11.5	V
ILM output voltage 3	V <sub>O</sub> 4"	I <sub>O</sub> 4 = 200mA, R1 = 100kΩ *4	6.8	8.0	9.2	V
ILM output current	I <sub>O</sub> 4	R1 = 270kΩ	300			mA
Line regulation	ΔV <sub>OLN</sub> 4	12V < V <sub>CC</sub> < 16V, I <sub>O</sub> 4 = 200mA, R1 = 270kΩ		30	90	mV
Load regulation	ΔV <sub>OLD</sub> 4	1mA < I <sub>O</sub> 4 < 200mA		70	150	mV
Dropout voltage 1	V <sub>DROP</sub> 4	I <sub>O</sub> 4 = 200mA		0.7	1.05	V
Dropout voltage 2	V <sub>DROP</sub> 4'	I <sub>O</sub> 4 = 100mA		0.35	0.53	V
Ripple rejection	R <sub>REJ</sub> 4	f = 120Hz, I <sub>O</sub> 4 = 200mA	40	50		dB
Remoto (EXT) ; CTRL1 = M2	1	1 2	1	I		
Output voltage	V <sub>O</sub> 5	I <sub>O</sub> 5 = 350mA	V <sub>CC</sub> -1.0	V <sub>CC</sub> -0.5		V
Output current	I <sub>O</sub> 5	V <sub>O</sub> 5 ≥ V <sub>CC</sub> -1.0	350			mA
ANT remoto ; CTRL1 = [H]			1	ı		
Output voltage	V <sub>O</sub> 6	I <sub>O</sub> 6 = 300mA	V <sub>CC</sub> -1.0	V <sub>CC</sub> -0.5		V
Output current	106	V <sub>O</sub> 6 ≥ V <sub>CC</sub> -1.0	300			mA
SW 5V Output ; CTRL2 = M			J I	J	<u> </u>	
Output voltage 1	V <sub>O</sub> 7	I <sub>O</sub> 7 = 1mA, I <sub>O</sub> 1, I <sub>O</sub> 8 = 0A *5	V <sub>O</sub> 1-0.25	V <sub>O</sub> 1		V
Output voltage 2	V <sub>O</sub> 7'	I <sub>O</sub> 7 = 200mA, I <sub>O</sub> 1, I <sub>O</sub> 8 = 0A *5	V <sub>O</sub> 1-0.45	V <sub>O</sub> 1-0.2		V
Output current	107	V <sub>O</sub> 7 ≥ 4.55	200			mA
ACC Detection ; ACC Integration	-	ı ~	<u> </u>	<u> </u>		
ACC detection voltage	V <sub>TH</sub> 8		2.8	3.0	3.2	V
Hysteresis width	V <sub>HIS</sub> 8		0.2	0.3	0.4	V
Input impedance	ZI8	(Pull-down resistance internal)	42	60	78	kΩ
ACC output voltage 1	V <sub>O</sub> 8	I <sub>O</sub> 8 = 0.5mA, I <sub>O</sub> 1, I <sub>O</sub> 7 = 0A *5	V <sub>O</sub> 1-0.25	V <sub>O</sub> 1	-	V
ACC output voltage 2	V08,	I <sub>O</sub> 8 = 100mA, I <sub>O</sub> 1, I <sub>O</sub> 7 = 0A *5	V <sub>O</sub> 1-0.45	V <sub>O</sub> 1-0.2		V
ACC output voltage	108	V <sub>O</sub> 8 ≥ 4.55	100	10. 3.2		mA
	.00	1 :0- =	100			, \

<sup>\*3 :</sup> When a component with a resistance accuracy of  $\pm 1\%$  is used

<sup>&</sup>lt;Reference> When a component with a resistance accuracy of  $\pm 0.5\%$  is used,  $V_O3$ " is  $8.67V \le 9.0V \le 9.33V$ .

<sup>\*4 :</sup> When a component with a resistance accuracy of  $\pm 1\%$  is used The absolute accuracy of the internal resistance is  $\pm 15\%$ .

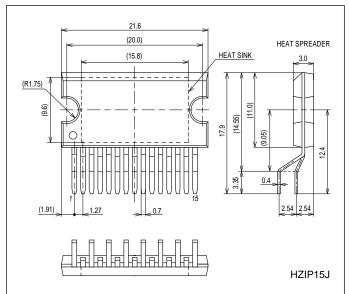
 $<sup>^{\</sup>star}5$ : Since the SW 5V and ACC 5V are output from  $V_{DD}$  5V through the SW, the voltage drops by an amount equivalent to the ON resistance of the SW.

<sup>\*6:</sup> The entire specification has been defined based on the tests performed under the conditions where Tj and Ta (=25°C) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (Tj).

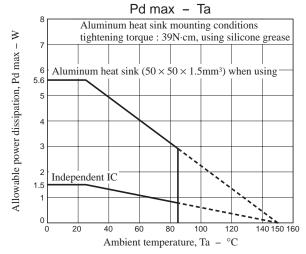
# **Package Dimensions**

unit: mm (typ)

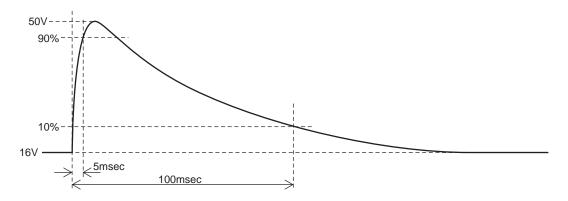
3395



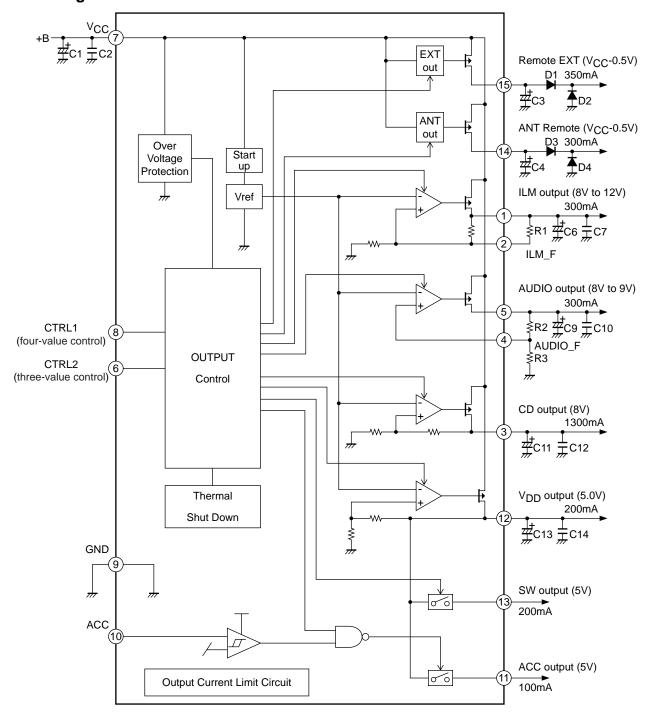
• Allowable power dissipation derating curve



• Waveform applied during surge test



# **Block Diagram**



### **Pin Function**

Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL1 = M1, M2, H 12.0V/300mA	7 VCC
2	ILM_F	ILM output voltage adjustment pin	2 \$59.67kΩ T W \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \

Continued on next page.

Continued from preceding page. Pin No. Pin name Description Equivalent Circuit CD 3 CD output pin VCC ON when CTRL2 = M, H 8.0V/1.3A (3) \$214kΩ } . \$40kΩ 9 GND AUDIO\_F AUIDO output voltage adjustment pin (7)VCC (5) AUDIO output pin 5 AUDIO ON when CTRL2 = M, H GND (9) CTRL2 6 CTRL2 input pin (7)VCC three-value input (6) GND 7 Supply terminal  $^{\text{VCC}}$ 8 CTRL1 CTRL1 input pin -Vcc four-value input GND 9 GND GND pin

Continued on next page.

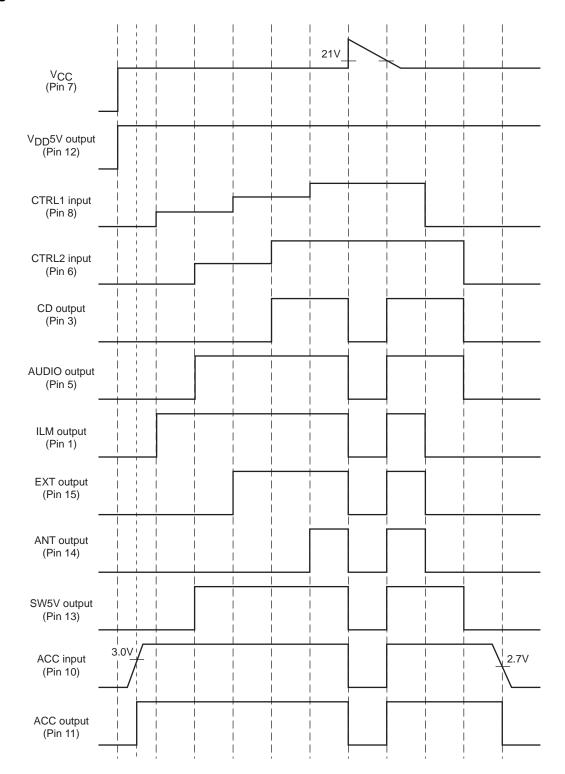
	rom preceding pag	1	Familia (O)
Pin No.	Pin name	Description	Equivalent Circuit
10	ACC	Accessory input	7 VCC VCC 45kΩ FI-W-?? 9 GND
11	ACC5V	Accessory detection output ON when ACC > 3V	7 VCC
12	V <sub>DD</sub> 5V	V <sub>DD</sub> 5V output pin 5.0V/200mA	(12) ■ ■ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □
13	SW5V	SW5V output pin ON when CTRL2 = M, H	(3) ▼ \$50kΩ \$50kΩ 9 GND
14	ANT	ANT output pin ON when CTRL1 = H V <sub>CC</sub> -0.5V/300mA	7 VCC VCC VCC VCC VCC VCC VCC VCC VCC VC
15	EXT	EXT output pin ON when CTRL1 = M2, H V <sub>CC</sub> -0.5V/350mA	7 VCC

**CTRL Pin Output Truth Table** 

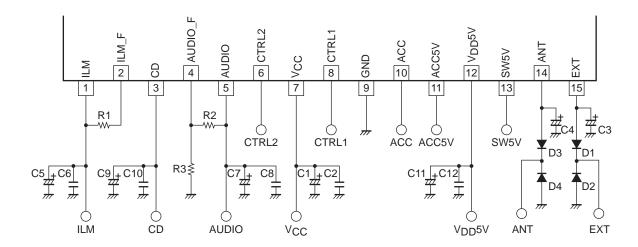
CTRL1	ANT	EXT	ILM			
L	OFF	OFF	OFF			
M1	OFF	OFF	ON			
M2	OFF	ON	ON			
Н	ON	ON	ON			

CTRL2	CD	AUDIO	SW5
L	OFF	OFF	OFF
М	OFF	ON	ON
Н	ON	ON	ON

#### **Timing Chart**



#### **Recommended Operation Circuit**



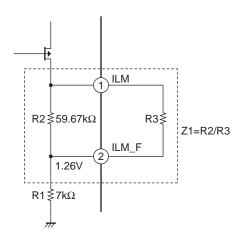
Peripheral parts list

Name of part	Description	Recommended value	Remarks
C1	Power supply bypass capacitor	100μF or more	These capacitors must be placed near
C2	Oscillation prevention capacitor	0.22μF or more	the V <sub>CC</sub> and GND pins.
C3	EXT output stabilization capacitor	2.2μF or more	
C4	ANT output stabilization capacitor	2.2μF or more	
C5, C7, C9, C11	Output stabilization capacitor	4.7μF or more	Electrolytic capacitor *
C6, C8, C10, C12	Output stabilization capacitor	0.22μF or more	Ceramic capacitor *
R1	Resistor for ILM voltage adjustment	ILM output voltage R1:without = 12.0V :270 $k\Omega$ = 10.0V :100 $k\Omega$ = 8.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
R2, R3	Resistor for AUDIO voltage setting	AUDIO output voltage R2/R3:30k $\Omega$ /5.6k $\Omega$ = 8.0V :27k $\Omega$ /4.7k $\Omega$ = 8.5V :24k $\Omega$ /3.9k $\Omega$ = 9.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
D1, D2, D3, D4	Diode for internal device breakdown protection		

<sup>\*:</sup> In order to stabilize the regulator outputs, it is recommended that the electrolytic capacitor and ceramic capacitor be connected in parallel.

Furthermore, the values listed above do not guarantee stabilization during the overcurrent protection operations of the regulator, so oscillation may occur during an overcurrent protection operation.

#### • ILM output voltage setting method



The ILM\_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for ILM voltage calculation

$$Z_1 = R_2 / / R_3 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

$$ILM = \frac{1.26[V]}{R_1} \times Z_1 + 1.26[V]$$

$$Z_1 = \frac{(ILM - 1.26) \cdot R_1}{1.26}$$
  $R_3 = \frac{R_2 \cdot Z_1}{R_2 - Z_1}$ 

Example : ILM = 9V setting method

$$Z_1 = \frac{(9V - 1.26V) \cdot 7k\Omega}{1.26V} \cong 43k\Omega$$

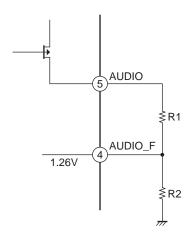
$$R_3 = \frac{59.67k\Omega \cdot 43k\Omega}{59.67k\Omega - 43k\Omega} \cong 153.9k\Omega \rightarrow 150k\Omega$$

When R3 = 150k, the ILM output voltage will be as follows:

$$Z_1' = \frac{59.67k\Omega \cdot 150k\Omega}{59.67k\Omega + 150k\Omega} \cong 42.69k\Omega$$

$$ILM = \frac{1.26V}{7k\Omega} \times 42.69k\Omega + 1.26V \cong 8.94V$$

• AUDIO output voltage setting method



The AUDIO\_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for AUDIO voltage calculation

$$AUDIO = \frac{1.26[V]}{R_2} \times R_1 + 1.26[V]$$

$$\frac{R_1}{R_2} = \frac{(AUDIO - 1.26)}{1.26}$$

The circuit must be designed in such a way that the R1:R2 ratio satisfies the formula given above for the AUDIO voltage that has been set.

Example : AUDIO = 8.5V setting method

$$\frac{R_1}{R_2} = \frac{\left(8.5 - 1.26\right)}{1.26} \cong 5.75$$

$$\frac{R_1}{R_2} = \frac{27k\Omega}{4.7k\Omega} \cong 5.74$$

$$AUDIO = 1.26V \times 5.74 + 1.26V \cong \boxed{8.49V}$$

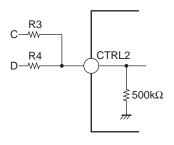
Note: In the above, the typical values are given in all instances for the values used and, as such, they will vary due to the effects of production-related variations of the IC and external resistors.

#### • CTRL1 Application Circuit Example

#### (1) 3.3V input: $R1 = 4.7k\Omega$ , $R2 = 10k\Omega$

Α	В	CTRL1
0V	0V	0V
0V	3.3V	1.05V
3.3V	0V	2.23V
3.3V	3.3V	3.20V

# • CTRL2 Application Circuit Example



#### (1) 3.3V input: $R3 = R4 = 4.7k\Omega$

Α	В	CTRL2
0V	0V	0V
0V	3.3V	1.61V
3.3V	0V	1.61V
3.3V	3.3V	3.29V

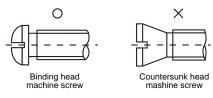
#### HZIP15J Heat sink attachment

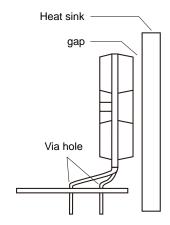
Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

#### b. Heat sink attachment

- · Use flat-head screws to attach heat sinks.
- · Use also washer to protect the package.
- · Use tightening torques in the ranges 39-59Ncm(4-6kgcm).
- · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Take care a position of via hole.
- · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Verify that there are no press burrs or screw-hole burrs on the heat sink.
- · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- · Twisting must be limited to under 0.05 mm.
- · Heat sink and semiconductor device are mounted in parallel. Take care of electric or compressed air drivers
- The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.





#### c. Silicone grease

- · Spread the silicone grease evenly when mounting heat sinks.
- · Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)

#### d. Mount

- · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.
- e. When mounting the semiconductor device to the heat sink using jigs, etc.,
  - · Take care not to allow the device to ride onto the jig or positioning dowel.
  - · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

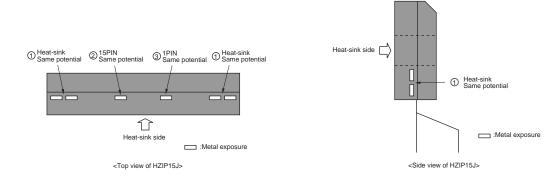
#### f. Heat sink screw holes

- · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.
- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

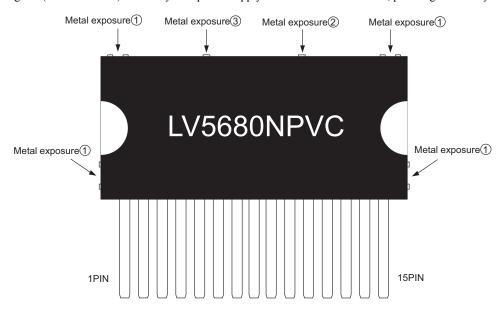
#### Caution for implementing LV5680P to a system board

The package of LV5680P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the  $V_{CC}$  pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and  $V_{CC}$ . The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

#### • HZIP15J outline



• Frame diagram (LV5680NPVC) \*In the system power supply other than LV5680NPVC, pin assignment may differ.



ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equa