

M64894FP/GP**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR****DESCRIPTION**

The M64894 is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using I²C BUS control. It contains the prescaler with operating up to 1.3GHz, 4 band drivers and tuning Amplifier for direct tuning. Built-in 4 band drivers.

FEATURES

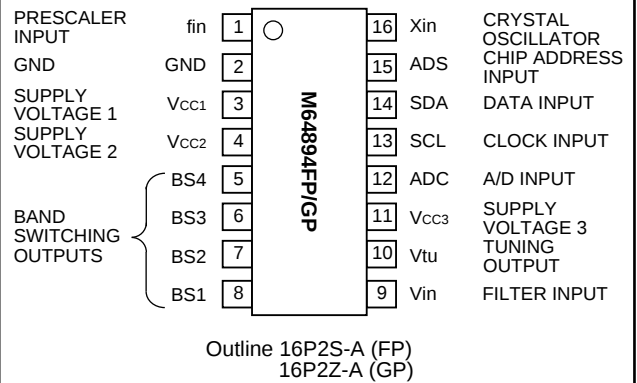
- 4 integrated PNP band drivers
($I_o=40\text{mA}$, $V_{\text{sat}}=0.2\text{V typ@Vcc1 to 13.2V}$)
- Built-in high-withstanding voltage tuning Amplifier
- Low power dissipation ($I_{\text{cc}}=20\text{mA}$, $V_{\text{cc}}=5\text{V}$)
- Built-in prescaler with input amplifier ($F_{\text{max}}=1.3\text{GHz}$)
- I²C bus control (Read and write mode)
- X'tal 4MHz is used to realize 3 type of tuning steps
(Division ratio 1/512, 1/640, 1/1024)
- Built-in 5-level A/D converter
- Programmable chip address
- 16-pin small SOP/SSOP package

APPLICATION

TV, VCR tuners

RECOMMENDED OPERATING CONDITION

Supply voltage range..... $V_{\text{cc1}}=4.5$ to 5.5V
 $V_{\text{cc2}}=V_{\text{cc1}}$ to 13.2V
 $V_{\text{cc3}}=28$ to 35V
 Rated supply voltage..... $V_{\text{cc1}}=5\text{V}$
 $V_{\text{cc2}}=12\text{V}$
 $V_{\text{cc3}}=33\text{V}$

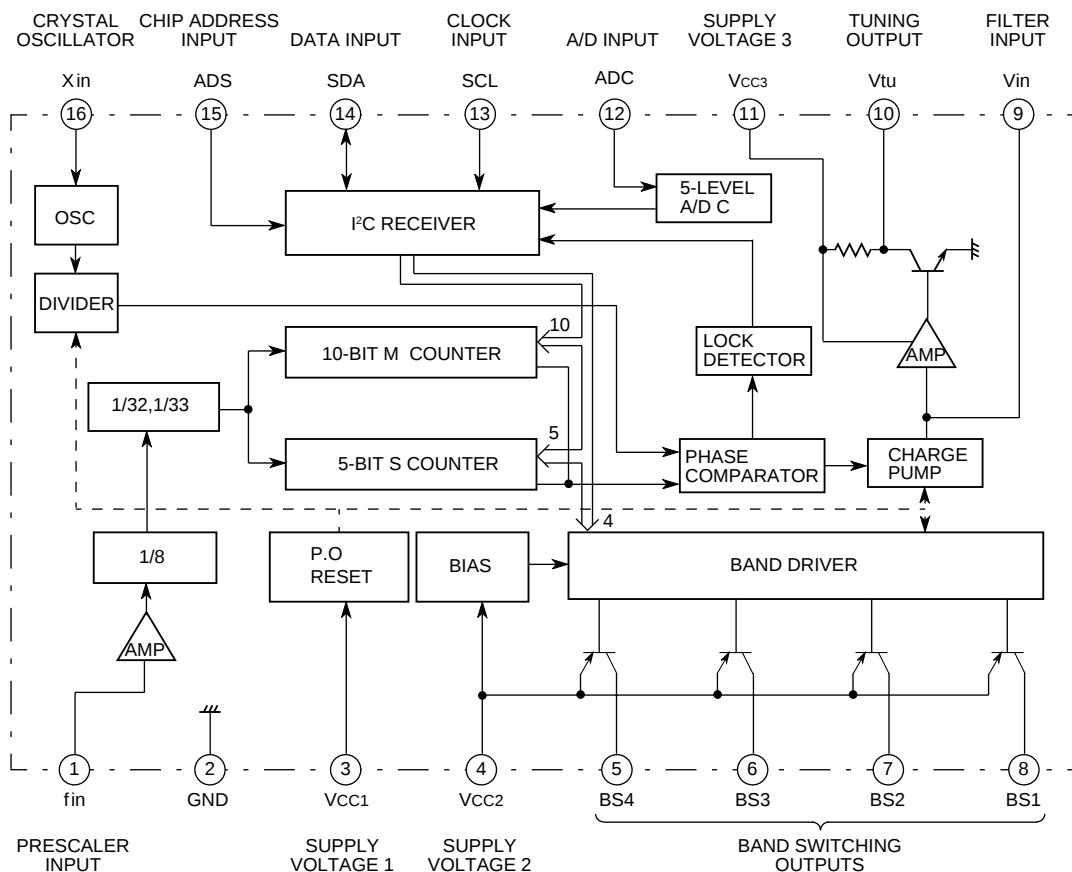
PIN CONFIGURATION (TOP VIEW)**FUNCTION**

- 2-modulus prescaler (1/32 and 1/33)
- Built-in 4MHz crystal oscillator and reference divider
- Programmable divider (10-bit M counter, 5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op. Amp for direct tuning
- I²C bus receiver
- 5-level A/D converter

M64894FP/GP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

BLOCK DIAGRAM



M64894FP/GP**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR****DESCRIPTION OF PIN**

Pin No.	Symbol	Pin name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	Vcc1	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	Vcc2	Power supply voltage 2	Power supply for band switching, Vcc1 to 13.2V
5 6 7 8	BS4 BS3 BS2 BS1	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
9	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
10	Vtu	Tuning output	This supplies the tuning voltage.
11	Vcc3	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
12	ADC/ftest	AD converter input/ Test port	A/D conversion of the input voltage. In control byte data input, the programmable freq. Divider output and reference freq. output is selected by the test mode.
13	SCL	Clock input	Data is read into the shift register when the clock signal falls.
14	SDA	Data input	Input for band SW and programmable freq. divider set up. In lead mode, it outputs lock detector output and power down flag and a state of 5 level A/D converter.
15	ADS	Address switching input	Chip address sets it up with the input condition of terminal.
16	Xin	This is connected to the crystal oscillator	4.0MHz crystal oscillator is connected.

ABSOLUTE MAXIMUM RATINGS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1	Supply voltage 1	Pin3	6.0	V
Vcc2	Supply voltage 2	Pin4	14.4	V
Vcc3	Supply voltage 3	Pin11	36.0	V
Vi	Input voltage	Not to exceed Vcc1	6.0	V
Vo	Output voltage	fREF output	6.0	V
VBSOFF	Voltage applied when the band output is OFF		14.4	V
IBSON	Band output current	Per 1 band output circuit	50.0	mA
tBSON	ON the time when the band output is ON	50mA per 1 band output circuit 3 circuit are on at same time	10	sec
Pd	Power dissipation	Ta=+75°C	450 (470)	mW
Topr	Operating temperature		-20 to +75	°C
Tstg	Storage temperature		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1	Supply voltage 1	Pin3	4.5 to 5.5	V
Vcc2	Supply voltage 2	Pin4	Vcc1 to 13.2	V
Vcc3	Supply voltage 3	Pin11	28 to 35	V
fopr1	Operating frequency (1)	Crystal oscillation circuit	4.0	MHz
fopr2	Operating frequency (2)		80 to 1,300	MHz
IBDL	Band output current 5 to 8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 40	mA

M64894FP/GP**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR****ELECTRICAL CHARACTERISTICS** (Ta=-20°C to +75°C, Vcc1=5.0V, Vcc2=12V, Vcc3=33V, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V _{IH}	Input pin	"H" input voltage	13 to 14		3.0	—	V _{CC1} +0.3	V
V _{IL}		"L" input voltage	13 to 14		—	—	1.5	V
I _{IH}		"H" input current	13 to 14	V _{CC1} =5.5V, V _i =4.0V	—	—	10	μA
I _{IL}		"L" input current	13, 14	V _{CC1} =5.5V, V _i =0.4V	—	-4/-14	-10/30	μA
V _{OL}	SDA output	"H" output voltage	14	V _{CC1} =5.5V, I _o =3mA	—	—	0.4	μA
V _{LO}		"L" output voltage	14	V _{CC1} =5.5V, V _o =5.5V	—	—	10	μA
V _{BS}	Band SW	Output voltage	5 to 8	V _{CC2} =12V, I _o =-40mA	11.6	11.8	—	V
I _{OLK1}		Leak current	5 to 8	V _{CC2} =12V band SW is OFF	—	—	-10	μA
V _{TOH}	Tuning output	Output voltage "H"	10	V _{CC3} =33V	32.5	—	—	V
V _{TOL}		Output voltage "L"	10	V _{CC3} =33V	—	0.2	0.4	V
I _{OH}	Charge pump	"H" output current	9	V _{CC1} =5.0V, V _o =2.5V	—	±270	±370	μA
I _{OL}		"L" output current	9	V _{CC1} =5.0V, V _o =2.5V	—	±70	±110	μA
I _{CPLK}		Leak current	9	V _{CC1} =5.5V, V _o =2.5V	—	—	±50	nA
I _{CC1}	Supply current 1		3	V _{CC1} =5.5V	—	20	30	mA
I _{CC2A}	Supply current 2	4 circuits: OFF	4	V _{CC2} =12V	—	—	0.3	mA
I _{CC2B}		1 circuits: ON, Output: OPEN	4	V _{CC2} =12V	—	6.0	8.0	mA
I _{CC2C}		Output current 40mA	4	V _{CC2} =12V I _o =-40mA	—	46.0	48.0	mA
I _{CC3}	Supply current 3		11	V _{CC3} =33V Output ON	—	3.0	4.0	mA

Note. Typical values are measured at V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V, Ta=+25°C.

SWITCHING CHARACTERISTICS (Ta=-20°C to +75°C, Vcc1=5.0V, Vcc2=12V, Vcc3=33V, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
f _{opr}	Prescaler operating frequency	1	V _{CC1} =4.5 to 5.5V V _{in} =V _{inmin} to V _{inmax}	80	—	1300	MHz
V _{in}	Operating input voltage	1	V _{CC1} =4.5 to 5.5V	80 to 100MHz	-24	—	4
				100 to 200MHz	-27	—	4
				200 to 800MHz	-30	—	4
				800 to 1000MHz	-27	—	4
				1000 to 1300MHz	-18	—	4
t _{SCL}	Clock pulse frequency	13	V _{CC1} =4.5 to 5.5V	0	—	100	kHz
t _{BUF}	Bus free time	14	V _{CC1} =4.5 to 5.5V	4.7	—	—	μs
t _{HDSTA}	Data hold time	13	V _{CC1} =4.5 to 5.5V	4	—	—	μs
t _{LOW}	SCL low hold time	13	V _{CC1} =4.5 to 5.5V	4.7	—	—	μs
t _{HIGH}	SCL high hold time	13	V _{CC1} =4.5 to 5.5V	4	—	—	μs
t _{SUSTA}	Set up time	13, 14	V _{CC1} =4.5 to 5.5V	4.7	—	—	μs
t _{HDDAT}	Data hold time	13, 14	V _{CC1} =4.5 to 5.5V	0	—	—	s
t _{SUDAT}	Data set up time	13, 14	V _{CC1} =4.5 to 5.5V	250	—	—	ns
t _r	Rise time	13, 14	V _{CC1} =4.5 to 5.5V	—	—	1000	ns
t _f	Fall time	13, 14	V _{CC1} =4.5 to 5.5V	—	—	300	ns
t _{SUSTO}	Set up time	13, 14	V _{CC1} =4.5 to 5.5V	4	—	—	μs

M64894FP/GP**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR****METHOD OF SETTING DATA**

The input information to consist of 2 or data of 4 bytes to lead to Chip Address is received in I²Cbus receiver. It shows a definition of bus protocol admitted in the following.

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1_STA CA CB BB STO
2_STA CA D1 D2 STO
3_STA CA CB BB D1 D2 STO
4_STA CA D1 D2 CB BB STO

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STA : Start condition

STO : Stop condition

CA : Chip address

CB : Control data byte

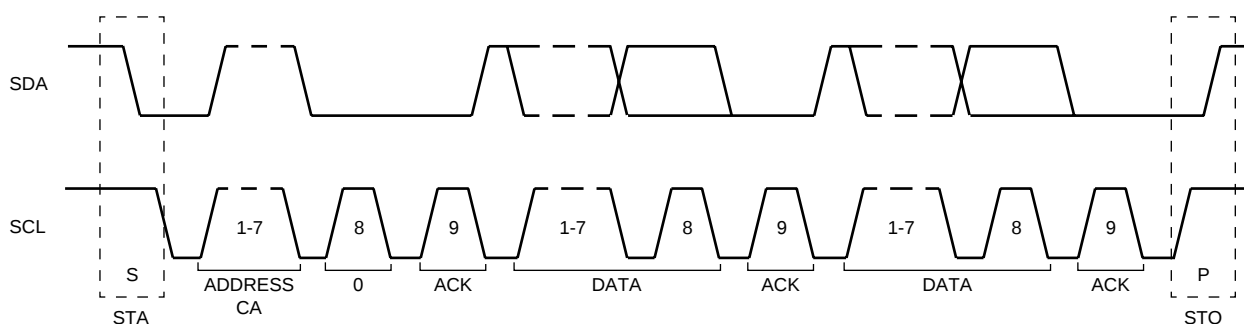
BB : BandS.W. data byte

D1 : Divider data byte

D2 : Divider data byte

The information of 5 bytes necessary for circuit operation is chip address and control data, bandS.W. data of 2 bytes and divider byte of 2 bytes. After the chip address input, 2 or data of 4 bytes are received.

Function bit is contained the first and the third data byte to distinguish between divider data and control data, band data, and "0" goes ahead of divider data, and "1" goes ahead of control data, bandS.W. data.

**Write mode format**

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	0	A
Devier Byte1	0	N14	N13	N12	N11	N10	N9	N8	A
Devier Byte2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte1	1	CP	T2	T1	T0	RSa	RSb	OS	A
Band SW Byte	X	X	X	X	BS4	BS3	BS2	BS1	A

Read mode format

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	1	A
Status Byte1	POR	FL	X	X	X	A2	A1	A0	A

M64894FP/GP**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR****DATA CORDING EXAMPLE****Write mode format example**

Byte	MSB								LSB	Condotion in data setting
Address Byte	1	1	0	0	0	1	1	0	1	ADS input Vcc1
Devider Byte1	0	1	0	0	0	0	0	0	1	Dividing ratio N=16544
Devider Byte2	1	0	1	0	0	0	0	0	1	
Control Byte1	1	1	0	0	0	0	1	0	1	C.P. current 270μA fREF division ratio 1/1024
Band SW Byte	0	0	0	0	1	0	0	0	1	BS4 output ON

$$f_{VCO} = N \times 8 \times f_{REF} = 16544 \times 8 \times (4\text{MHz}/1024) = 517\text{MHz}$$

Read mode format example

Byte	MSB								LSB	Condotion in divide
Address Byte	1	1	0	0	0	1	1	1	1	
Status Byte1 input	1	1	1	1	1	1	1	1	1	
Status Byte1 output	0	1	1	1	1	0	1	1	1	FL "1" output at locked ADC input at open

TEST MODE DATA SET UP METHOD**Test Mode Bit Set Up**

X : Random, 0 or 1. normal "0"

MA1 ,MA0 : Programmabule Address Bit

Address input voltage	MA1	MA0
0 to 0.1*Vcc1	0	0
Always valid	0	1
0.4*Vcc1 to 0.6*Vcc1	1	0
0.9*Vcc1 to Vcc1	1	1

N14 to N0 : How to set dividing ratio of the programable the divider

$$\text{Dividing ratio } N = N_{14}(2^{14} = 16384) + \dots + N_0(2^0 = 1)$$

Therefore, the range of division N is 1,024 to 32,768

$$\text{Example) } f_{VCO} = f_{REF} \times 8 \times N$$

$$= 3.90625 \times 8 \times N$$

$$= 31.25 \times N \text{ (kHz)}$$

CP: Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70μA	Test
1	270μA	Normal

T2, T1, T0 : Setting up for the test mode

T2 T1 T0	Charge pump	Pin 12 condition	Mode
0 0 X	Normal operation	ADC input	Normal operation
0 1 X	High impedance	ADC input	Test mode
1 1 0	Sink	ADC input	Test mode
1 1 1	Source	ADC input	Test mode
1 0 0	High impedance	fREF output	Test mode
1 0 1	High impedance	f1/N output	Test mode

RSa, RSb : Set up for the reference frequency division ratio

RSa	RSb	Division ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS : Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

POR : Power on reset flag. "1" output at reset

FL : Lock detector flag. "1" output at locked,
"0" output at unlocked

A2, A1, A0: 5level A/D converter output data

ADC input voltage	A2	A1	A0
0.6*Vcc1 to Vcc1	1	0	0
0.45*Vcc1 to 0.6*Vcc1	0	1	1
0.3*Vcc1 to 0.45*Vcc1	0	1	0
0.15*Vcc1 to 0.3*Vcc1	0	0	1
0 to 0.15*Vcc1	0	0	0

The voltage accuracy allowance range: $\pm 0.03 \times V_{cc1}$ (V)

POWER ON RESET OPERATION

(Initial state the power is turned ON)

BS4 to BS1 : OFF

Charge pump : High impedance

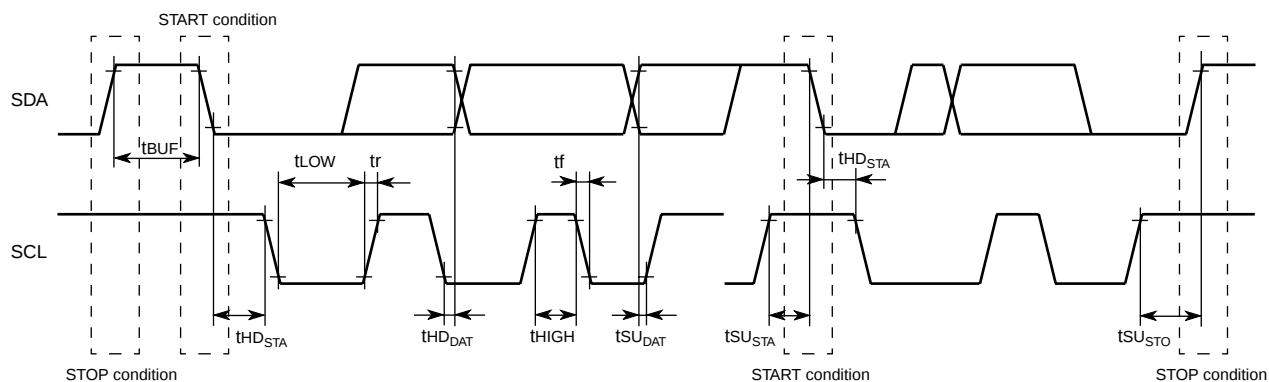
Tuning amplifier : OFF

Charge pump current : 270μA

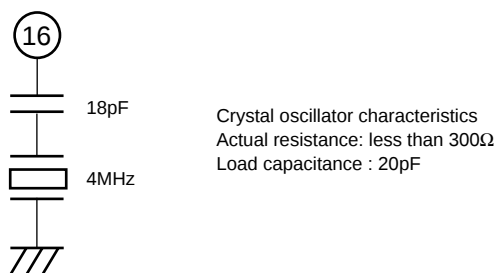
Frequency division ratio : 1/1024

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

TIMING DIAGRAM



CRYSTAL OSCILLATOR CONNECTION DIAGRAM



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APPLICATION EXAMPLE

