

FDZ2553NZ

Monolithic Common Drain N-Channel 2.5V Specified PowerTrench[®] BGA MOSFET

General Description

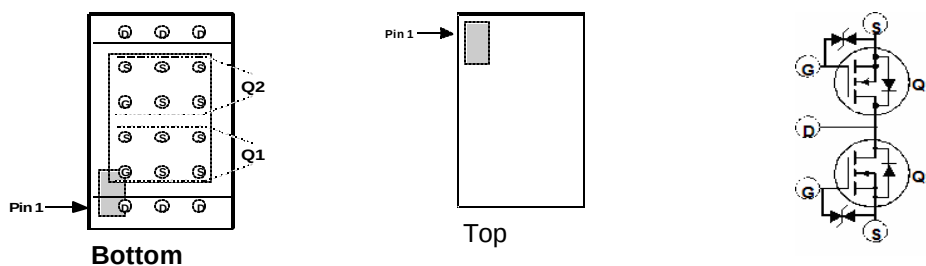
Combining Fairchild's advanced 2.5V specified PowerTrench process with state-of-the-art BGA packaging, the FDZ2553N minimizes both PCB space and $R_{DS(ON)}$. This common drain BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

- Battery management
- Load switch
- Battery protection

Features

- 9.6 A, 20 V. $R_{DS(ON)} = 14 \text{ m}\Omega$ @ $V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 20 \text{ m}\Omega$ @ $V_{GS} = 2.5 \text{ V}$
- Occupies only 0.10 cm² of PCB area:
1/3 the area of SO-8.
- Ultra-thin package: less than 0.70 mm height when mounted to PCB.
- ESD protection diode (note 3)
- Outstanding thermal transfer characteristics:
significantly better than SO-8.
- Ultra-low $Q_g \times R_{DS(ON)}$ figure-of-merit
- High power and current handling capability



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a)	9.6	A
		20	
P_D	Power Dissipation (Steady State) (Note 1a)	2.1	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Ball (Note 1)	6.3	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.6	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2553NZ	FDZ2553NZ	7"	12mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, \quad I_D = 250\text{ }\mu\text{A}$	20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		12		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, \quad V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 12\text{ V}, \quad V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, \quad I_D = 250\text{ }\mu\text{A}$	0.6	0.9	1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		–0.3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, \quad I_D = 9.6\text{ A}$ $V_{GS} = 2.5\text{ V}, \quad I_D = 7.9\text{ A}$ $V_{GS} = 4.5\text{ V}, \quad I_D = 9.6\text{ A}, \quad T_J = 125^\circ\text{C}$		12 16 16	14 20 24	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, \quad V_{DS} = 5\text{ V}$	10	20		A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, \quad I_D = 9.6\text{ A}$		45		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, \quad V_{GS} = 0\text{ V},$		1240		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		320		pF
C_{rss}	Reverse Transfer Capacitance			170		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, \quad f = 1.0\text{ MHz}$		2.1		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, \quad I_D = 1\text{ A},$		10	20	ns
t_r	Turn–On Rise Time	$V_{GS} = 4.5\text{ V}, \quad R_{GEN} = 6\text{ }\Omega$		14	26	ns
$t_{d(off)}$	Turn–Off Delay Time			26	42	ns
t_f	Turn–Off Fall Time			11	19	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, \quad I_D = 9.6\text{ A},$		13	18	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = 5\text{ V}$		3		nC
Q_{gd}	Gate–Drain Charge			3		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				1.7	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, \quad I_S = 1.7\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 9.6\text{ A},$		20		nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		6		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

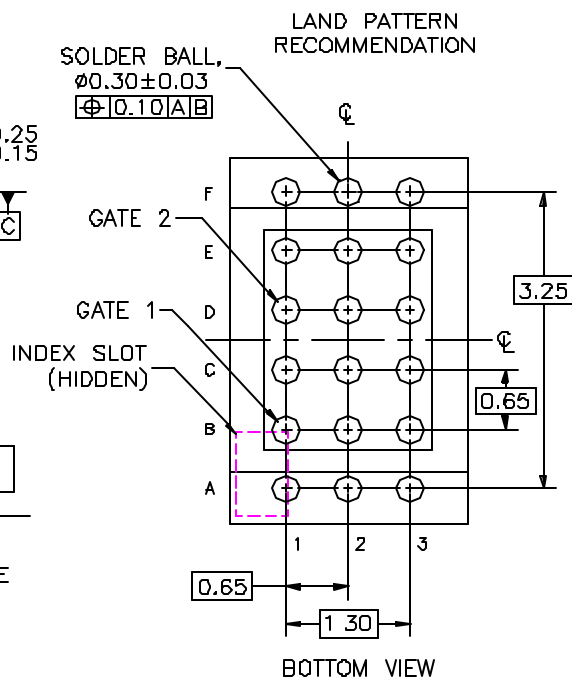
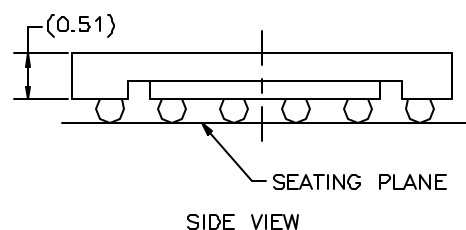
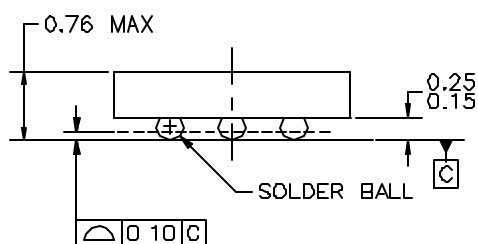
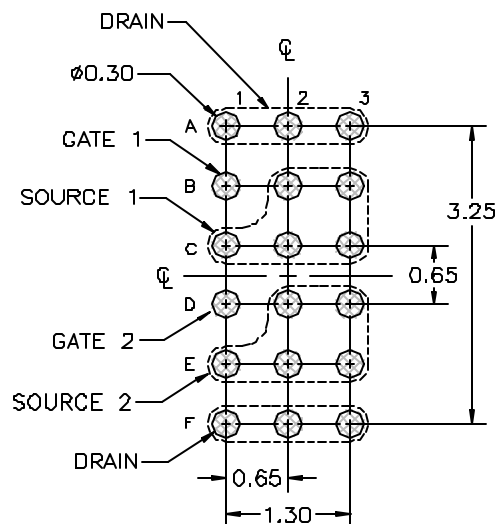
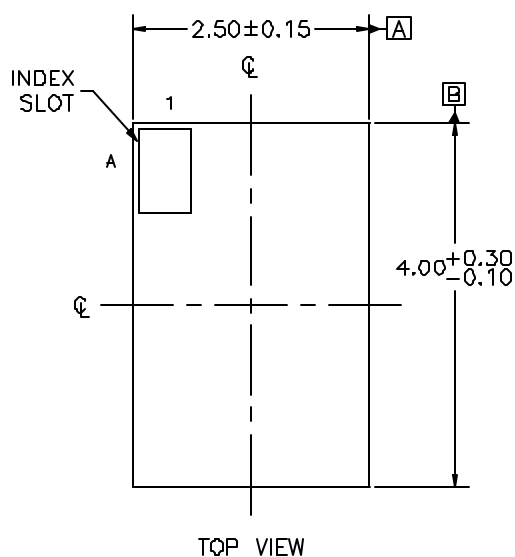
(a). $R_{\theta JA} = 60^\circ\text{C/W}$ when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

(b). $R_{\theta JA} = 108^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS
 B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
 C) BALL CONFIGURATION TABLE

BALL TERMINAL	DESIGNATION
A1, A2, A3, F1, F2, F3	DRAIN
B1	GATE 1
B2, B3, C1, C2, C3	SOURCE 1
D1	GATE 2
D2, D3, E1, E2, E3	SOURCE 2

FC018AAREVA

Typical Characteristics

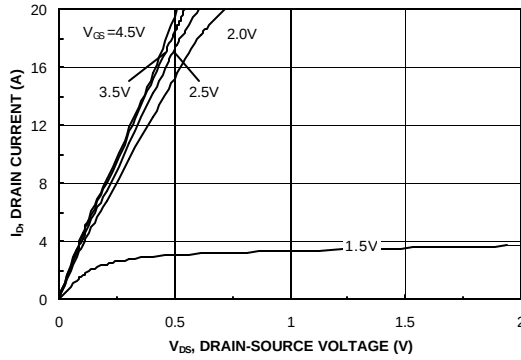


Figure 1. On-Region Characteristics.

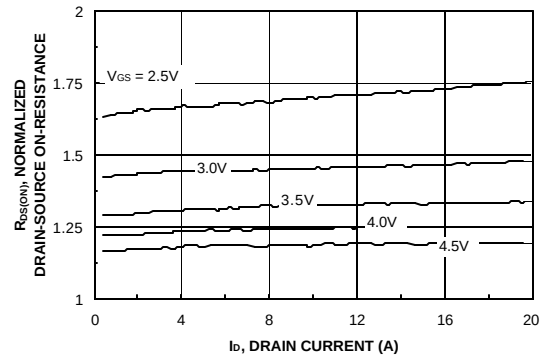


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

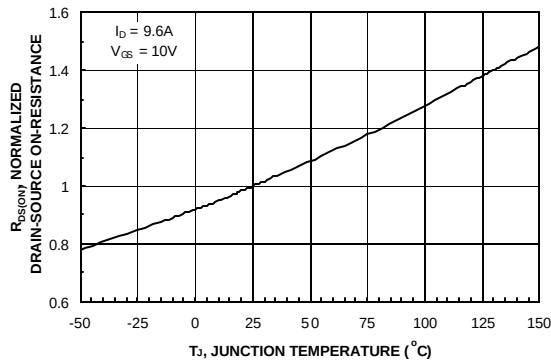


Figure 3. On-Resistance Variation with Temperature.

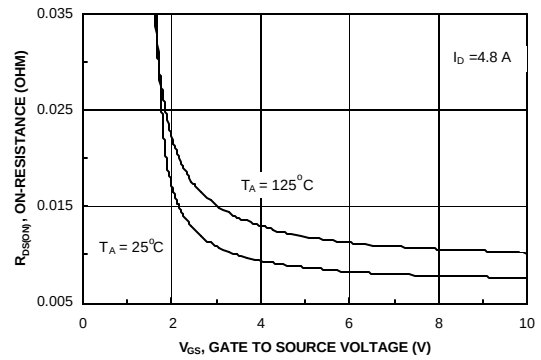


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

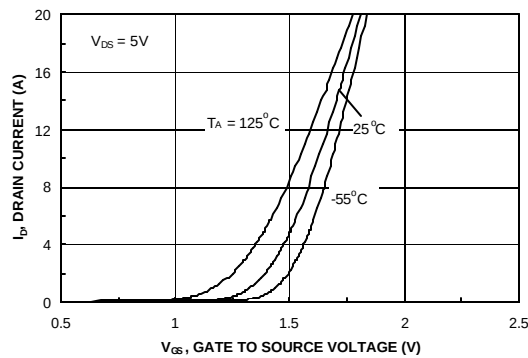


Figure 5. Transfer Characteristics.

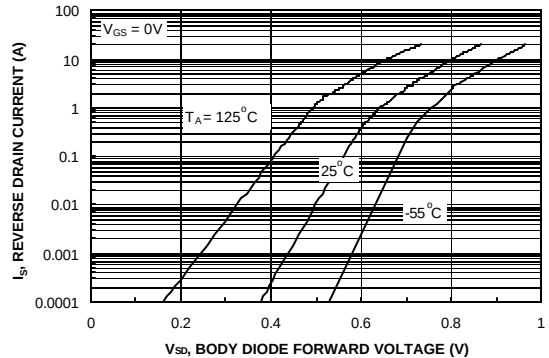


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

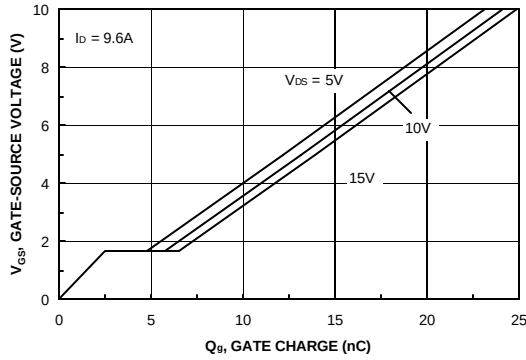


Figure 7. Gate Charge Characteristics.

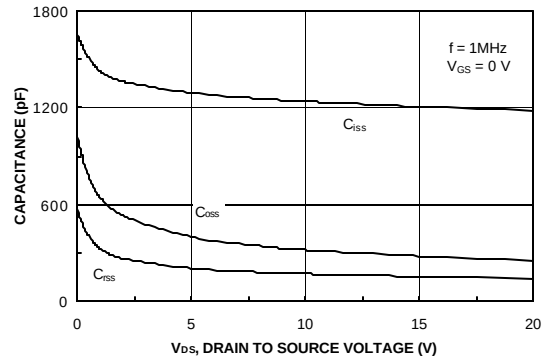


Figure 8. Capacitance Characteristics.

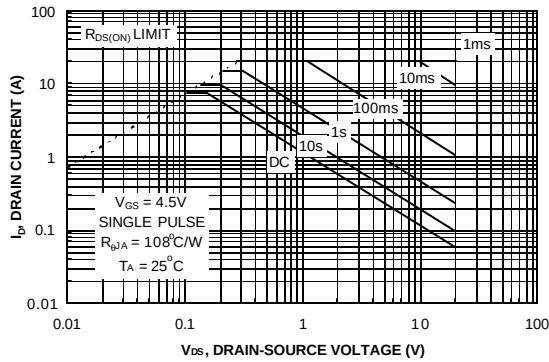


Figure 9. Maximum Safe Operating Area.

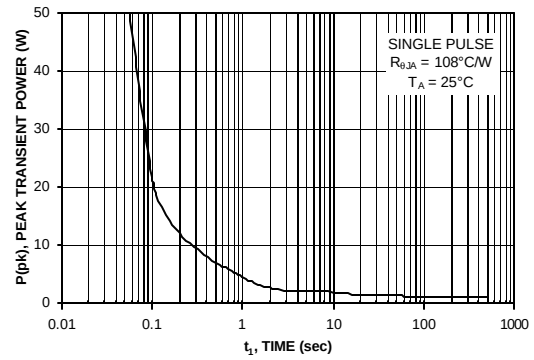


Figure 10. Single Pulse Maximum Power Dissipation.

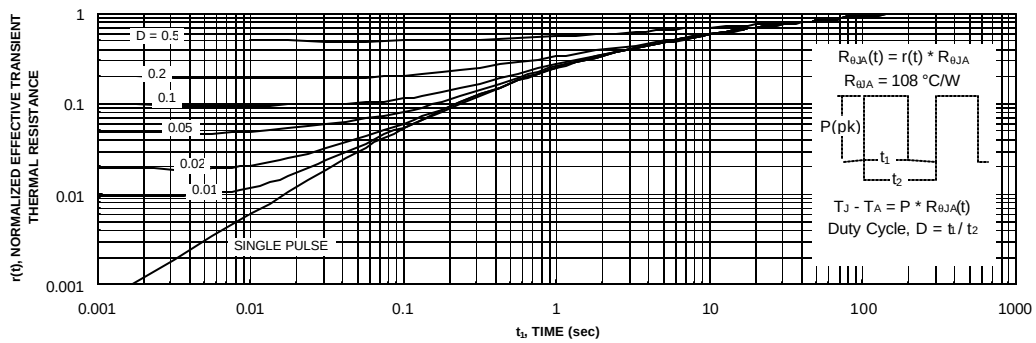


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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