Advance Product Information

VSC7961

3.125Gb/s PECL Limiting Amplifier with LOS Detect

Features

- 3.3V or 5V Power Supply
- Typical Supply Current of 32mA
- Positive Emitter-Coupled Logic (PECL) Outputs
- Optional Output Squelch
- Loss of Signal Detect
- Output Offset Correction
- Rise/Fall Times Faster than 100ps
- Packages: TSSOP-16, Bare Die

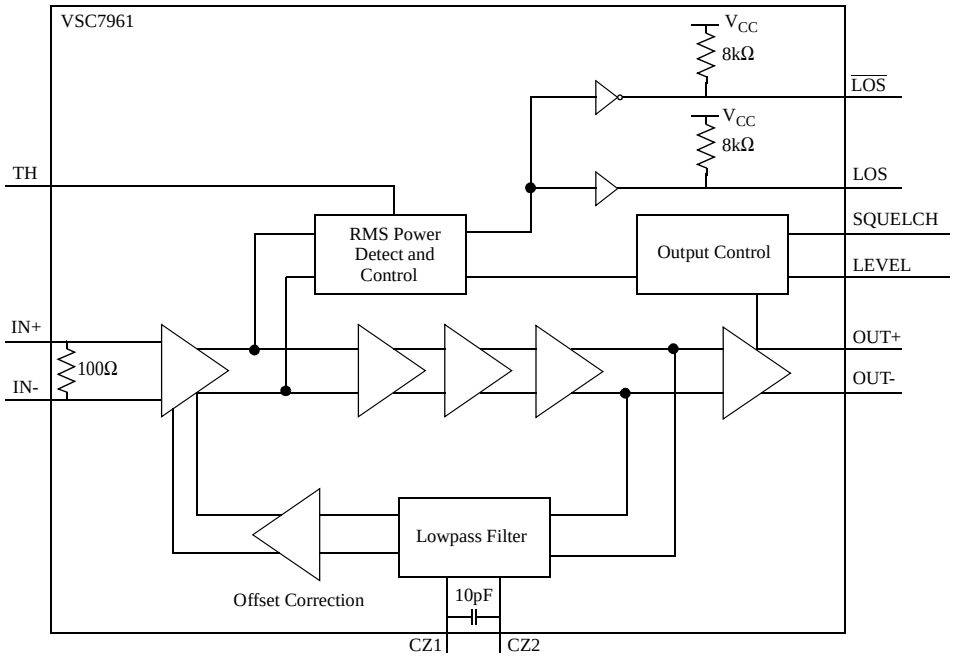
Applications

- SONET/SDH at 622Mb/s, 1.244Gb/s, 2.488Gb/s, and 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)
- Small Form Factor (SFF) Receivers
- ATM Optical Receivers

General Description

The VSC7961 is a single-supply limiting amplifier with Loss of Signal (LOS) detect for SONET/SDH and Fibre Channel applications up to 3.125Gb/s. The VSC7961 provides a constant output signal swing for a wide range of input voltages and has Positive Emitter-Coupled Logic (PECL). The VSC7959 provides the same functionality as the VSC7961 with Current-Mode Logic (CML) outputs. Key features of the VSC7961 are its RMS power detectors for programmable LOS detection, optional output squelch, adjustable output levels, excellent jitter performance, and fast edge rates. The VSC7961 is available in die form or in a TSSOP-16 package.

Block Diagram



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Electrical Characteristics

Table 1: DC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{CC}	Power Supply Voltage	3.135		5.5	V	
I_{CC}	Power Supply Current(1)		59		mA	V_{CC} = 3.3V
			62		mA	V_{CC} = 5V
I_{EE}	Power Supply Current(1)		31		mA	V_{CC} = 3.3V
			35		mA	V_{CC} = 5V
I_{CCSQ}	Power Supply Current when Squelched(1)		58		mA	V_{CC} = 3.3V
			62		mA	V_{CC} = 5V
I_{EESQ}	Power Supply Current when Squelched(1)		20		mA	V_{CC} = 3.3V
			23		mA	V_{CC} = 5V
I_{SQ}	Squelch Input Current	0		400	µA	
PSSR	Power Supply Rejection Ratio	20			dB	f < 2MHz

NOTE: (1) See Figure 4 for supply current measurement setup.

Table 2: DC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
	Data Rate	3.125			Gb/s	
V_{IN}	Input Voltage Range	10		1200	mV	Peak-to-peak
J_D	Deterministic Jitter			25	ps	See Note 1
J_R	Random Jitter			8	ps	See Note 2, RMS
$t_{R,}$ t_F	Rise and Fall Times		55	100	ps	20% to 80%
V_N	Input Referred Noise			230	µV	RMS, IN+ to IN-
R_{DIFF}	Differential Input Resistance		100		Ω	IN+ to IN-
f_L	Low Frequency Cutoff		2		MHz	C_Z open
			2		kHz	C_Z = 0.1µF
V_{SQ}	Output Signal When Squelched			20	mV	Output AC-coupled
V_{OH}	PECL Output High Voltage	-1025		-850	mV	
				-850	mV	Squelched
V_{OL}	PECL Output Low Voltage	-1810		-1620	mV	
				-1620	mV	Squelched
Z_O	Output Resistance		100		Ω	Single-ended

NOTES: (1) Deterministic jitter measured peak-to-peak with K28.5 pattern. (2) Random jitter measured with minimum input.

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Table 3: Loss of Signal Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
H_{LOS}	LOS Hystersis	3.1	3.3	5.5	dB	$H_{LOS} = 20 \log (V_{THD}/V_{THA})$
I_{LOS}	LOS Assert/Deassert Time	0.22	0.25	0.28	µs	
V_{THA}	LOS Assert Threshold		8.2		mV	R_{TH} = 2.5kΩ
		12.8	19.8	21.8	mV	R_{TH} = 7kΩ
			57.2		mV	R_{TH} = 20kΩ
V_{THD}	LOS Deassert Threshold		11.4		mV	R_{TH} = 2.5kΩ
		26.2	29.0	31.6	mV	R_{TH} = 7kΩ
			75.2		mV	R_{TH} = 20kΩ
V_{LOSH}	LOS Output HIGH Voltage	3.3			V	I_{LOS} = –30µA
V_{LOSL}	LOS Output LOW Voltage		0.168		V	I_{LOS} = +1.2µA

Table 4: Loss of Signal Truth Table

SQUELCH	*LOS*	*Output*
High	Low	Off
Low	High	On
High	Low	On
Low	Low	On

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC})..... -0.5V to +6V
Maximum Junction Temperature Range .....TBD
Storage Temperature Range (T_S)..... -55°C to +150°C

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Positive Voltage Rail (V_{CC})..... 3.3V or 5V
Junction Temperature Range (T_J)..... -40°C to +100°C
Ambient Temperature Range (T_A)..... -40°C to +85°C

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Package Pin Descriptions

Figure 1: Pin Diagram

Top View
TSSOP-16 Package

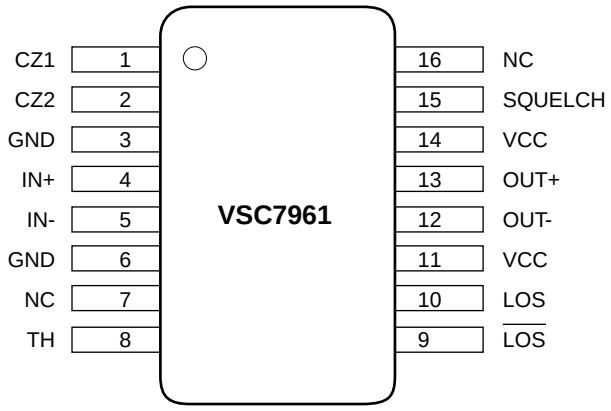


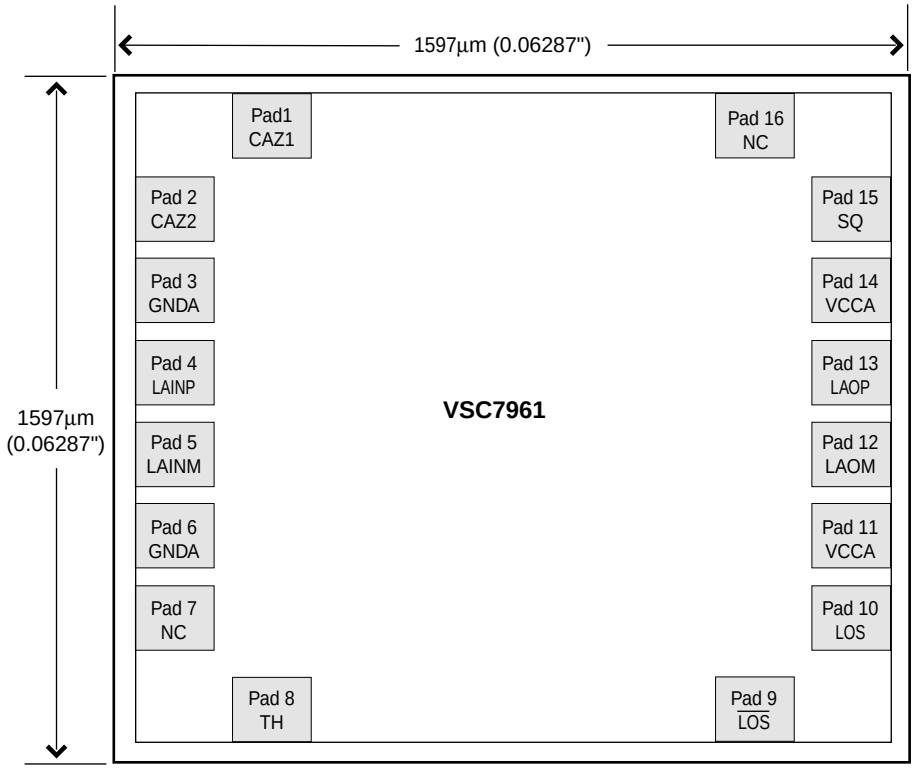
Table 5: Pin Identifications

Pin Name	*Pin No.*	*Description*
CZ1	1	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop. See *Detailed Description* section.
CZ2	2	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop. See *Detailed Description* section.
GND	3	Supply Ground
IN+	4	Noninverted Input Signal
IN-	5	Inverted Input Signal
GND	6	Supply Ground
NC	7	This pin may be either connected to ground of left unconnected. This pin does not effet the performance of the device.
TH	8	Loss of Signal (LOS) Threshold. Connect a resistor from this pin to ground to set the input signal level at which LOS outputs will be asserted. See *Application Information* section.
$\overline{\text{LOS}}$	9	Inverted Loss of Signal Output. LOS is HIGH for input signals above the threshold programmed by TH. See *Detailed Description* section.
LOS	10	Noninverted Loss of Signal Output. LOS is LOW for input signals above the threshold programmed by TH. See *Detailed Description* section.
VCC	11	Power Supply
OUT-	12	Inverted Data Output
OUT+	13	Noninverted Data Output
VCC	14	Power Supply
SQUELCH	15	Squelch Input. Squelch is disabled if this pin is unconnected or set LOW. When SQUELCH is HIGH, OUT+ and OUT- are forced to static levels. See *Detailed Description* section.
NC	16	No Connection

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Bare Die Descriptions

Figure 2: Pad Assignments



Die Size:	1597µm x 1597µm (0.06287" x 0.06287")
Pad Pitch:	180µm (0.00709")
Pad Passivation Opening:	95µm x 95µm (0.00374" x 0.00374")

The back side of the die may either be left floating or connected ot ground.

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Table 6: Pad Coordinates

Pad Name	*Pin Name*	*Pad/Pin Number*	*Coordinates (µm)*		*Description*
			X	*Y*	
CZ1	CZ1	1	270.525	1359.05	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop. See *Detailed Description* section.
CZ2	CZ2	2	80.95	1170.525	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop. See *Detailed Description* section.
GNDA	GND	3	80.95	990.525	Supply Ground
LAINP	IN+	4	80.95	810.525	Noninverted Input Signal
LAINM	IN-	5	80.95	630.525	Inverted Input Signal
GNDA	GND	6	80.95	450.525	Supply Ground
NC	NC	7	80.95	270.525	This pin may be either connected to ground of left unconnected. This pin does not effet the performance of the device.
TH	TH	8	270.525	80.95	Loss of Signal (LOS) Threshold. Connect a resistor from this pin to ground to set the input signal level at which LOS outputs will be asserted. See *Application Information* section.
$\overline{\text{LOS}}$	$\overline{\text{LOS}}$	9	1169.475	80.95	Inverted Loss of Signal Output. LOS is HIGH for input signals above the threshold programmed by TH. See *Detailed Description* section.
LOS	LOS	10	1359.05	270.525	Noninverted Loss of Signal Output. LOS is LOW for input signals above the threshold programmed by TH. See *Detailed Description* section.
VCCA	VCC	11	1359.05	450.525	Power Supply
LOAM	OUT-	12	1359.05	630.525	Inverted Data Output
LAOP	OUT+	13	1359.05	810.525	Noninverted Data Output
VCCA	VCC	14	1359.05	990.525	Power Supply
SQ	SQUELCH	15	1359.05	1170.525	Squelch Input. Squelch is disabled if this pin is unconnected or set LOW. When SQUELCH is HIGH, OUT+ and OUT- are forced to static levels. See *Detailed Description* section.
NC	—	—/16	1169.475	1359.05	No Connection

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Detailed Description

The VSC7961 is a high-speed limiting amplifier with Loss of Signal (LOS) detect. The device is designed to operate with a 3.3V or 5V supply in SDH/SONET and Fibre Channel applications up to 3.125Gb/s. The VSC7961 has positive emitter-coupled logic (PECL) outputs. The VSC7959 provides the same functionality as the VSC7961 with current-mode logic (CML) outputs. The key features of the VSC7961 are Loss-of-Signal (LOS) detect, output offset correction, output squelch, low power supply current, and fast rise and fall times.

The inputs of the device provide 100Ω input impedance between IN+ and IN- and are intended to be DC-coupled. The PECL output circuits should be terminated through 50Ω to V_{CC} - 2V.

Loss of Signal (LOS) Detect

This feature utilizes an rms power detector with programmable LOS indicator to provide two outputs, LOS and $\overline{\text{LOS}}$. The input TH is used to set the threshold at which the loss of signal detector outputs, LOS and $\overline{\text{LOS}}$, change state. See Loss of Signal Specifications (Table 3) for setting the resistor value between TH and ground. The Loss-of-Signal Truth Table (Table 4) clarifies how LOS and SQUELCH interact.

Optional Squelch

Squelch is disabled when SQUELCH is not connected or is set to TTL low level. When SQUELCH is set to TTL high level and LOS is asserted, the data outputs, OUT+ and OUT- are forced to static levels. If LOS is not asserted, the outputs will not be squelched.

Offset Correction

This feature is provided to ensure that the offsets in the amplifier coupled with its gain do not cause the output buffer to give a false output. Because of the high gain of the amplifier, offset correction using a low-frequency feedback loop reduces input offset. If no component is placed between pins CZ1 and CZ2, the low frequency cut-off is 2MHz. If a 0.1µF capacitor is placed between CZ1 and CZ2, the low frequency cut-off is lowered to about 2kHz. For Fibre Channel and Gigabit Ethernet applications, leave pins CZ1 and CZ2 open. For ATM/SONET and other scrambled non-return-to-zero (NRZ) applications, place a 0.1µF capacitor between CZ1 and CZ2. This maintains a one-decade separation between the lowest input frequency and the low frequency cut-off. The low frequency cut-off of the offset correction loop is given by the following equation:

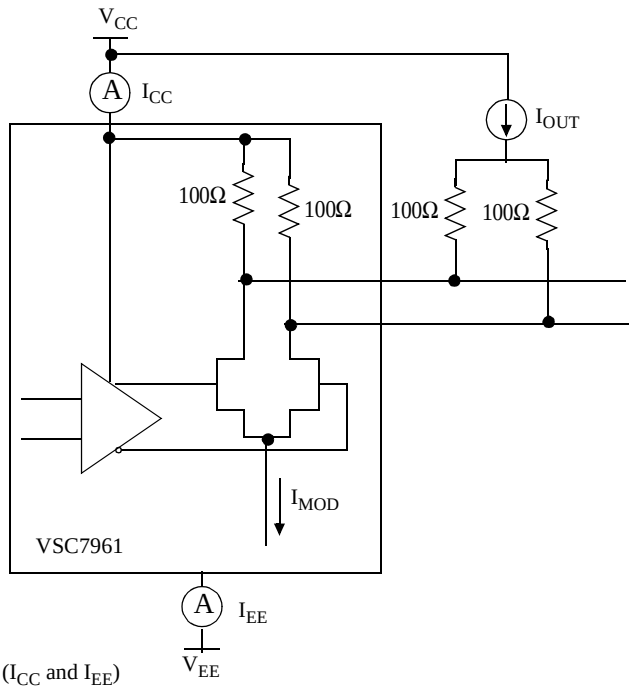
$$f_{OC} = 43 / [2\pi * 35k\,(C_Z + 100pF)]$$
$$= 196 * 10^{-6} / (C_Z + 100pF)$$
$$= 196 * 10^{-6} / (0.1\mu F + 100pF)$$
$$= 1.96kHz$$

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Output Level Control

The LEVEL pin adjusts the output levels to 20mA when grounded and to 16mA when left unconnected.

Figure 3: Supply Current Measurement



Supply Current (I_{CC} and I_{EE})

Applications Information

Wire Bonding

For best performance, gold ball-bonding techniques are recommended. To minimize inductance, keep wire bond lengths short.

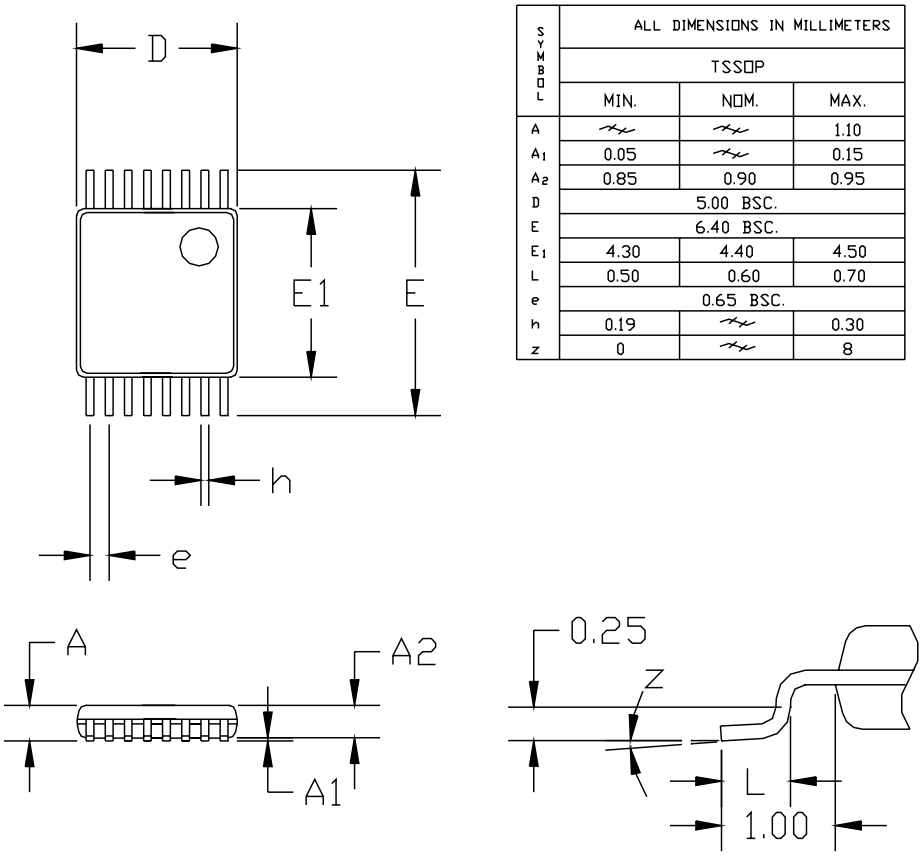
PCB Layout Guidelines

Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. Short input and output traces will provide best performance.

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Package Information

TSSOP-16



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	TSSOP		
	MIN.	NOM.	MAX.
A	---	---	1.10
A_1	0.05	---	0.15
A_2	0.85	0.90	0.95
D	5.00 BSC.		
E	6.40 BSC.		
E_1	4.30	4.40	4.50
L	0.50	0.60	0.70
e	0.65 BSC.		
h	0.19	---	0.30
z	0	---	8

1. All dimensioning and tolerancing per ASME. Y14.5-1994
2. Controlling dimension: millimeter
3. This outline conforms to JEDEC Publication 95 Registration MS-026

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Ordering Information

The order number for this product is formed by a combination of the device type and package type.

VSC7961 xx

Device Type
3.125Gb/s PECL Limiting Amplifier with LOS Detect

Package
YD: TSSOP-16
W: Dice Waffle Pack

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