BVA304B

DIGITAL VARIABLE GAIN AMPLIFIER

50-4000 MHz

Product Description

The BVA304B is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 3.3V supply with a broad-band frequency range of 50 to 4000 MHz.

The BVA304B integrates a high performance digital step attenuator and a high linearity, broadband gain block.
using the small package(4x4mm QFN package) and operating V_{DD} 3.3V voltage. and designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

Both stages are internally matched to 50 Ohms and It is easy to use with no external matching components required.

A serial output port enables cascading with other serial controlled devices.

An integrated digital control interface supports both serial and parallel programming of the attenuation,
including the capability to program an initial attenuation state at power-up.
Covering a 31.5 dB attenuation range in 0.5 dB steps.

The BVA304B is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Figure 1. Functional Block Diagram

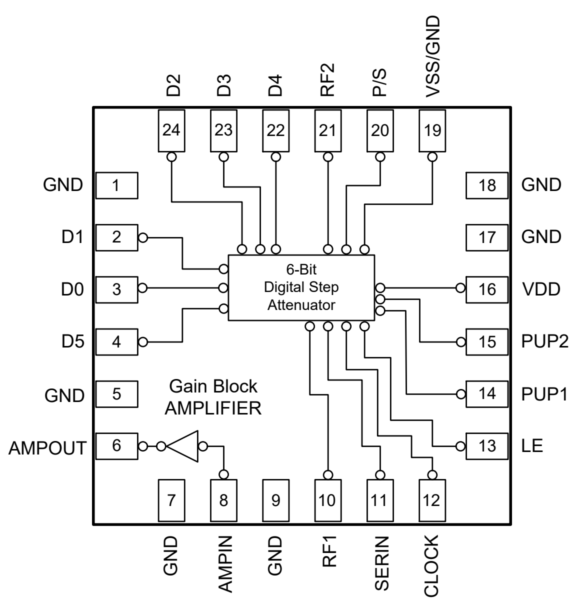


Figure 2. Package Type

24-lead 4x4 mm QFN

Device Features

- Small 24-Pin 4 x 4 mm QFN Package
- Integrate DSA to Amp Functionality
- Wide Power supply range of +2.7 to +5.5V(DSA)
- Single Fixed +3.3V supply(Amp)
- 50-4000MHz Broadband Performance
- 12.8dB Gain at 2.14GHz
- 3.5dB Noise Figure at max gain setting at 2.14GHz
- 19.3dBm P1dB at 2.14GHz
- 33.3dBm OIP3 at 2.14GHz
- No matching circuit needed
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy(DSA to Amp)
  ±(0.15 + 5% x Atten) @ 2.14 GHz
- 1.8V control logic compatible
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection

Application

- 3G/4G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			50		4000	MHz
Gain[2]		Attenuation = 0dB, at 1900MHz	12.5	13.5	14.5	dB
Attenuation Control range		0.5dB Step		31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	50MHz — 1GHz	Any bit or bit combination			±(0.15 + 3% of atten setting)	dB
	>1GHz — 2.2GHz				±(0.15 + 5% of atten setting)	
	>2.2GHz — 3GHz				±(0.15 + 8% of atten setting)	
	>3GHz — 4GHz				±(0.15 + 11% of atten setting)	
Return loss (input or output port)	1GHz — 2.2GHz	Attenuation = 0dB	17	22		dB
	>2.2GHz — 4GHz		8	13		
Output Power for 1dB Compression		Attenuation = 0dB , at 1900MHz		19.4		dBm
Output Third Order Intercept Point[3]		Attenuation = 0dB, at 1900MHz two tones at an output of –3 dBm per tone separated by 1 MHz.		33.2		dBm
Noise Figure		Attenuation = 0dB, at 1900MHz		3.4		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		3.3		V
Supply Current			21	26	31	mA
Control Interface		Serial / parallel mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Impedance				50		Ω

[1] Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3.3V, measure on Evaluation Board (DSA to AMP)
[2] Gain data has PCB & Connectors insertion loss de-embedded
[3] OIP3 _ measured with two tones at an output of –3 dBm per tone separated by 1 MHz.

Table 2. Typical RF Performance[1]

Parameter	Frequency					Unit
	70[2]	900[3]	1900[4]	2140[4]	2650[4]	MHz
Gain[5]	23.7	18.3	13.5	12.8	11.1	dB
S11	-17.8	-18.1	-23.7	-35.9	-15.1	dB
S22	-13.6	-13.8	-14.8	-19.4	-18.8	dB
OIP3[6]	30.3	28.7	33.2	33.3	31.8	dBm
P1dB	20.5	19.8	19.4	19.3	19.0	dBm
Noise Figure	3.2	3.3	3.4	3.5	4.1	dB

[1] Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3.3V,50 Ω system. measure on Evaluation Board (DSA to AMP)

[2] 70MHz measured with application circuit refer to table 13.

[3] 900MHz measured with application circuit refer to table 15

[4] 1900MHz,2140MHz,2650MHz measured with application circuit refer to table 17

[5] Gain data has PCB & Connectors insertion loss de-embedded

[6] OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(VDD)	Amp/DSA			5.0/5.5	V
Supply Current	Amp		110		mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+24/+30	dBm
Operating Temperature	Amp/DSA	-40		85/105	℃
Storage Temperature		-55		150	℃
Junction Temperature			220		℃

Operation of this device above any of these parameters may result in permanent damage.

Figure 3. Pin Configuration(Top View)

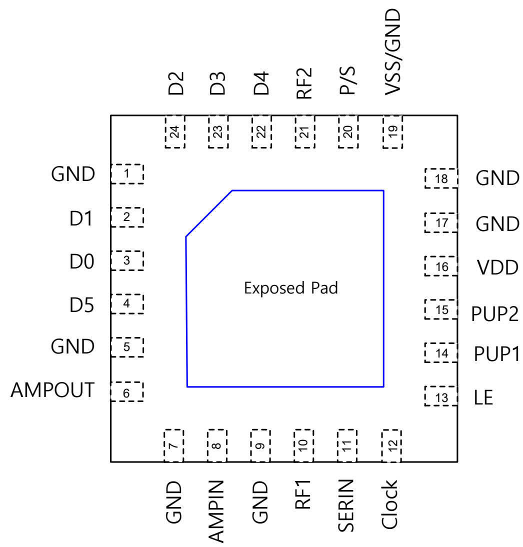


Table 4. Pin Description

Pin	Pin name	Description
1,5,7,9,17,18	GND	Ground, These pins must be connected to ground
2	D1	Parallel Control Voltage Inputs, Attenuation control bit 1dB
3	D0	Parallel Control Voltage Inputs, Attenuation control bit 0.5dB
4	D5	Parallel Control Voltage Inputs, Attenuation control bit 16dB
6	AMPOUT	RF Gain block Amplifier output Port
8	AMPIN	RF Gain block Amplifier input Port
10	RF1[1]	RF1 port (Digital Step Attenuator RF Input) This pin can also be used as an output because the design is bidirectional. RF1 is dc-coupled and matched to 50 Ω
11	SERIN	Serial interface data input
12	Clock	Serial interface clock input
13	LE	Latch Enable input
14	PUP1	Power-Up State Selection Bits. These pins set the attenuation value at power-up (see Table 9). There is no internal pull-up or pull- down
15	PUP2	resistor on these pins; therefore, they must always be kept at a valid logic level (V_{CTLH} or V_{CTLL}) and not be left floating
16	VDD	DSA Power Supply (nominal 3.3V)
19	VSS/GND[2]	External V_{SS} negative voltage control or ground Do not want to use negative voltage supply, These pins must be connected to ground (GND, Default setting is GND)
20	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to low. For serial mode operation, set this pin to High.
21	RF2[1]	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bidirectional. RF2 is dc-coupled and matched to 50 Ω.
22	D4	Parallel Control Voltage Inputs, Attenuation control bit 8dB
23	D3	Parallel Control Voltage Inputs, Attenuation control bit 4dB
24	D2	Parallel Control Voltage Inputs, Attenuation control bit 2dB
EXPOSE PAD	GND	Exposed pad: The exposed pad must be connected to ground for proper operation

Note: 1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met
2. Connect VssEXT (pin 19, VssEXT = GND) to enable internal negative voltage generator

Programming Options

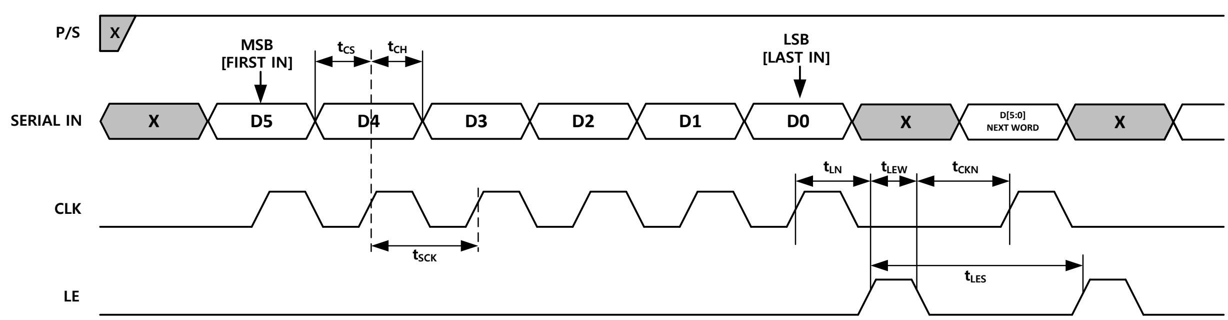
BVA304B can be programmed using either the parallel or serial inter-face, which is selectable via P/S pin(Pin20).
Serial mode is selected by floating P/S or pulling it to a voltage logic LOW and parallel mode is selected by setting P/S to logic low

Serial Control Mode
The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (2,3,4,22,23,24) **must** be grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 5. 6-Bit Serial Word Sequence

D5	Attenuation 16dB Control Bit
D4	Attenuation 8dB Control Bit
D3	Attenuation 4dB Control Bit
D2	Attenuation 2dB Control Bit
D1	Attenuation 1dB Control Bit
D0	Attenuation 0.5dB Control Bit

Figure 4. Serial Mode Resister Timing Diagram



The BVA304B has a 3-wire serial peripheral interface (SPI): serial data input (Data), clock (CLK), and latch enable (LE). The serial control inter-face is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled High to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept High (see Figure 4 and Table 8).

Table 6. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

Table 7. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
fClk	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			
t_{CS}	Control setup time	30			
t_{CH}	Control hold time	30			
t_{LN}	LE setup time	10			
t_{LEW}	Minimum LE pulse width	10			
t_{LES}	Minimum LE pulse width		600		
t_{CKN}	Serial clock hold time from LE	10			

Table 8. Truth Table for Serial Control Word

Digital Control Input						Attenuation
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	(dB)
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	0 (Reference)
HIGH	HIGH	HIGH	HIGH	HIGH	LOW	0.5
HIGH	HIGH	HIGH	HIGH	LOW	HIGH	1
HIGH	HIGH	HIGH	LOW	HIGH	HIGH	2
HIGH	HIGH	LOW	HIGH	HIGH	HIGH	4
HIGH	LOW	HIGH	HIGH	HIGH	HIGH	8
LOW	HIGH	HIGH	HIGH	HIGH	HIGH	16
LOW	LOW	LOW	LOW	LOW	LOW	31.5

Parallel Control Mode
The BVA304B has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 9. The parallel control interface is activated when P/S is set to low. There are two modes of parallel operation: direct parallel and latched parallel

Direct Parallel Mode
The LE pin must be kept LOW. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 2, 3, 4, 22,23, 24]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode
The LE pin must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled LOW to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 5 and Table 9).

Figure 5. Latched Parallel Mode Timing Diagram

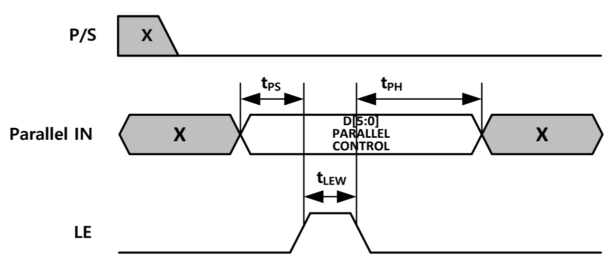


Table 9. Truth Table for the Parallel Control Word

D0	D1	D2	D3	D4	D5	P/S	LE	Attenuation State
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	Reference Loss
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0.5dB
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	1dB
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	2dB
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	4dB
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	8dB
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	16dB
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5dB

Table 10. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Power-UP Interface
The BVA304B uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in either serial or parallel mode. When the attenuator powers up with LE set to low, the state of PUP1 and PUP2 determines the power-up state of the device per the truth table shown in Table 11. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Table 11. PUP Truth Table

Attenuation state	P/S	LE	PUP1	PUP2
31.5 dB	LOW	LOW	HIGH	HIGH
16 dB	LOW	LOW	HIGH	LOW
8 dB	LOW	LOW	LOW	HIGH
Reference Loss	LOW	LOW	LOW	LOW
Defined by C0.5-C16	LOW	HIGH	Don’t Care	Don’t Care

Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:50~500MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

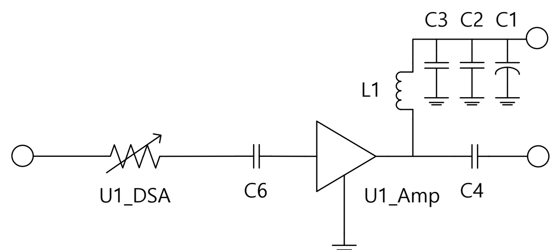
Table 12. Typical RF Performance(50~500MHz)

parameter	Frequency		Unit
	70	200	MHz
Gain[1]	23.7	23.3	dB
S11	-17.8	-21.2	dB
S22	-13.6	-18.7	dB
OIP3[2]	30.3	29.6	dBm
P1dB	20.5	20.8	dBm
N.F	3.2	3.6	dB

[1] Gain data has PCB & Connectors insertion loss de-embedded

[2] OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 13. 50~500MHz IF Application Circuit



Application Circuit Values	Freq.	IF Circuit
		50MHz ~ 500MHz
	C6/C4	2.2nF
	L1(1005 Chip Ind)	330nH

Figure 6. Gain vs. Frequency

over Temperature

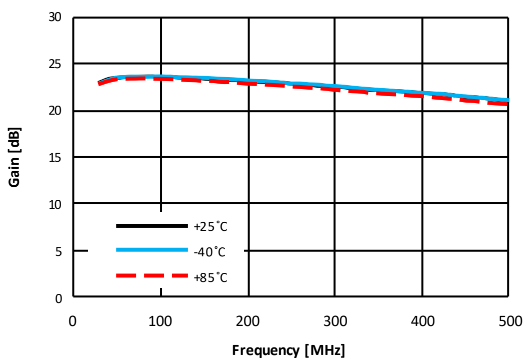


Figure 7. Gain vs. Frequency

over Major Attenuation States

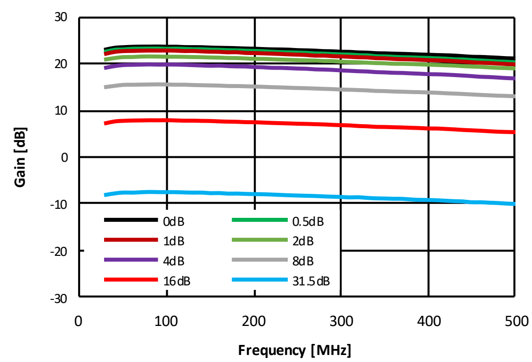


Figure 8. Input Return Loss vs. Frequency

over Major Attenuation States

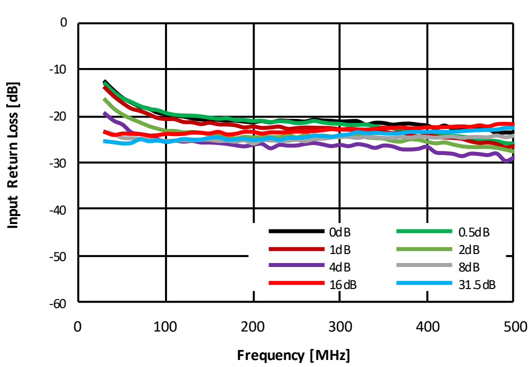
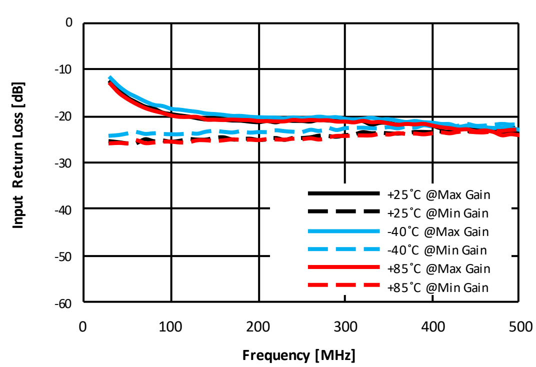


Figure 9. Input Return Loss vs. Frequency

over Temperature (Min,Max Gain State)



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:50~500MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

Figure 10. Output Return Loss vs. Frequency
over Major Attenuation States

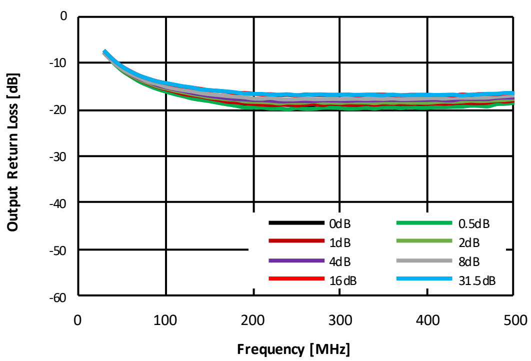
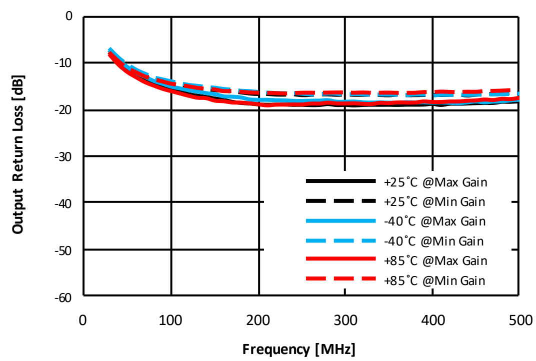


Figure 11. Output Return Loss vs. Frequency
over Temperature (Min[1], Max Gain State)



* [1]Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 12. OIP3 vs. Frequency
Over Temperature (Max Gain State)

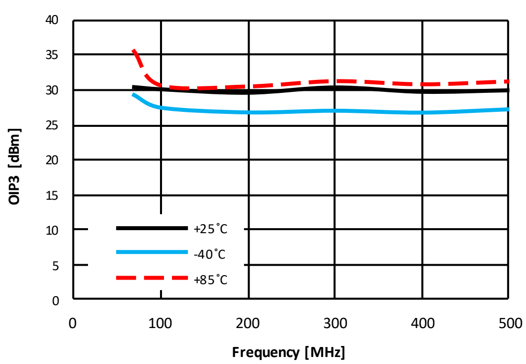


Figure 13. OIP3 vs. Frequency
Over Temperature (15.5dB Atteuation State)

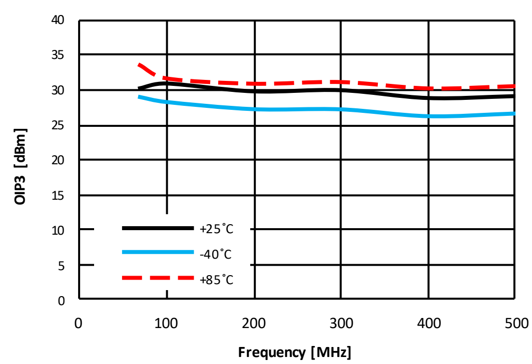


Figure 14. P1dB vs. Frequency
Over Temperature (Max Gain State)

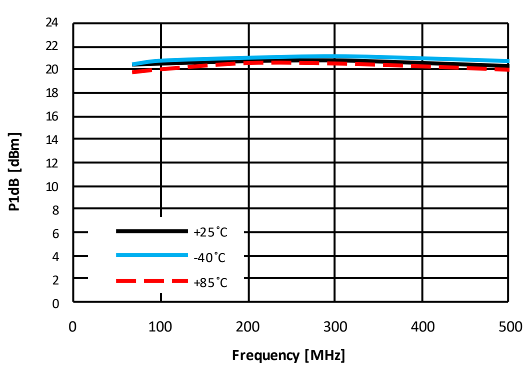
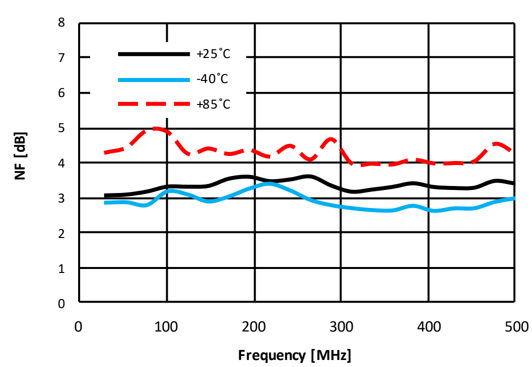


Figure 15. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:50~500MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

Figure 16. Attenuation Error vs Frequency
over Major Attenuation Steps

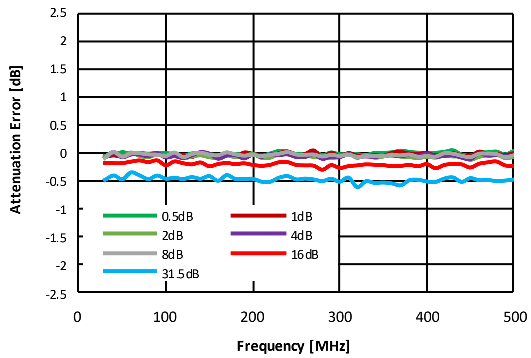


Figure 17. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

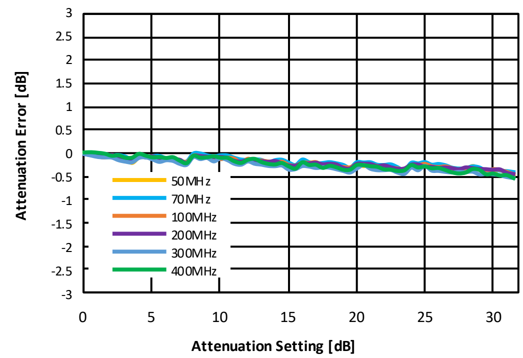


Figure 18. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency

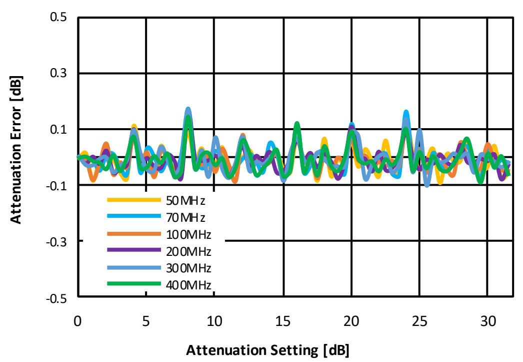


Figure 19. Attenuation Error at 50MHz vs Temperature
Over All Attenuation States

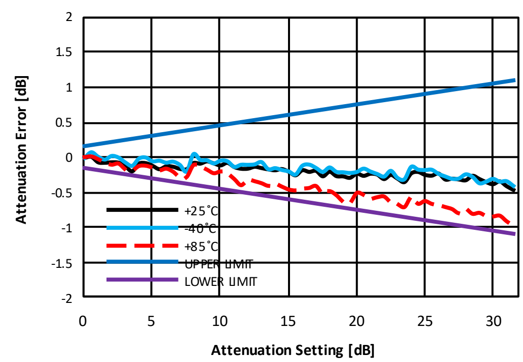


Figure 20. Attenuation Error at 70MHz vs Temperature
Over All Attenuation States

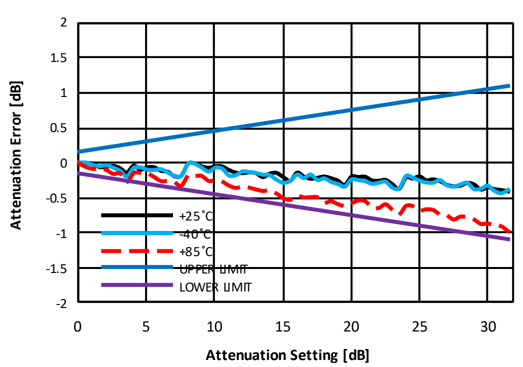
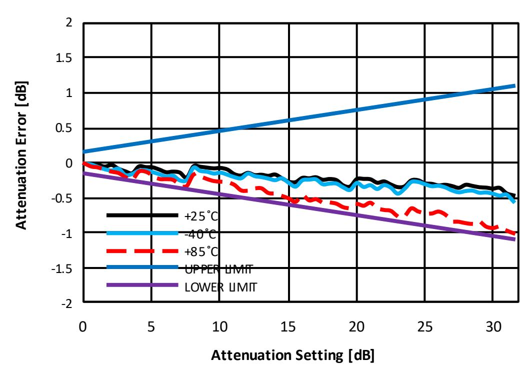


Figure 21. Attenuation Error at 200MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:500~1700MHz)

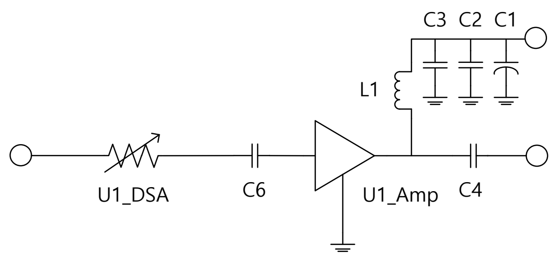
Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Table 14. Typical RF Performance(500~1700MHz)

parameter	Frequency					Unit
	700	800	900	1000	1100	MHz
Gain[1]	19.6	18.9	18.3	17.7	17.0	dB
S11	-13.3	-15.1	-18.1	-19.5	-21.5	dB
S22	-12.9	-13.5	-13.8	-14.2	-14.4	dB
OIP3[2]	29.6	29.1	28.7	28.5	28.9	dBm
P1dB	20.1	20.0	19.8	19.7	19.7	dBm
N.F	3.2	3.2	3.3	3.3	3.3	dB

[1] Gain data has PCB & Connectors insertion loss de-embedded
[2] OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 15. 500~1700MHz RF Application Circuit



Application Circuit Values	Freq.	RF Circuit
		500MHz ~ 1700MHz
	C6/C4	56pF
	L1(1005 Chip Ind)	22nH

Figure 22. Gain vs. Frequency
over Temperature (Max Gain State)

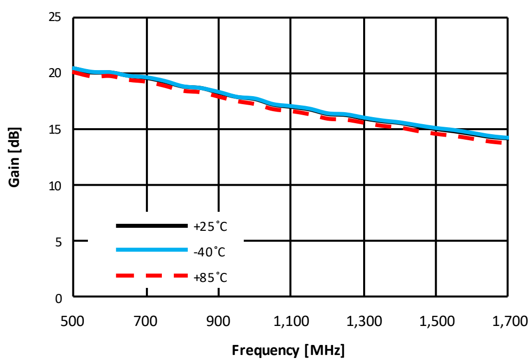


Figure 23. Gain vs. Frequency
over Major Attenuation States

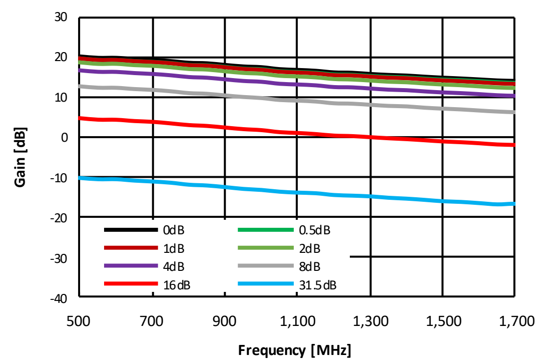


Figure 24. Input Return Loss vs. Frequency
over Major Attenuation States

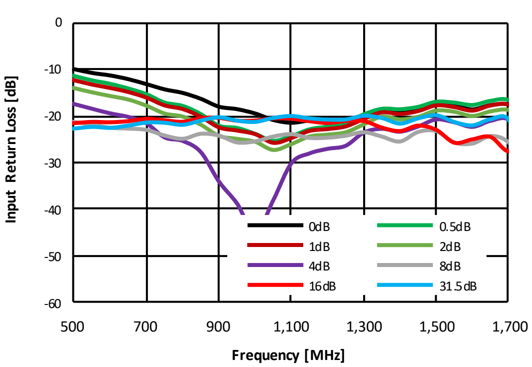
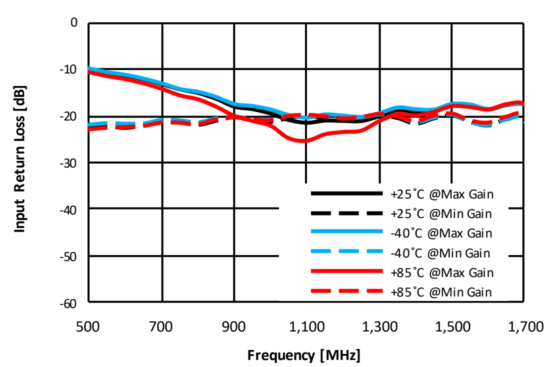


Figure 25. Input Return Loss vs. Frequency
over Temperature (Min[1],Max Gain State)



* [1]Min Gain was measured in the state is set with attenuation 31.5dB.

Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:500~1700MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Figure 26. Output Return Loss vs. Frequency
over Major Attenuation States

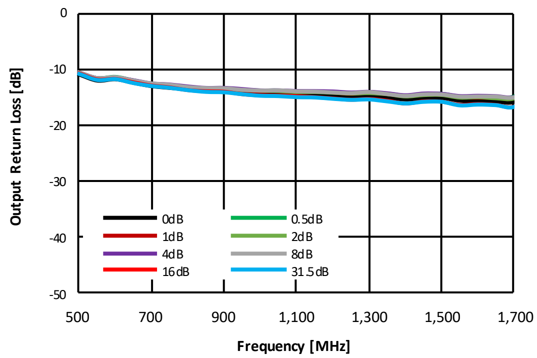
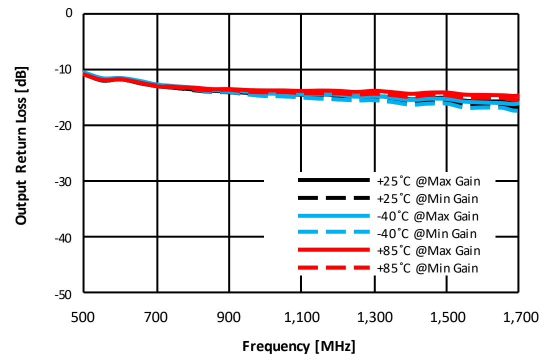


Figure 27. Output Return Loss vs. Frequency
over Temperature (Min[1], Max Gain State)



* [1]Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 28. OIP3 vs. Frequency
Over Temperature (Max Gain State)

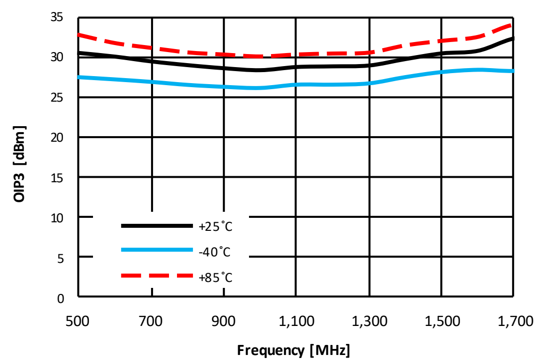


Figure 29. OIP3 vs. Frequency
Over Temperature (15.5dB Atteuation State)

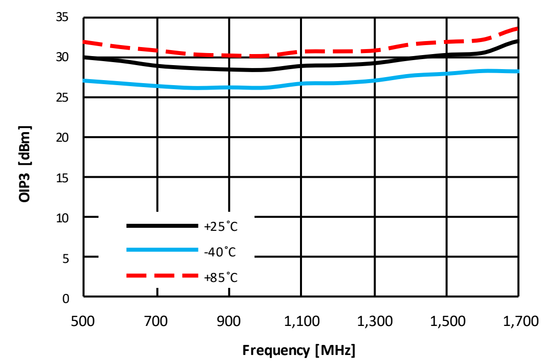


Figure 30. P1dB vs. Frequency
Over Temperature (Max Gain State)

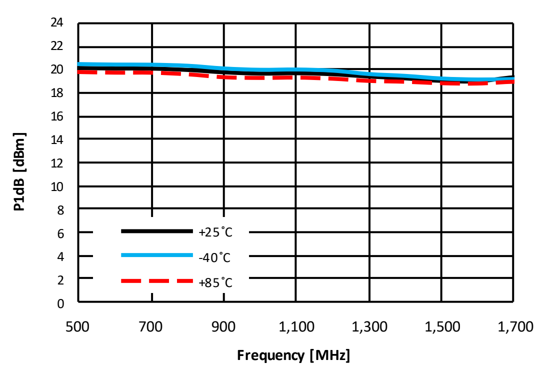
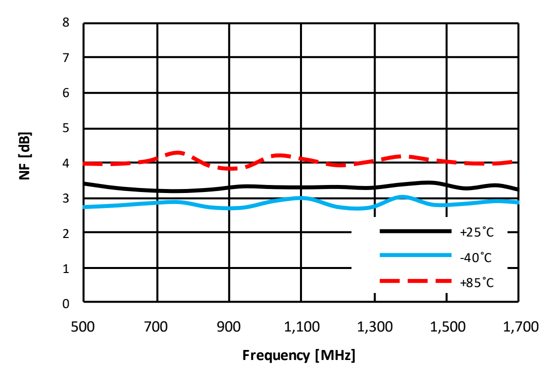


Figure 31. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:500~1700MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Figure 32. Attenuation Error vs Frequency
over Major Attenuation Steps

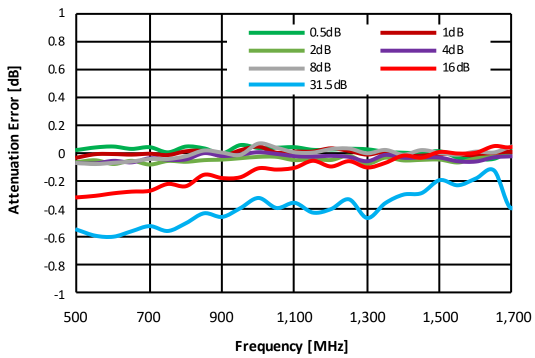


Figure 33. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

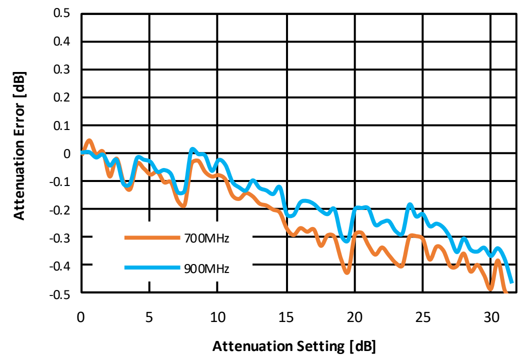


Figure 34. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency (Max Gain State)

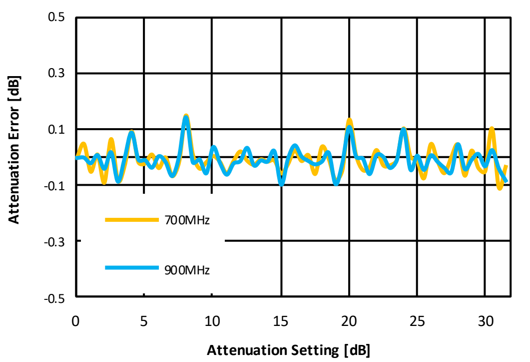
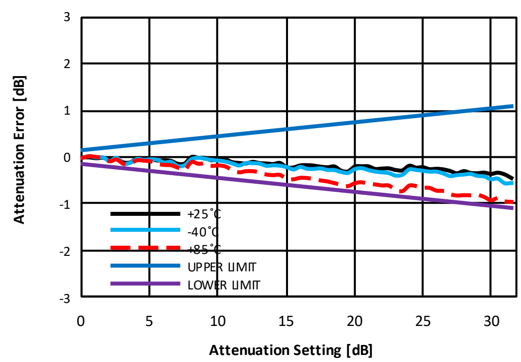


Figure 35. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:1700~4000MHz)

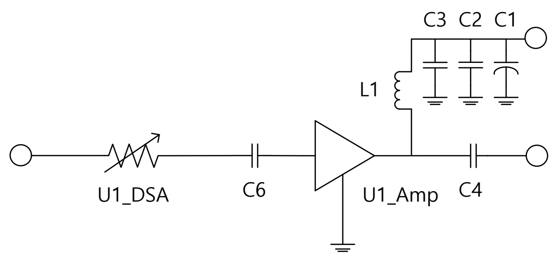
Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Table 16. Typical RF Performance(1700~4000MHz)

parameter	Frequency					Unit
	1700	1900	2140	2650	3500	MHz
Gain[1]	14.2	13.5	12.8	11.1	7.5	dB
S11	-17.6	-23.7	-35.9	-15.1	-8.7	dB
S22	-15.7	-14.8	-19.4	-18.8	-11.6	dB
OIP3[2]	32.4	33.2	33.3	31.8	31.8	dBm
P1dB	19.4	19.4	19.3	19.0	18.4	dBm
N.F	3.2	3.4	3.5	4.1	5.2	dB

[1] Gain data has PCB & Connectors insertion loss de-embedded
[2] OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 17. 1700~4000MHz RF Application Circuit



Application Circuit Values	Freq.	RF Circuit
		1700MHz ~ 4000MHz
	C6/C4	10pF
	L1(1005 Chip Ind)	7.5nH

Figure 36. Gain vs. Frequency
over Temperature (Max Gain State)

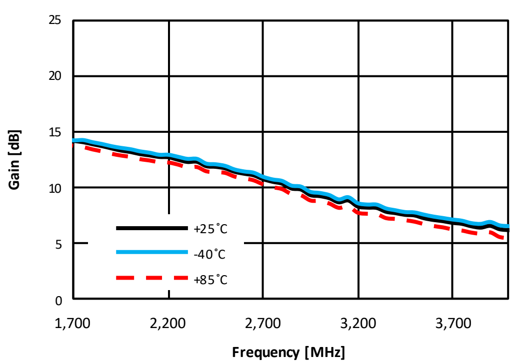


Figure 37. Gain vs. Frequency
over Major Attenuation States

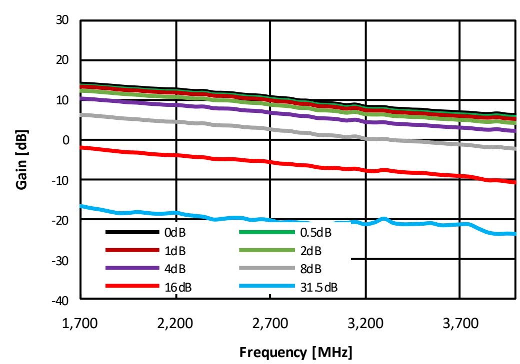


Figure 38. Input Return Loss vs. Frequency
over Major Attenuation States

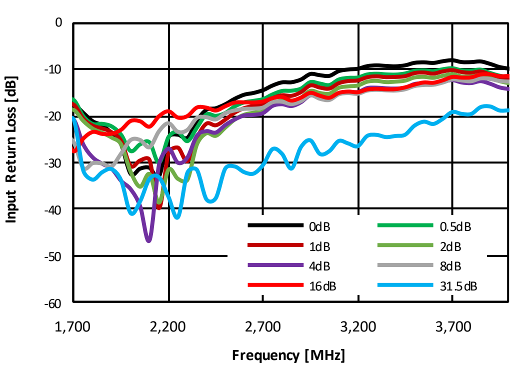
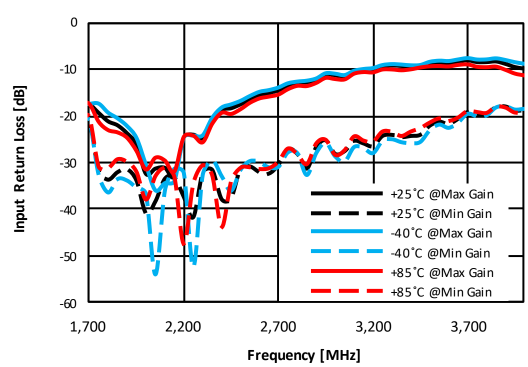


Figure 39. Input Return Loss vs. Frequency
over Temperature (Min[1],Max Gain State)



* [1]Min Gain was measured in the state is set with attenuation 31.5dB.

Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:1700~4000MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Figure 40. Output Return Loss vs. Frequency
over Major Attenuation States

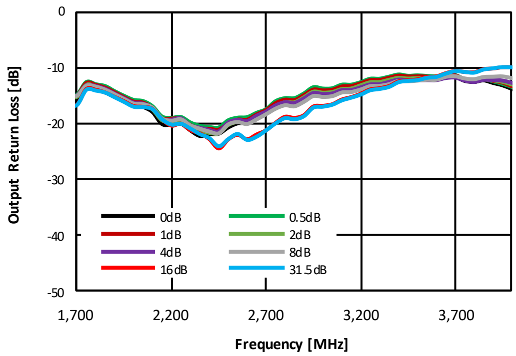
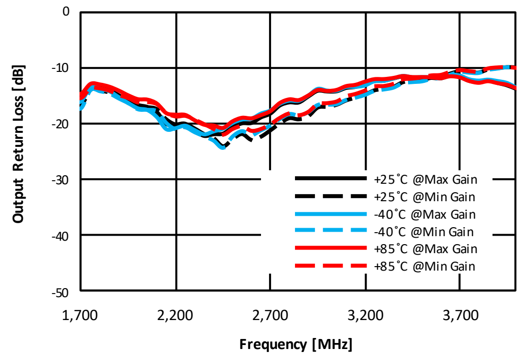


Figure 41. Output Return Loss vs. Frequency
over Temperature (Min[1], Max Gain State)



* [1]Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 42. OIP3 vs. Frequency
Over Temperature (Max Gain State)

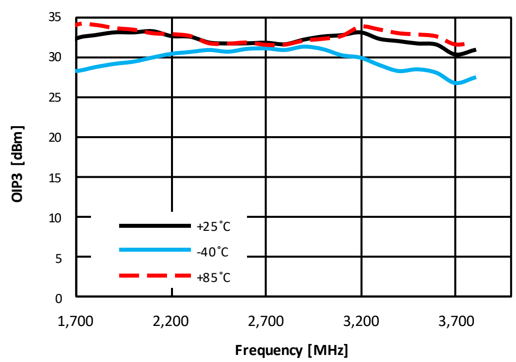


Figure 43. OIP3 vs. Frequency
Over Temperature (15.5dB Atteuation State)

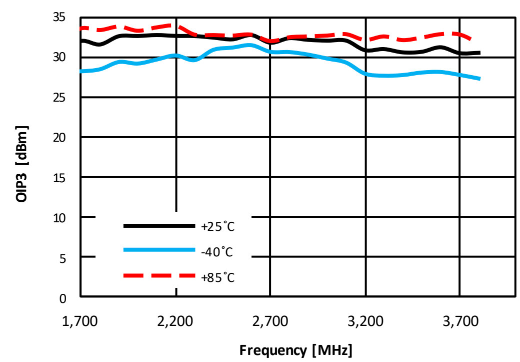


Figure 44. P1dB vs. Frequency
Over Temperature (Max Gain State)

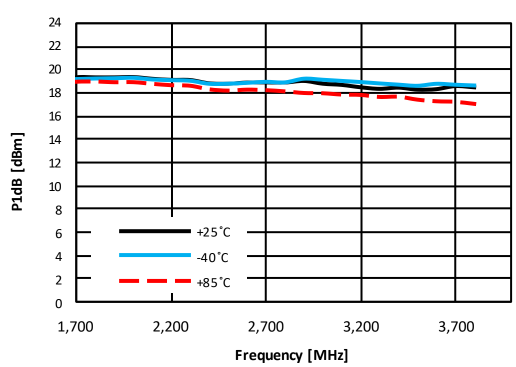
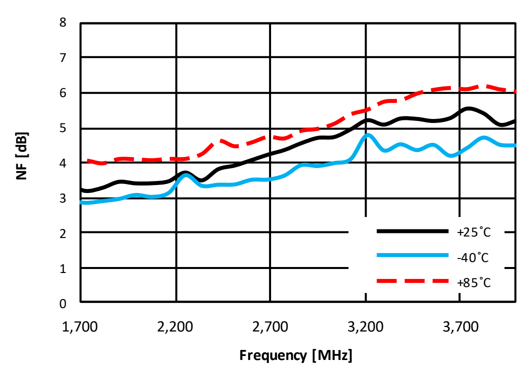


Figure 45. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:1700~4000MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Figure 46. Attenuation Error vs Frequency
over Major Attenuation Steps

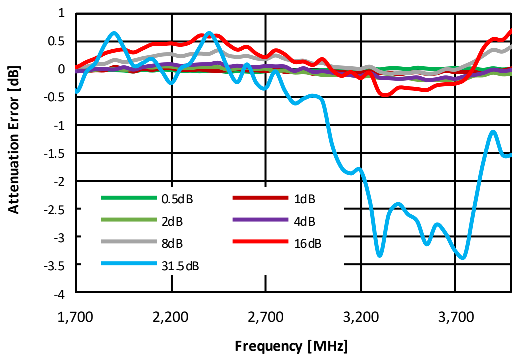


Figure 47. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

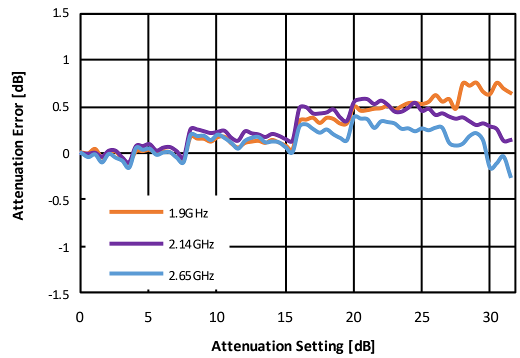


Figure 48. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency (Max Gain State)

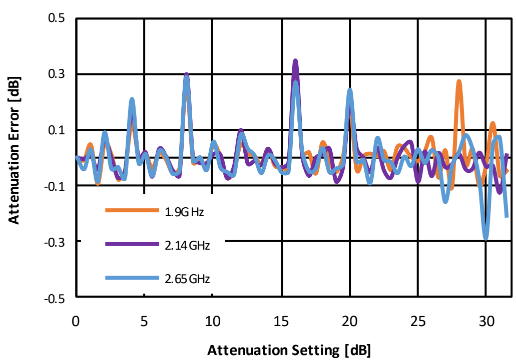


Figure 49. Attenuation Error at 1.9GHz vs Temperature
Over All Attenuation States

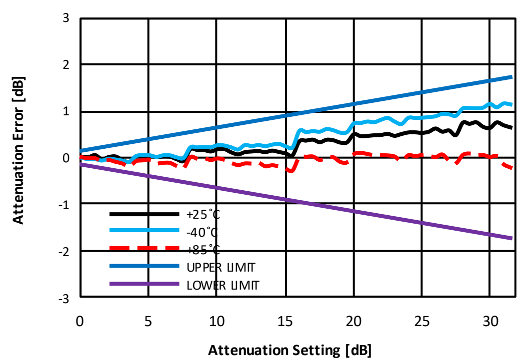


Figure 50. Attenuation Error at 2.14GHz vs Temperature
Over All Attenuation States

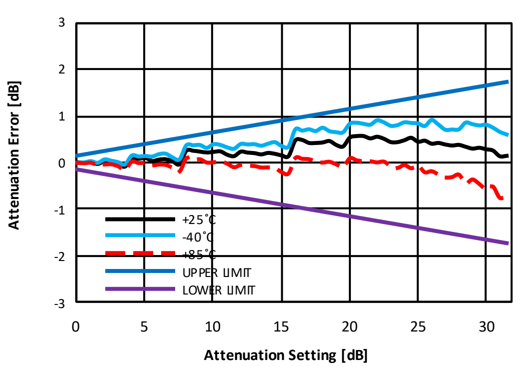
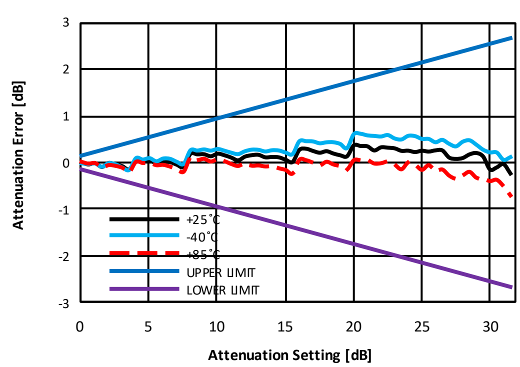


Figure 51. Attenuation Error at 2.65GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA304B EVK - PCB (Application Circuit:1700~4000MHz)

Typical Performance Data @ 25°and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Figure 52. Attenuation Error at 3.9GHz vs Temperature

Over All Attenuation States

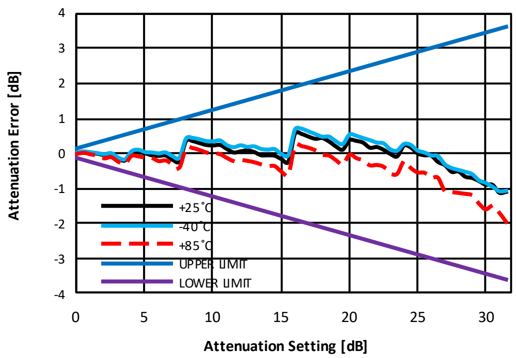


Figure 53. Evaluation Board Schematic

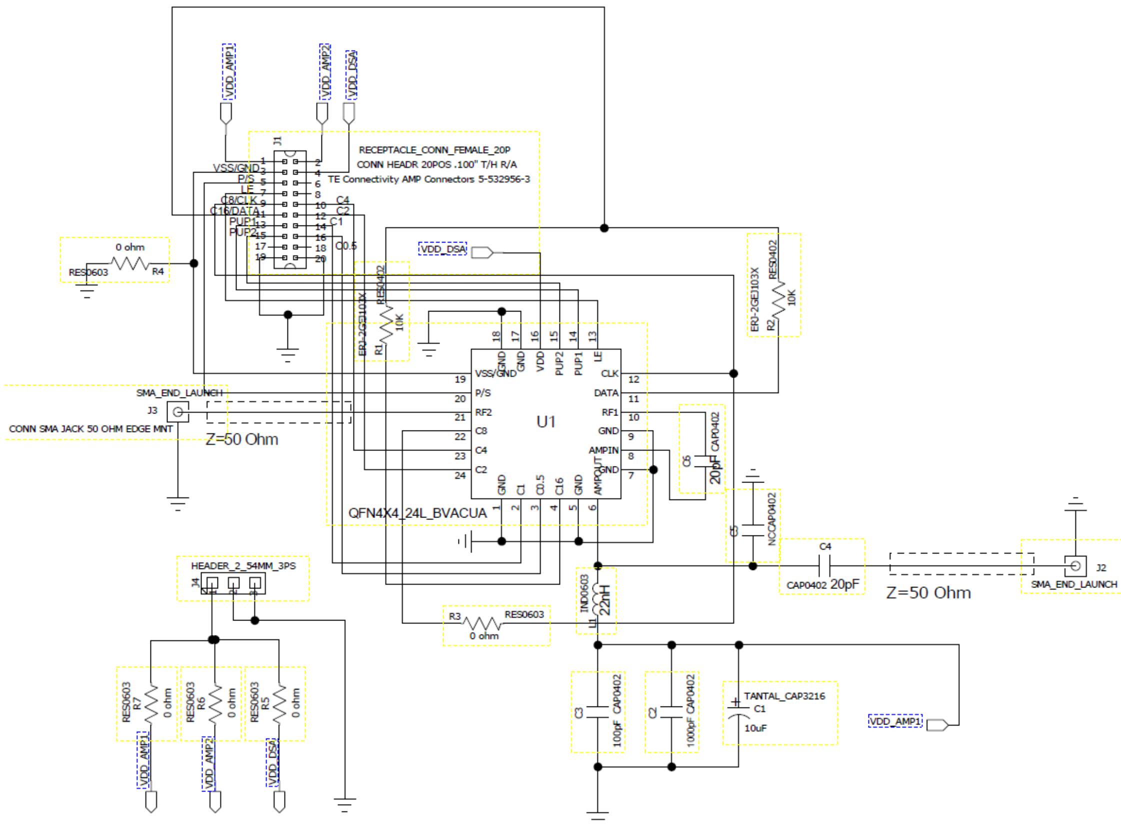


Figure 54. Evaluation Board PCB

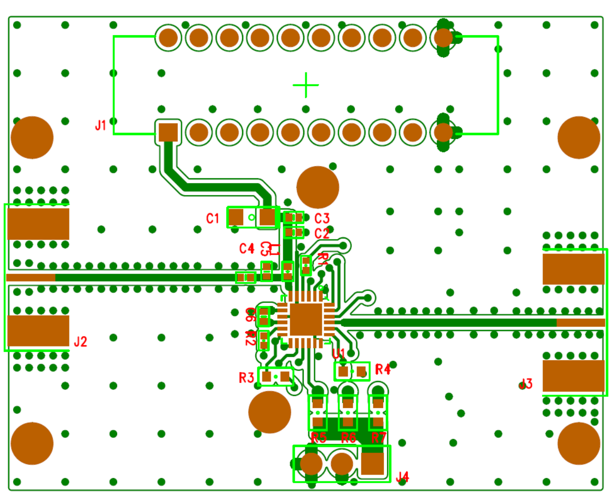


Table 18. Application Circuit

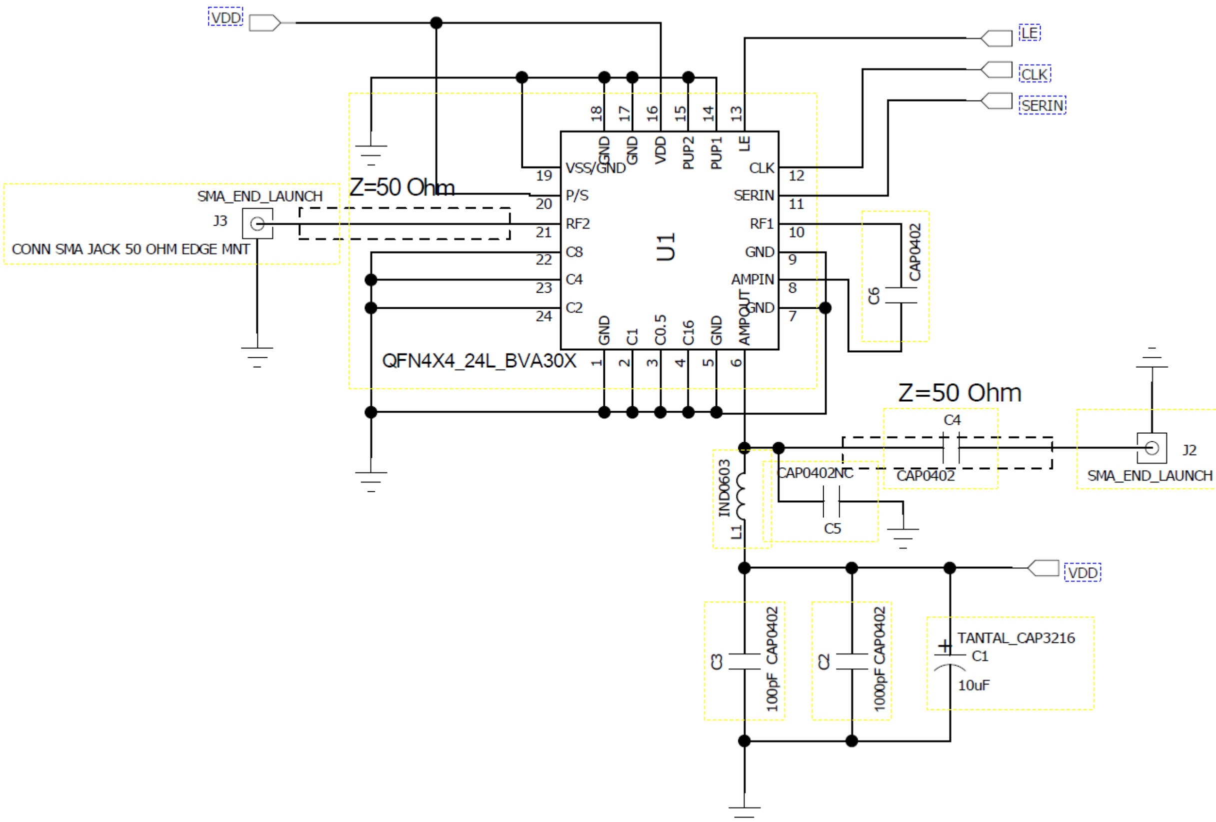
Application Circuit Values Example			
Freq.	IF Circuit 50~500MHz	RF Circuit 500MHz ~ 1.7GHz	RF Circuit 1.7GHz ~ 4GHz
C6/C4	2nF	56pF	10pF
L1(1005 Chip Ind)	820nH	22nH	7.5nH

Table 19. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C4,C6	2	CAP 0402 10pF J 50V	Another circuit refer to table 18
2	C2	1	CAP 0402 1000pF J 50V	
3	C1	1	TANTAL 3216 10UF 16V	
4	C22	1	TANTAL 3216 0.1uF 35V	
5	L1	1	IND 1608 7.5nH	Another circuit refer to table 18
6	C3	1	CAP 0402 100pF J 50V	
7	R1,R2	2	RES 1005 J 10K	
8	R3,R4,R5,R7	3	RES 1608 J 0ohm	
9	J1	1	Receptacle connector	
10	U1	1	QFN4X4_24L_BVA304B	
11	J2,J3	2	SMA_END_LAUNCH	

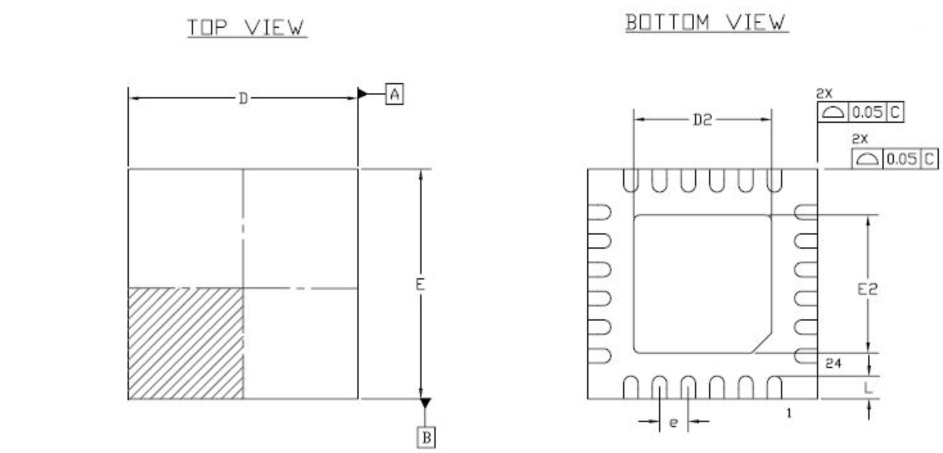
Notice: Evaluation Board for Marketing Release was set to 1.7GHz to 4GHz application circuit (Refer to Table 17)

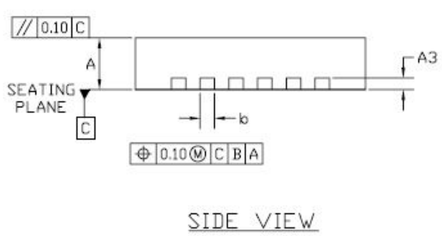
Figure 55. Application Circuit schematic*
(Use only Serial mode)



* notice. The serial mode PUP state of this Figure. 55 is setting in Reference Loss (Refer to Table 11.) and each combinations of C0.5-C16 are shown in the Table 8. Truth Table.

Figure 55. Package Outline Dimension





NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATION 'A'					
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.925	4.00	4.075	0.154	0.157	0.160
D2	2.30	2.40	2.50	0.090	0.094	0.098
E	3.925	4.00	4.075	0.154	0.157	0.160
E2	2.30	2.40	2.50	0.090	0.094	0.098
e	0.500 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017

SYMBOL	VARIATION 'A'					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
QFN	0.85	0.90	0.95	0.033	0.035	0.037
TQFN	0.70	0.75	0.80	0.027	0.029	0.031

Figure 56. Evaluation Board PCB Layer Information

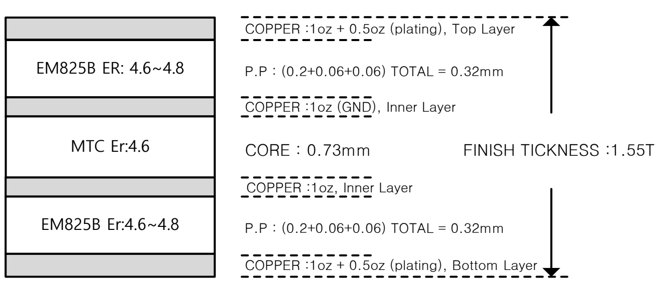


Figure 57. Recommend Land Pattern

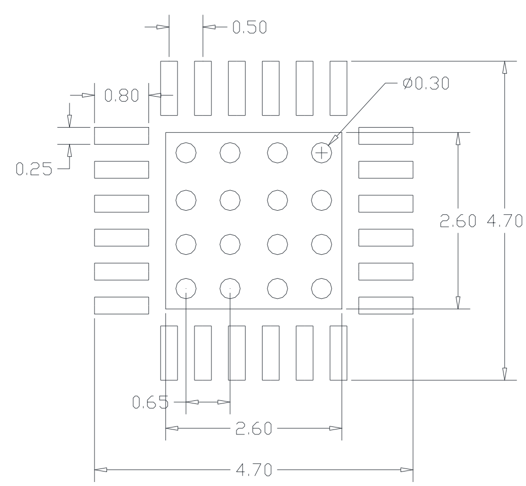
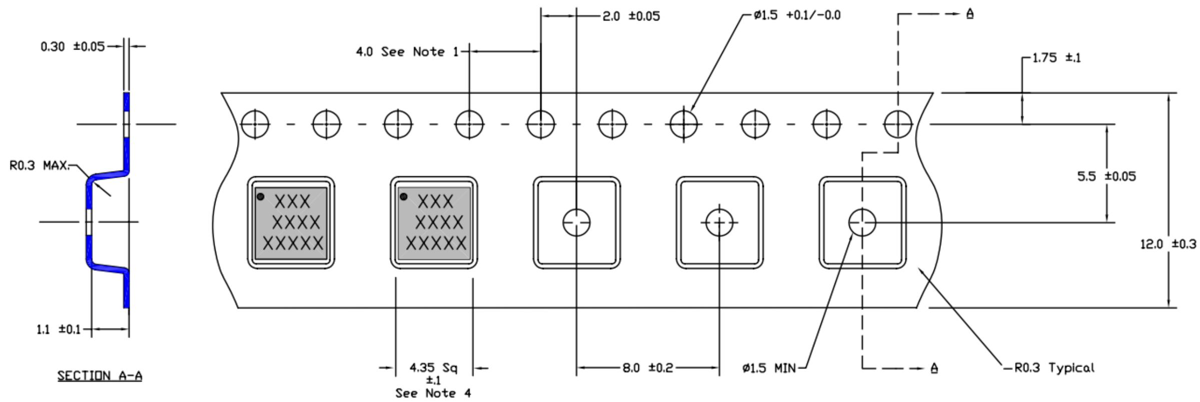


Figure 58. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 59. Package Marking

Marking information:	
BVA304B	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Lead plating finish

100% Tin Matte finish

MSL / ESD Rating

ESD Rating: Class 1C

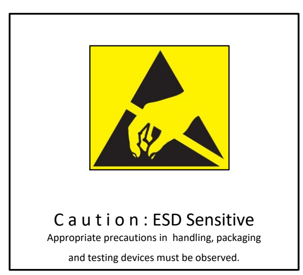
Value: Passes ≤ 2000V

Test: Human Body Model(HBM)

Standard: JEDEC Standard JESD22-A114B

MSL Rating: **Level 1 at +265°C convection reflow**

Standard: JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

NATO CAGE code:

2	N	9	6	F