

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOSIV)

2SK3565

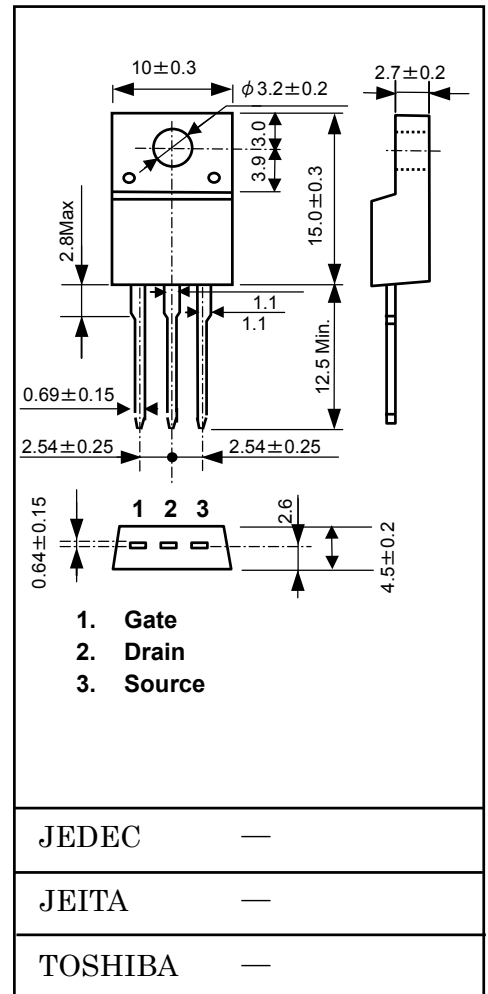
unit : mm

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS(ON)} = 2.0 \Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 4.5 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 100 \mu\text{A}$ ($V_{DS} = 720 \text{ V}$)
- Enhancement-mode: $V_{th} = 2.0 \sim 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	900	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	900	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	5	A
	Pulse ($t = 1 \text{ ms}$) (Note 1)	I_{DP}	15	
Drain power dissipation ($T_c = 25^\circ\text{C}$)		P_D	45	W
Single pulse avalanche energy (Note 2)		E_{AS}	595	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 3)		E_{AR}	4.5	mJ
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55~150	$^\circ\text{C}$



Thermal Characteristics

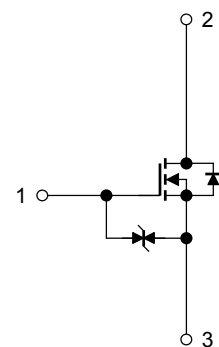
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	2.78	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	62.5	$^\circ\text{C/W}$

Note 1: Please use devices on conditions that the channel temperature is below 150°C .

Note 2: $V_{DD} = 90 \text{ V}$, $T_{ch} = 25^\circ\text{C}$, $L = 43.6 \text{ mH}$, $I_{AR} = 5.0 \text{ A}$, $R_G = 25 \Omega$

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.



Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Gate-source breakdown voltage		$V_{(BR)GSS}$	$I_G = \pm 10\ \mu\text{A}, V_{GS} = 0\text{ V}$	± 30	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = 720\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	900	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$	—	2.0	2.5	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 20\text{ V}, I_D = 3\text{ A}$	2.0	4.5	—	S
Input capacitance		C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1150	—	pF
Reverse transfer capacitance		C_{rss}		—	20	—	
Output capacitance		C_{oss}		—	100	—	
Switching time	Rise time	t_r		—	30	—	ns
	Turn-on time	t_{on}		—	70	—	
	Fall time	t_f		—	60	—	
	Turn-off time	t_{off}		Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$	—	170	
Total gate charge		Q_g	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	—	28	—	nC
Gate-source charge		Q_{gs}		—	17	—	
Gate-drain charge		Q_{gd}		—	11	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)		I_{DR}	—	—	—	5	A
Pulse drain reverse current (Note 1)		I_{DRP}	—	—	—	15	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time		t_{rr}	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V},$	—	900	—	ns
Reverse recovery charge		Q_{rr}	$dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	5.4	—	μC

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