73S8010R
Low Cost Smart Card Interface

DATA SHEET

ISO/IEC 7816-3

January 2008

DESCRIPTION

The TERIDIAN 73S8010R is a single smart card interface IC. The TERIDIAN 73S8010R has been designed to provide full electrical compliance with ISO-7816-3 and EMV 4.0 (EMV2000) specifications.

Interfacing with the host is done through the two-wire I^2C bus, and one interrupt output to inform the system controller of the card presence and faults.
The card clock signal can be generated by an on-chip oscillator using an external crystal, or by connection to a clock signal.

The TERIDIAN 73S8010R incorporates an ISO-7816-3 activation/deactivation sequencer that controls the card signals. Level-shifters drive the card signals with the selected card voltage (3V or 5V), coming from an internal Low Drop-Out (LDO) voltage regulator. This LDO regulator is powered by a dedicated power supply input V_{PC}. Digital circuitry is separately powered by a digital power supply V_{DD}.

With its embedded LDO regulator, the TERIDIAN 73S8010R is a cost-effective solution for any application where a 5V (typically -5% +10%) power supply is available.
Hardware support for auxiliary I/O lines, C4 / C8 contacts, is provided.

Emergency card deactivation is initiated upon card extraction or upon any fault generated by the protection circuitry. The fault can be a card over-current, a V_{DD} (digital power supply), a V_{PC} (regulator power supply), a V_{CC} (card power supply) or an over-heating fault.

The card over-current circuitry is a true current detection function, as opposed to V_{CC} voltage drop detection, as usually implemented in ICC interface ICs.

The V_{DD} voltage fault has a threshold voltage that can be adjusted with an external resistor or resistor network. It allows automated card deactivation at a customized V_{DD} voltage threshold value. It can be used, for instance, to match the system controller operating voltage range.

APPLICATIONS

- **Set-Top-Box Conditional Access and Pay-per-View**
- **Point of Sales & Transaction Terminals**
- **Control Access & Identification**
- **Multiple card and SAM reader configurations**

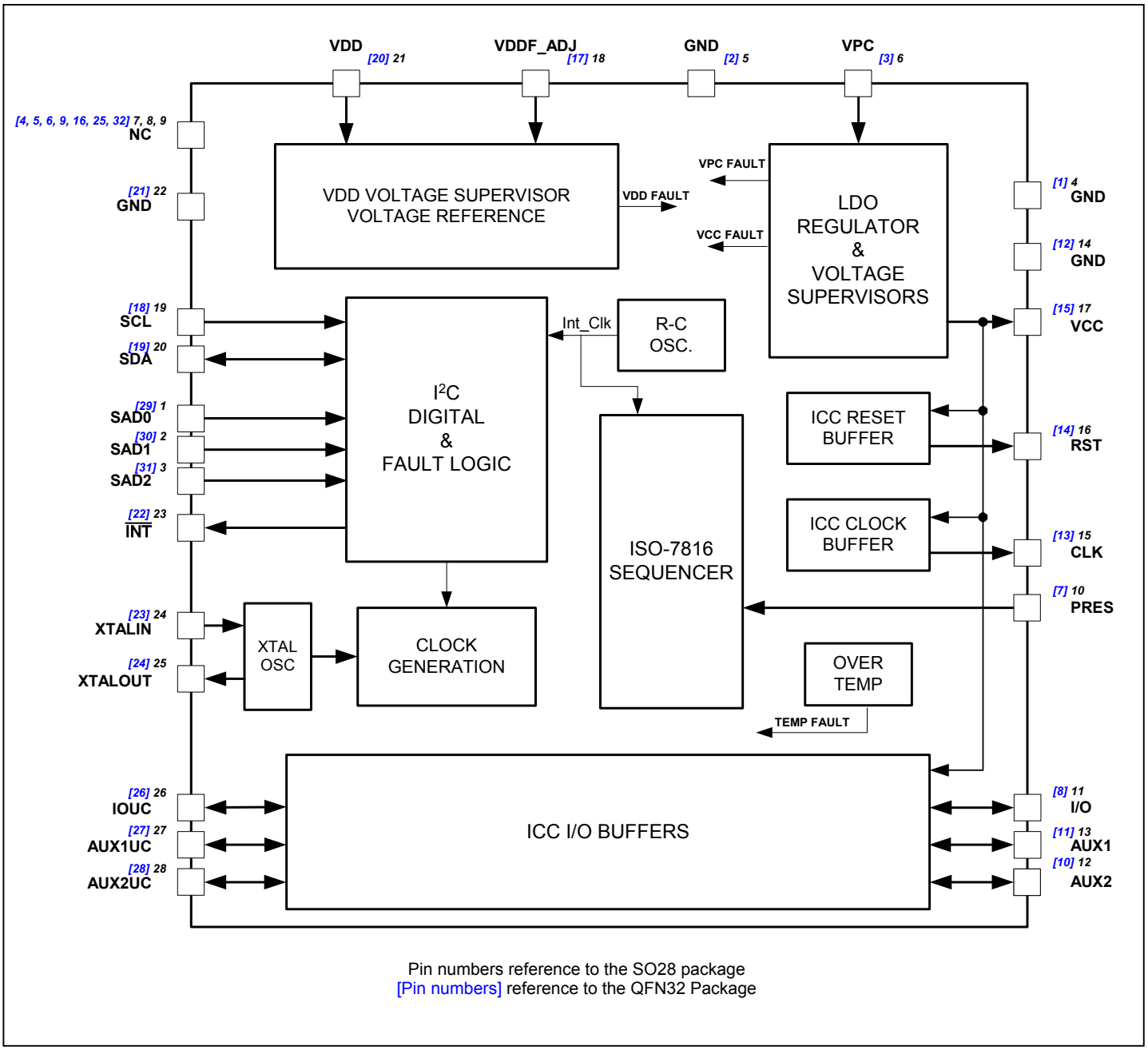
ADVANTAGES

- **Single smart card interface**
- **IC firmware compatible with TDA8020**
- **Traditional step-up converter is replaced by a LDO regulator:**
  - **→ Greatly reduced power dissipation**
  - **→ Fewer external components are required**
  - **→ Better noise performance**
  - **→ High current capability (90mA supplied to the card)**
- **Small format (5x5x0.8mm) QFN32 package option**
- **True card over-current detection**

FEATURES

- **Card Interface:**
  - **Complies with ISO-7816-3 and EMV 4.0**
  - **A LDO voltage regulator provides 3V / 5V to the card from an external power supply input**
  - Provides at least 90mA to the card
  - ISO-7816-3 Activation / Deactivation sequencer with emergency automated deactivation on card removal or fault detected by the protection circuitry
  - Protection includes 3 voltage supervisors that detects voltage drops on V_{CC} card and on power supplies V_{DD} and V_{PC}
  - The V_{DD} voltage supervisor threshold value can be externally adjusted
  - Over-current detection 150mA max.
  - 1 card detection input
  - Auxiliary I/O lines, for C4 / C8 contact signals
  - CLK signal up to 20MHz
- **Host Interface:**
  - Fast mode, 400kbps I^2C slave bus
  - 8 possible devices in parallel
  - One control register and one status register
  - Interrupt output to the host for fault detection
  - Crystal oscillator or host clock, up to 27MHz
- **Power Supply:**
  - V_{PC}: 4.75V to 5.5V
  - V_{DD}: 2.7V to 5.5V
- **6kV ESD Protection on the card interface**
- **Package: SO28 or QFN32**

FUNCTIONAL DIAGRAM



Pin numbers reference to the SO28 package
[Pin numbers] reference to the QFN32 Package

Figure 1: 73S8010R Block Diagram

PIN DESCRIPTION

CARD INTERFACE

NAME	PIN (SO)	PIN (QFN)	DESCRIPTION
I/O	11	8	Card I/O: Data signal to/from card. Includes a pull-up resistor to V_{CC}.
AUX1	13	11	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to V_{CC}.
AUX2	12	10	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to V_{CC}.
RST	16	14	Card reset: provides reset (RST) signal to card.
CLK	15	13	Card clock: provides clock (CLK) signal to card. The rate of this clock is determined by crystal oscillator frequency and CLKSEL bits in the control register.
PRES	10	7	Card Presence switch: active high indicates card is present. Includes a pull-down resistor.
VCC	17	15	Card power supply – logically controlled by sequencer, output of LDO regulator. Requires an external filter capacitor to the card GND.
GND	14	12	Card ground.

MISCELLANEOUS INPUTS AND OUTPUTS

NAME	PIN (SO)	PIN (QFN)	DESCRIPTION
XTALIN	24	23	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock.
XTALOUT	25	24	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as external clock input.
VDDF_ADJ	18	17	V_{DD} threshold adjustment input: this pin can be used to overwrite higher V_{DDF} value (that controls deactivation of the card). Must be left open if unused.
NC	7, 8, 9	4, 5, 6, 9, 16, 25, 32	Non-connected pin.

POWER SUPPLY AND GROUND

NAME	PIN (SO)	PIN (QFN)	DESCRIPTION
VDD	21	20	System controller interface supply voltage and supply voltage for internal circuitry.
VPC	6	3	LDO regulator power supply source.
GND	4	1	LDO regulator ground.
GND	14	12	Smart Card I/O Ground.
GND	5, 22	2,21	Digital ground.

MICROCONTROLLER INTERFACE

NAME	PIN (SO)	PIN (QFN)	DESCRIPTION
$\overline{INT}$	23	22	Interrupt output(negative assertion). Interrupt output signal to the processor. A 20kΩ pull up to V_{DD} is provided internally
SAD0 SAD1 SAD2	1 2 3	29 30 31	Serial device address bits. Digital inputs for address selection that allows for the connection of up to 8 devices in parallel. Address selections as follows: SAD2 SAD1 SAD0 I^2C Address (7 bits) 0 0 0 40h 0 0 1 42h 0 1 0 44h 0 1 1 46h 1 0 0 48h 1 0 1 4Ah 1 1 0 4Ch 1 1 1 4Eh Note: Pins SADO and SAD1 are internally pulled-down and SAD2 is internally pulled-up. The default address when left unconnected is 48h.
SCL	19	18	I^2C clock signal input
SDA	20	19	I^2C bi-directional serial data signal
I/OUC	26	26	System controller data I/O to/from the card. Includes internal pull-up resistor to V_{DD}
AUX1UC	27	27	System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to V_{DD}
AUX2UC	28	28	System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to V_{DD}

SYSTEM CONTROLLER INTERFACE (I^2C BUS)

A fast-mode 400kHz I^2C bus slave interface is used for controlling the device and reading the status of the device via the data pin SDA and clock pin SCL. The bus has 3 address select pins, SAD0, SAD1, and SAD2. This allows up to 8 devices to be connected in parallel.

Device Address Selections

SAD2	SAD1	SAD0	I^2C Address (7 bits)
0	0	0	40h
0	0	1	42h
0	1	0	44h
0	1	1	46h
1	0	0	48h
1	0	1	4Ah
1	1	0	4Ch
1	1	1	4Eh

Note: bit 0 of the I^2C address is the R/W bit. Refer to figures 2 and 3 for usage.

CONTROL register

Power On Reset = 00h

Name	Bit	Description
Start/Stop	0	When set, initiates an activation and a cold reset procedure; when reset, initiates a deactivation sequence
Warm reset	1	When set, initiates a warm reset procedure; automatically reset by hardware when the card starts answering or when the card is declared mute
5Vand 3V	2	When set, V_{CC} = 3v; when reset, V_{CC} = 5v. When de-activating (setting bit 0 = 0) and operating with 3V (bit 2 =1), do not simultaneously set bit 2 =0.
Clock Stop	3	When set, the card clock is stopped. Bit 4 determines the card clock stop level
Clock Stop Level	4	When set, card clock stops high; when reset card clock stops low
Clksel1	5	Bits 5 and 6 determine the clock rate to the. See card clock rate selection table for more details.
Clksel2	6	
I/O enable	7	I/O enable bit. When set, I/O is transferred on I/OUC; when reset I/O to I/OUC is high impedance.

Card clock rate selection table

Bit Clksel2	Bit Clksel1	Card Clock
0	0	Clkin/8
0	1	Clkin/4
1	0	Clkin/2
1	1	Clkin (Xtalin)

I²C-bus Write to Control Register:

I²C-bus Write command to the control register follows the format shown below. After the START condition, a slave address is sent by the master. This address is seven bits long followed by an eighth bit which is an opcode bit (R/$\overline{W}$) – a 'zero' indicates the master will write data to the control register. After the R/$\overline{W}$ bit, the 'zero' ACK bit is sent to the master by the device. The master now starts sending the 8 bits of data to the control register during the DATA bits. After the DATA bits, the 'zero' ACK bit is sent to the master by the device. The master should send the STOP condition after receiving this ACK bit.

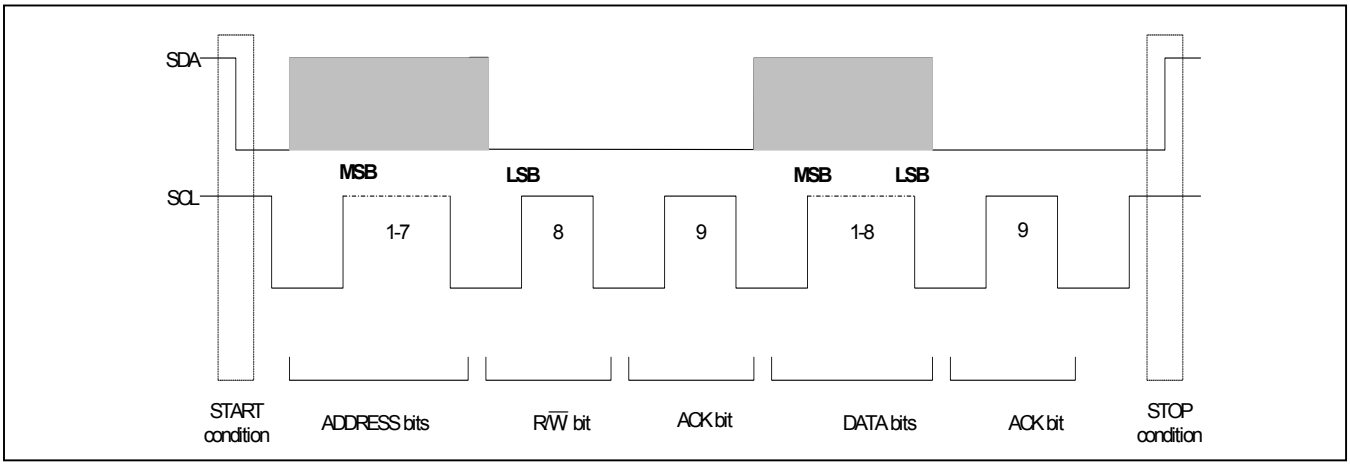


Figure 2 - I²C Bus Write Protocol

STATUS register

Power On Reset = 04h

Name	Bit	Description
PRES	0	Set when the card is present (pin PRES is high); reset when the card is not present.
PRESL	1	Set when the PRES pin changes state (rising/falling edge); reset when the status register is read. Generates an interrupt when set.
I/O	2	Set when I/O is high; reset when I/O is low.
SUPL	3	Set when a voltage fault is detected; reset when the status register is read. Generates an interrupt when set
PROT	4	Set when an over-current or over-heating fault has occurred during a card session; reset when the status register is read. Generates an interrupt when set
MUTE	5	Set during ATR when the card has not answered during the ISO 7816-3 time window (40000 card clock cycles); reset when the next session begins.
EARLY	6	Set during ATR when the card has answered before 400 card clock cycles; reset when the next session begin.
ACTIVE	7	Set when the card is active (V_{CC} is on); reset when the card is inactive.

I²C-bus Read from Status Register:

I²C-bus Read Command from the Status Register follows the format shown below. After the START condition, a slave address is sent by the master. This address is seven bits long followed by an eighth bit which is an opcode bit (R/$\overline{W}$) – a 'one' indicates the master will read data from the status register. After the R/$\overline{W}$ bit, the 'zero' ACK bit is sent to the master by the device. The device now starts sending the 8-bit status register data to the control register during the DATA bits. After the DATA bits, the 'one' ACK bit is sent to the device by the master. The master should send the STOP condition after receiving the ACK bit.

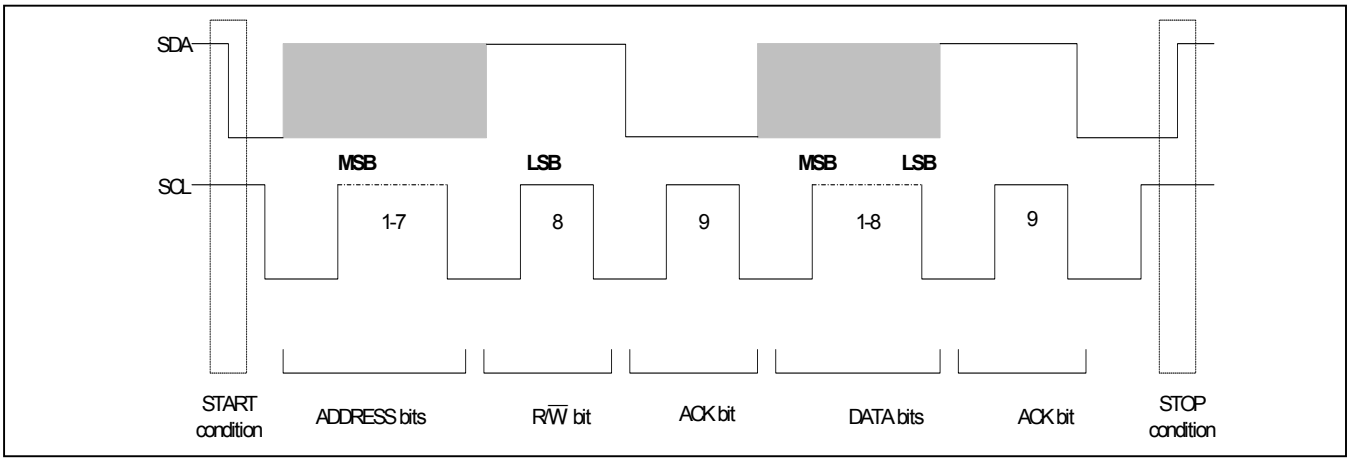


Figure 3 - I²C Bus Read Protocol

I²C-bus timing definition:

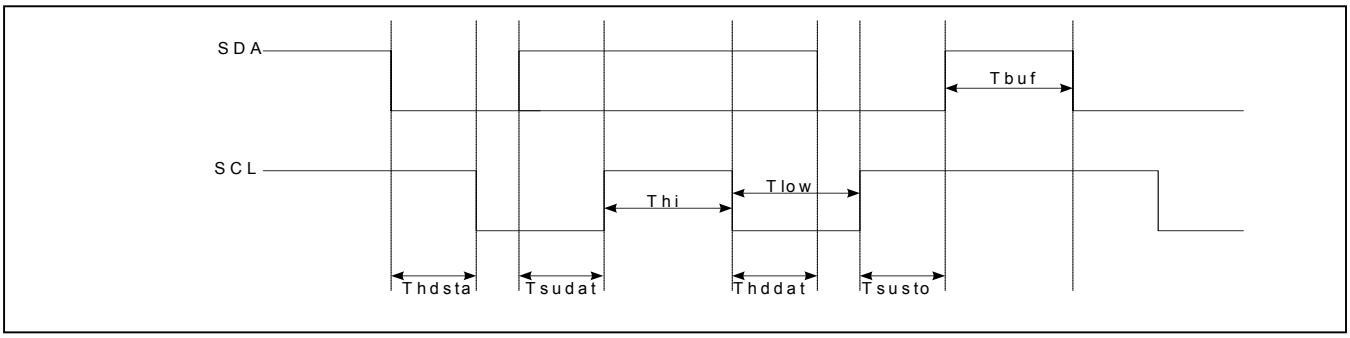


Figure 4 - I²C Bus Timing Definitions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fsclk	Clock frequency			400	kHz
Tlow	Clock low	1.3			µs
Thi	Clock high	0.6			µs
Thdsta	Hold time START condition	0.6			µs
Tsudat	Data set up time	100			ns
Thddat	Data hold time	5		900	ns
Tsusto	Set up time STOP condition	0.6			µs
Tbuf	Bus free time between a STOP and START condition	1.3			µs

POWER SUPPLY AND VOLTAGE SUPERVISON

The TERIDIAN 73S8010R smart card interface IC incorporates a LDO voltage regulator. The voltage output is controlled by the digital input 5V/$\overline{3V}$. This regulator is able to provide either 3V or 5V card voltage from the power supply applied on the VPC pin.

Digital circuitry is powered by the power supply applied on the VDD pin. V_{DD} also defines the voltage range to interface with the system controller.

Three voltage supervisors constantly check the presence of the voltages V_{DD}, V_{PC} and V_{CC}. A card deactivation sequence is forced upon fault of any of these voltage supervisors. The two voltage supervisors for V_{PC} and V_{CC} are linked so that a fault is generated to activate a deactivation sequence when the voltage V_{PC} becomes lower than V_{CC}. It allows the 73S8010R to operate at lower V_{PC} voltage when using 3V cards only.
The voltage regulator can provide a current of at least 90mA on V_{CC} that comply easily with EMV 4.0 specification. The V_{PC} voltage supervisor threshold values are defined from EMV 4.0 standard. A third voltage supervisor monitors the V_{DD} voltage. It is used to initialize the ISO-7816-3 sequencer at power-on, and to deactivate the card at power-off or upon fault. The voltage threshold of the V_{DD} voltage supervisor is internally set by default to 2.3V nominal. However, it may be desirable, in some applications, to modify this threshold value. The pin VDDF_ADJ (pin 18 in the SO package, pin 17 in the QFN package) is used to connect an external resistor R_{EXT} to ground to raise the V_{DD} fault voltage to another value V_{DDF}. The resistor value is defined as follows:

$$R_{EXT} = 56k\Omega / (V_{DDF} - 2.33)$$

An alternative method (more accurate) of adjusting the V_{DD} fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see applications diagram). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as R1/(R1+R3). Kx is calculated as:

Kx = (2.789 / V_{TH}) - 0.6125 where V_{TH} is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas.

R3 = 24000 / Kx R1 = R3*(Kx / (1 – Kx))

Taking the example above, where a V_{DD} fault threshold voltage of 2.7V is desired, solving for Kx gives:
→ Kx = (2.789 / 2.7) - 0.6125 = 0.42046.
Solving for R3 gives: → R3 = 24000 / 0.42046 = 57080.
Solving for R1 gives: → R1 = 57080 *(0.42046 / (1 – 0.42046)) = 41412.
Using standard 1 % resistor values gives R3 = 57.6KΩ and R1 = 42.4KΩ.
These values give an equivalent resistance of Kx = 0.4228, a 0.6% error.

If the 2.3V default threshold is used, this pin must be left unconnected.

CARD POWER SUPPLY

The card power supply is provided by the LDO regulator, and controlled by the digital ISO-7816-3 sequencer. Card voltage selection is carried out by bit 2 of the control register.

Choice of the V_{CC} capacitor:

Depending on the applications, the requirements in terms of both V_{CC} minimum voltage and transient currents that the interface must be able to provide to the card are different. An external capacitor must be connected between the VCC pin and to the card ground in order to guarantee stability of the LDO regulator, and to handle the transient requirements. The type and value of this capacitor can be optimized to meet the desired specification. The table below shows the recommended capacitors for each V_{PC} power supply configuration and applicable specification.

Specification Requirements			System Requirements		
Specification	**Min V_{CC} Voltage allowed during transient current**	**Max transient current charge**	**Min V_{PC} Power Supply required**	**Capacitor Type**	**Capacitor Value**
EMV 4.0	4.6V	30nA.s	4.75V	X5R/X7R w/ ESR < 100mΩ	3.3 μF
ISO-7816-3	4.5V	20nA.s	4.75V		1μF

Table 1: Choice of VCC pin capacitor

OVER-TEMPERATURE MONITOR

A built-in detector monitors die temperature. Upon over-temperature condition (most likely resulting from a heavily loaded card interface, including short circuits), a card deactivation sequence is initiated, and a fault condition is reported to the system controller (sets bit 4 of the status register and generates an interrupt).

ON-CHIP OSCILLATOR AND CARD CLOCK

The TERIDIAN 73S8010R device has an on-chip oscillator that can generate the smart card clock using an external crystal, connected between the pins XTALIN and XTALOUT, to set the oscillator frequency. When the card clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected.

The card clock frequency may be chosen between 4 different division rates, defined by bits 5 and 6 of the I^2C Control register, as per the following table:

Bit Clksel2	Bit Clksel1	Card Clock
0	0	Clkin/8
0	1	Clkin/4
1	0	Clkin/2
1	1	Clkin (Xtalin)

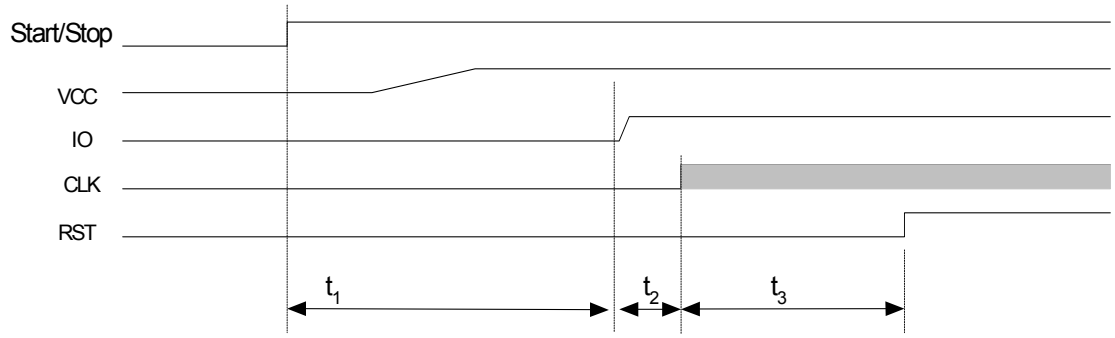
Card power down mode (card clock STOP) is supported and is controllable through the dedicated digital inputs bits 3 and 4 of the I^2C Control register, respectively Clock Stop, and Clock Stop Level.

ACTIVATION SEQUENCE

After Power on Reset, the signal $\overline{INT}$ is low until the V_{DD} is stable. When V_{DD} has been stable for approximately 10 ms and the signal $\overline{INT}$ is high, the system controller may read the status register to see if the card is present. If all the status bits are satisfied, the system controller can initiate the activation sequence by writing a '1' to Start/Stop bit (bit 0) of control register.

The following steps show the activation sequence and the timing of the card control signals when the system controller initiates the Start/Stop bit (bit 0) of the control register:

- Voltage V_{CC} to the card should be valid by the end of t_1. If V_{CC} is not valid for any reason, then the session is aborted.
- Turn I/O to reception mode at the end of t_1.
- CLK is applied to the card at the end of t_2.
- RST (to the card) is set high at the end of t_3.



t_1 = 0.510 ms (timing by 1.5MHz internal Oscillator), I/O in reception mode
t_2 =1.5µs, CLK starts
t_3 = >42000 card clock cycles, RST set high

Figure 5 - Activation Sequence

DEACTIVATION SEQUENCE

Deactivation is initiated either by the system controller by resetting the Start/Stop bit, or automatically in the event of hardware faults. Hardware faults are over-current, over-temperature, V_{DD} fault, V_{PC} fault, V_{CC} fault, and card extraction during the session.

The following steps show the deactivation sequence and the timing of the card control signals when the system controller clears the start/stop bit:

- RST goes low at the end of t_1.
- CLK goes low at the end of t_2.
- I/O goes low at the end of t_3. Out of reception mode.
- Shut down V_{CC} at the end of time t_4.

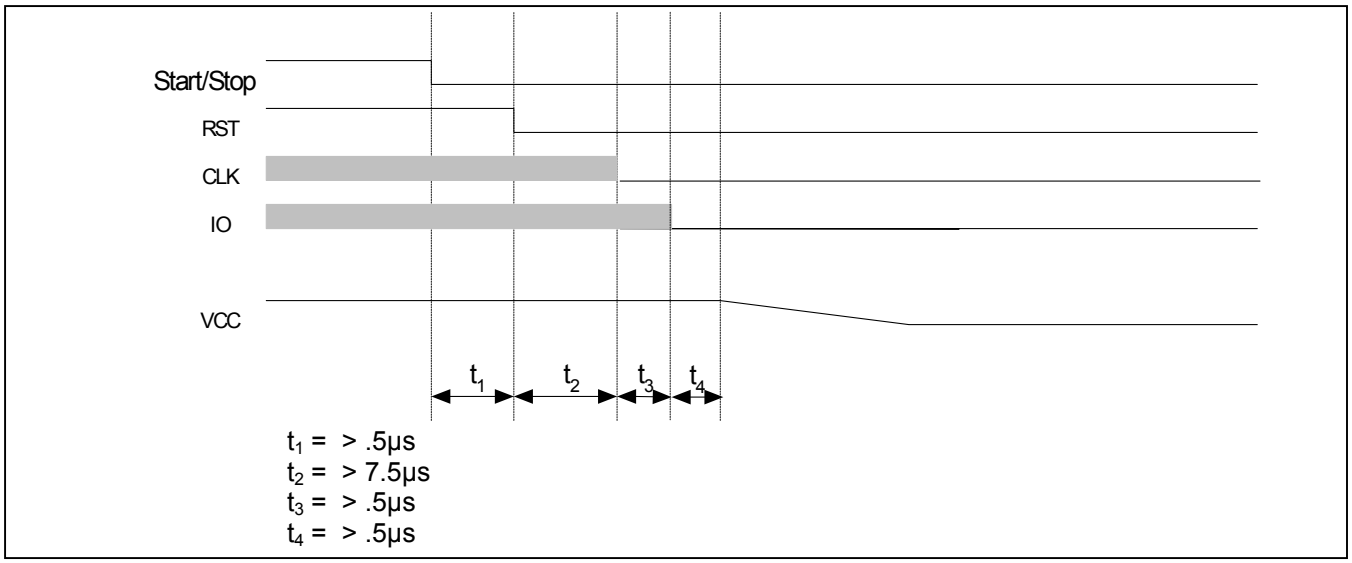


Figure 6 - Deactivation Sequence

INTERRUPT

Interrupt is an active low interrupt. It is set low if any of these internal faults are detected:

-V_{CC} fault
-V_{DD} fault
-V_{PC} fault

Or if one of these status bits condition is detected:

-Early ATR
-Mute ATR
-Card insert or card extract
-Protection status from Over-current or Over-heating

In case the interrupt is set low by the detection of these status bits, then the interrupt is set high when these status bits are read. (READ STATUS DONE)

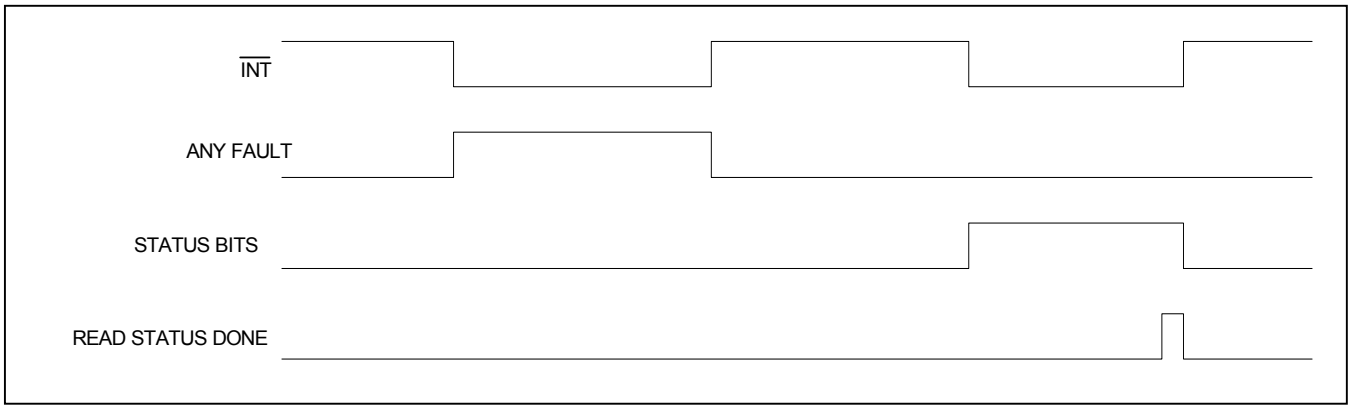


Figure 7 - FAULT Functions, $\overline{INT}$ operation

Note that a power-on-reset event will reset all of the control and status registers to their default states. A V_{DD} fault event does not reset these registers, but it will signal an interrupt condition and by the action of the timer that creates interval "t_1," not clearing the interrupt until V_{DD} is valid for at least t_1. V_{DD} fault can be considered valid for V_{DD} as low as 1.5 to 1.8 volts. At the lower range of V_{DD} fault, POR will be asserted.

WARM RESET

The 73S8010R automatically asserts a warm reset to the card when instructed through the bit 1 of the I^2C Control register (bit Warm Reset). The warm reset length is automatically defined as 42,000 card clock cycles. The bit Warm Reset is automatically reset when the card starts answering or when the card is declared mute.

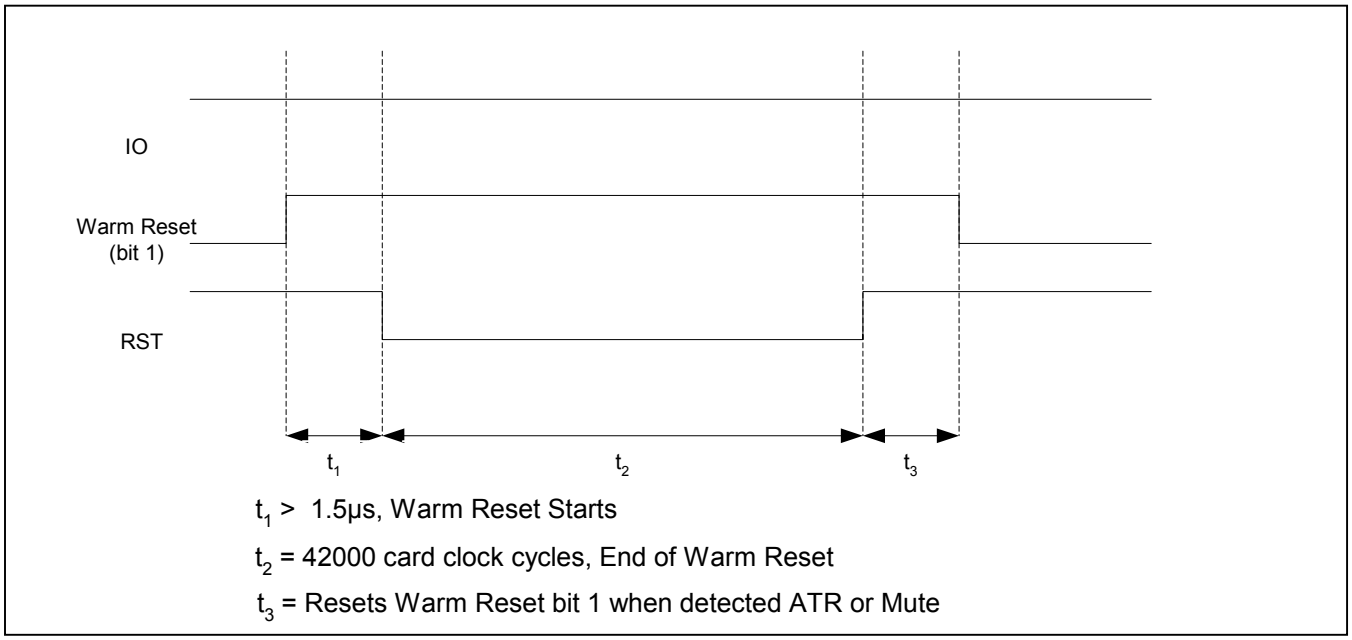
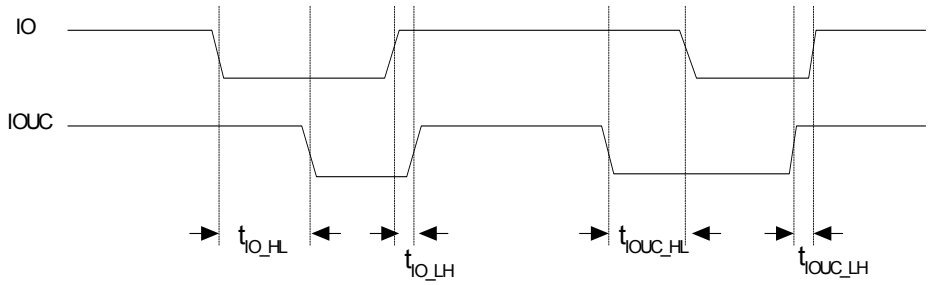


Figure 8 – Warm Reset operation

I/O CIRCUITRY AND TIMING

The states of the I/O, AUX1, and AUX2 pins are low after power-on-reset and they are high when the activation sequencer enables the I/O reception state. See Activation Sequence timing section for more details on when the I/O reception is enabled. The states of the I/OUC, AUX1UC, and AUX2UC are high after power on reset. When the control I/O enable bit 7 of control register is set, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected then both I/O lines return to their neutral state. The delay between these signals is shown in Figure 9.



Delay from I/O to I/OUC:	t_{IO_HL} = 100ns	t_{IO_LH} = 25ns
Delay from I/OUC to I/O:	t_{IOuc_HL} = 100ns	t_{IOUC_LH} = 25ns

Figure 9 - I/O Timing Definition

TYPICAL APPLICATION SCHEMATIC

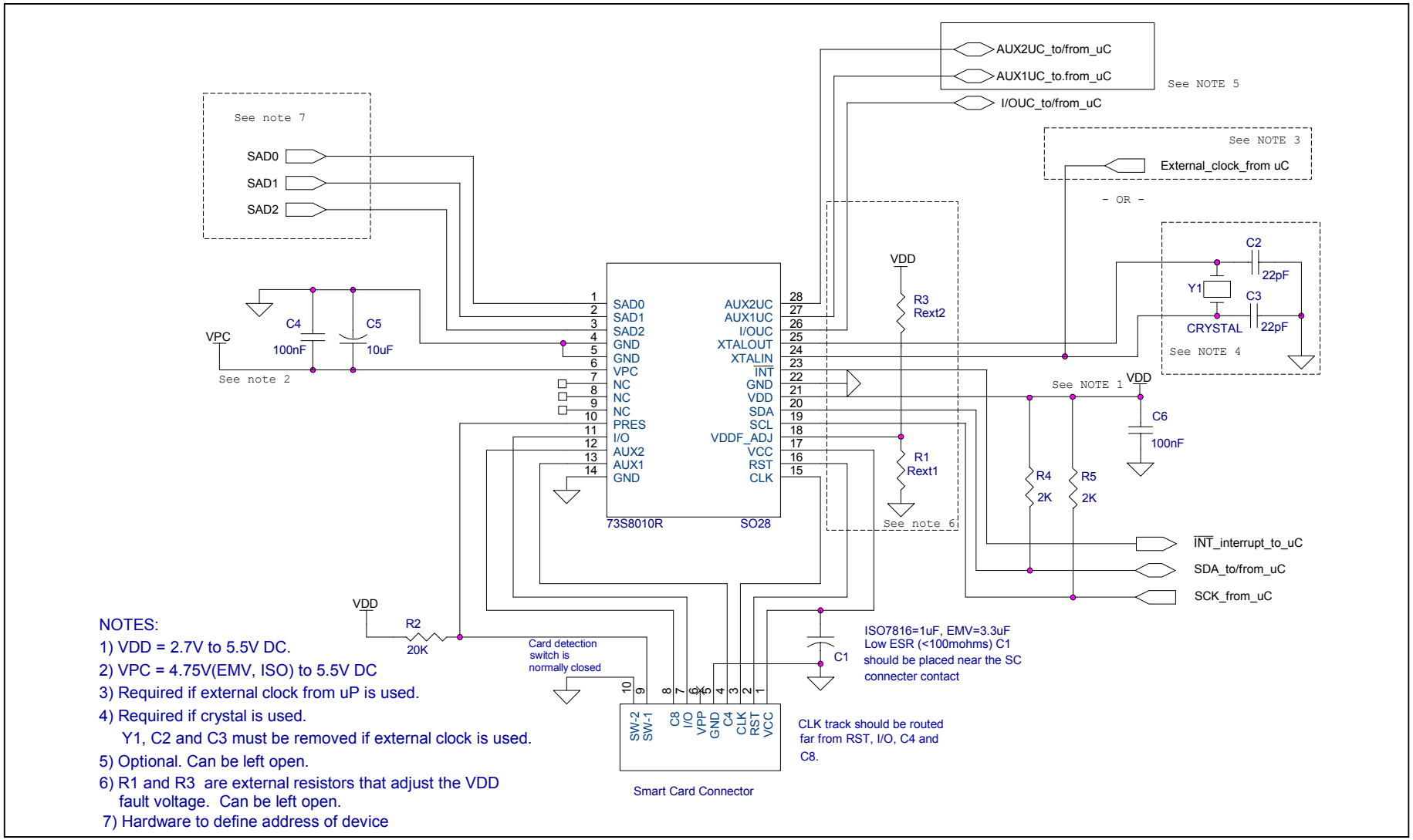


Figure 10: 73S8010R – Typical Application Schematic

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to the device.

PARAMETER	RATING
Supply Voltage V_{DD}	-0.5 to 6.0 VDC
Supply Voltage V_{PC}	-0.5 to 6.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to (V_{DD} +0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD Tolerance – Card interface pins	+/- 6kV
ESD Tolerance – Other pins	+/- 2kV

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage V_{DD}	2.7 to 5.5 VDC
Supply Voltage V_{PC}	4.75 to 5.5 VDC
Ambient Operating Temperature	-40°C to +85°C
Input Voltage for Digital Inputs	0V to V_{DD} + 0.3V

CHARACTERISTICS: CARD INTERFACE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Card Power Supply (V_{CC}) Regulator *General conditions, -40°C < T < 85°C, 4.75v < V_{PC} < 5.5v, 2.7v < V_{DD} < 5.5v*						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode I_{CC} = 1mA	-0.1		0.4	V
		Active mode; I_{CC} <65mA; 5v	4.60		5.25	V
		Active mode; I_{CC} <90mA; 5v	4.55			V
		Active mode; I_{CC} <90mA; 3v	2.80		3.2	V
		Active mode; single pulse of 100mA for 2µs; 5 volt, fixed load = 25mA	4.6		5.25	V
		Active mode; single pulse of 100mA for 2µs; 3v, fixed load = 25mA	2.76		3.2	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 5v	4.6		5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 3v	2.76		3.2	V
I_{CCmax}	Maximum supply current to the card	Static load current, V_{CC}>4.6 or 2.7 volts as selected,	90			mA
I_{CCF}	I_{CC} fault current		100		150	mA
V_{SR}	V_{CC} slew rate - Rise rate on activate	C_F = 3.3µF on V_{CC}	0.02	0.05	0.08	V/µs
V_{SF}	V_{CC} slew rate - Fall rate on de-activate	C_F = 3.3µF on V_{CC}	0.025	0.06	0.08	V/µs
C_F	External filter capacitor (V_{CC} to GND)		1	3.3	5	µF

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, AUX1UC, and AUX2UC.						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} =0	0.9 V_{CC}		V_{CC}+v0.1	V
		I_{OH} = -40µA	0.75 V_{CC}		V_{CC} + 0.1	V
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} =0	0.9 V_{DD}		V_{DD}+0.1	V
		I_{OH} = -40µA	0.75 V_{DD}		V_{DD} + 0.1	V
V_{OL}	Output level, low	I_{OL}=1mA			0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		1.8		V_{CC} +0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)		1.8		V_{DD} +0.30	V
V_{IL}	Input level, low		-0.3		0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	µA
I_{IL}	Input current, low	V_{IL} = 0			0.65	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 ohms			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 ohms			15	mA
t_R, t_F	Output rise time, fall times	C_L = 80pF, 10% to 90% For I/OUC, AUX1UC, AUX2UC, CL=50pF			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	µs
R_{PU}	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
T_{FDIO}	Delay, I/O to I/OUC, I/OUC to I/O, AUX1 to AUX1UC, AUX1UC to AUX1, AUX2 to AUX2UC, AUX2UC to AUX2	Falling edge from master to slave measured at 50% point	60	100	200	ns
T_{RDIO}	Delay, I/O to I/OUC, I/OUC to I/O, AUX1 to AUX1UC, AUX1UC to AUX1, AUX2 to AUX2UC, AUX2UC to AUX2	Rising edge from master to slave measured at 50% point		25	90	ns
C_{IN}	Input capacitance				10	pF

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} =-200µA	0.9 V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL}=200µA	0		0.3	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	mA
I_{CLK_LIM}	Output current limit, CLK				70	mA
t_R, t_F	Output rise time, fall time	C_L = 35pF for CLK, 10% to 90%			8	ns
		C_L = 200pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK	C_L =35Pf, F_{CLK} ≤ 20MHz	45		55	%

CHARACTERISTICS: DIGITAL SIGNALS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Digital I/O except for OSC I/O						
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		0.7*V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{DD} - 0.45			V
R_{OUT}	Pull-up resistor, $\overline{INT}$			20		kΩ
$\|I_{IL1}\|$	Input Leakage Current	GND < V_{IN} < V_{DD}	-5		5	µA
Oscillator (XTALIN) I/O Parameters						
V_{ILXTAL}	Input Low Voltage - XTALIN		-0.3		0.5	V
V_{IHXTAL}	Input High Voltage - XTALIN		0.7*V_{DD}		V_{DD}+0.3	V
I_{ILXTAL}	Input Current - XTALIN	GND < V_{IN} < V_{DD}	-30		30	µA

DC CHARACTERISTICS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
I_{DD}	Supply Current on V_{DD}			1.5	3.0	mA
I_{PC}	Supply Current on V_{PC}	V_{CC} on, ICC=0 I/O, AUX1, AUX2=high		0.45	0.65	mA

CHARACTERISTICS I^2C INTERFACE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
SDA, SCL						
V_{IL}	Input Low Voltage		-0.3		0.3* V_{DD}	V
V_{IH}	Input High Voltage		0.7*V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.40	V
C_{IN}	Pin capacitance				10	pF
I_{IN}	Output High Voltage	I_{OH} = -1mA	V_{DD} - 0.45			V
T_F	Output fall time	C_L = 0 to 400pF	20 + 0.1*C_L		250	ns
T_{SP}	Pulse width of spikes that are suppressed	Transition from valid logic level to opposite level			50	ns

VOLTAGE / TEMPERATURE FAULT DETECTION CIRCUITS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_{DDF}	V_{DD} fault (V_{DD} Voltage supervisor threshold)	No external resistor on VDDF_ADJ pin	2.15		2.4	V
V_{PCF}	V_{PC} fault (V_{PC} Voltage supervisor threshold)	V_{PC}<V_{CC}, a transient event		V_{CC} - 0.2		V
V_{CCF}	V_{CC} fault (V_{CC} Voltage supervisor threshold)	V_{CC} = 5v	4.20		4.55	V
		V_{CC}= 3v	2.5		2.7	V
T_F	Die over temperature fault		115		145	°C

MECHANICAL DRAWING (QFN)

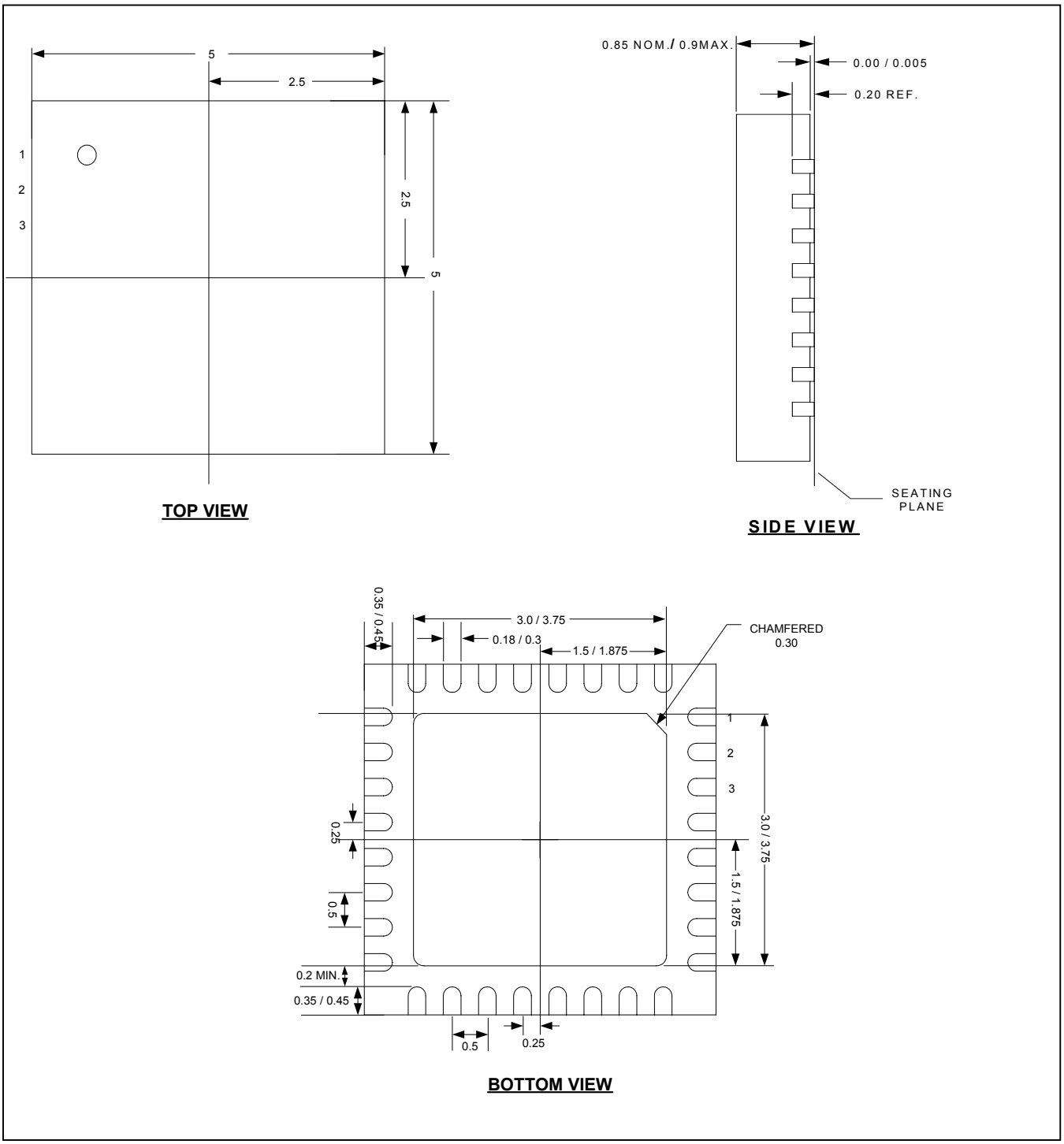


Figure 11: QFN 32

PACKAGE PIN DESIGNATION (QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

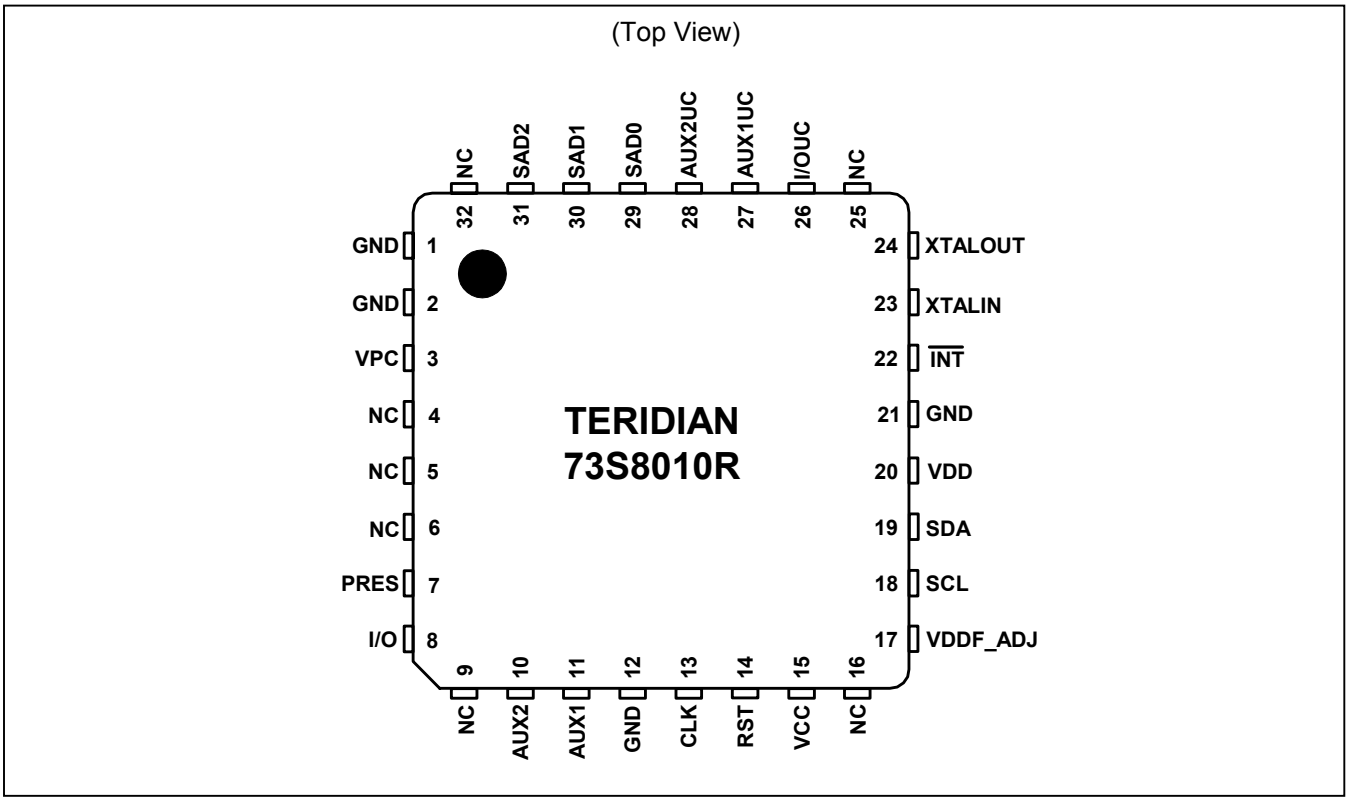


Figure 12: QFN32 73S8010R Pin Out

MECHANICAL DRAWING (SO)

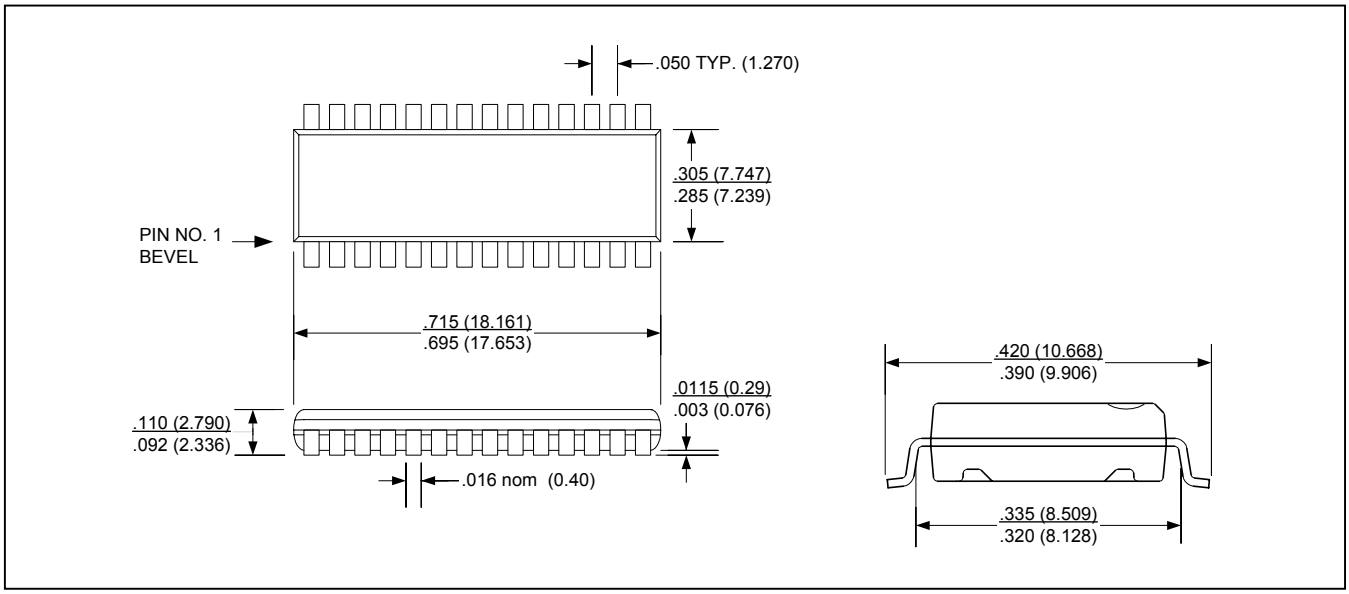


Figure 13: 28 Lead SO

PACKAGE PIN DESIGNATION (SO)

CAUTION: Use handling procedures necessary for a static sensitive component

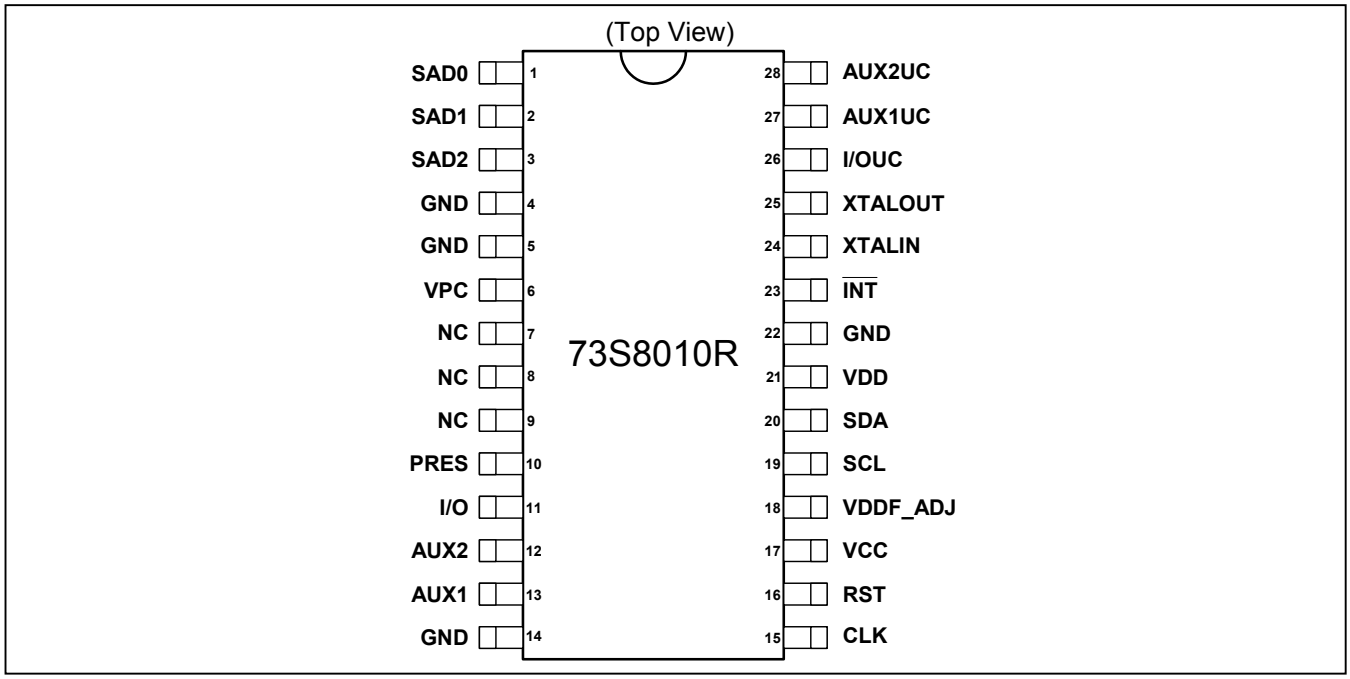


Figure 14: 28SO 73S8010R Pin Out

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGING MARK
73S8010R -SOL 28-pin Lead-Free SO	73S8010R -IL/F	73S8010R -IL
73S8010R -SOL 28-pin Lead-Free SO Tape / Reel	73S8010R -ILR/F	73S8010R -IL
73S8010R -QFN 32-pin Lead-Free QFN	73S8010R -IM/F	73S8010R
73S8010R -QFN 32-pin Lead-Free QFNTape / Reel	73S8010R -IMR/F	73S8010R

Data Sheet

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